JUNO (Jiangmen Underground Neutrino Observatory)

A multipurpose **neutrino experiment** designed to determine neutrino mass hierarchy with a **20,000 tons liquid scintillator detector** at 700-meter deep underground

- ~ 18,000 PMTs (20" diameter) → Large-PMT system (LPMT) → **75 % of the inner surface**
- ~ 25,000 PMTs (3" diameter) → Small-PMT system (SPMT) →
  - Increase coverage of the surface → Improve energy reconstruction
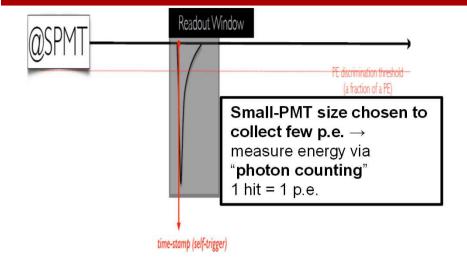 - Cross calibration

SPMT

Ωmega

Readout Window
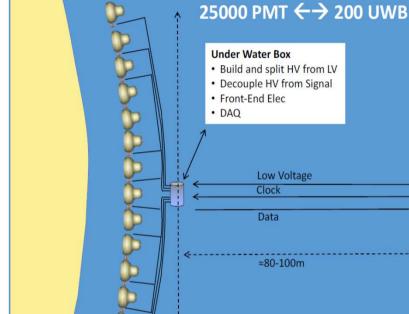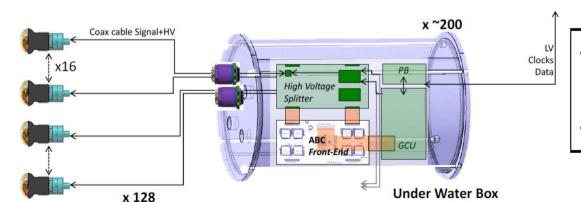
@SPMT

PE discrimination threshold
(a fraction of a PE)

Small-PMT size chosen to collect few p.e. →
measure energy via
"**photon counting**"
1 hit = 1 p.e.

time-stamp (self-trigger)

25000 PMT ⟷ 200 UWB

Under Water Box
• Build and split HV from LV
• Decouple HV from Signal
• Front-End Elec
• DAQ

Low Voltage
Clock
Data

SURFACE
MAIN
DAQ

≈80-100m

≈ 20m → >100 channels

3' PMT   High Voltage divider   Potting   Cable   Connector   Under Water Box   ABC board   Splitter board

Coax cable Signal+HV

x16

x 128

x ~200

High Voltage Splitter

PB

ABC
Front-End

GCU

LV
Clocks
Data

Under Water Box

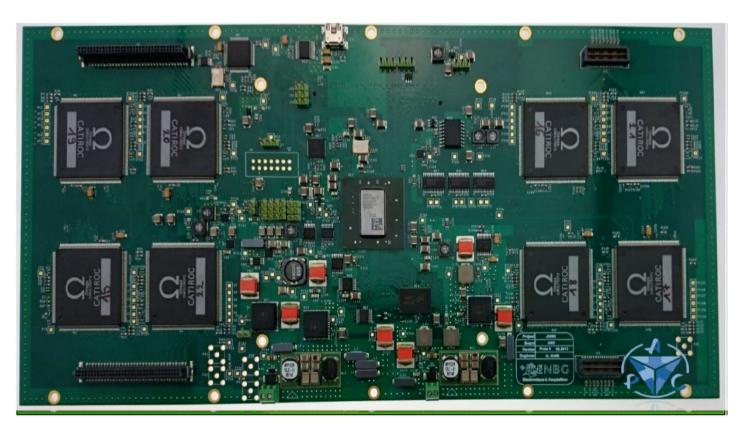• **128 Small PMTs** with a read-out system:

   the Under Water Box (UWB)

• A dedicated FEB based on **CATIROC**

Small PMT front-end board

- SPMT front-end with **8 ASIC CATIROC** each of 16 channels

- **FPGA** (Kindex 7 425-T)+ 2GB DDR3 **RAM memory** (large storage and processing on board)

- **4 connector (2 ERNI, 2 SAMTEC)** x 32 signals (CATIROC inputs)

- Power supply for ASIC and FPGA

- Low cost concept (**one board/ 128 PMTs/** one under water cable to send out data)

CATIROC for JUNO

A complex System on Chip (SoC). Technology: 0.35 µm SiGe AMS

| CATIROC general features	Application to JUNO
16 independent channels	**Reduce the number of electronic** board (only 200 boards for 25,000 SPMTs)
Analog F.E. with **16 trigger outputs +** **charge and time digitization**	**Photon counting +** **charge and time measurements**. Resolutions very good
Autotrigger mode: all the PMTs signals above the threshold (1/3 p.e.) generate a trigger and are converted in digital data	Simplify online-DAQ
100% trigger efficiency @ 1/3 p.e.	**Good 1 p.e. detection** photon counting mode
Dual gain front-end: HG and LG channel Charge dynamic range 0 to 400p.e. (at PMT gain 10^6)	Only **HG** actually used (only few p.e. expected)
Time stamping (resolution ~ 170 ps rms)	**< 1ns required**
Each channel has a **variable gain**	**To compensate gain vs HV spread** for the 16 PMTs
One output for **DATA**	**Less number of cables to the surface**
Hit rate 100 kHz/ch (all channels hit) **50 bits of data / hit channel**	**Very "light" data output** (compared to a FADC waveform)

CATIROC schematic
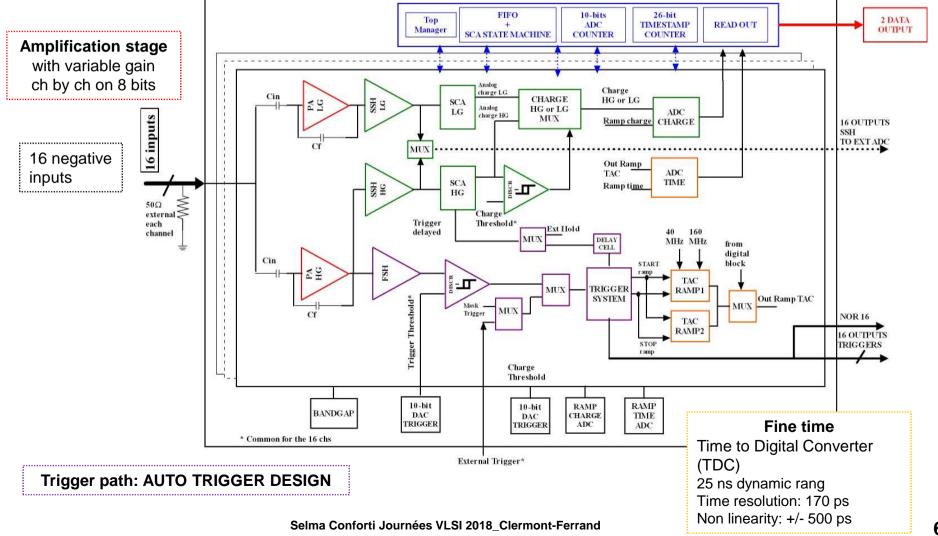
Charge path
- Shaping (variable shaping time)
- Switched capacitor array (**2 Capacitors: ping-pong mode**)
- 10 bits ADC conversion @ 160 MHz
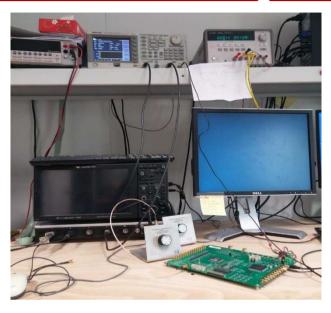- **50 fC ÷ 70 pC (PMT gain 10^6)**

Coarse time
by 26-bit gray counter
(Digital part) 25 ns steps

Amplification stage
with variable gain
ch by ch on 8 bits

16 negative
inputs

Fine time
Time to Digital Converter
(TDC)
25 ns dynamic rang
Time resolution: 170 ps
Non linearity: +/- 500 ps

Trigger path: AUTO TRIGGER DESIGN

The input signal is made by a pulse generator signal: a negative voltage pulse (rise time= 5ns, fall time= 5ns, width= 10 ns, Amplitude @1 p.e.~ 0.8 mV).
The M.I.P. is 1 p.e.= 160 fC @ PMT gain 10^6

Chip status:
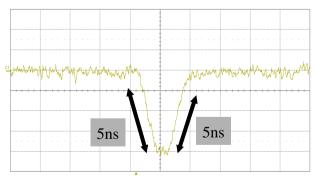Submission: **February 2015**
Received: July 2015
Process: **AMS 0.35 µm SIGe**
Die dimensions: 3.3 mm x 4 mm (13.2 mm²)
Packaging: **LQFP208**
Power Supply: 3.3V
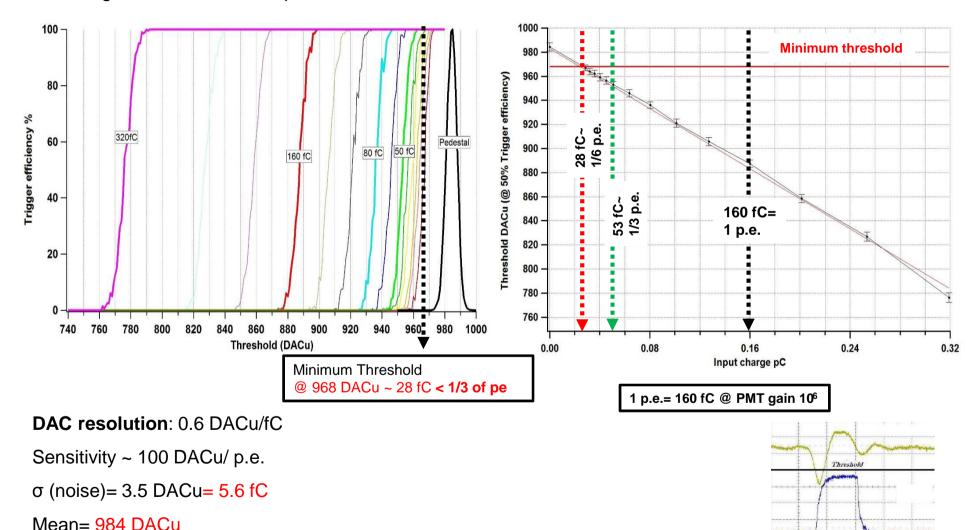Dissipation: **20mW/ch** on 3.3 V
Clocks: 40 MHz (Coarse time) and 160 MHz (Conversion)
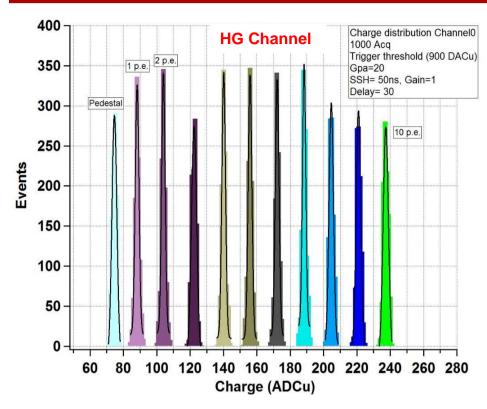

5ns   5ns

Trigger efficiency

The trigger efficiency is investigated by scanning the threshold (by the internal DAC) for a fixed channel and monitoring the discriminator response.
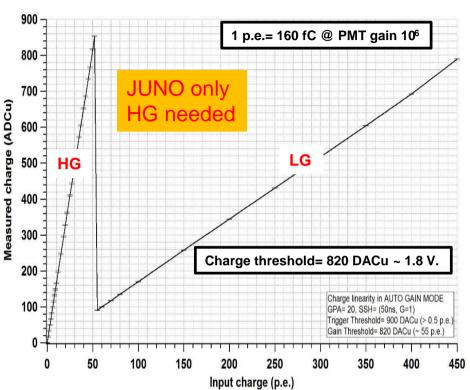

Minimum Threshold
@ 968 DACu ~ 28 fC < 1/3 of pe

1 p.e.= 160 fC @ PMT gain 10^6

DAC resolution: 0.6 DACu/fC

Sensitivity ~ 100 DACu/ p.e.

σ (noise)= 3.5 DACu= 5.6 fC

Mean= 984 DACu

Minimum threshold= Pedestal mean value (DACu)- 5 σ (DACu)= 968 DACu (~ 28 fC)

Charge resolution and linearity

Charge distribution Channel0
1000 Acq
Trigger threshold (900 DACu)
Gpa=20
SSH= 50ns, Gain=1
Delay= 30

HG Channel

Pedestal   1 p.e.   2 p.e.   10 p.e.

1 p.e.= 160 fC @ PMT gain 10^6

JUNO only
HG needed

HG   LG

Charge threshold= 820 DACu ~ 1.8 V.

Charge linearity in AUTO GAIN MODE
GPA= 20, SSH= (50ns, G=1)
Trigger Threshold= 900 DACu (> 0.5 p.e.)
Gain Threshold= 820 DACu (~ 55 p.e.)

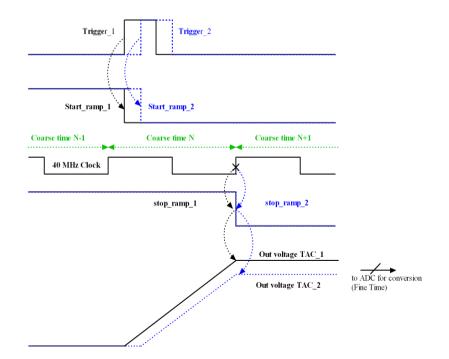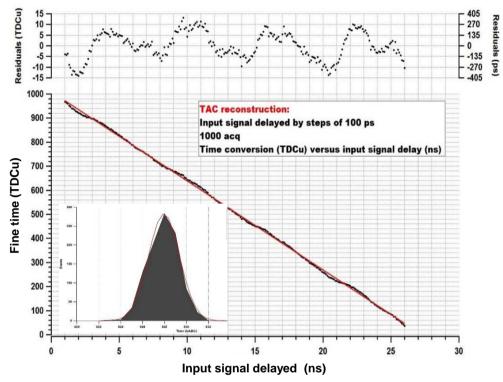|	HG charge performance	LG charge performance
Linearity residuals	< 0.7 % Up to 50 p.e.	< 1 % up to 400 p.e.
LSB	10 fC/ADCu → 16 ADCu/ 1 p.e.	80 fC/ADCu
Charge resolution	1.5 ADCu (HG) ~ **15 fC**	1.2 ADCu (LG) ~ 100 fC

The ASIC provides the signal "time of arrival" operating in self-triggered mode.

The time measurement is composed of two values:

- The "coarse time" (Timestamp)
    - 26-bit Gray Counter with a resolution of 25 ns
    - This time is saved in a 26-bit register when the channel has a trigger indicating a detected signal.
- The "fine" time
    - Two TAC ramps in each channel.

TAC reconstruction:
Input signal delayed by steps of 100 ps
1000 acq
Time conversion (TDCu) versus input signal delay (ns)

TDC measurements: fine time (10 bits)

INL: [-375.3, 356.4] ps

TDC bin= 27 ps

TDC non linearity= 167 ps rms

TDC noise= 38 ps

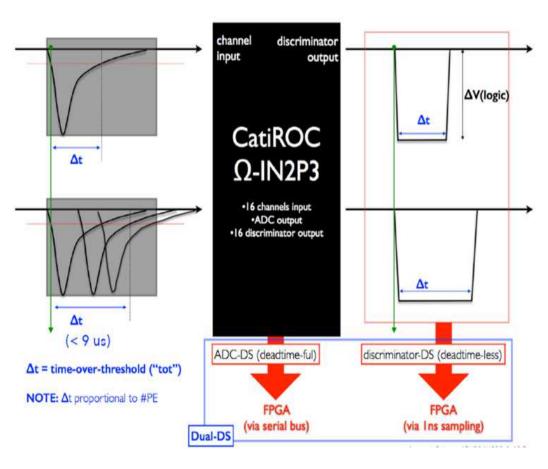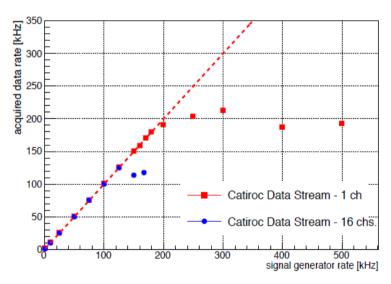**Clock coupling** seen on the TDC (residuals) Well reproducible and may be correct (not need for Juno)

SPMT · Ωmega

HIT RATE			
Tconv (1 ch)	6.4 µs	Tconv (16 ch)	6.4 µs
Tread-out (1 ch)	0.36 µs	Tread-out (16 ch)	3 µs
Tcycle (1 ch)	6.8 µs	Tcycle (16 ch)	9.4 µs
Hit rate (1 ch)	150 kHz	**Hit rate (16 ch)**	100 kHz

$$Tconv = \frac{2^n}{F_{conv}} = 6.4 \ \mu s$$

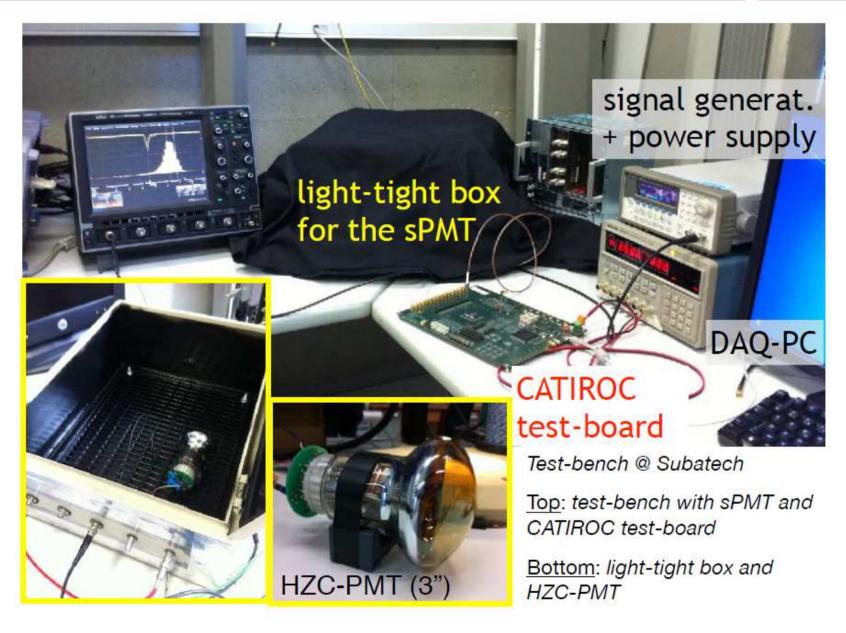$$TRO = \frac{n° \ of \ channels * number \ of \ bit}{F_{RO}}$$

channel input — discriminator output

CatiROC Ω-IN2P3
- 16 channels input
- ADC output
- 16 discriminator output

ΔV(logic)   Δt

Δt

Δt
(< 9 us)

Δt = time-over-threshold ("tot")

NOTE: Δt proportional to #PE

ADC-DS (deadtime-ful)   discriminator-DS (deadtime-less)

Dual-DS

FPGA (via serial bus)   FPGA (via 1ns sampling)

Catiroc Data Stream - 1 ch
Catiroc Data Stream - 16 chs.

16 trigger outputs: a cross check and

a Double DATA Stream (DDS):

- Photon counting

- ToT up to 6 p.e.

signal generat. + power supply

light-tight box for the sPMT

CATIROC test-board

DAQ-PC

HZC-PMT (3")

Test-bench @ Subatech

Top: test-bench with sPMT and CATIROC test-board

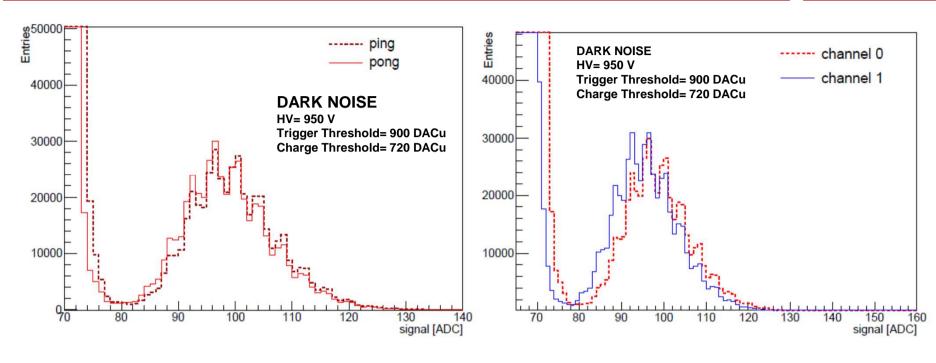Bottom: light-tight box and HZC-PMT
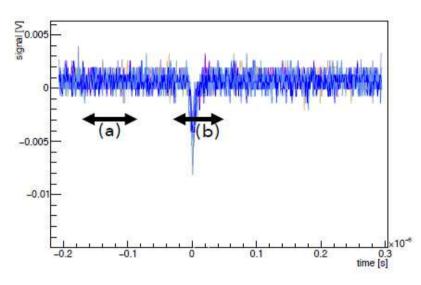
Single p.e. with PMT + Catiroc

Charge resolution: σp.e./ μ p.e.**= 30%**

Ping-pong: charge difference < 5 %

Good **charge uniformity** (only 2 chs)

Wiggles due to the clock coupling

Conclusions

- CatiROC performance fits very well for JUNO-SPMT:
  - 100% trigger efficiency @ **1/3 p.e.** (50 fC @ PMT gain 10^6)
  - Charge resolution (**only HG used**) : 1.5 ADCu ~ **15 fC** (50 fC @ PMT gain 10^6)
  - Time resolution= **167 ps rms**
- Tests with the HZC 3" PMT shows
  - **Good p.e. spectrum**
  - Some features (ping/pong and wiggles) that have not significant effects on the data taking
- To do:
  - **Tests with the ABC board V0 → Ongoing**
  - **ABC V0 Board and a module of 128 PMTs → Test bench in China**
  - **ABC V1 board→ Ongoing (December 2018)**

- **2000 ASICs** CATIROC production at the end of 2018

SPMT

Ωmega

CATIROC
was
conceived
as a
FLEXIBLE
chip
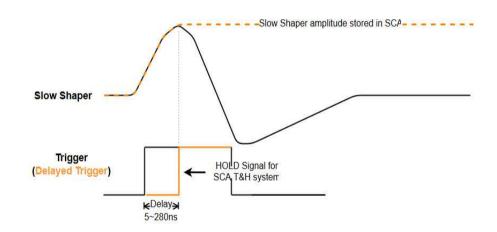
|	
Detector Read-Out	PMTs
Number of Channels	16
Signal Polarity	negative
Sensitivity	voltage
Outputs	16 trigger outputs NOR16 16 slow shaper outputs Charge measurement over 10 bits Time measurement over 10 bits
Main Internal Programmable Features (328 configuration bits)	Variable preamplifier gain Shaping time of the charge shaper (variable shaping and gain) Common trigger threshold adjustment Common gain threshold adjustment
Timing	**Time stamp: 26 bits counter @ 40 MHz** **Fine time**: resolution < 100 ps (simulation) **A TDC ramp for each channel**
Charge Dynamic Range	160 fC up to 100pC
Trigger	**Triggerless acquisition** Noise= 5 fC; Minimum threshold= 25 fC (5σ)
Digital	**Conversion: 10 bits ADC at 160 MHz** **Two Read out: 80 MHz** Read out frame: **50 bits/ch** 2 frames of (29+21) bits 1st frame/8chs: Ch nb= 3; coarse time= 26 2nd frame/8chs: Gain used= 1; Charge converted= 10, Fine time converted= 10
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) die : 3.3 mm x 4 mm
Power Consumption	30 mW/channel
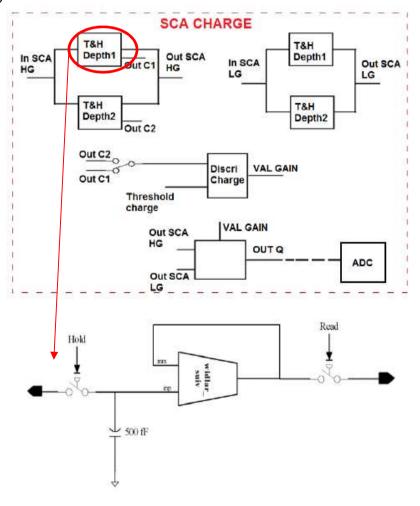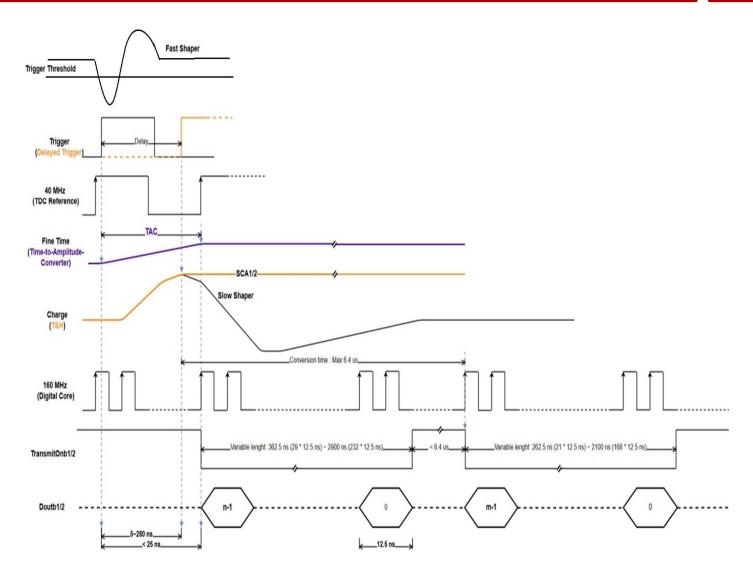
- Shaping (variable shaping time up to 175 ns) (default value tp= 40 ns; RC= 70 ns) and it has 2 function:

  - Optimize the SNR

  - Shape the PA signal in order to allow the charge measurement

- Switched capacitor array (**2 Capacitors: ping-pong mode**)
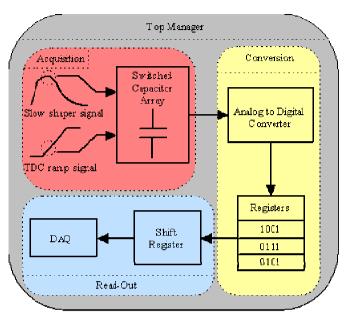
- 10 bits Wilkinson ADC conversion @ 160 MHz

All channels are handled independently

by the digital part

and only channels that have created triggers

are digitized, transferred to the internal memory

and then sent-out in a data-driven way.

The **digital part** manages:

Acquisition: Analog memory: 2 depths for HG and LG

Conversion: Analog charge and time into 10 bits digital values saved in the register (RAM)

Read Out: RAM read out to an external system
- Readout clock : **80 MHz**
- Max Readout time (16 ch hit) : **3 µs**
- **50 bits of data / hit channel**
- **Readout format** (MSB first) : **coarse time**= 26 bits ; **channel number**= 3bits; **fine time**=10 bits, **charge**=10 bits, **gain**=1 bit
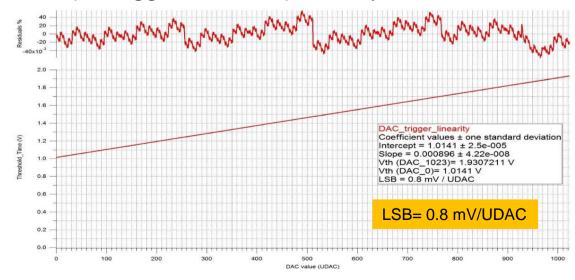
CATIROC measurements @ OMEGA

General test:

- power dissipation per channel : 20 mW/ch
- Input charge made by a pulse generator: 1 p.e. = 160 fC @ PMT gain 10^6
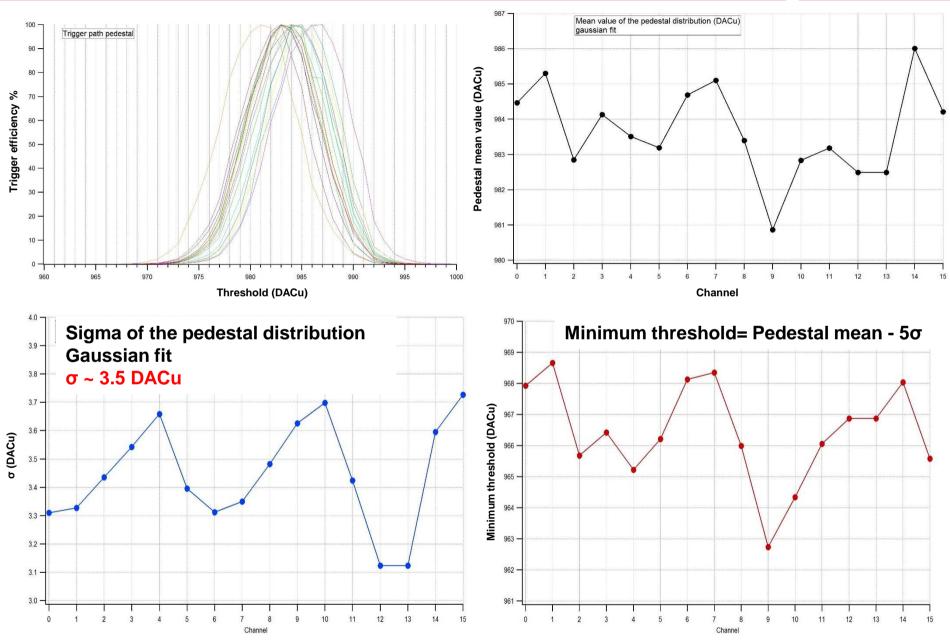- Analog signals OK:

1 p.e. = 160 fC PA: (gain= 20), SSH: (50ns, gain=1)	PA_HG Meas.	PA_HG Sim.	SSH_HG Meas.	SSH_HG Sim.	FSH_HG Meas.	FSH_HG Sim.
Peaking time (ns)	10	5	33	40	7	5
GAIN (mV/p.e.)	10	13.5	15	16	77	108
NOISE (mV)	0.6	0.67	1	1	2.8	3.4
SNR	16.6	20.1	15	16	28	32

- DAC (for trigger threshold) linearity OK :

DAC_trigger_linearity
Coefficient values ± one standard deviation
Intercept = 1.0141 ± 2.5e-005
Slope = 0.000896 ± 4.22e-008
Vth (DAC_1023)= 1.9307211 V
Vth (DAC_0)= 1.0141 V
LSB = 0.8 mV / UDAC

LSB= 0.8 mV/UDAC

Pedestal: min= 966.64 UDAC; max= 971.9 UDAC; mean= 969.52 UDAC; delta= 5.25 UDAC

1 pe: min= 885.77 UDAC; max= 889.93 UDAC; mean= 887.83 UDAC; delta= 4.16 UDAC

2 pe: min= 788.14 UDAC; max= 793.48 UDAC; mean= 790.9 UDAC; delta= 5.34 UDAC

3 pe: min= 689.19 UDAC; max= 695.54 UDAC; mean= 691.84 UDAC; delta= 6.42 UDAC

5min= 483.6 UDAC; max= 496.2 UDAC; mean= 490.4790.9 UDAC; delta= 12.6 UDAC

50 % trigger efficiency all channels

ToT (Time over Threshold)

Charge linearity (DATA)_NO pedestal

Charge linearity ch0 (PA_gain= 20);(ssh= 50 ns, G=1):
LG:
Trigger threshold= 0.5pe, Gain threshold= 55 p.e.
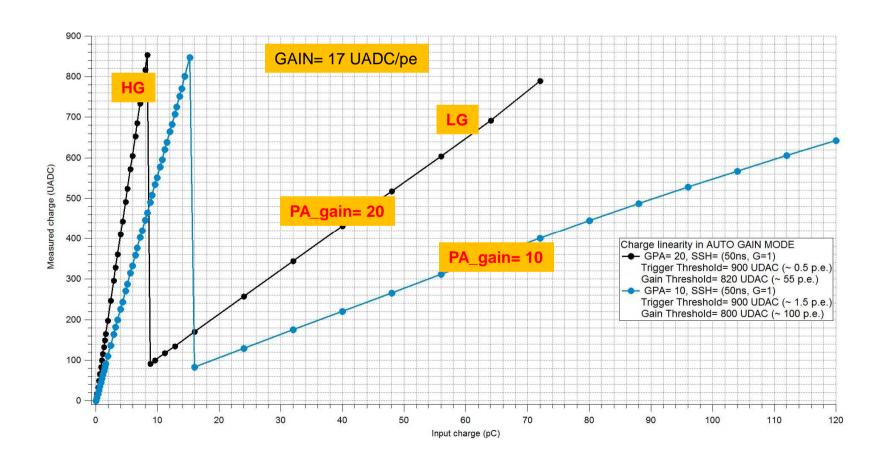Residuals%: [-0.5, 1] % up to 70 pC
LSB= 0.5 p.e.= 80 fC
HG:
Trigger threshold= 0.5pe, Gain threshold= 55 p.e.
Residuals%: [-0.7, 0.5] % up to 9 pC
LSB= 0.06 p.e.= 10 fC

Charge linearity ch0 (PA_gain= 10);(ssh= 50 ns, G=1):
LG:
Trigger threshold= 1.5pe, Gain threshold= 100 p.e.
Residuals%: [-2.3, 1.3] % up to 120 pC
LSB= 1 p.e.= 160 fC
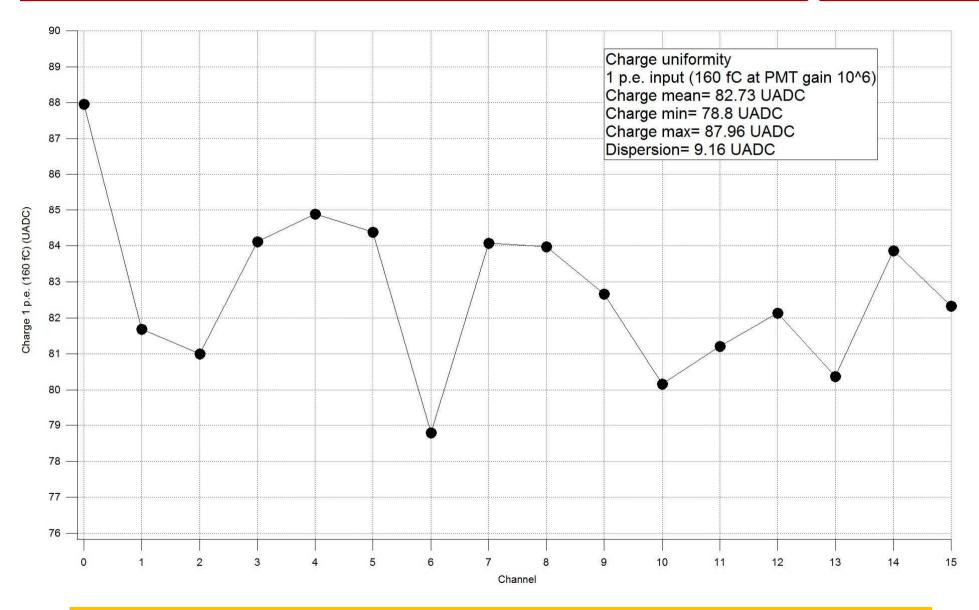**HG:**
Trigger threshold= 1 pe, Gain threshold= 100 p.e.
Residuals%: [-0.4, 1] % up to 15 pC
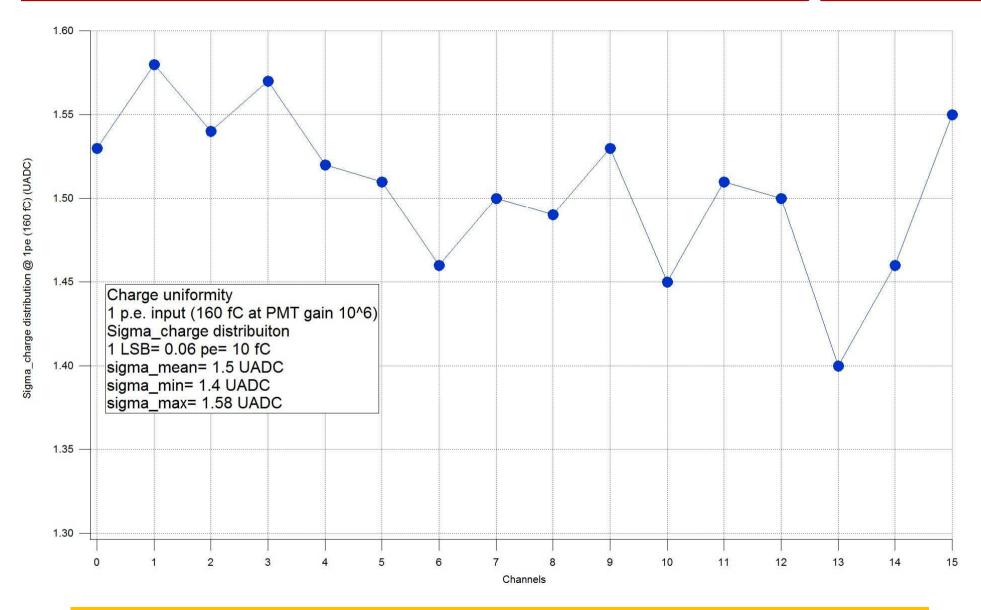LSB= 0.1 p.e.= 16 fC

Charge uniformity (DATA) @ 160 fC (1 pe)

Charge uniformity
1 p.e. input (160 fC at PMT gain 10^6)
Charge mean= 82.73 UADC
Charge min= 78.8 UADC
Charge max= 87.96 UADC
Dispersion= 9.16 UADC

Dispersion= 9.16 UADC*10 fC (LSB_HG)= 91.6 fC= 0.57 p.e. (1 p.e. @ 160 fC)
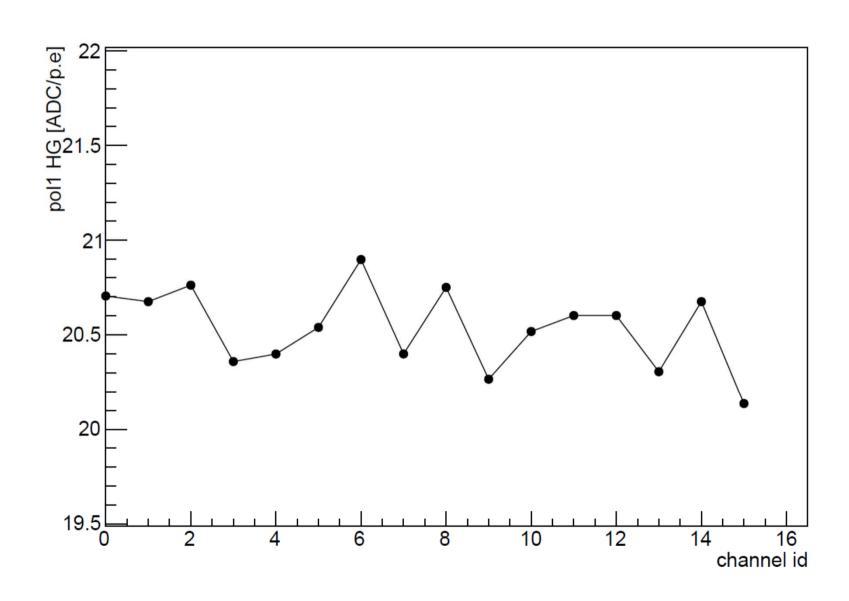
Charge uniformity (DATA) @ 160 fC (1 pe)

Charge uniformity
1 p.e. input (160 fC at PMT gain 10^6)
Sigma_charge distribuiton
1 LSB= 0.06 pe= 10 fC
sigma_mean= 1.5 UADC
sigma_min= 1.4 UADC
sigma_max= 1.58 UADC
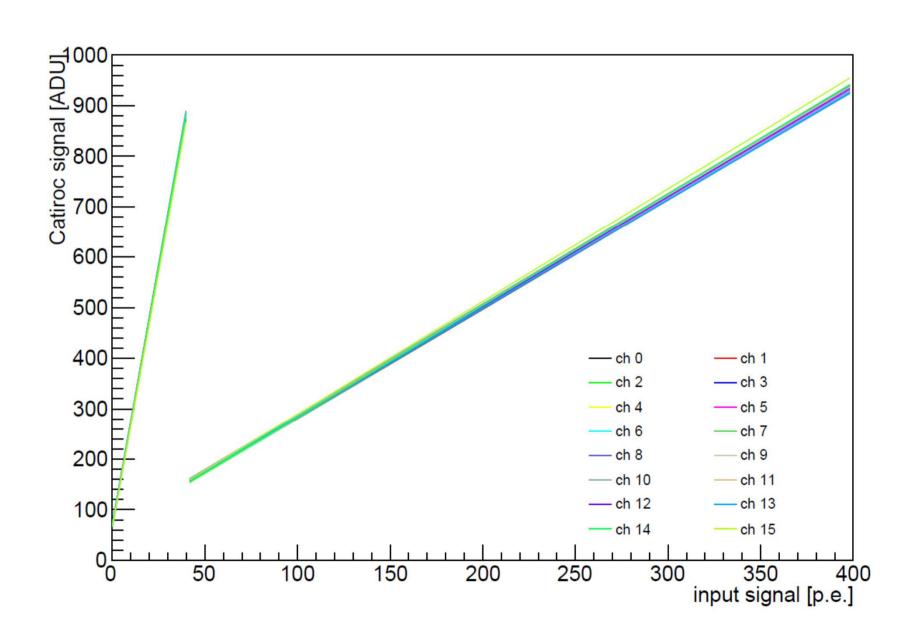
Sigma mean= 1.5 UADC*10 fC (LSB_HG)= 15 fC= 1/10 p.e. (1 p.e. @ 160 fC)
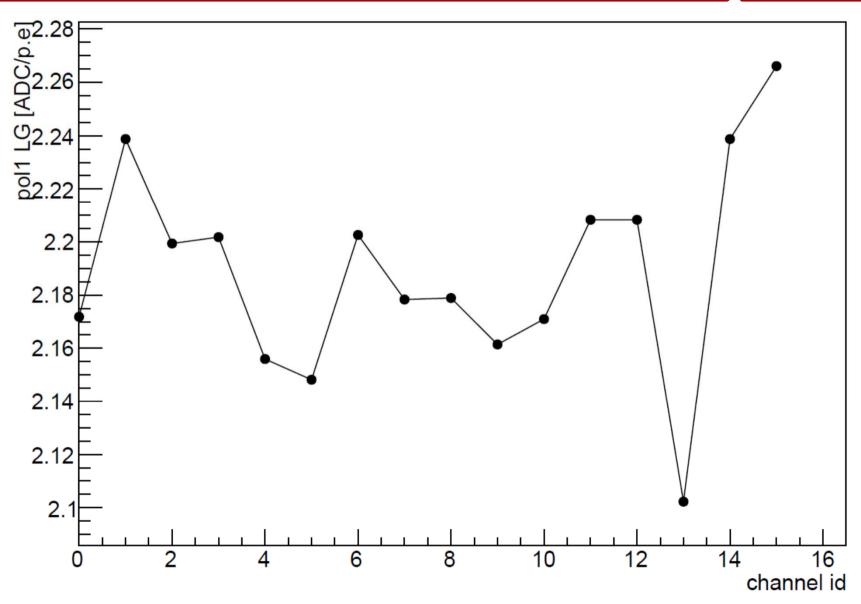
Charge linearity all channels

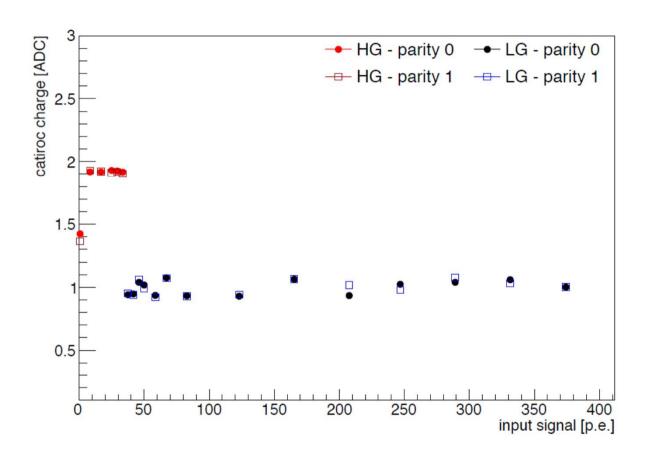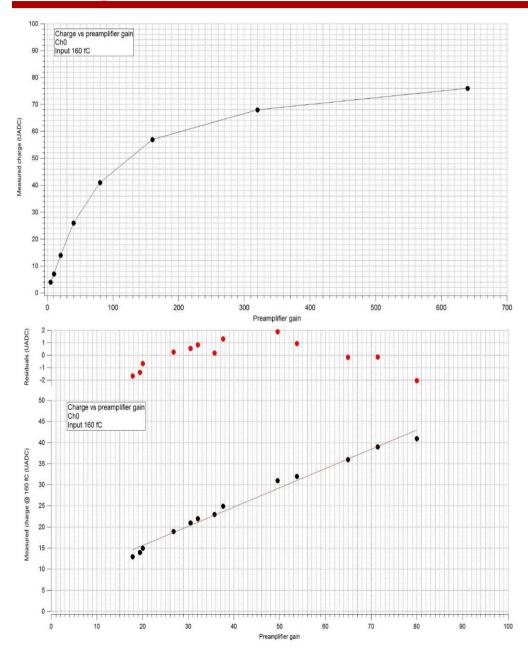# Charge linearity: slope distribution lg

Charge rms

RMS of the charge histograms. Same results in all channels. Wide signal range

Preamplifier gain= Cin/Cf so we have 256 gain values
Example:

GAIN	CIN pF	CFpF
16.02	5	0.25+0.062
17.30	5	0.25+0.031+0.008
17.79	5	0.25+0.031
…..		
80	5	0.062

The minimum Cf step is of 0.008 pF
With a gain of 20:
$G=Cin/Cf= 5/0.25p=20$
$G1=Cin/Cf=5/0.25p+0.008p=19.38$
$\Delta G/G= 20-19.38/20=0.032 \sim 3.2\%$
With a gain of 40:
$G=Cin/Cf= 5/0.125p=40$
$G1=Cin/Cf=5/0.125p+0.008p=37.59$
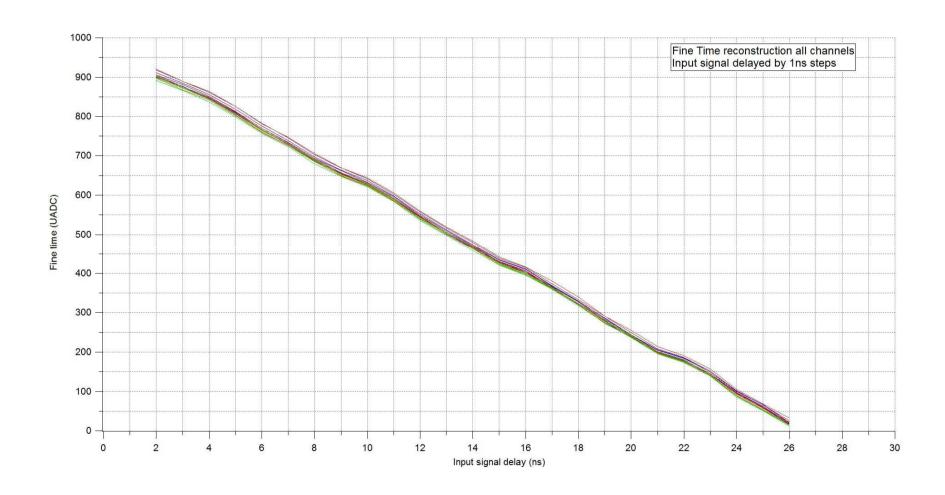$\Delta G/G= 40-37.59/40=0.06 \sim 6\%$

Figure shows the measured charge vs the preamplifier gain for an input signal of 160 fC(1pe)
The plot is linear from Gain= 16.2 to Gain=80
Before 16.2 the gain is too small to trigger at 1/3 of pe, after gain 80 the charge is saturated.

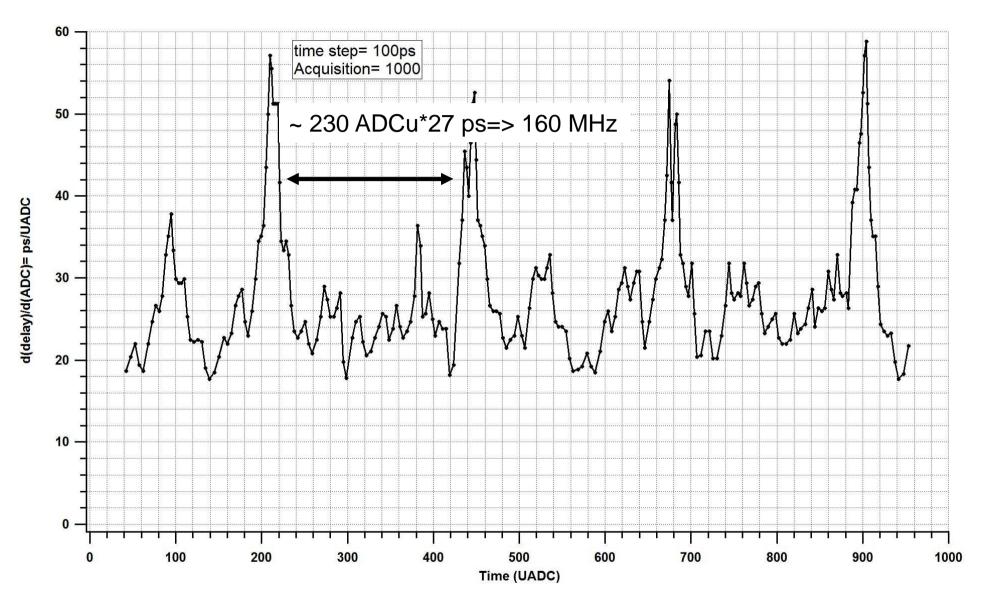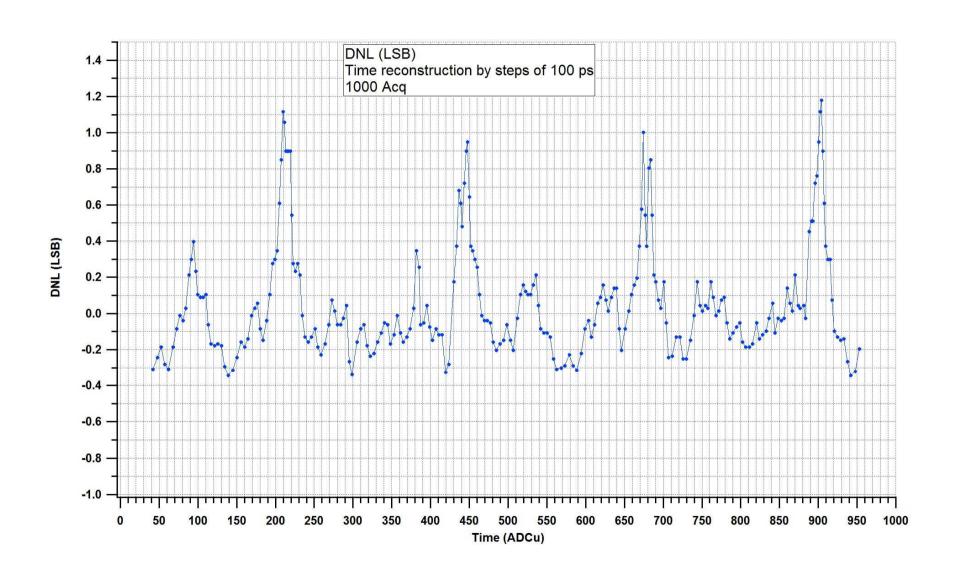# TAC reconstruction (Dout) all channels

TAC all chs:
Intercept dispersion: 27.26 UADC= 736 ps
Slope dispersion= 0.572 UADC/ns= 1.74 ns/UADC

DNL (LSB)
Time reconstruction by steps of 100 ps
1000 Acq

TDC residuals Zoom

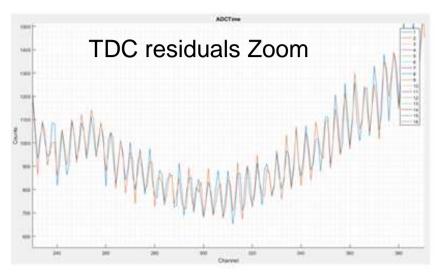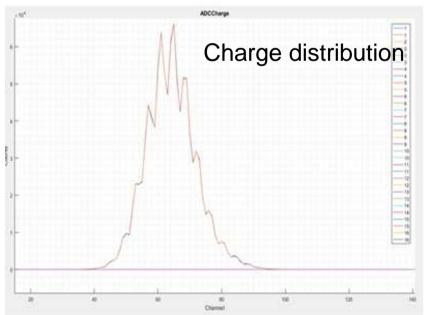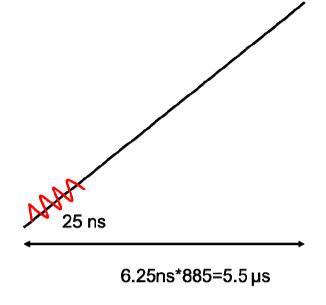Charge distribution

25 ns

6.25ns*885=5.5 µs

The small peaks: indicate the 40 MHz coupling on the ADC ramp.

This is visible on the time and charge conversion.

Peaks every 4 ADCu
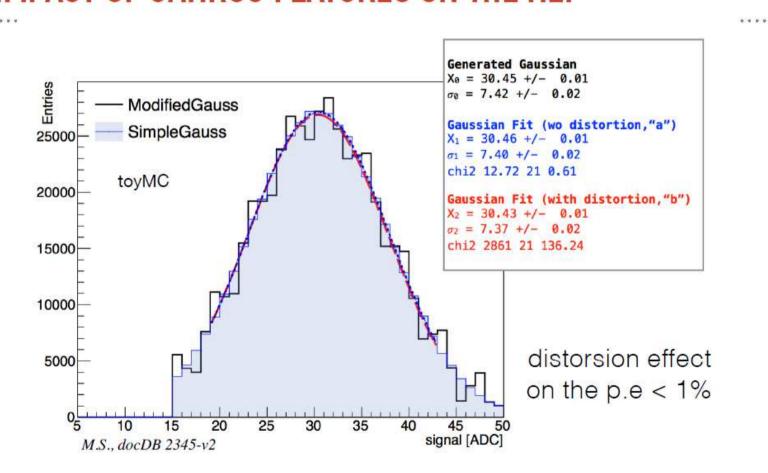
The ADC range is of 885 ADCu -> 885 Adcu*6.25 ns= 5.5 µs

5.5 µs/ 25 ns (40 MHz period) = 221.25

885 ADCu/221.25 = 4

IMPACT OF CATIROC FEATURES ON THE P.E.

Generated Gaussian
$X_0 = 30.45 +/- 0.01$
$\sigma_0 = 7.42 +/- 0.02$

Gaussian Fit (wo distortion,"a")
$X_1 = 30.46 +/- 0.01$
$\sigma_1 = 7.40 +/- 0.02$
chi2 12.72 21 0.61

Gaussian Fit (with distortion,"b")
$X_2 = 30.43 +/- 0.01$
$\sigma_2 = 7.37 +/- 0.02$
chi2 2861 21 136.24

distorsion effect
on the p.e < 1%

ModifiedGauss
SimpleGauss

toyMC

M.S., docDB 2345-v2

ToyMC to study the impact of the wiggle effect on the resolution and mean P.E. position for different width of the s.p.e distribution and for different Φ