HGCROC for CMS HGCAL Readout ASIC

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On behalf of CMS collaboration

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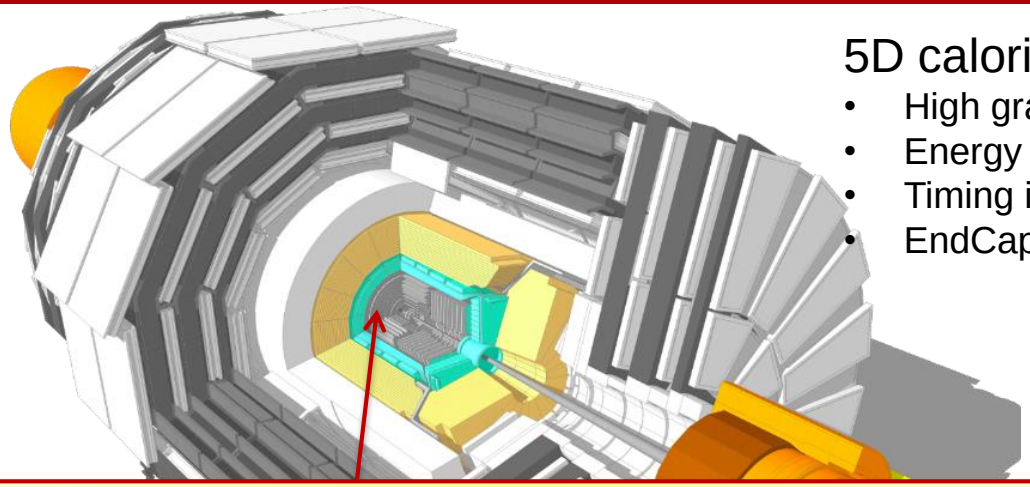
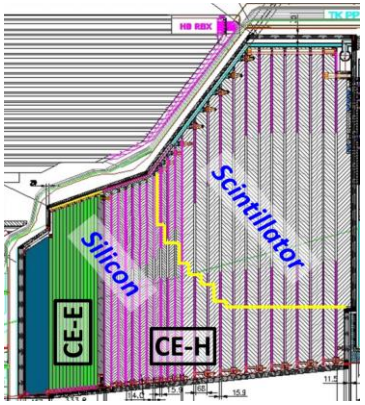
Organization for Micro-Electronics desiGn and Applications

HGCAL: CMS EndCap Calorimeters for the LHC Phase-II upgrade



5D calorimetry: x, y, z, E, t

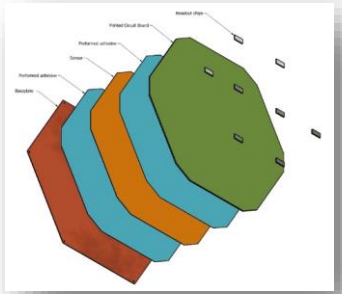
- High granularity ➔ Millions of channels ➔ low power
- Energy measurement: large dynamic range (0,1fC/10pC)
- Timing information: pile-up mitigation, need few tens of ps
- EndCap calorimetry ➔ 200 Mrad, 1E16 N



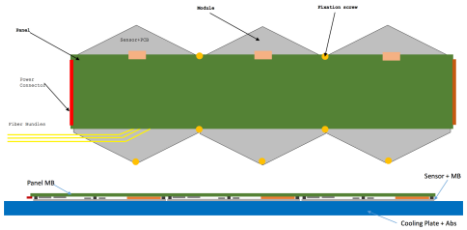
New Endcap Calorimeters

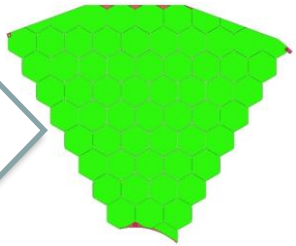
- Rad. tolerant
- High Granularity: increased transverse and longitudinal segmentation, needed to mitigate pileup effects to select events with a hard scatter process at L1-Trigger and to identify the associated vertex and particles
- precise timing capability: further mitigation of pileup effects

Modules (22k)
Glued stack of W/Cu baseplate, kapton, Hexagonal 8" Si sensor, PCB



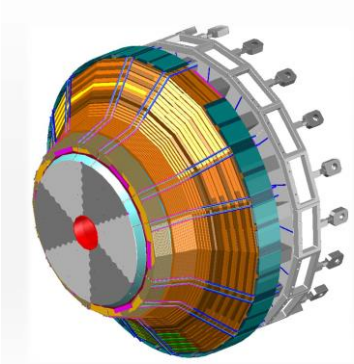
Motherboard Panel with concentrator ASIC and optical transmitters to readout data and trigger data of 6M channels





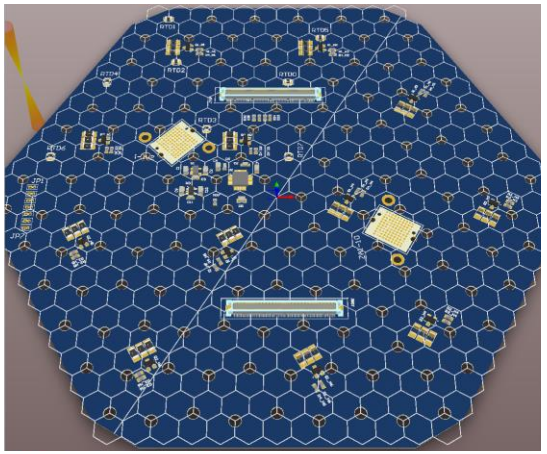
Cassette

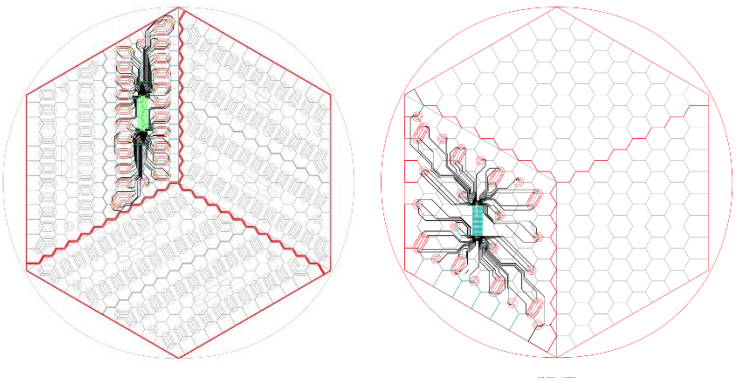
Cassettes mounted together to form the **ECAL (EE)** and **Front HCal (FH)**

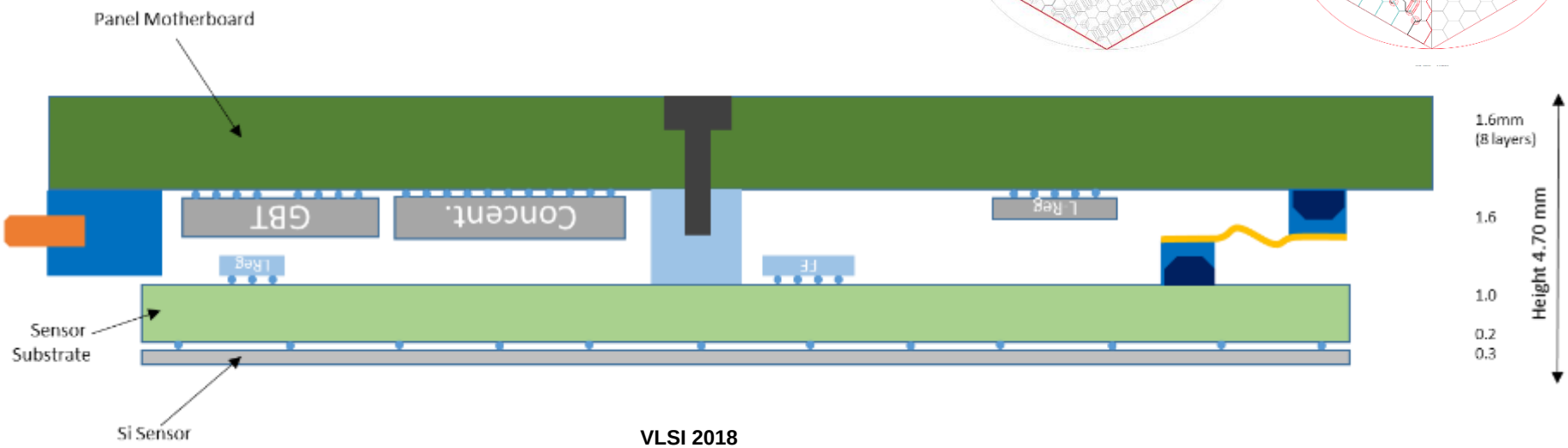


Challenges for electronics

- Stringent requirements for Front-End Electronics
  - Low power (~10mW for analogue channel, ~5mW for digital)
  - low noise (< 2000 e-), MIP ~ 1-4 fC
  - Detector capacitance 40 – 60 pF, 10µA max. leakage
  - High dynamic range: up to 3000 MIP (10pC), 17 bits required with 0,1 fC resolution
  - Time measurement: 20 ps resolution, PU mitigation
  - High radiation (200 Mrad, 10^E16 N)
  - System on chip (charge, time, digitization, data and trigger processing, on-chip zero-supress…)
  - High speed readout (1,28 Gb/s)
  - ~ 1^E5 FE chips

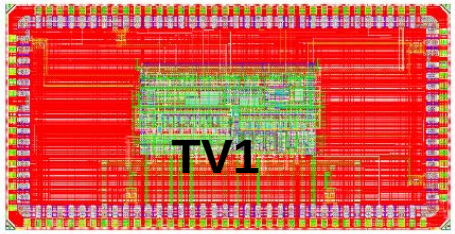




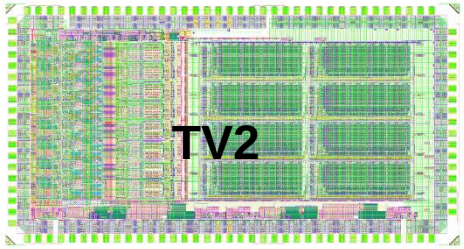


4 ASICs submitted in the past two years

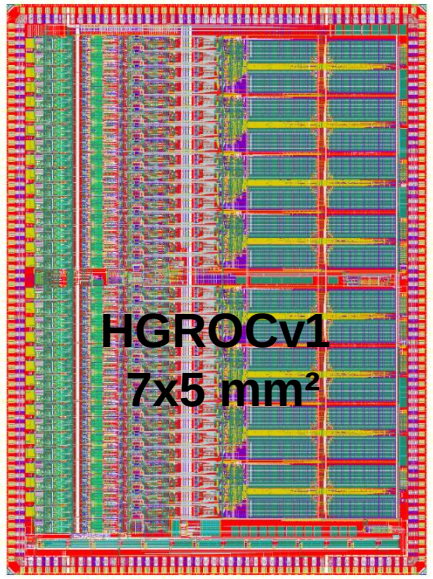
- **SKIROC2_CMS**
  - SiGe 350 nm
  - Submitted in January 2016
  - Dedicated to test beam



- 1st test vehicle: **TV1**
  - CMOS 130 nm
  - Submitted in May 2016, received in august 2016
  - Dedicated to preamplifier studies



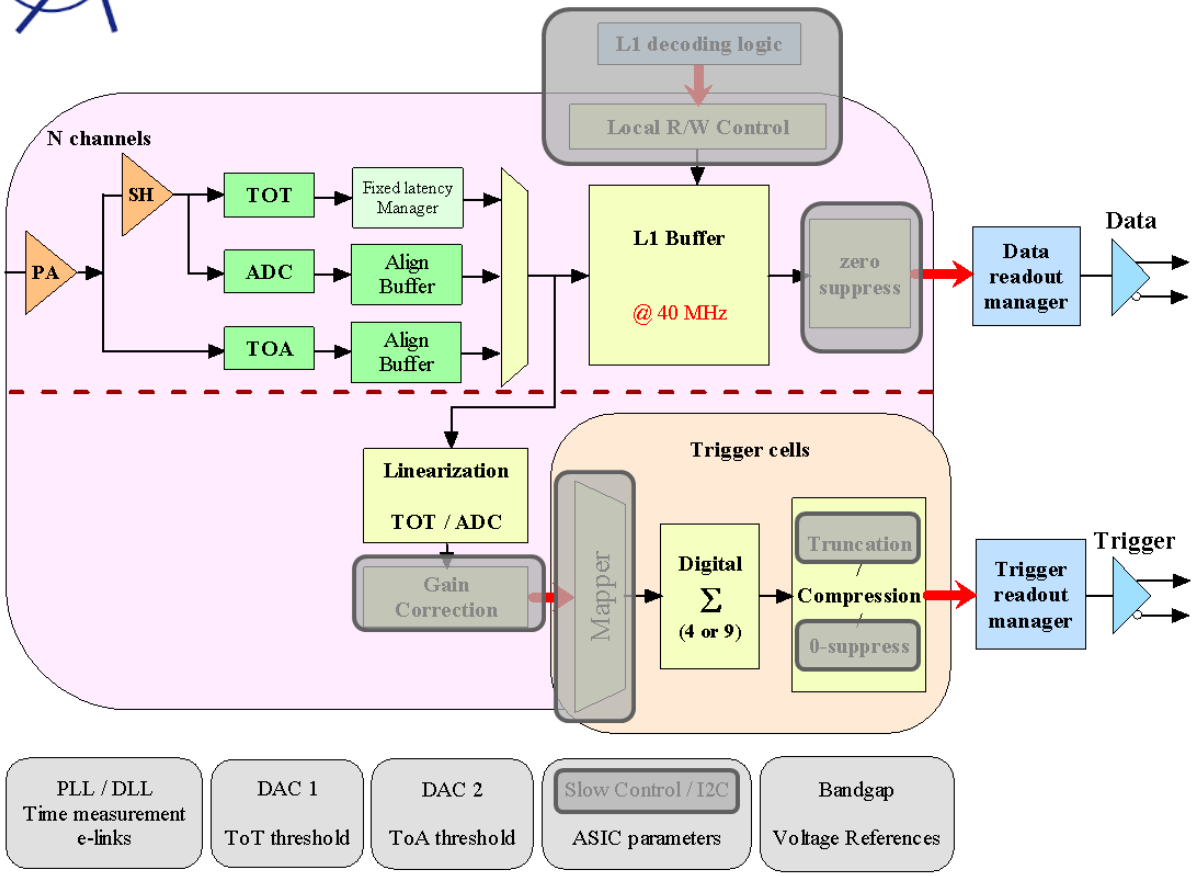
- 2nd test vehicle: **TV2**
  - CMOS 130 nm
  - Submitted in December 2016, received in may 2017
  - Dedicated to technical proposal' analog channel study
- **HGROCv1**
  - CMOS 130 nm
  - Submitted in July 2017, received in Nov 2017
  - all analog and mixed blocks; large part, but not complete, digital blocks

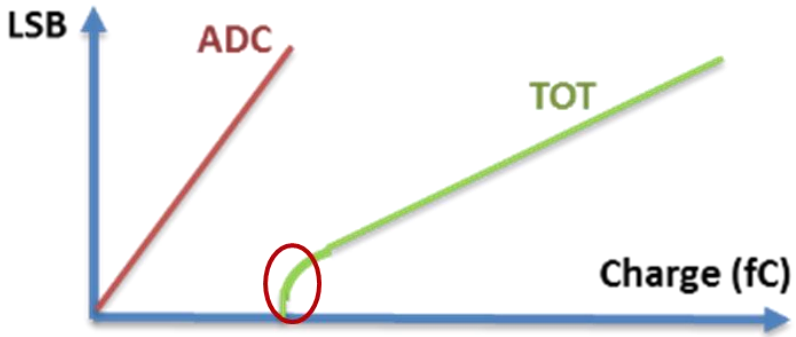


HGROCv1

HGROCv1 features:

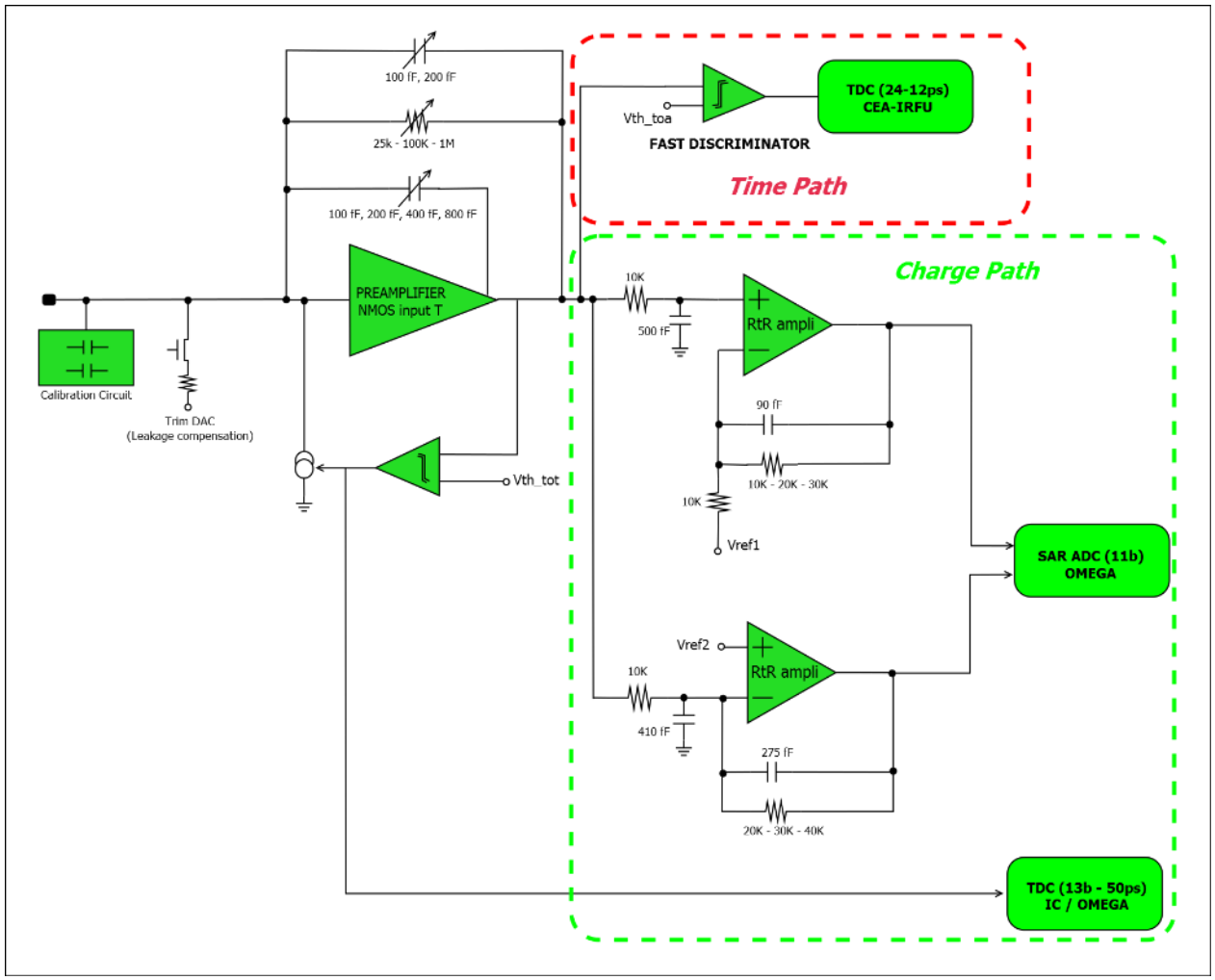
- 32 channels
- Dual polarity
- TOT with 2 variants:
  - Low power @ Imperial
  - DLL @ OMEGA (CERN based)
- TOA (CEA-IRFU)
- 11-bit SAR ADC @ 40MHz (OMEGA)
- Simplified Trigger path
  - Only sum by 4
  - No 0-suppress (4+4 log)
- Data readout @ 320MHz
- SC with triple voting (like SK2-CMS)
- Many digital block with simplified architecture
- Services
  - Bandgap from CERN
  - PLL from CEA-IRFU
  - 10b DAC from TV2





Analog and Mixed channel

- DC coupled
- Preamplifier gain adjustable on 4bit
- New shaper without SK
  - In a next version, with SK and tunable shaping time and gain
- Decay time given by R_{f_pa}
  - 25K
  - 100K
- New TOT architecture
  - Gain adjustable by SC
  - Undershoot ➔ dead time
  - In a next version, find a way to remove/reduce it (dynamic reset)
- New TOA fast discriminator
  - In a next version, higher preamp bias current and fast output to improve the time measurement
- Local 5bit DAC to adjust the Vrefs and the thresholds
- Local input current DAC to compensate the leakage
- Internal calibration circuit
  - Low range up to 600 fC
  - High range up to 12 pC

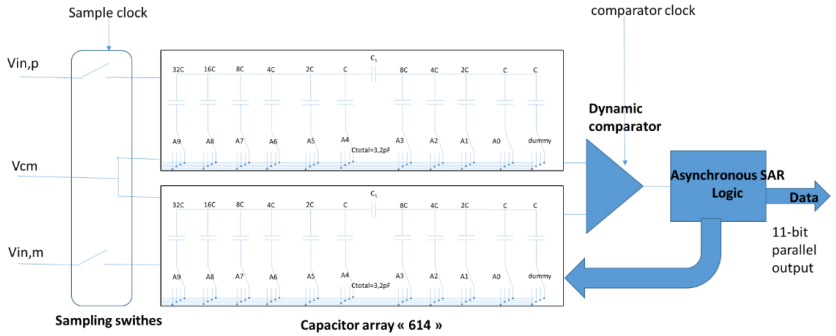


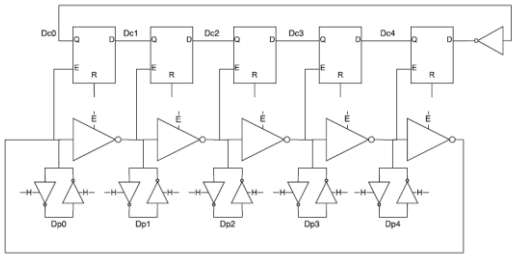
Power dissipation @ 1,5V supply

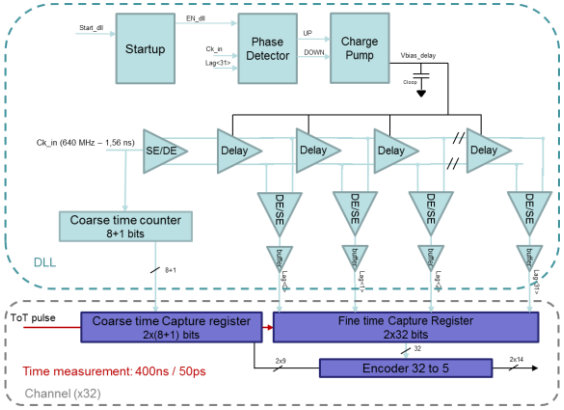
- Vdda (preamp): 1,6mA
- Vdd (tot): 160µA
- Vdd(shaper, toa): 1,1mA

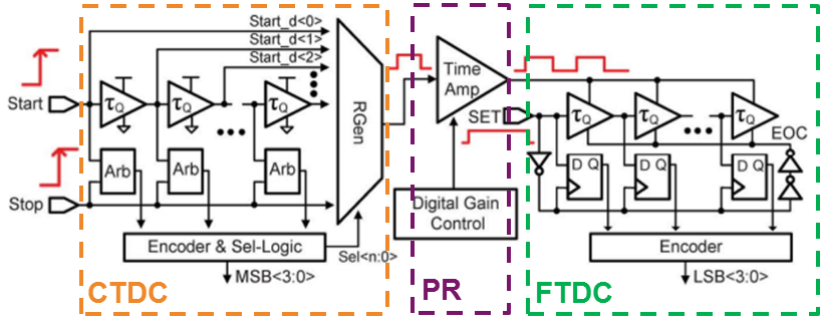
New mixed-signal circuits

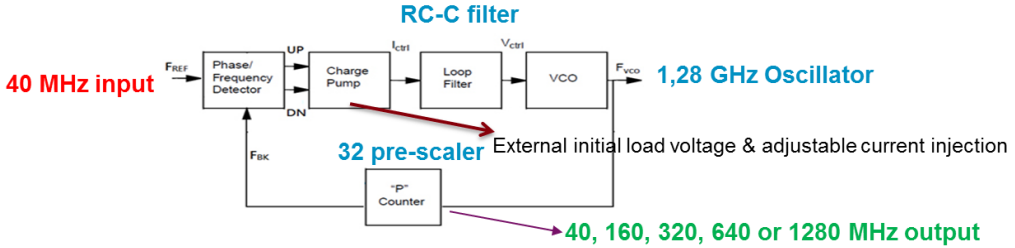
- ADC SAR
  - Inspired from Krakow design, 11 bit
- 2 TDCs for TOT
  - IC design, 50ps/200ns, based on a ring oscillator
  - OMEGA design, 50ps/400ns, based on a global DLL running at 640MHz
- TDC for TOA
  - CEA-IRFU design
  - 10/11 bit
- PLL
  - CEA-IRFU design
  - 40MHz input clock
  - 1,28GHz running frequency



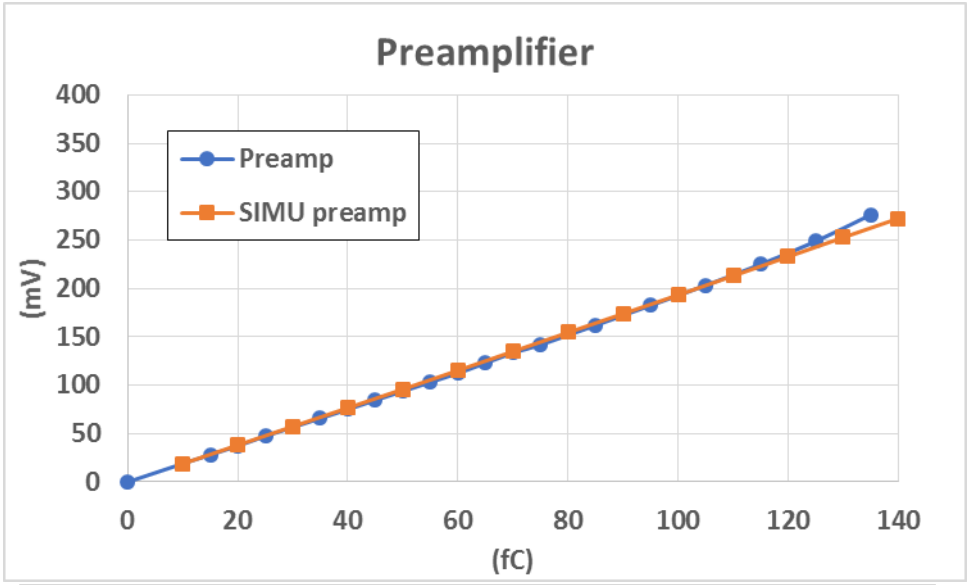


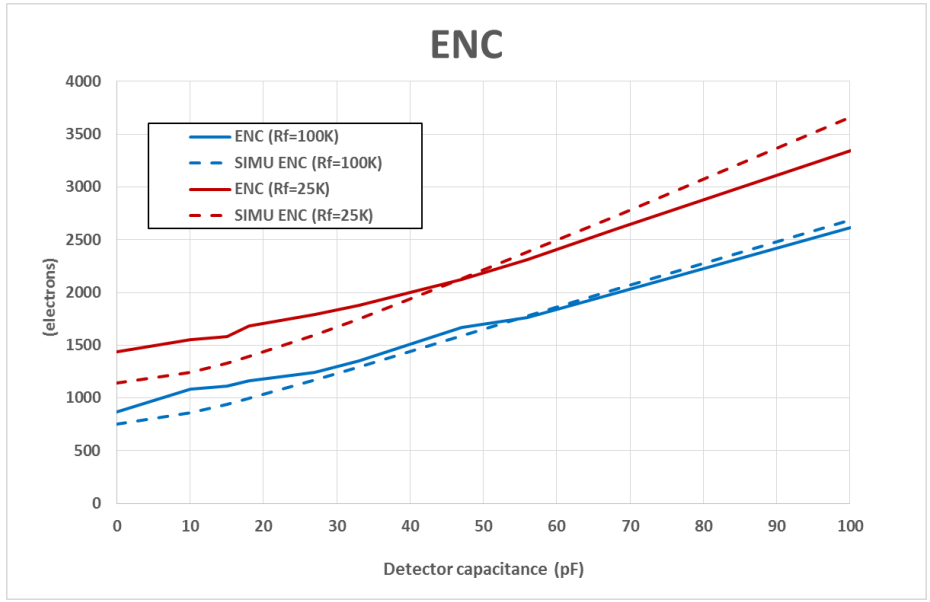


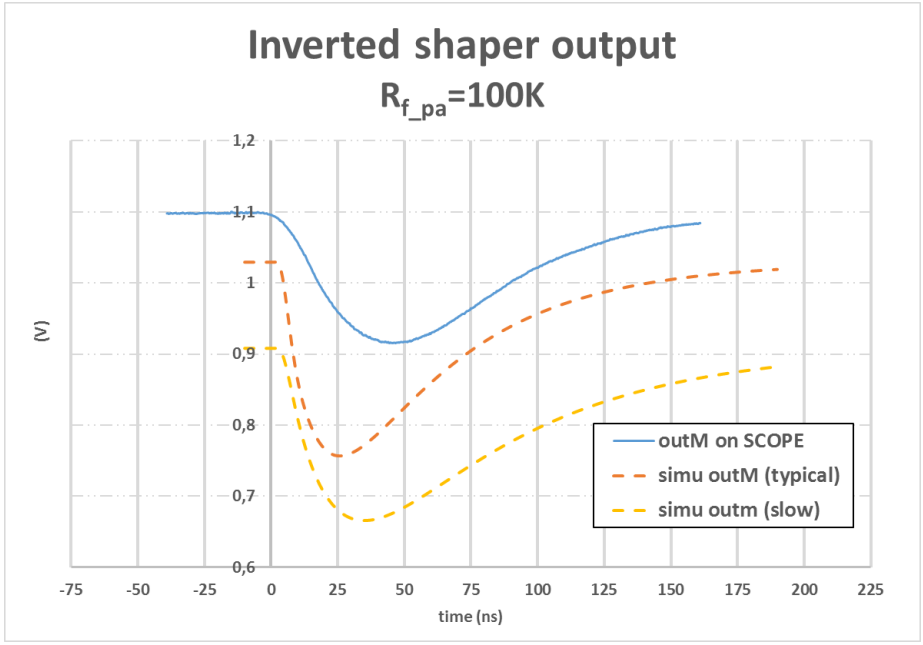




Analog measurements (May 2018)

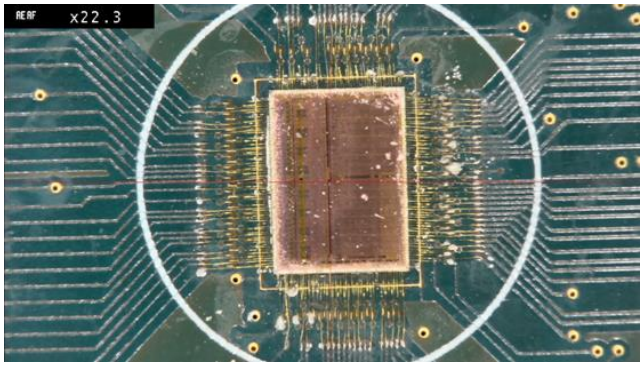






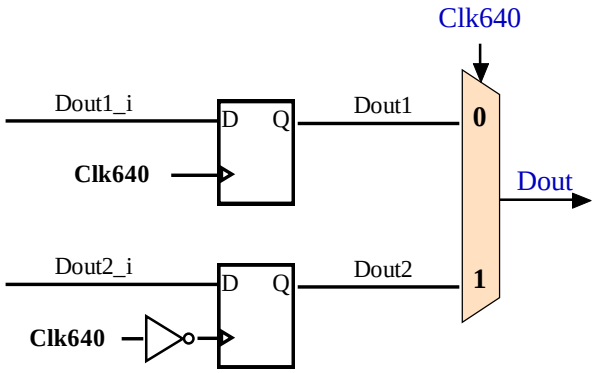
Ralated to bonding issues ?

New boards available by the end of May

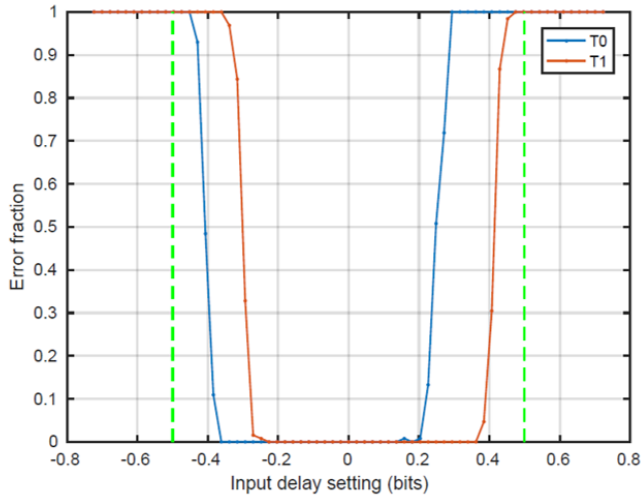


HGROCv1: elink for trigger readout

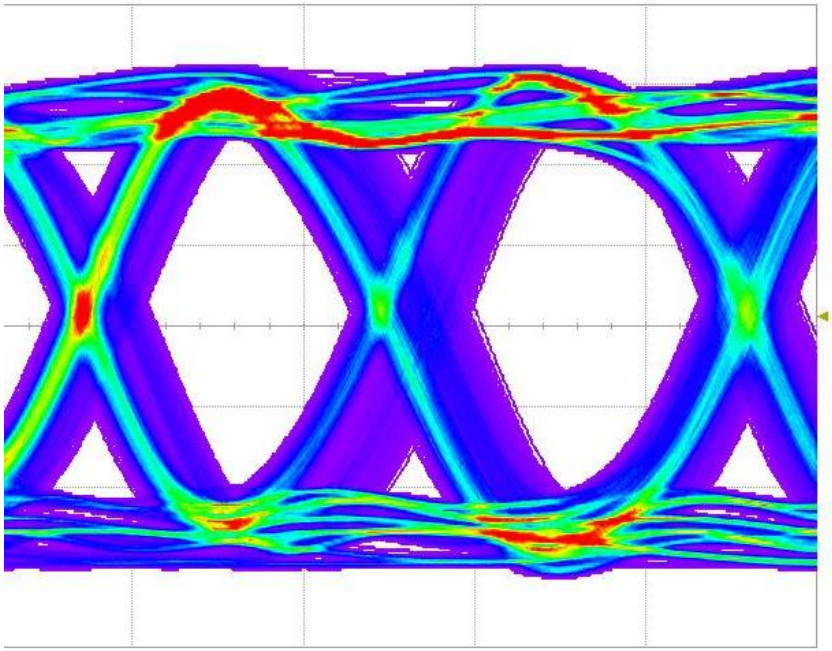
- The chip integrates 2 elink transmitter to handle the 64 bits from the trigger path
  - 4 channels are encoded into 8 bits (with 4+4 encoding)
  - 2 variants (fully digital or mixed ➔ way the last mux is done)
  - Possibility to readout a known frame (set by SC)
  - Default is 1,28 Gb/s (DDR)



Specification description	Value
Max speed	1,28 Gb/s
Levels	CLPS (LpGBT)
Pre-emphasis	Yes (Programmable)
Sync Pattern	Yes
Vcm (common voltage)	0,6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0,5 to 4 mA
Termination load	100 Ω

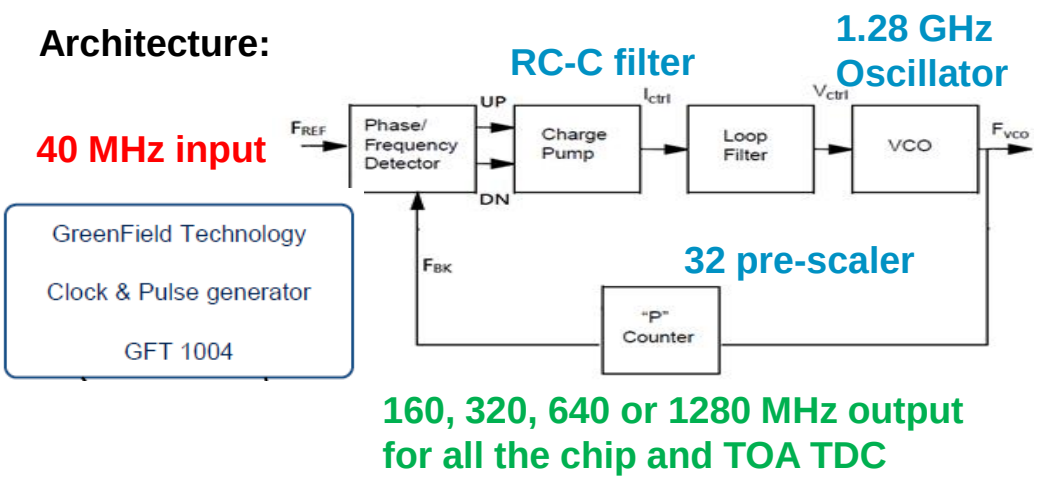


Imperial College London



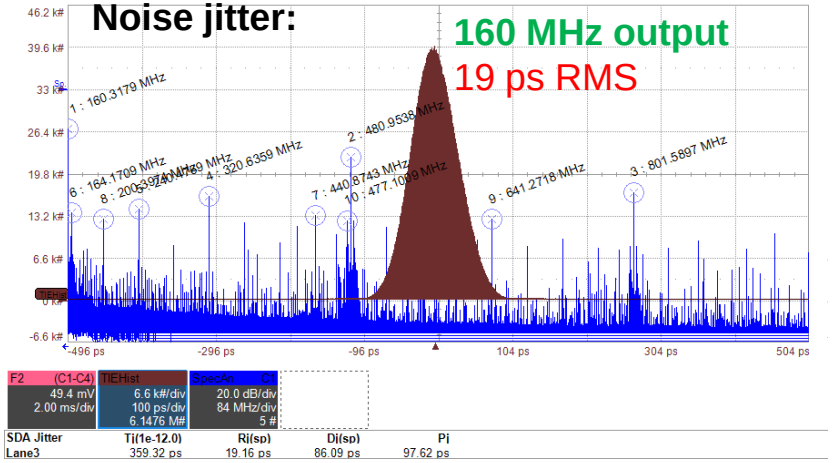
PLL MESUREMENT

Architecture:



Noise jitter:

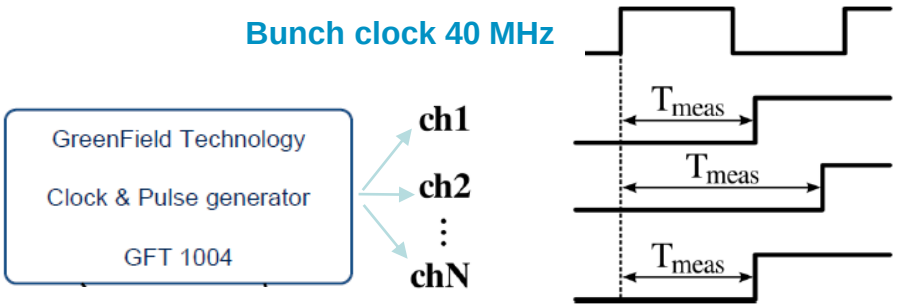
160 MHz output
19 ps RMS



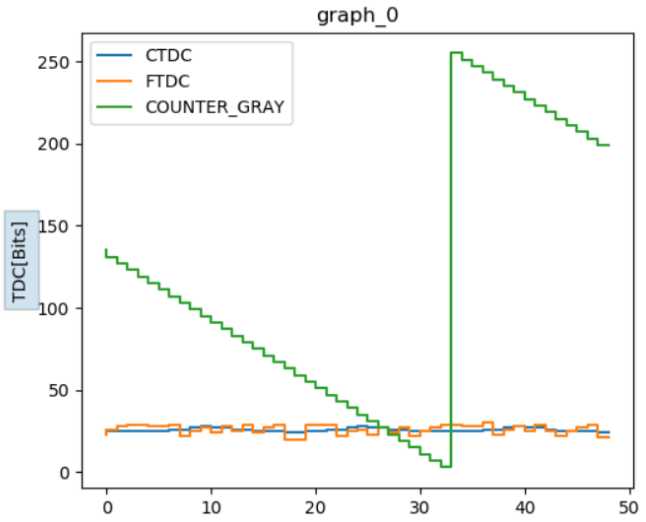
TDC for ToA measurements :

Multi channel TDC

Bunch clock 40 MHz



Data reconstruction: 50 events



The time conversion result is composed of:

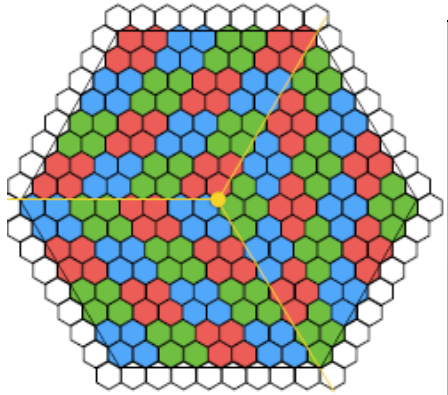
Gray counter (8 bits)

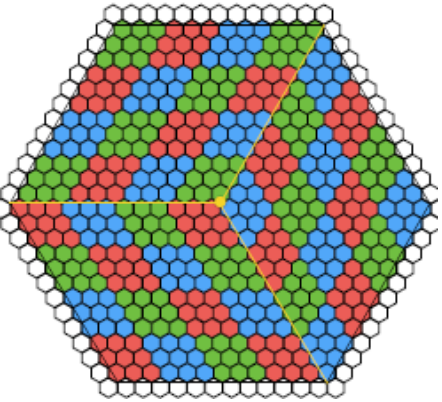
Coarse TDC (CTDC) (5 bits)

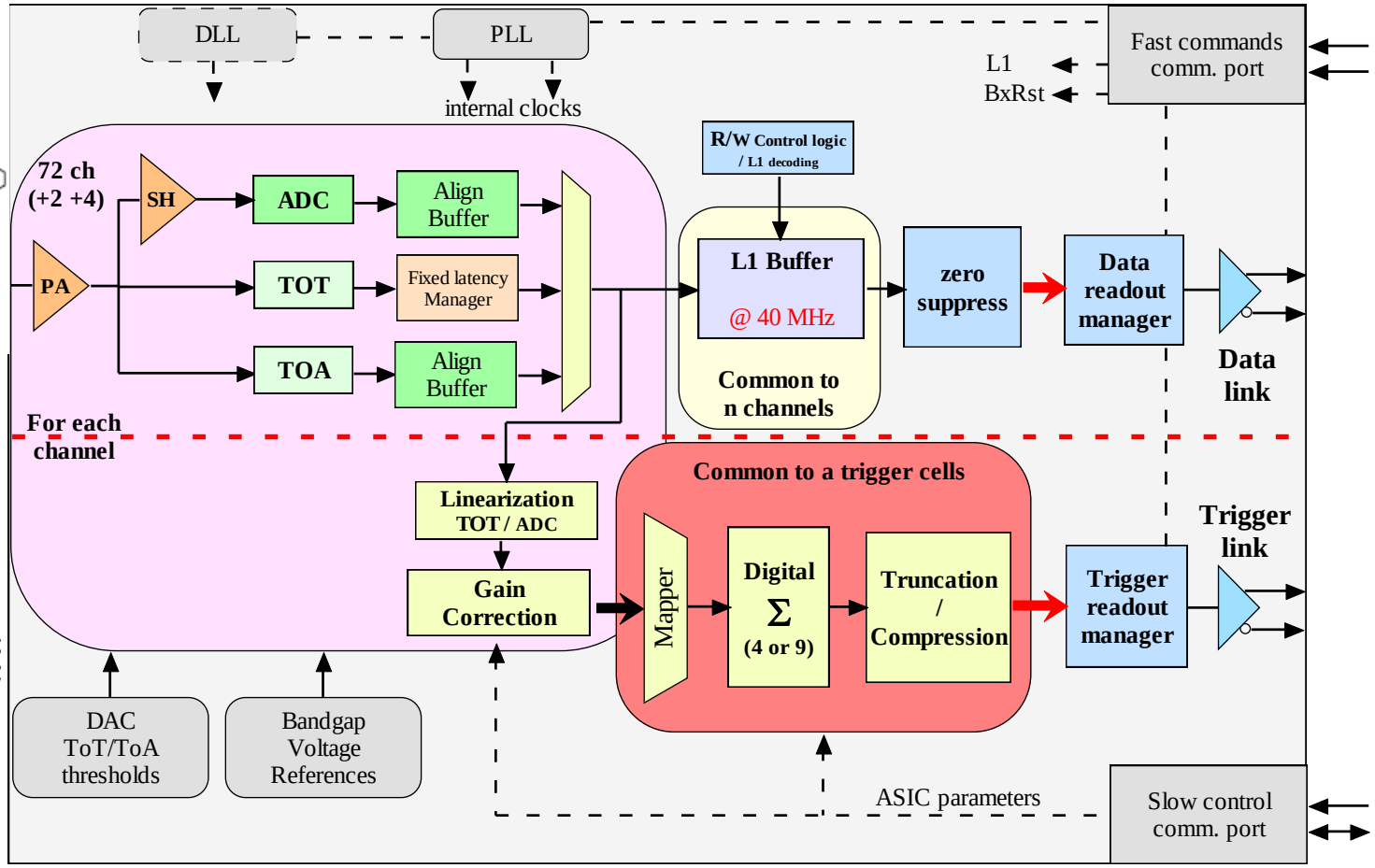
Fine TDC (FTDC) (5 bits)

All channels work in parallel with the same master internal DLL

Towards HGROCdv1 block diagram + sensors

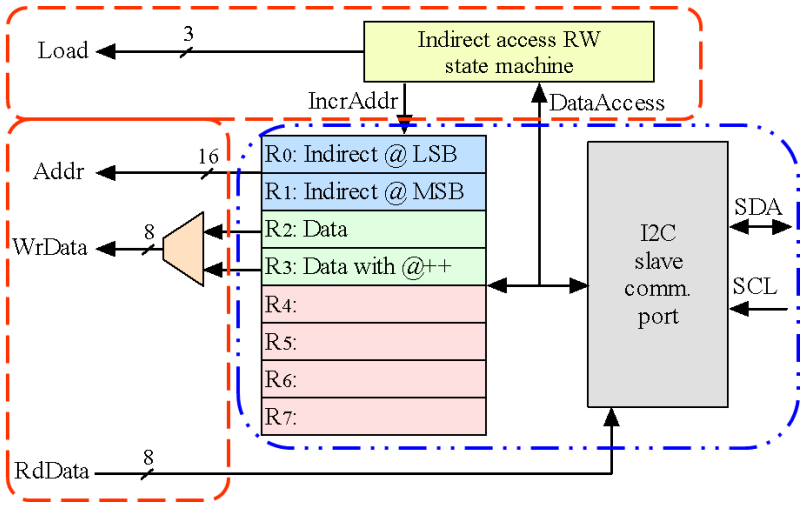






HGROCdv1: slow control - I2C

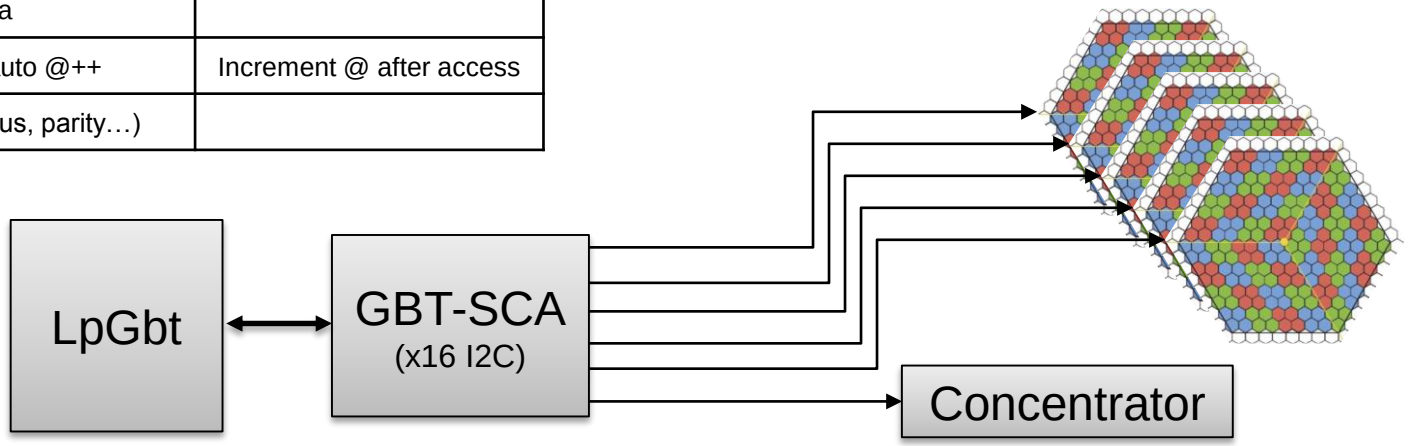
- Slow-control comm. Port:
  - Read / write ASIC parameters
  - Defined @ system level (spec available)
  - A first set of rtl code available/modified
  - Need to set-up realistic simulation with ASIC parameter
  - SC cell with TV defined



- First I2C word (7 bits + 1 RW bit) divide in 2 parts:
  - 4 bits for chip addressing + 3 bits for extd addressing

I2C @	Register	Comments
0	ASIC parameter address (LSB)	Indirect @
1	ASIC parameter address (MSB)	Indirect @
2	Data	
3	Data with auto @++	Increment @ after access
4-7	Tbd (TMR status, parity…)	

1 modules = 3 to 6 HGCROC

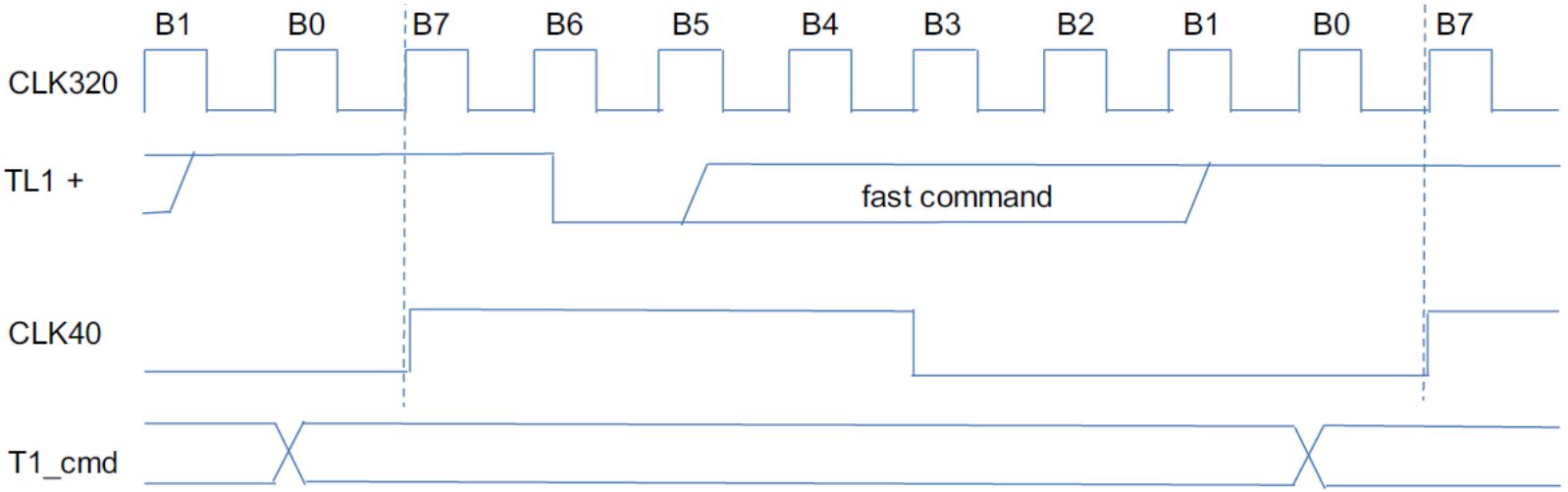


HGROCDv1: Fast commands (tracker)

- Fast control comm. Port
  - Fast commands + 40 MHz clock
  - Defined @ system level (spec available)
  - Need to Also need to define which combinations are possible
  - Next step: define for each command the actions @ ASIC level

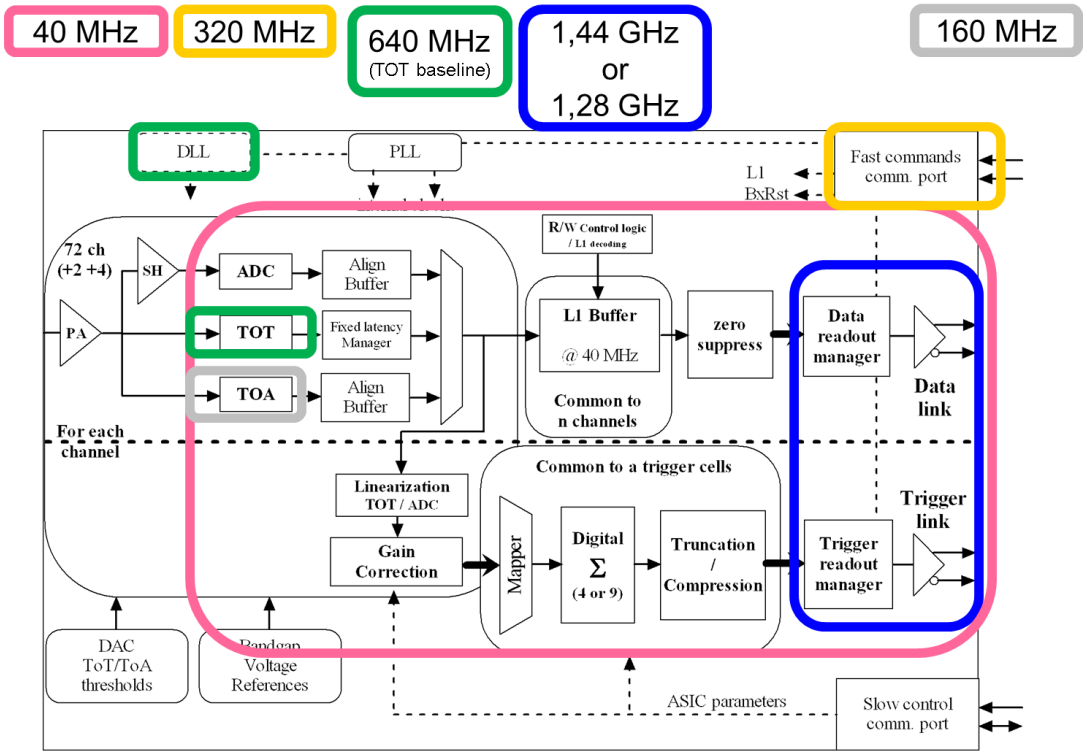
T1_cmd (serial command)	B7	B6	B5	B4	B3	B2	B1	B0
Idle (No Command)	1	1	0	0	0	0	0	1
ReSync (Fast Reset)	1	1	0	1	0	0	0	1
L1-Trigger (Trigger)	1	1	0	0	1	0	0	1
CalPulse (Test Pulse Trigger)	1	1	0	0	0	1	0	1
BC0 (Orbit Reset)	1	1	0	0	0	0	1	1
Tdb 1	1	1	0	1	0	0	1	1
Tbd 2	1	1	0	0	1	0	1	1
Tbd 3	1	1	0	0	0	1	1	1
	Sync code			Command code				

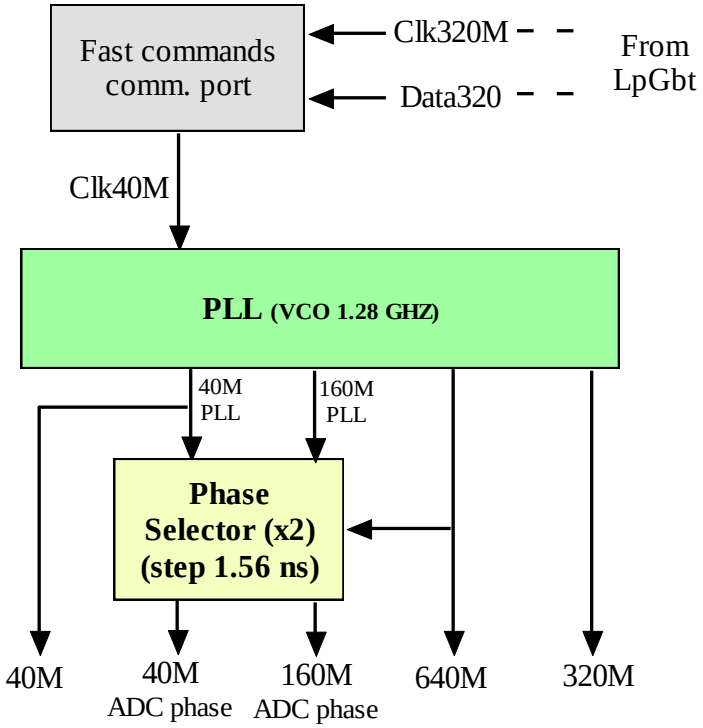
- Fast commands (LHC clock synchronous):
  - Command frame: 110 xxxx 1
  - Synchronisation code: 110 (this code does not appear elsewhere in bitstream)
  - Serial commands transmitted MSB first at 320Mb/s



Clock tree

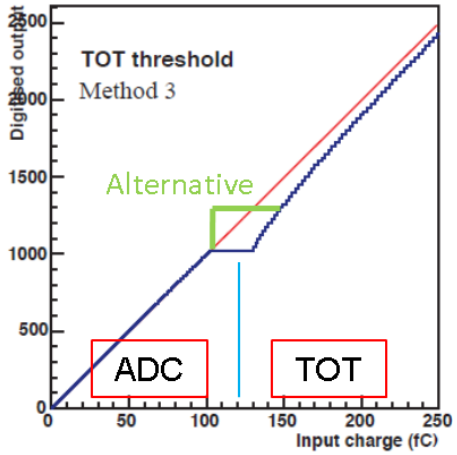
- Only 1 clock received by the chip through LbGbt fast commands line (320 MHz)
- PLL is used to generate all 40 MHz multiples
- Try to minimize CDC

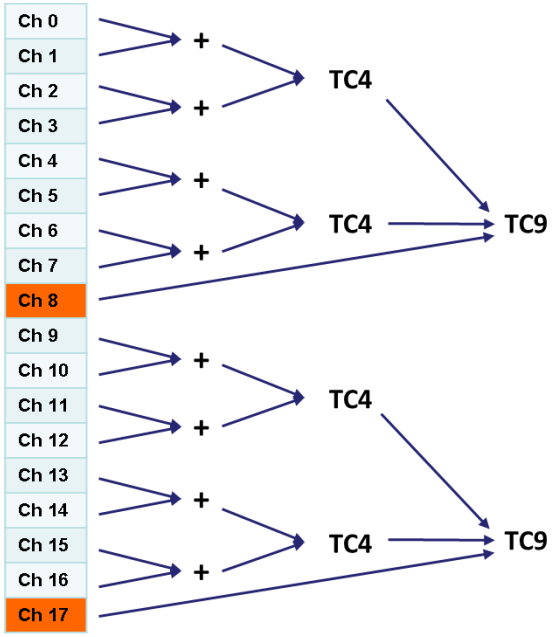




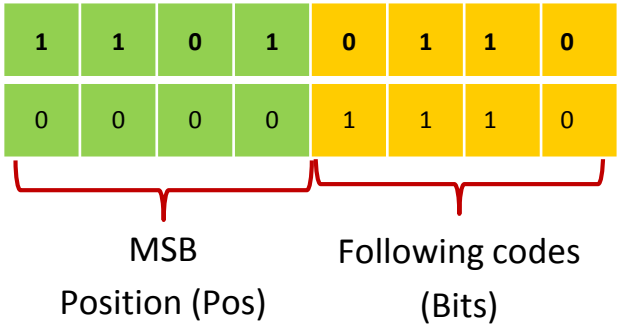
Trigger path: HGROCdv1 (already in v1)

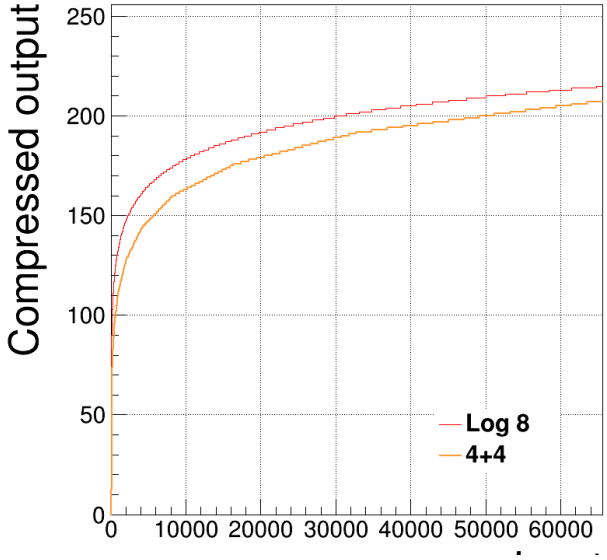
- Data processing (charge):
  - Data alignment
  - LSB linearization (ADC vs TOT)
  - Sum 4 or 9 channels
  - Log compression (4E+4M)
- Data serialized @ 1,28 Gb/s





- 19-bit linearized charge compressed into 8-bit Log:

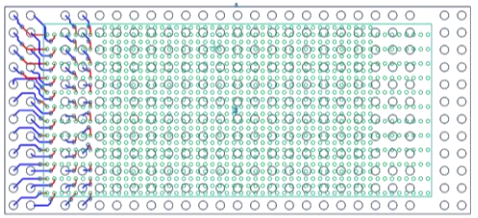


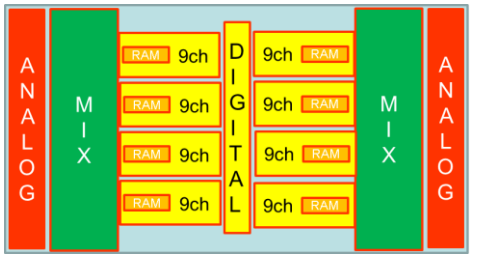


* Data path in backup slides

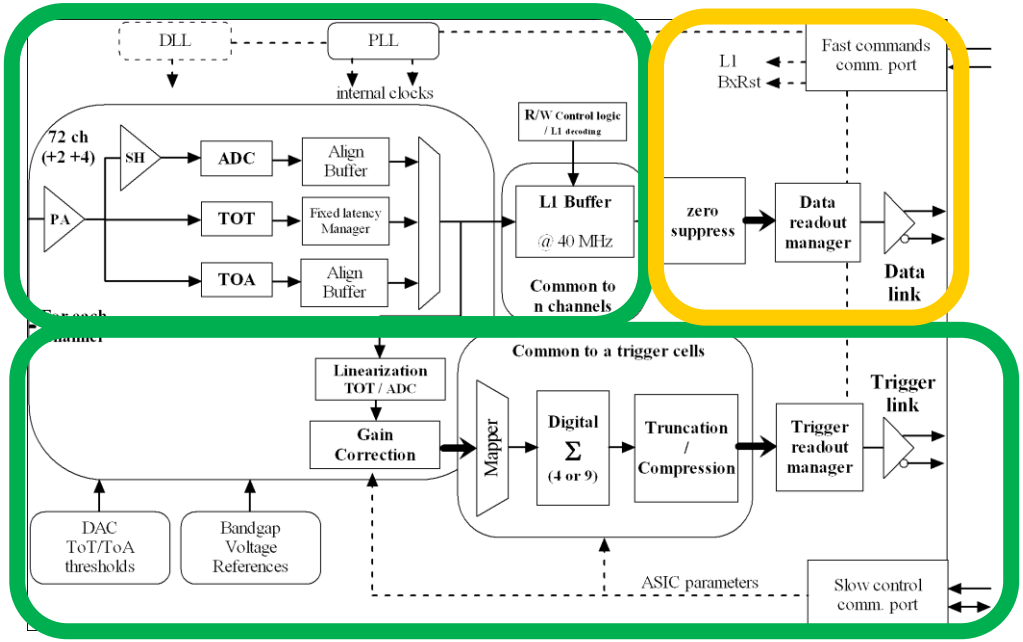
Conclusion

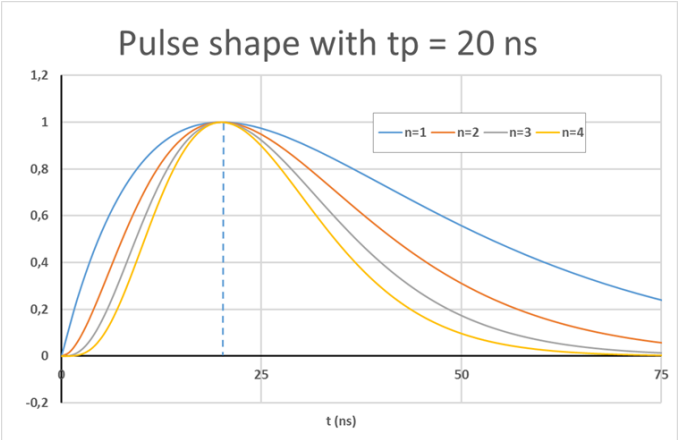
- HGROCdv1 will be submitted by the end of the year with:
  - 72 channels with “final” BGA package (pitch ,5 or ,6 mm)
  - Final analog part (many block in validation stage)
  - Slow control through I2C + partial fast commands (full clock tree)
  - New DRAM for L1 buffering + “Final” trigger path (details…)
  - Partial DAQ readout (not final)
  - OOT pile-up mitigation
  - TMR





- Try to see as soon as possible integration issues

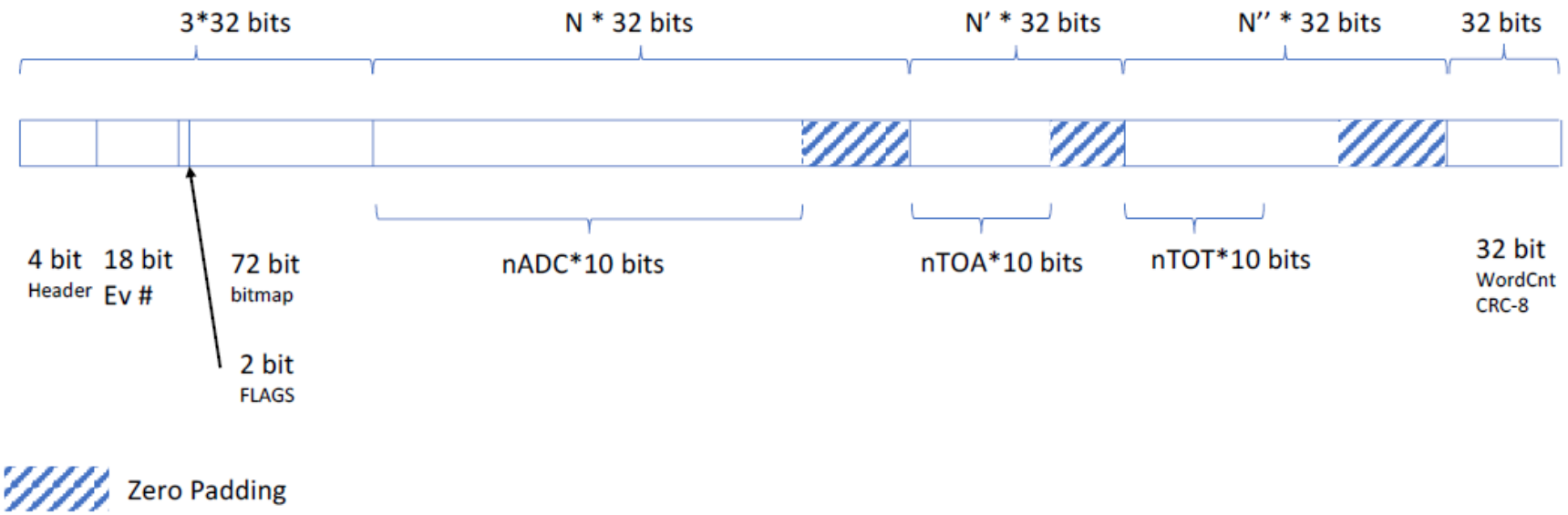




Additional slides

Data path: HGROCdv1

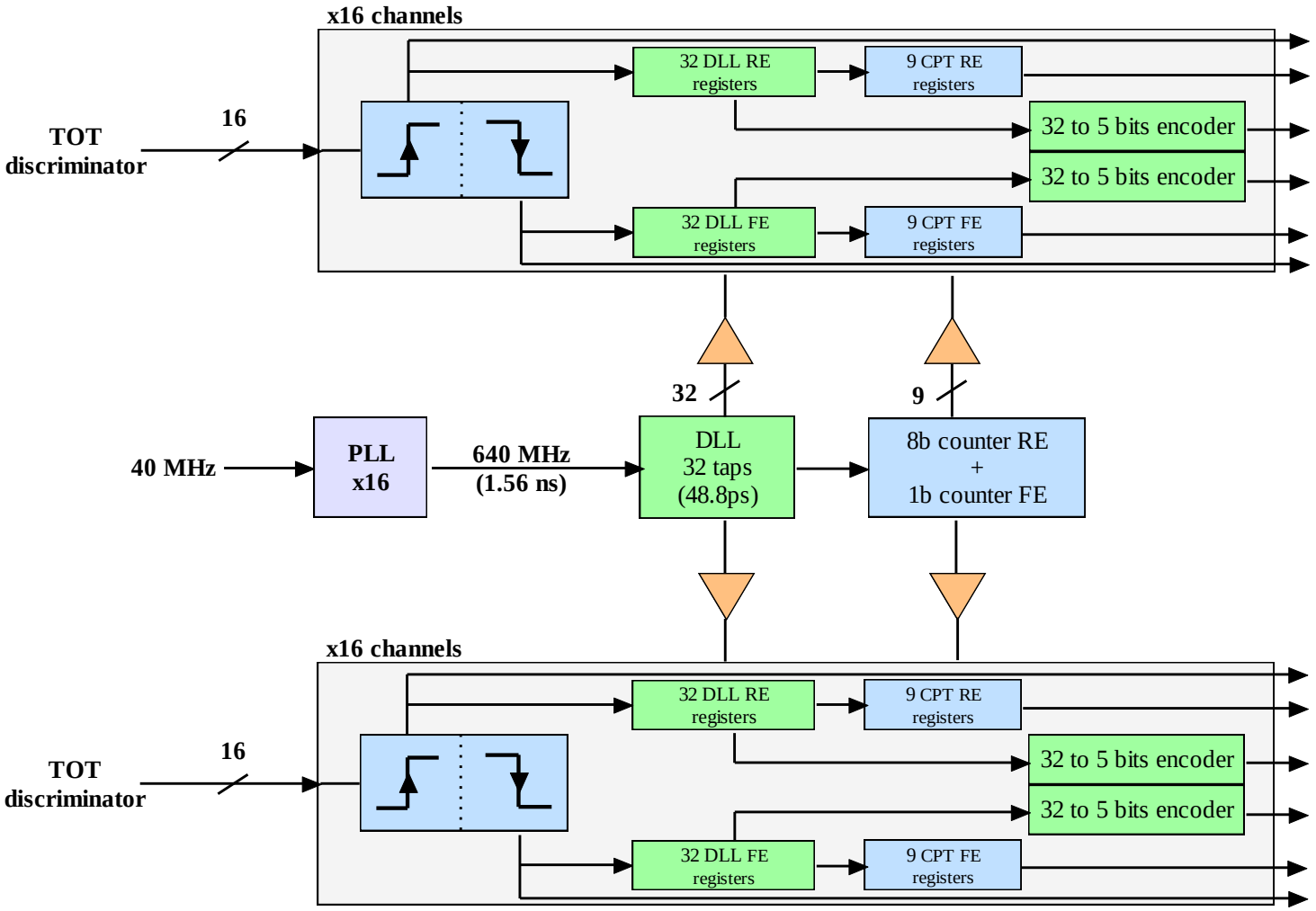
- With online 0-suppression
- Data serialized @ 1,28 Gb/s




```
FLAGS = 00   : Normal event; i.e. 3x32+(N + N'+ N'')*32+32 (Nch = 72)
      = 01   : Empty (Lost) Event, only first 32 bit word, no bitmap, no trailer word
      = 10   : Raw Event: all ADCs, PreADCs, TOAs, TOTs, fixed length (Nch = 78)
      = 11   : Idle word (no L1A), only first 32 bit word, no bitmap, no trailer
```

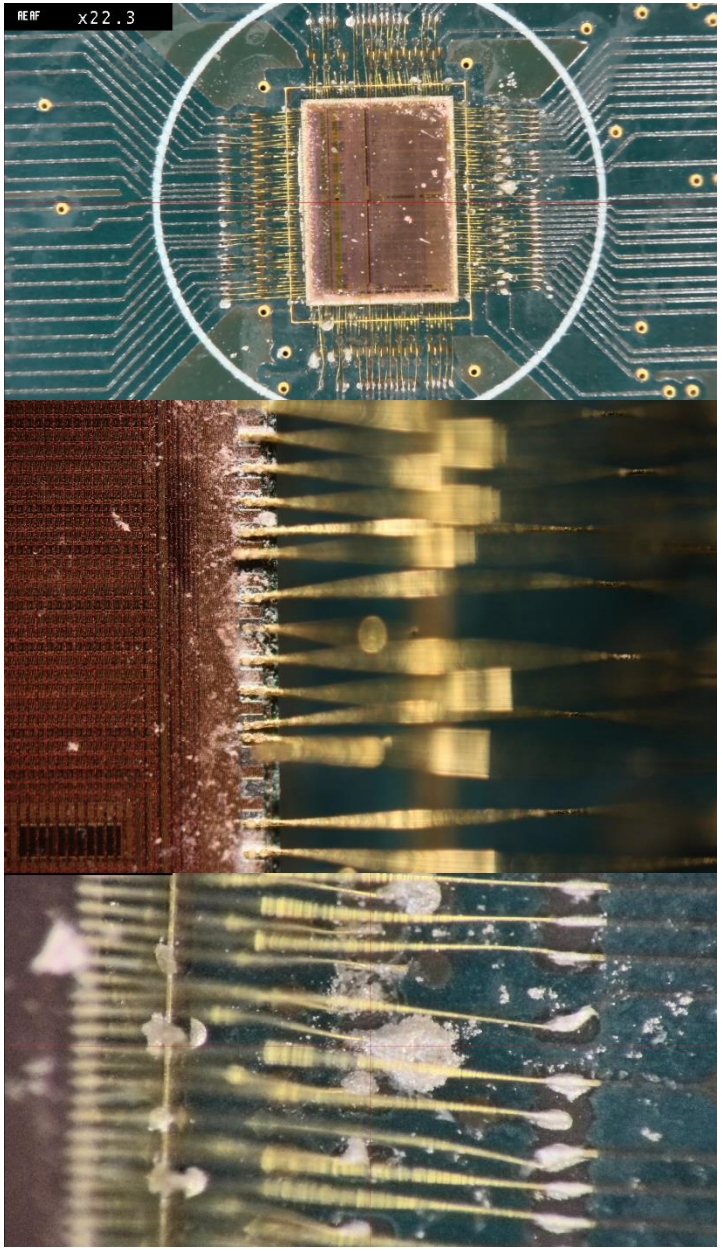
HGROCv1 TOT path bloc diagram (baseline)

- Based on DLL + 1 counter @ 640MHz ➔ 400 ns with 48,8ps steps
  - 32 tap DLL ➔ 48,8 ps LSB
  - 8b counter ➔ step of 1,56 ns + 1b counter to mitigate TOT near 640MHz edges
- Raw data available (28 bits/ch) or TOT value (TOE-TOA)



Bonding issues

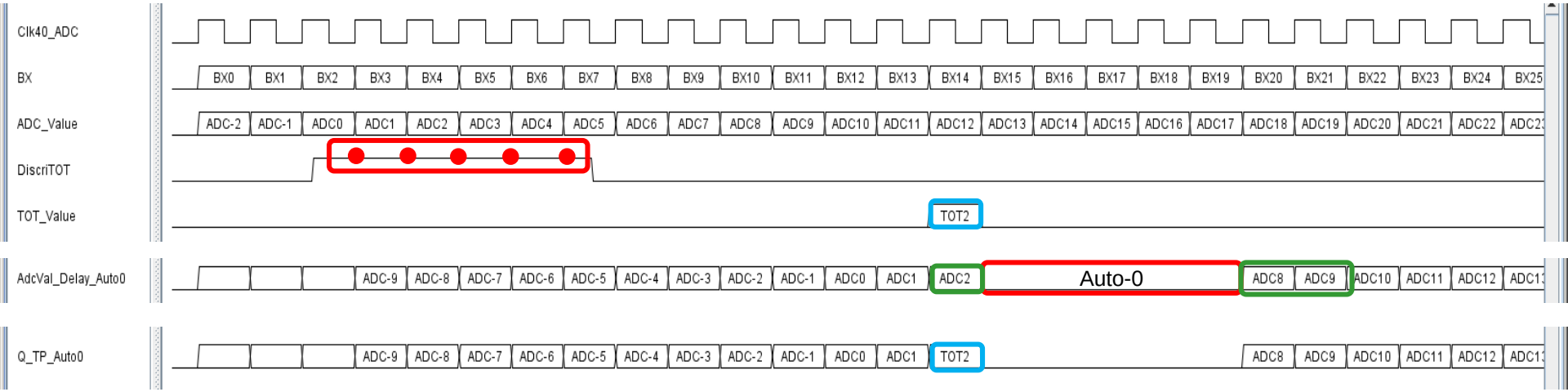
- Many issues during the dicing, cabling and bonding
- 3 boards over 5 are more or less usable
  - At OMEGA, some wire bonds missing (probe outp, vdd_tdc_ic), some doubts on the quality of some power supplies and ground, but all parts are accessible
  - At IC, for now impossible to see an analog waveform but the TOT TDC and digital seem working well
  - At IRFU: bandgap missing, no analog part accessible, but PLL, TOA TDC and digital seem working well
- New boards are in cabling and will be send to wire bonding at CERN
- Fermilab has also launched a new batch



Reminder 2

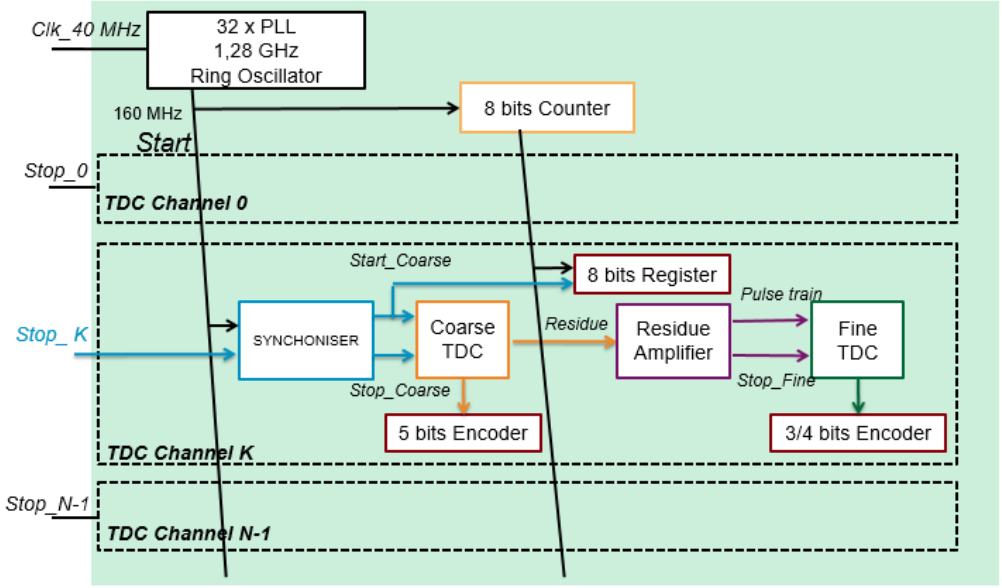
- When the TOT is fired (current source on PA), ADC not usable until the end of TOT conversion

- Auto-0 ADC directly in the AlignBuffer Flip-Flops



MULTI-CHANNEL TDC ARCHITECTURE FOR THE TOA

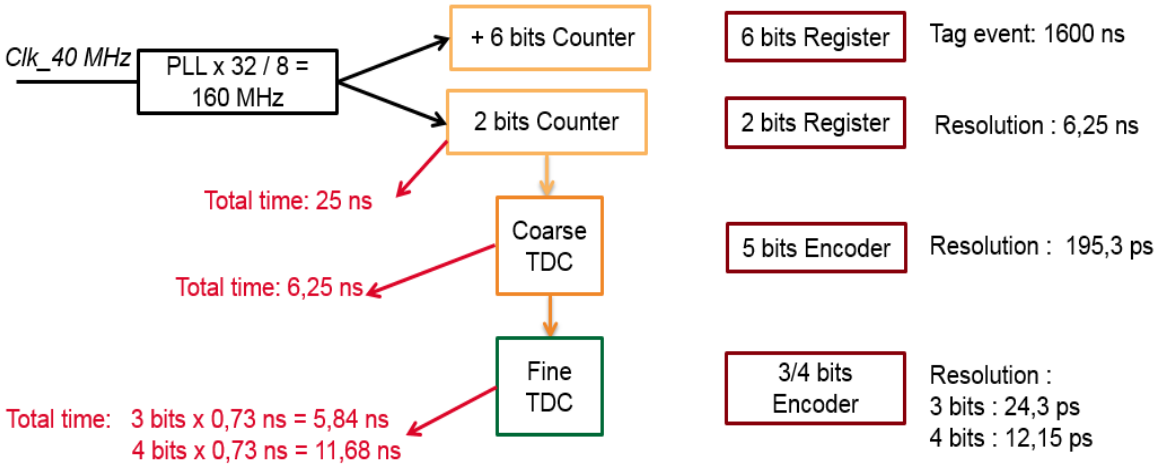
10/11 bits over 25 ns multichannel TDC architecture :



TDC resolution is increased by a counter ➔ the 2 most significant bits of the TDC are now obtained by a **counter** operating at the CTDC frequency who is also a multiple of the 40 MHz bunch clock.0
The common 8-bit counter ➔ 2 bits for LSB and 6 other bits for bunch marking.

A common PLL in phase with the external bunch clock (40 MHz)

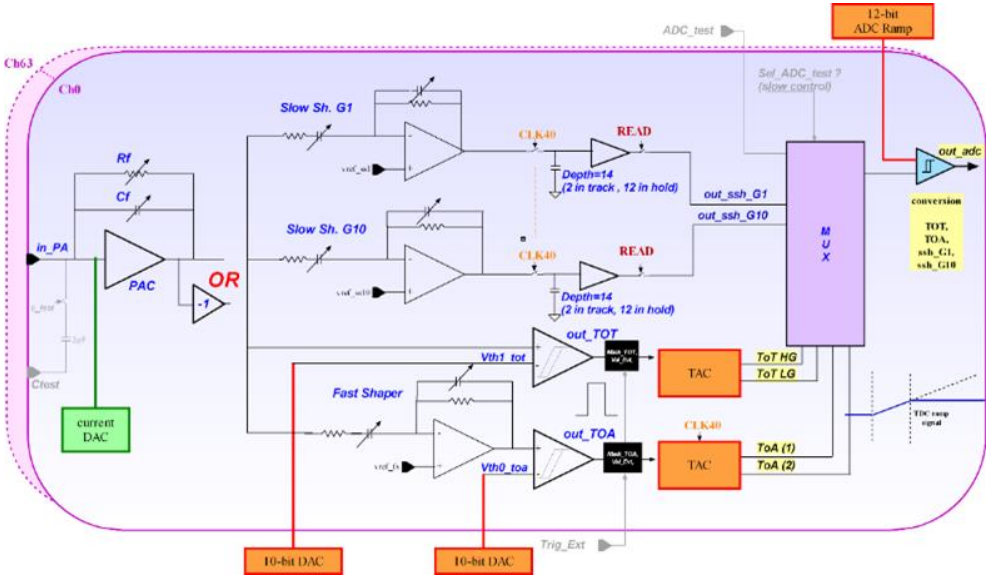
Timing and resolution :

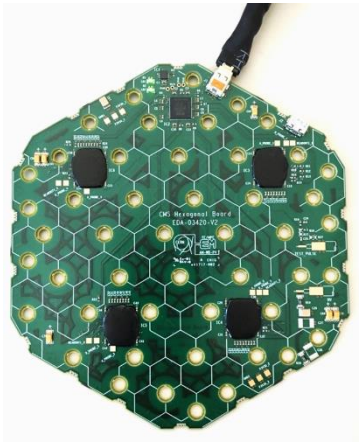


$$RMS_{Noise} < \frac{LSB}{\sqrt{12}} = 3{,}5 \text{ ps}$$

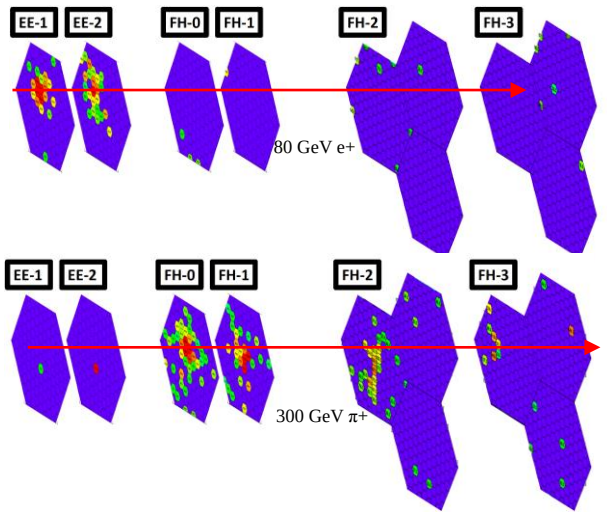
SKIROC2_CMS for HGCAL

- new SKIROC2 for CMS
  - Optimized version for CMS testbeam, pin to pin compatible
  - Dual polarity charge preamplifier
  - Faster shapers (25 ns instead of 200 ns)
  - 40 MHz circular analog memory, depth= 300 ns
  - TDC (TAC) for ToA and ToT , accuracy : ~50 ps
  - Submitted jan 2016, SiGe 350nm
- Test beam :
  - Pedestal stability, MIP calibration
  - HG to LG calibration
  - Showers for e+ and π+





Hexaboard designed at CERN



Electron and pions signals seen in testbeam