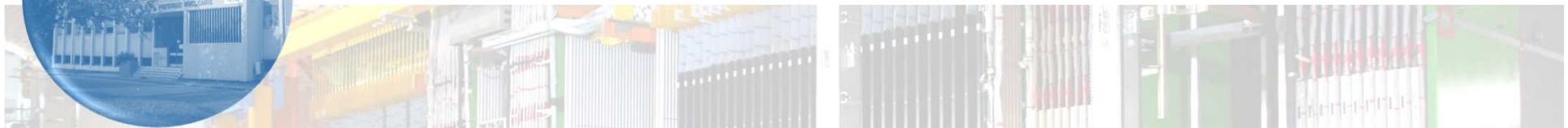


2018 Journées VLSI - FPGA - PCB et Outils CAO de l'IN2P3 Clermont-Ferrand

**Data acquisition board for a Beam-Tagging
Hodoscope Used in Hadrontherapy Monitoring**

X. Chen



Summary



1

Introduction



2

Data Acquisition Board

2.1

Hardware

2.2

Firmware

2.3

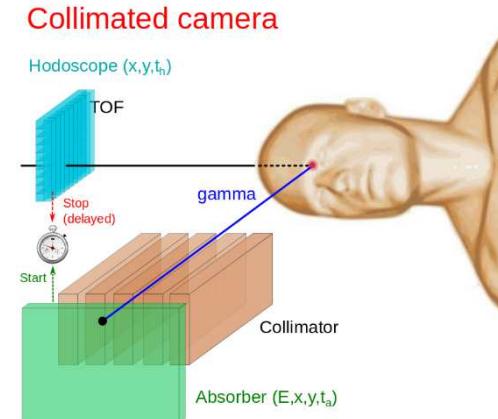
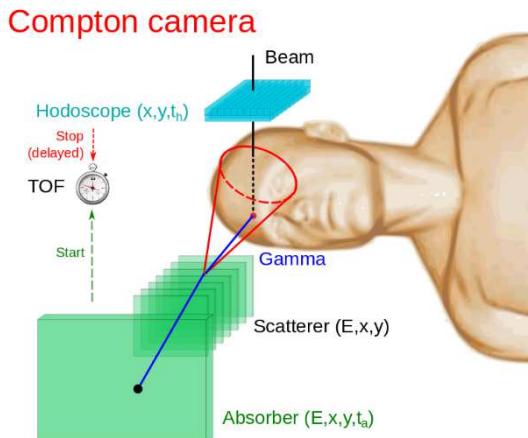
Beam test

3

Conclusion et perspective

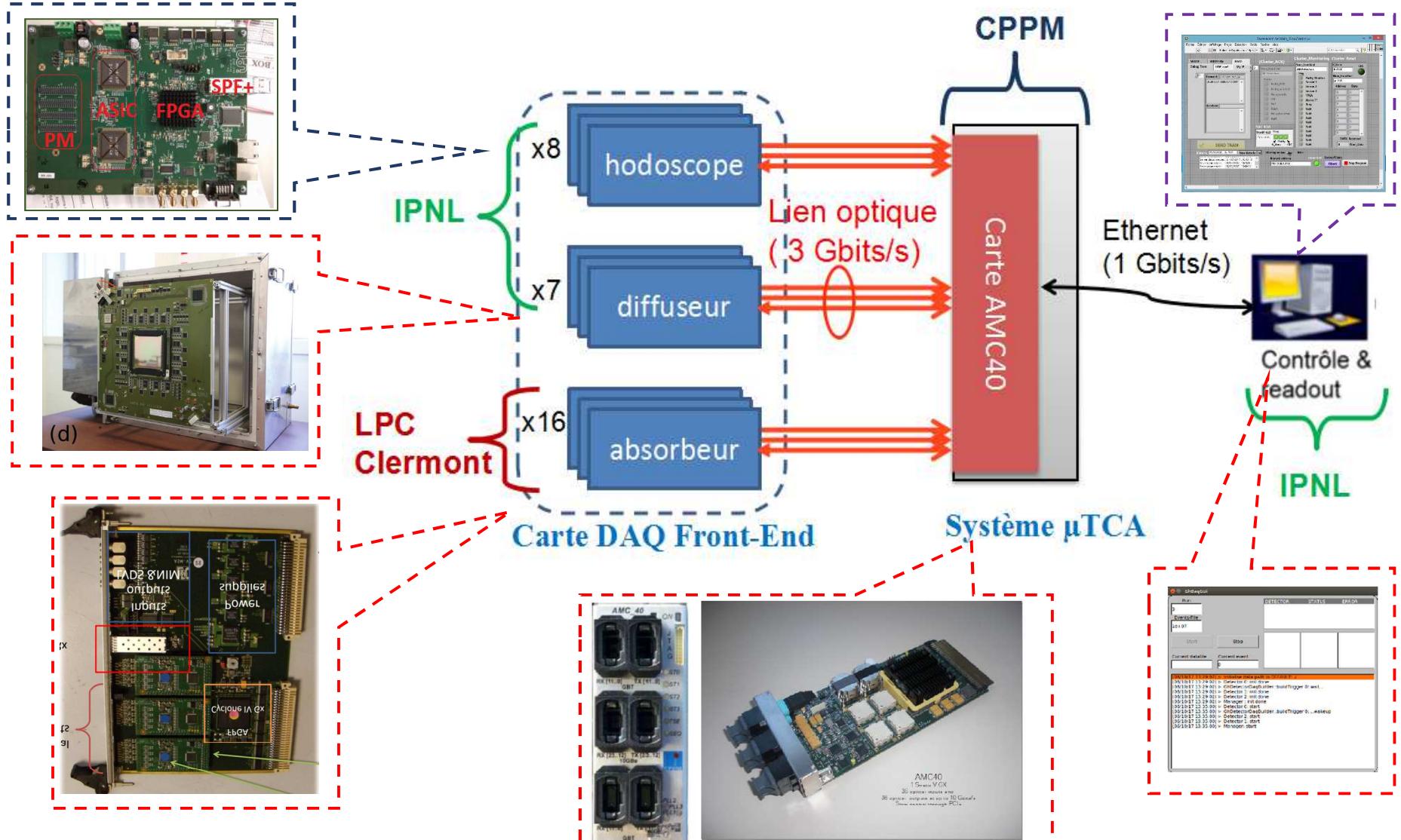
Ion-range monitoring during hadrontherapy

- Hadrontherapy treatment uncertainties
 - Need for ion-range verification
 - Correlation between “ion-range and Prompt Gamma (PG) profile”
 - => Development of PG detection systems
- PG systems by the French collaboration CLaRyS
 - PG cameras coupled with beam hodoscope for time-of-flight (TOF) measurement
 - CLaRyS collaboration: 4 IN2P3 laboratories (for instrumentation)
- Beam hodoscope
 - Time of arrival and position of incident ions



Introduction

Data acquisition system for the Compton camera



Hodoscope prototype

➤ Specifications

- position resolution: 1 mm
- time resolution: 1 ns
- count rate: 10^8 Hz



➤ Prototypes

- Consisting of an array of scintillating fibers (BCF10/12)
- Readout: optical fibers FORETEC + multi-anode PM H-8500
- 2 prototypes: 32×32 (small) and 128×128 fibers (large)

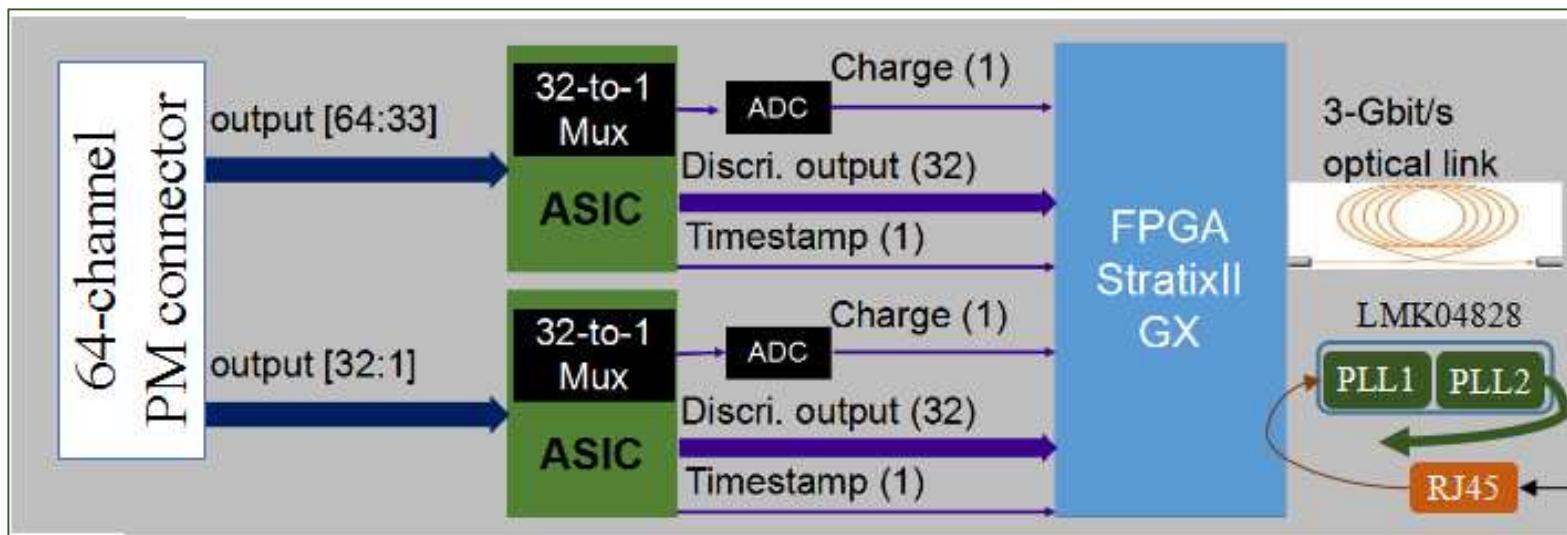
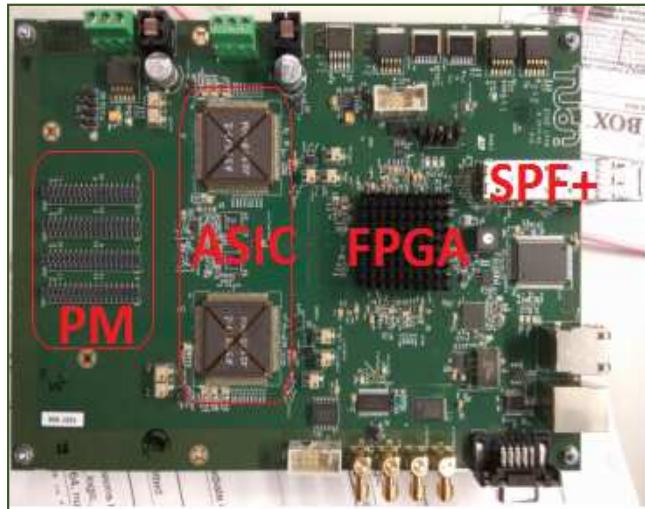
Hodoscope board specifications

- **Memory**
 - 1 μ s depth of memory (due to trigger generation time from gamma camera)
- **Count rate** (for Compton camera application)
 - Absorber single rate: $\sim 10^6$ Hz
 - Coincidence trigger rate: $\sim 10^5$ Hz
 - Final data rate: a few 10^8 bits/s
- **Timing resolution**
 - Relatively good timing: ~ 500 ps

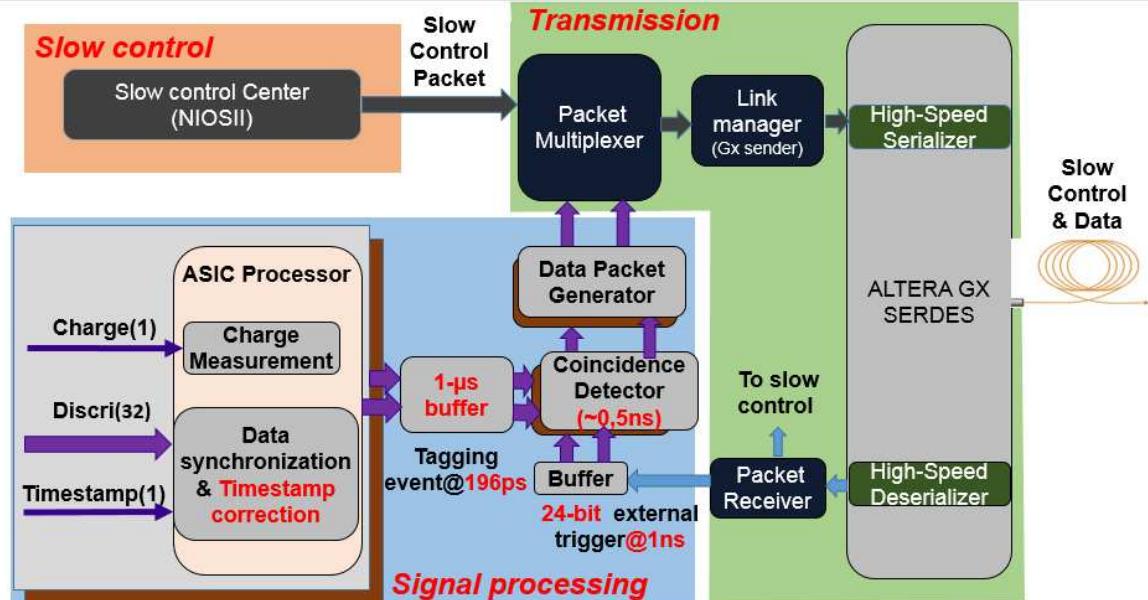
Summary

- 
- 1 **Introduction**
- 
- 2 **Data Acquisition Board**
- 
- 2.1 **Hardware**
- 
- 2.2 **Firmware**
- 
- 2.3 **Beam test**
- 
- 3 **Conclusion et perspective**

Hodoscope readout board : Hardware



Principle



- 3 triggers:
 - Auto trigger
 - External triggers
 - Optical link
 - SMA connector

Specificities

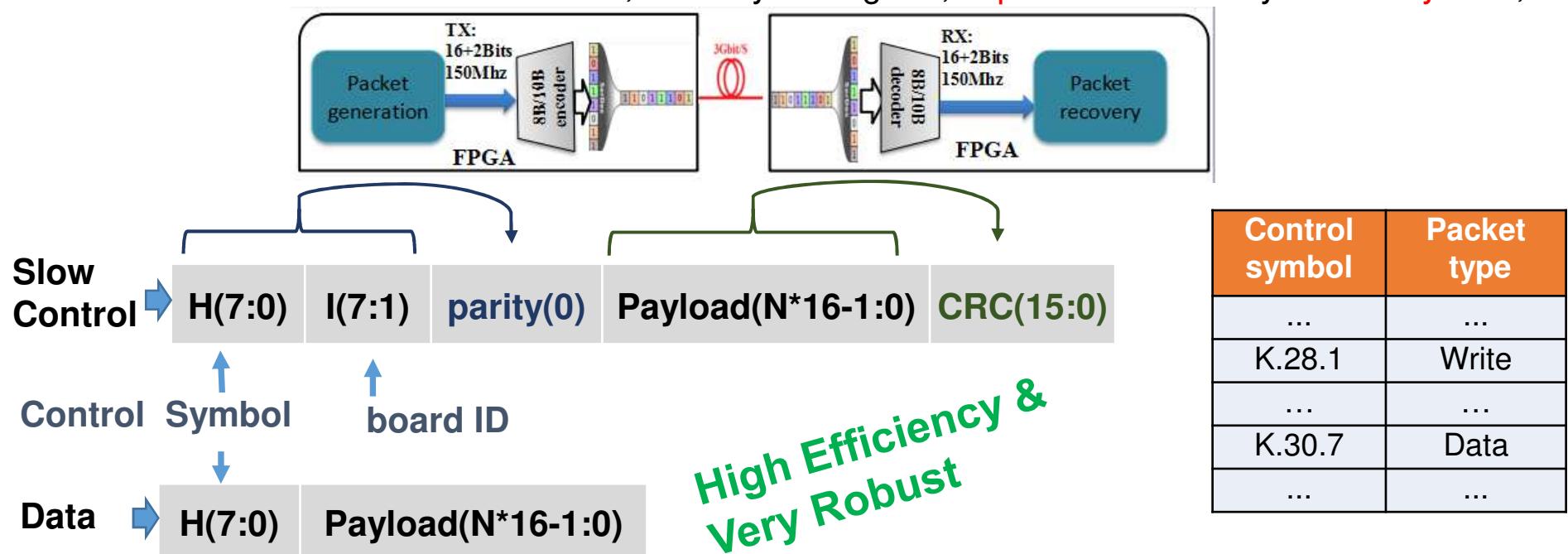
- Custom protocol for fast data transfer
- Multi-phase clock based **TDC (MPTDC)**
- TDC-based time reference (**T0**)
- Fast histogram-based time-delay estimation

Specifications

- Mix of trigger and acquisition data on the same (optical) link
- Fast data transfer protocol
 - Trigger latency ($T_{\text{pretrigger}} + T_{\text{trigger}} < 1\mu\text{s}$)
 - Dead time minimization

Key features

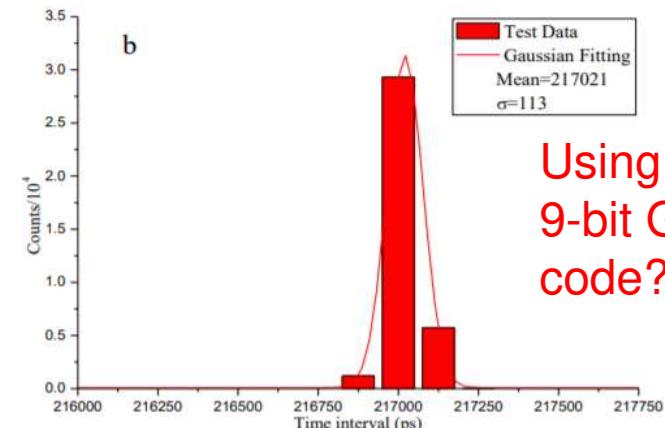
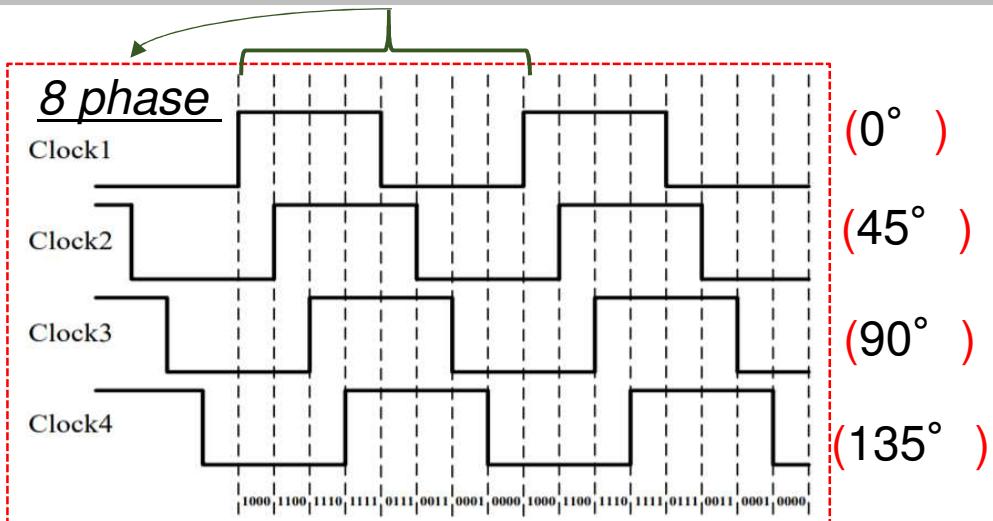
- Basic protocol: **8B/10B** encoding
- Simultaneous bidirectional transmission
- Transmission mode: master-slave, even-bytes aligned, in **packets** delimited by **control symbol**,



Motif

- Problems of using AISC-TDC(Single reset, noise, time unit etc.)
- Requirement of FPGA-based TDC for ASM and silicon board

Principle



Using only one
9-bit Gray-
code???

Principle of operation of the interpolation clock

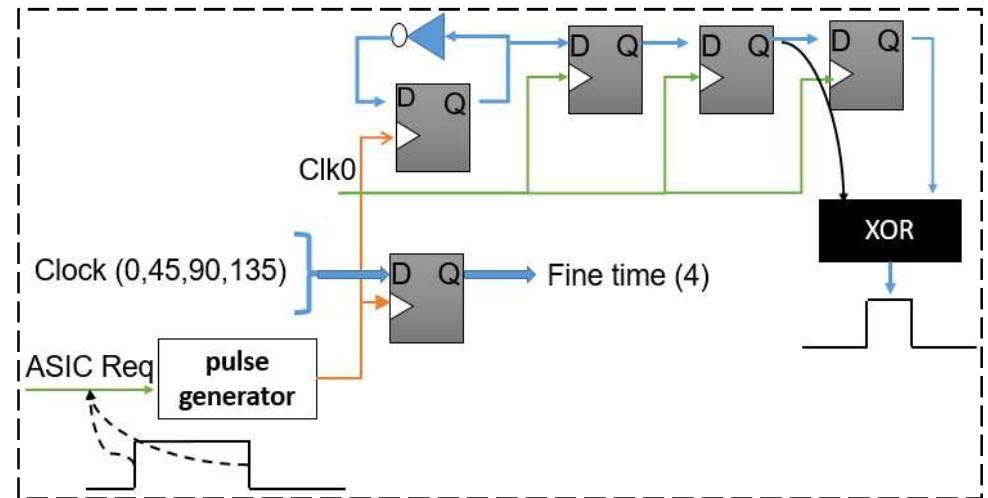
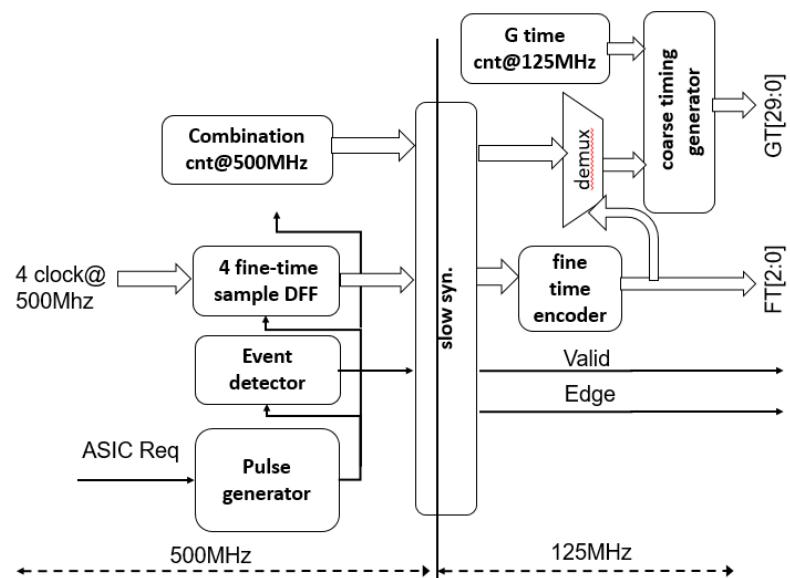
[QI Zhong et al.-2015 [arXiv:1502.01079](https://arxiv.org/abs/1502.01079)]

Distributions of the time interval

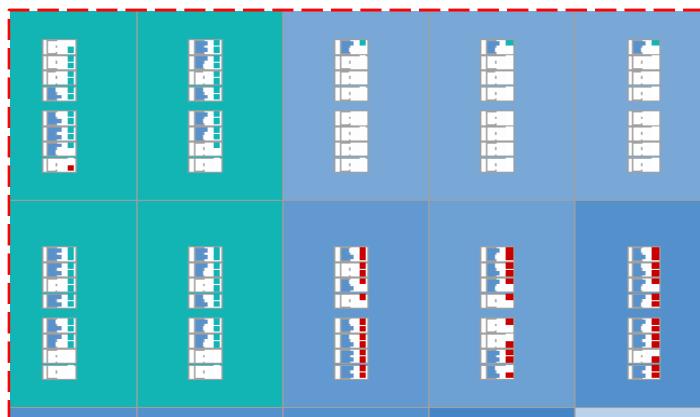
- Theoretical value:
 - LSB: 2ns / 8 = 256ps

- Issue:
Coarse time implement

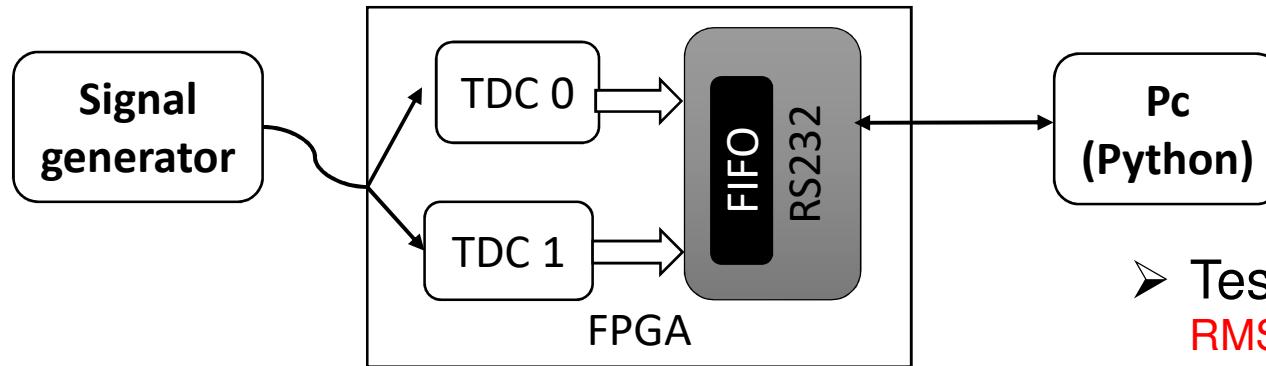
Implementation



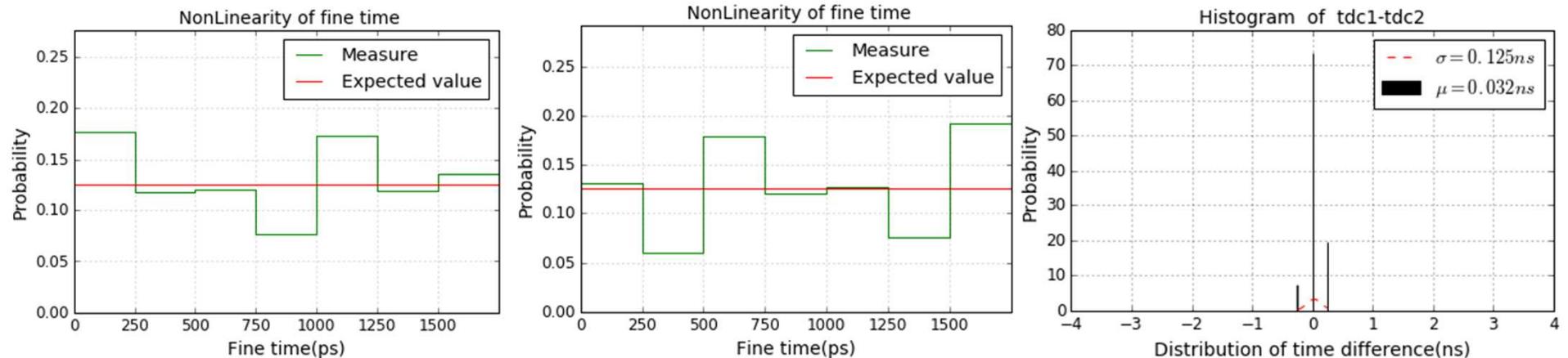
Max clock path skew: 200ps



Test without AISC

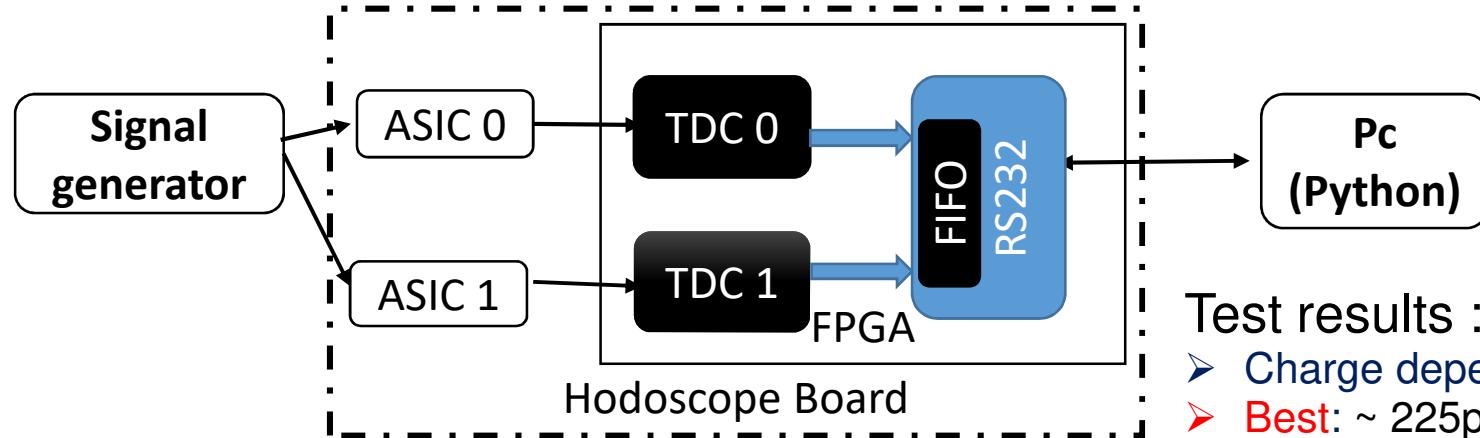


➤ Test result :
 RMS: $\sim 125\text{ps} / \sqrt{1,4} = \sim 89\text{ps}$



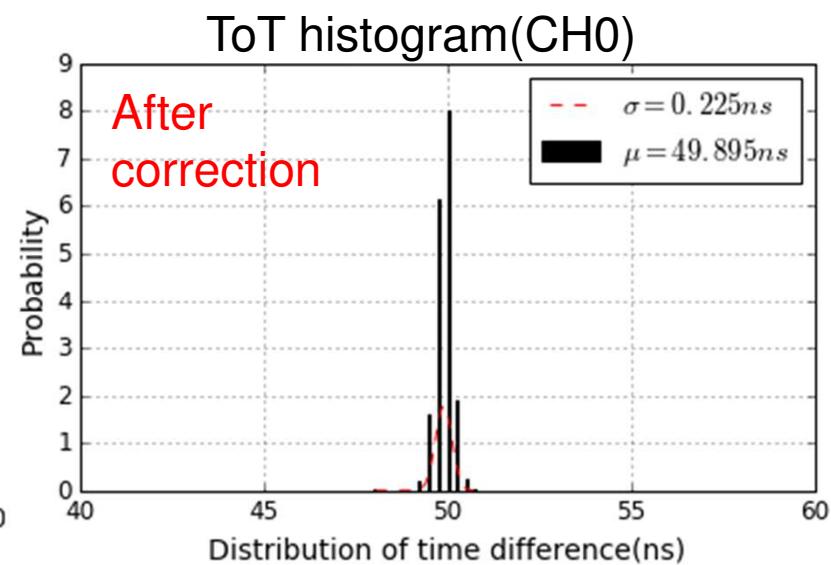
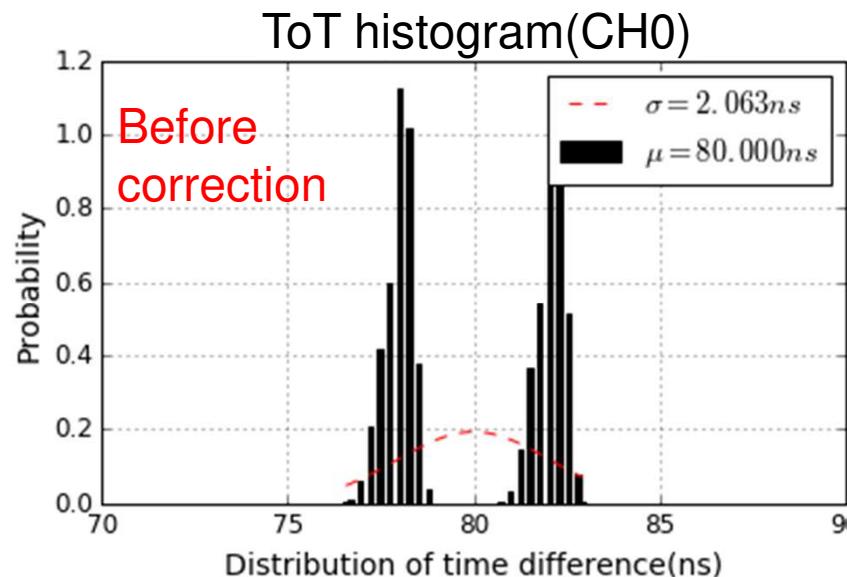
Specificités 2 : MPTDC

Test with AISC

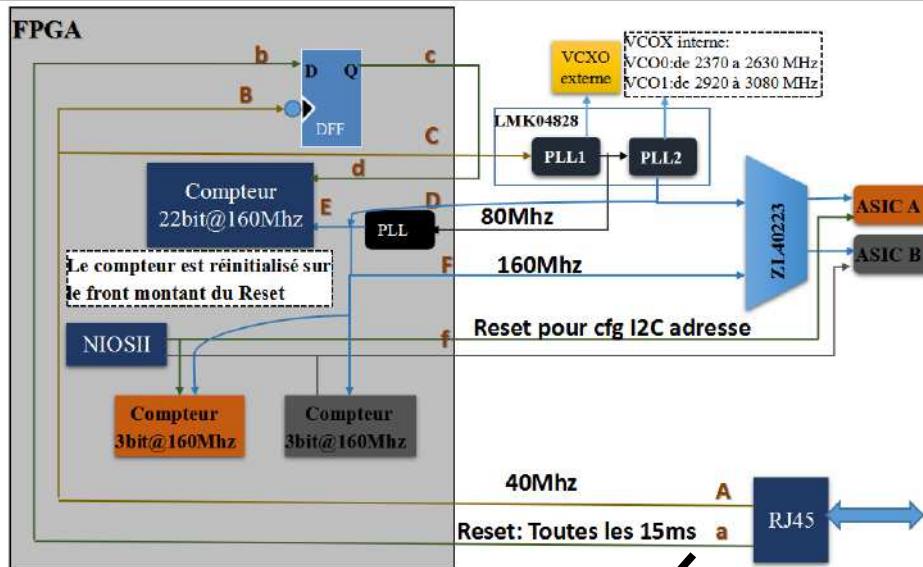


Test results :

- Charge dependent
- Best: $\sim 225\text{ps} / 1,4 = \sim 161\text{ps}$

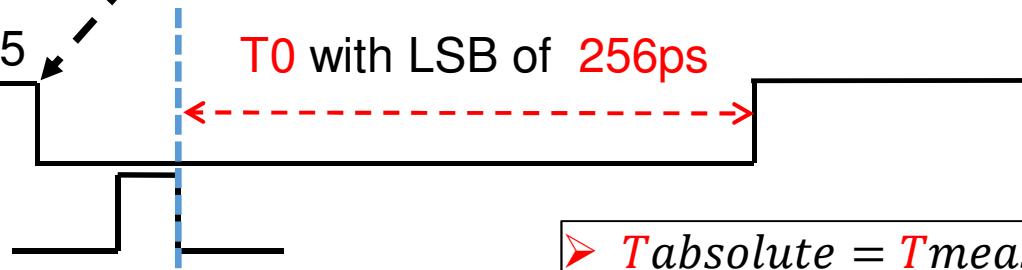


Asynchronous reset issue



Approach

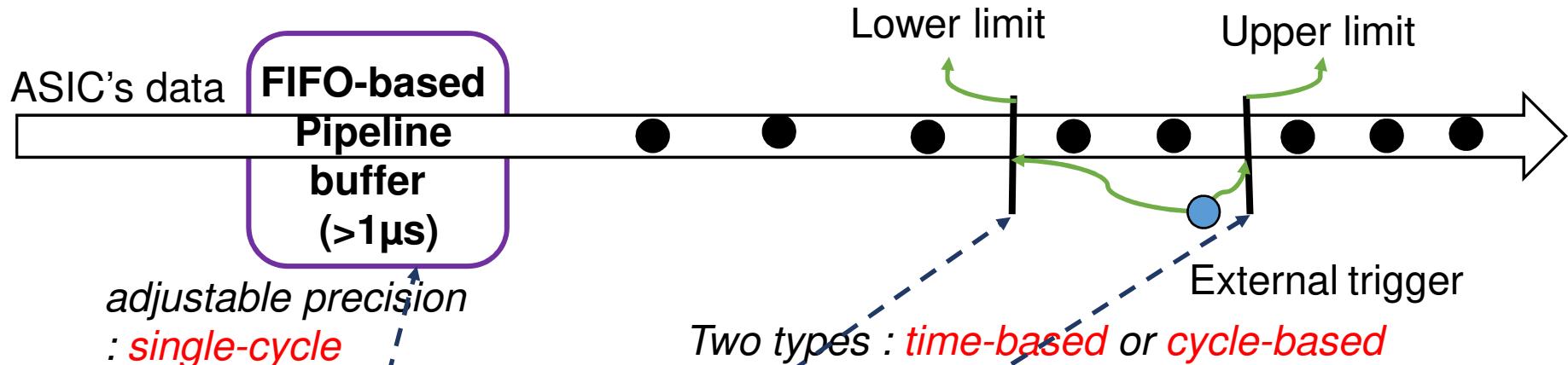
System reset input via RJ45



Reset the whole TDC
(sync to slow clock)

- $T_{absolute} = T_{measure} - T_0$
- Resolution degradation : 1,4
- Using T_0 for sync checking

Coincidence detector

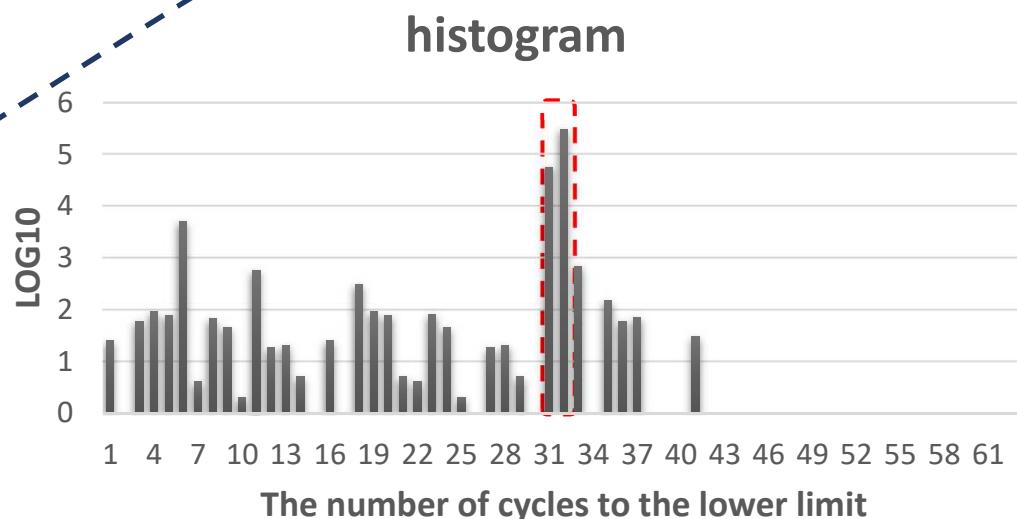


Approach: using histogram

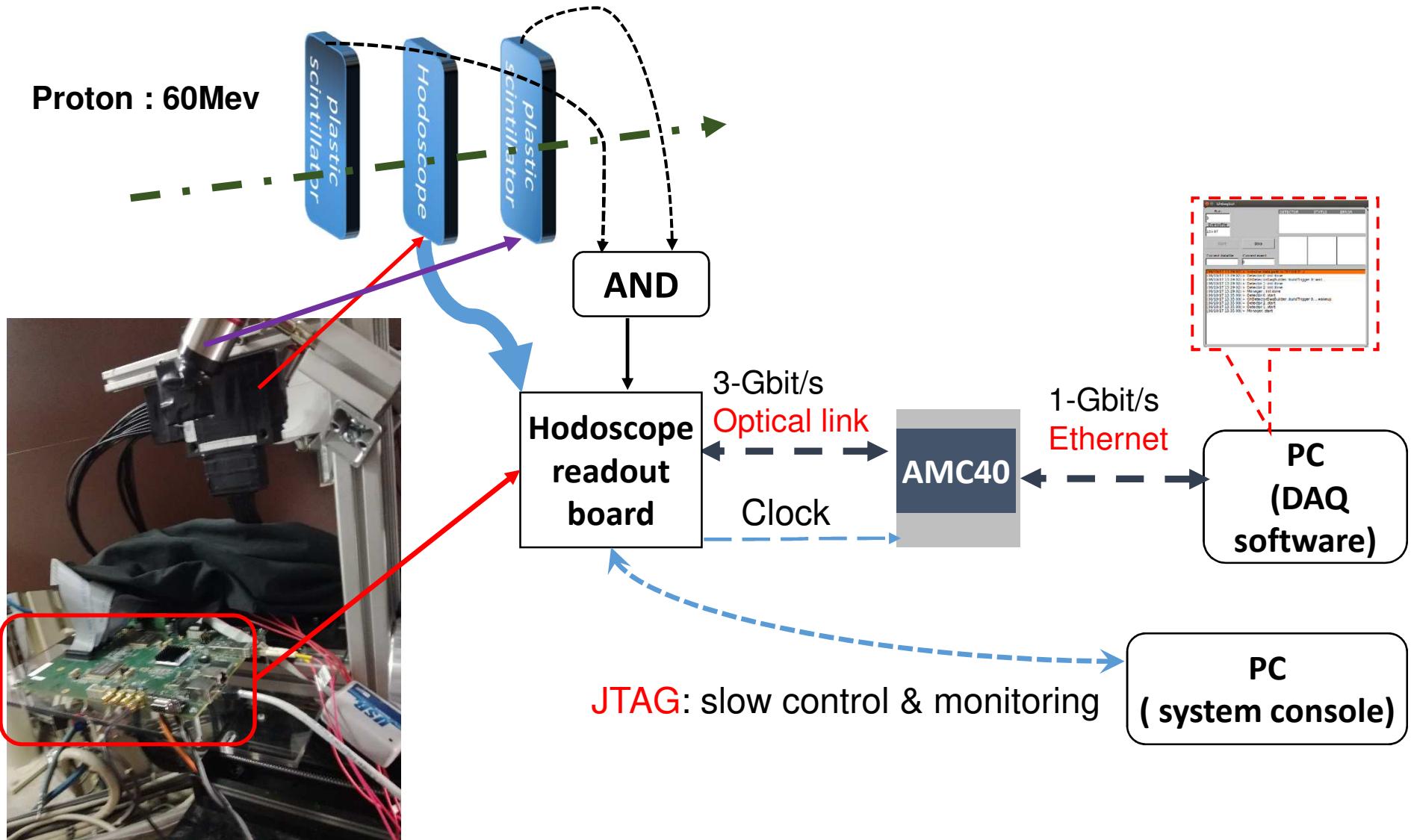
Cycle-based example(*cycle*):

- Buffer cycle: 64
- Lower limit : 3
- Upper limit : 3+63

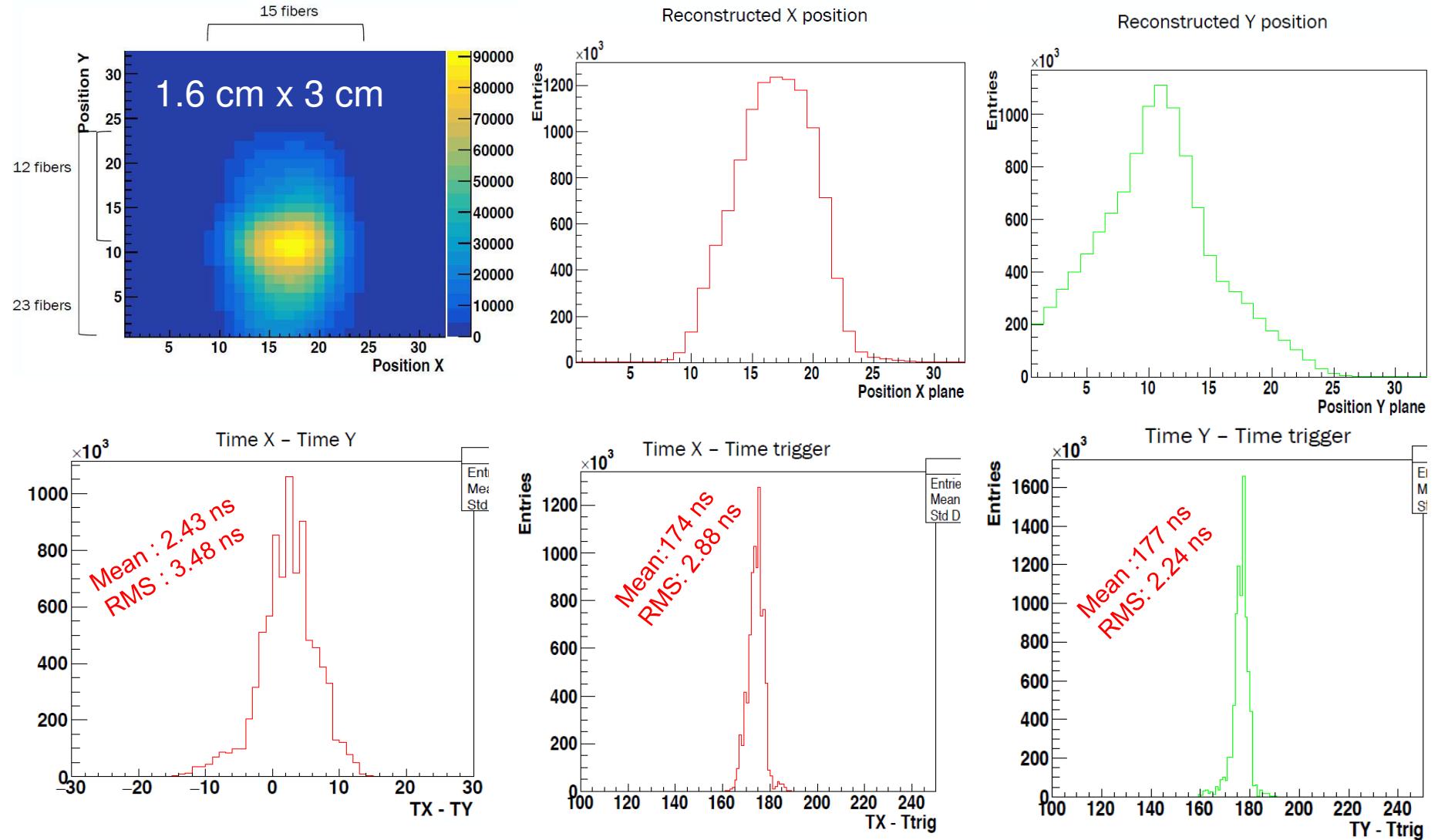
Result after 12 seconds



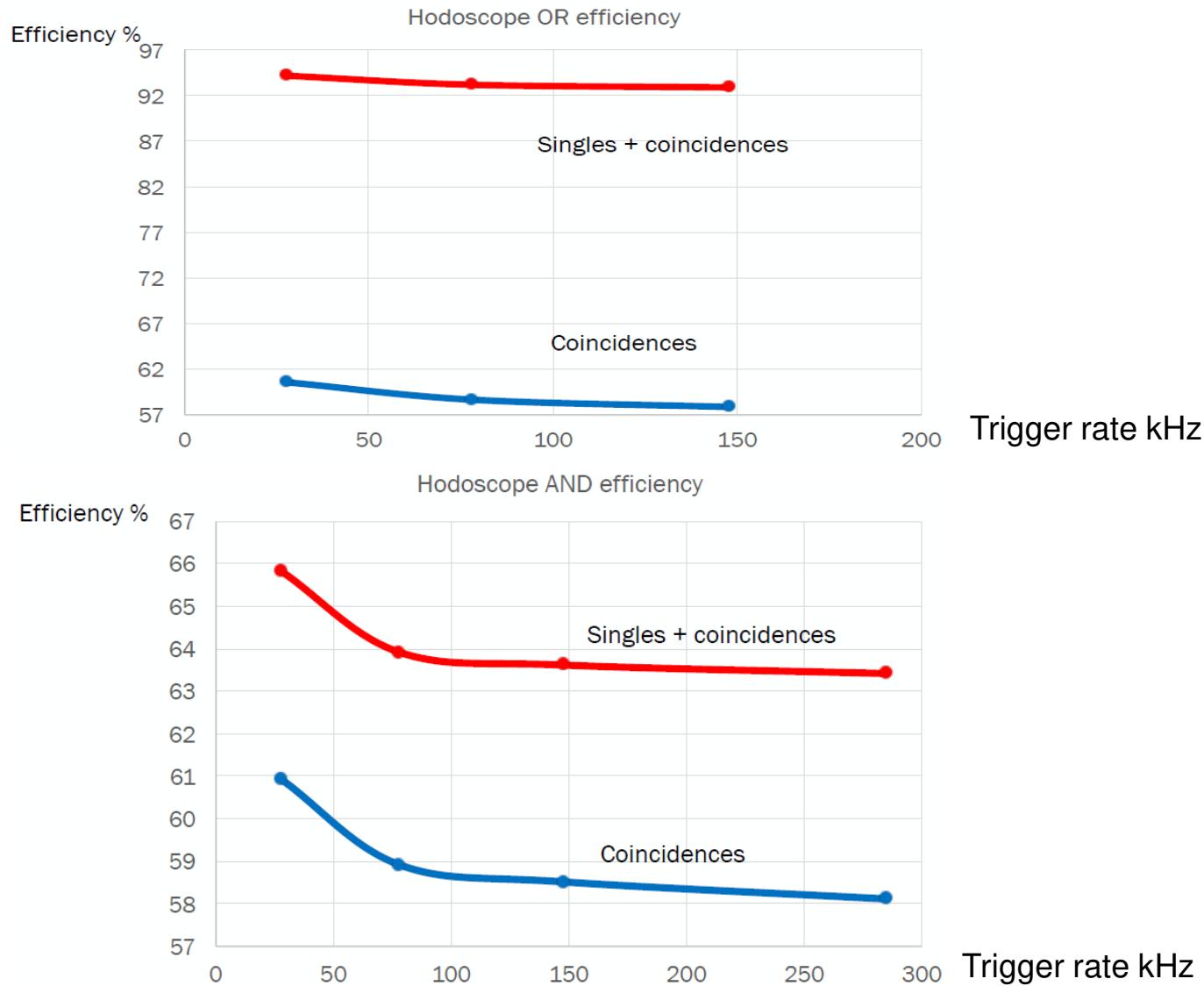
Data acquisition system



Test results



Test results



Summary

- 
- 1 **Introduction**
- 
- 2 **Data Acquisition Board**
- 
- 2.1 **Hardware**
- 
- 2.2 **Firmware**
- 
- 2.3 **Beam test**
- 
- 3 **Conclusion et perspective**

Conclusion

- Successful **in-beam test** of the **small size hodoscope** prototypes with the associated DAQ chain : hodoscope board, optical link with custom protocol, AMC40, DAQ software, etc.

Perspectives

- **In-beam tests**
 - Sep 2018 : simplest collimated camera using only one hodoscope board and one ASM board
 - Begin of 2019: collimated camera with hodoscope
 - End of 2019 : Compton camera with hodoscope



➤ Development history

- V1 : 16 channel [S. Deng, 2012]
- V2 : TDC [S. Deng, 2012]
- V3 : 32 channel + TDC

➤ Technology (V3)

- AMS BiCMOS 0.35 technology: about 13 mm²

➤ Key features (V3)

- Single channel features:
 - 525 fC—25.2 pC input dynamic range
 - about 2 Ohm input impedance
- time stamping feature via a divided-by-32 reference clock (internal DLL): 140 ps resolution
- internal event FIFO (40bx4) memory stores tagging information with asynchronous readout interface
- I2C interface for slow control parameters
- 1 32-to-1 analogue output channel (fiber ageing monitoring)

