

# TDC development

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Pôle MicRhAu

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# Plan

## 1 Introduction

- Time Line of TDC application in MicRHAU pole

## 2 TDC Application in pole MicRHAU

- CRONOTIC
- CRONOTIC2

## 3 Conclusion

## 4 Bibliographie



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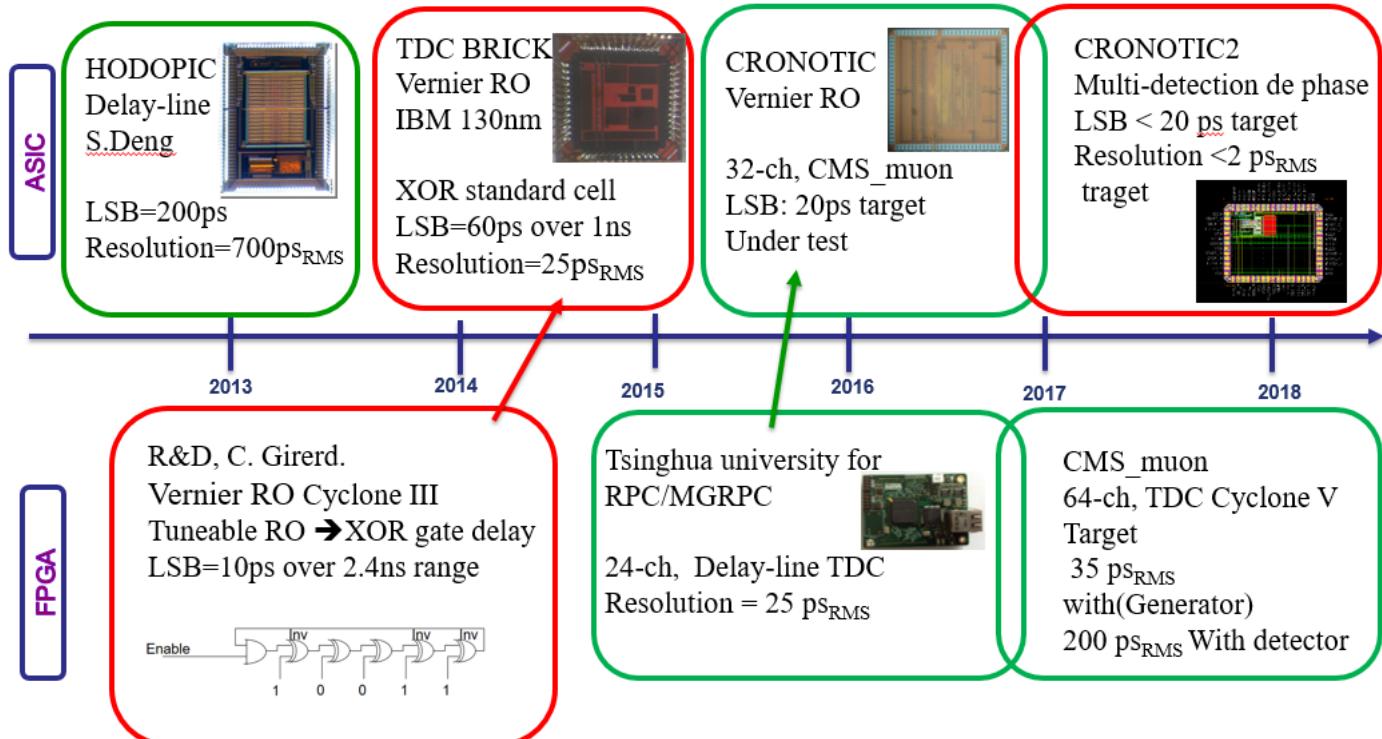
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# Time Line of TDC application in MicRHUAU pole



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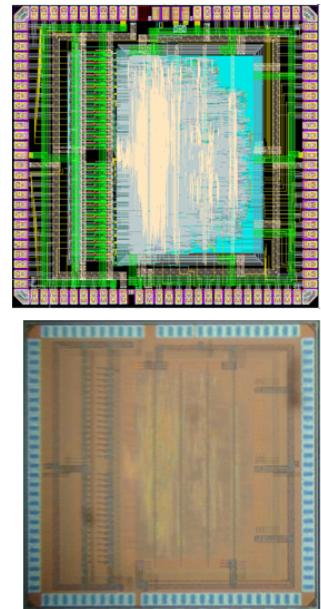
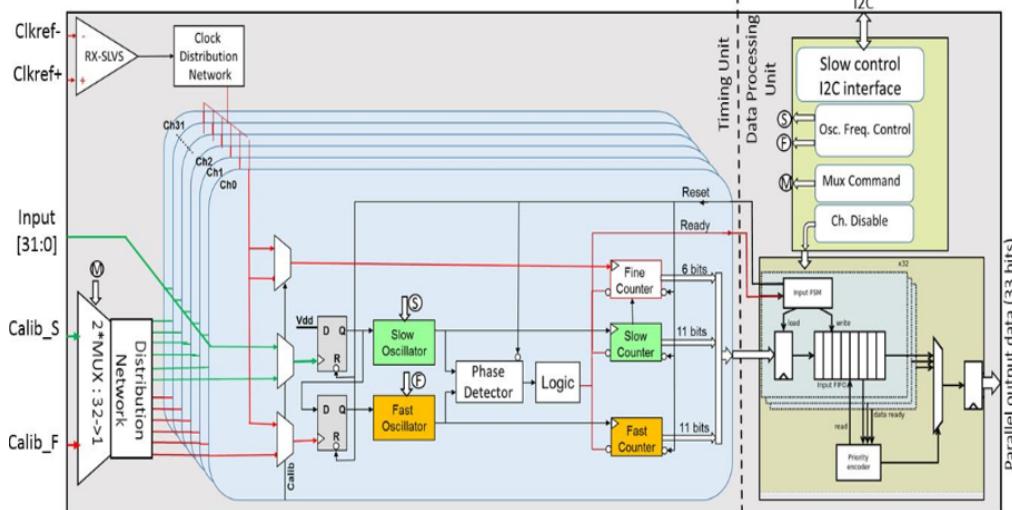
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# CRONOTIC

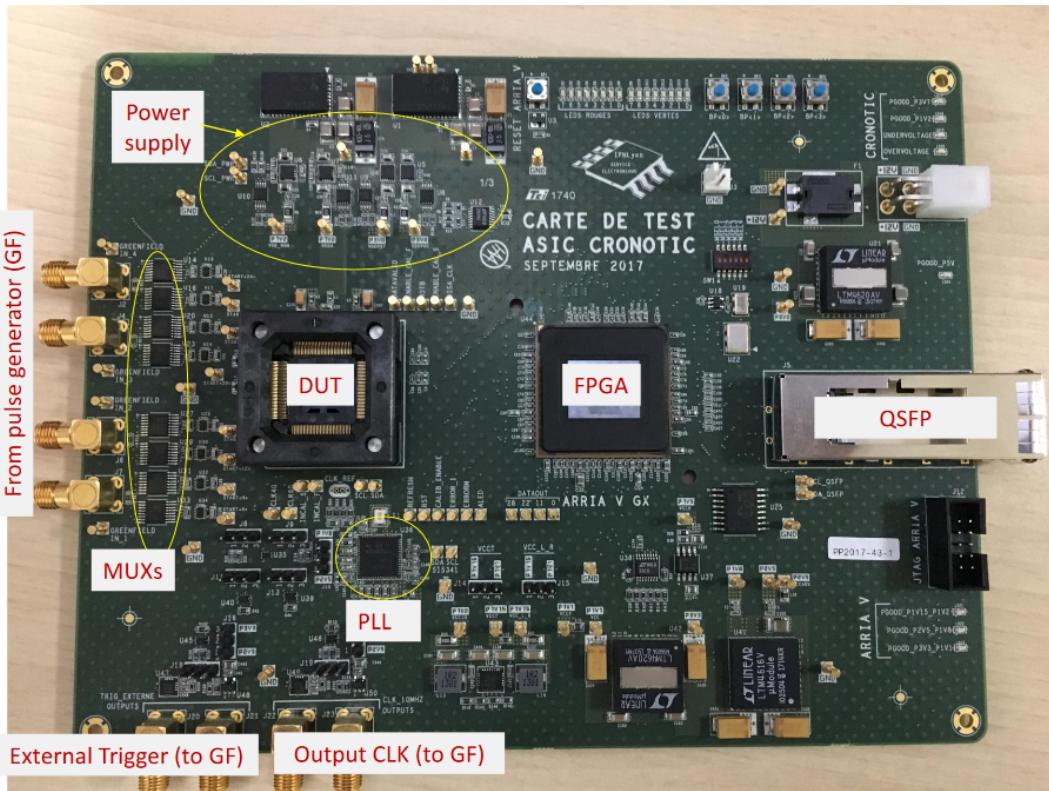
CRONOTIC : block diagram



x32 TDC channels TSMC 130nm

- Vernier Ring Oscillator with a single phase detector technique
- Standard cells used to build the Ring Oscillators(R.O)
- Tsmc 130nm process is chosen according to the technology used in the front-end electronics (PETIROC from OMEGA group)

# CRONOTIC : test board



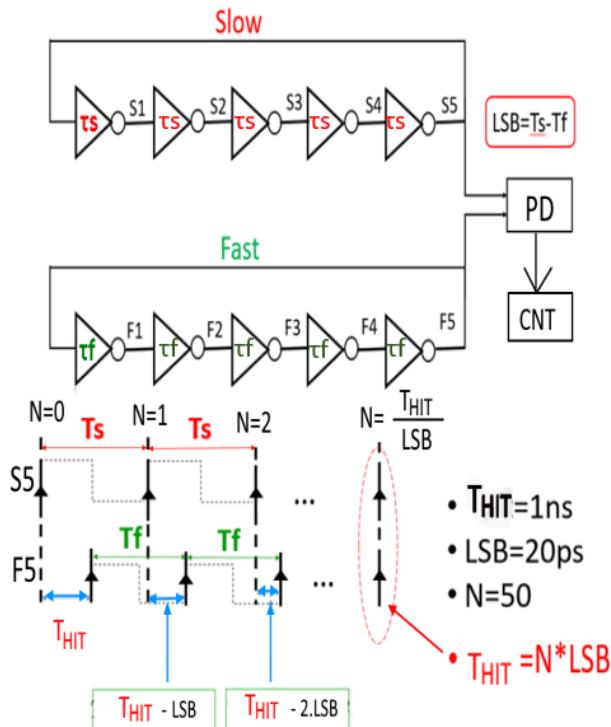
# CRONOTIC : summary

- Preliminary results of CRONOTIC:
  - The configuration of the ASIC through the I2C link is working correctly
  - The digital processing part of the ASIC works (up to a frequency of 90 MHz)
  - Both the calibration and data acquisition modes of CRONOTIC work normally
  - Significant offsets were found on the value of the slow and fast oscillator periods ( during calibration)
  - The slvs circuit operates at frequencies ranging from 100MHz to 900MHz
- Next steps:
  - Calibrate as precisely as possible the frequencies of the oscillators.  
This will allow to :
    - Study the cross talk between the 32 channels of CRONOTIC
    - Measure the resolution (Sigma) of CRONOTIC

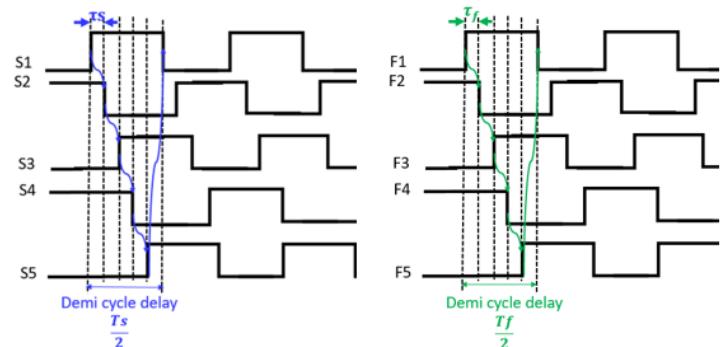


# Vernier technique architecture TDC

## Vernier technique TDC : simple phase detection



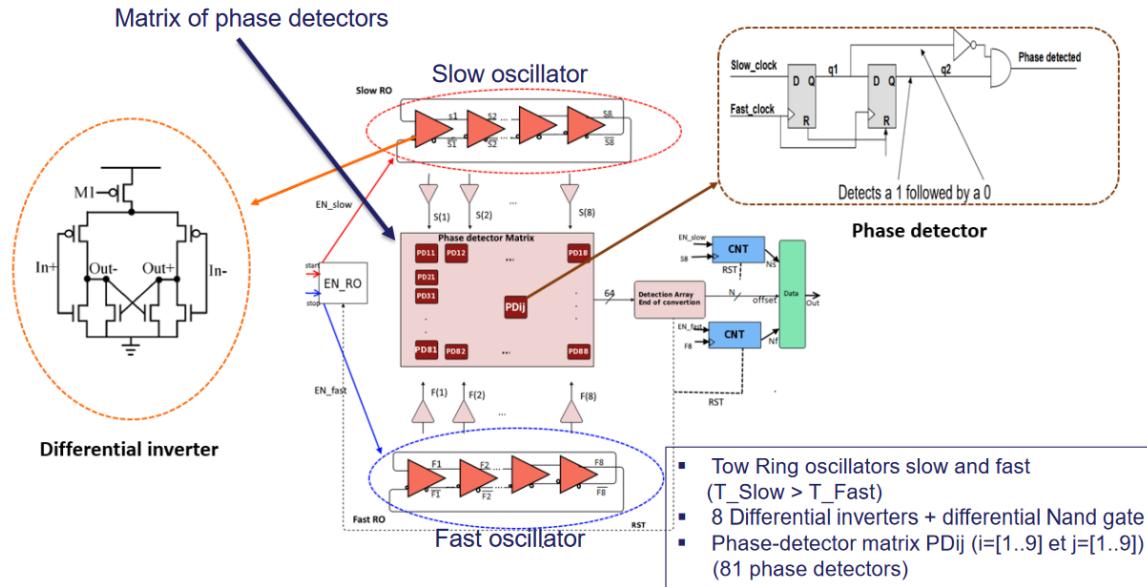
## Ring oscillator chronogramme



S5	$N - \frac{4\tau_s}{\text{LSB}}$	$N - \frac{8\tau_s}{\text{LSB}}$	$N - \frac{2\tau_s}{\text{LSB}}$	$N - \frac{6\tau_s}{\text{LSB}}$	$N_{55} = N$
S4	$N - \frac{4\tau_f}{\text{LSB}} - \frac{4\tau_s}{\text{LSB}}$	$N - \frac{8\tau_f}{\text{LSB}} + \frac{6\tau_s}{\text{LSB}}$	$N - \frac{2\tau_f}{\text{LSB}} - \frac{4\tau_s}{\text{LSB}}$	$N - 6$	$N - \frac{4\tau_s}{\text{LSB}}$
	$N - \frac{4\tau_f}{\text{LSB}} + \frac{2\tau_s}{\text{LSB}}$	$N - \frac{8\tau_f}{\text{LSB}} + \frac{6\tau_s}{\text{LSB}}$	$N - 2$	$N - \frac{6\tau_f}{\text{LSB}} + \frac{2\tau_s}{\text{LSB}}$	$N + \frac{2\tau_s}{\text{LSB}}$
S2	$N - \frac{4\tau_f}{\text{LSB}} - \frac{2\tau_s}{\text{LSB}}$	$N - 8$	$N - \frac{2\tau_f}{\text{LSB}} - \frac{2\tau_s}{\text{LSB}}$	$N - \frac{6\tau_f}{\text{LSB}} + \frac{8\tau_s}{\text{LSB}}$	$N - \frac{2\tau_s}{\text{LSB}}$
	$N - 4$	$N - \frac{8\tau_f}{\text{LSB}} + \frac{4\tau_s}{\text{LSB}}$	$N - \frac{2\tau_f}{\text{LSB}} - \frac{4\tau_s}{\text{LSB}}$	$N - \frac{6\tau_f}{\text{LSB}} + \frac{4\tau_s}{\text{LSB}}$	$N + 2\tau_s \frac{\text{LSB}}{\text{LSB}}$
Edge	F1	F2	F3	F4	F5

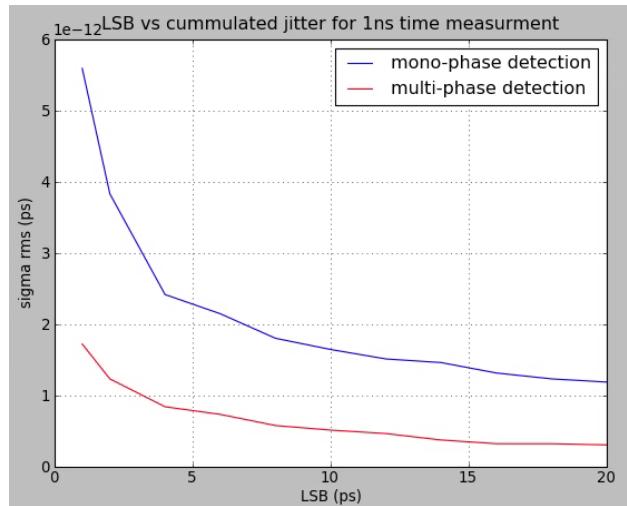
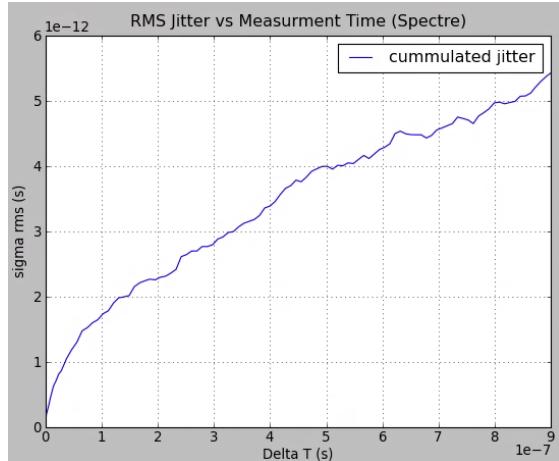
5-cell example Multiphase Edges

# CRONOTIC2 R&D : Multi-phase detector TDC



- TDC LSB =  $T_{slow} - T_{fast}$  (same as signe phase detector TDC)
- Full custom Inverter cells are designed (Sharp edge, 22fs noise jitter simulation )
- Advantage of the multi-phase technique : reducing dead time, cumulated jitter

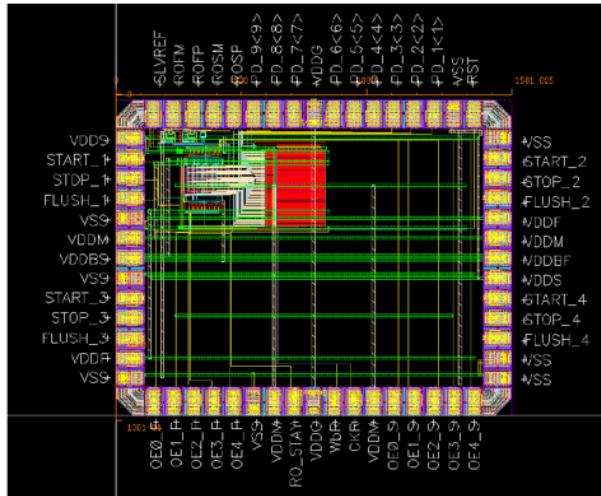
# CRONOTIC 2: Simulation results



- Cumulated jitter  $\sigma_j$  (due to noise or any other source) is the most undesired side effect of the Ring oscillator
- $\sigma_j = K\sqrt{\Delta t}$ :
  - $K$ =cst proportional to the inverter noise jitter (22fs)
  - $\Delta T$  is the measurement time

- Dead time  $\Delta t = \frac{DR}{LSB}$
- For an LSB=20ps and Dynamic range  $DR= 1\text{ns}$  :
  - $\sigma_{j_{simple}} = 3 \times \sigma_{j_{multi}}$

# CRONOTIC2 : Layout of the submitted circuit



TDC prototype in Tsmc 130nm technology

- Demonstrate an architecture suitable for high-resolution TDC
- Observe the Ring oscillator behavior to imperfections and noise
- Highlighted the advantage :
  - Dead time, Cummulated jitter
- Disadvantage:
  - Digital processing, Power Consumption(  $I_{avg} = 34mA$  for both ROs mainly dominate by the matrix buffers)

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# Conclusion

- MicRhAu pole support strongly the TDC *R&D* activity in tsm130nm technology
  - Cronotic A Vernier RO TDC using single phase detector is under test:
    - Simplicity of digital processing unit, less power consumption, less area
    - cumulated jitter and dead time
  - Cronotic 2 A multi phase detector version of the TDC was designed and on fabrication:
    - less cumulated jitter and less dead time
    - complexity of the digital processing unit, more power consumption , bigger area(power and area can be reduce with the matrix size)
  - Improved version of Cronotic will be submitted after the final testing (Cronotic, Cronotic2)
  - Combine Petiroc front-end (OMEGA) and Cronotic in one ASIC for the CMS-RPC time measurement
  - Observe in real situation the advantage and drawback of a multi-phase technique and include improvement for a full and complete chip

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[5] [4]

