CIC project status

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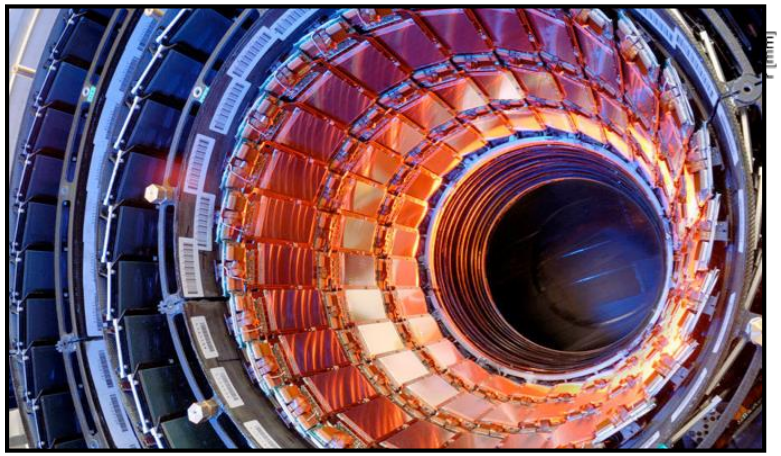
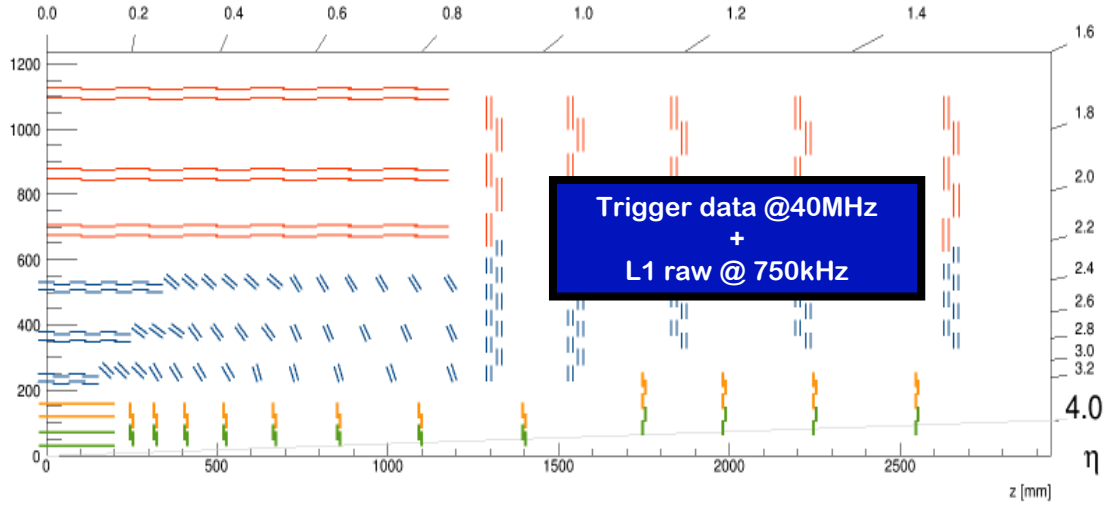
Outline

- Principle and context
- Chip requirements
- CIC model
- CIC physical design
- CIC test system
- Project status
- Project planning & Conclusion

Principle

- Main requirements of the future CMS Phase-II upgrade tracker:
  - HL-LHC running conditions will be very harsh. The future tracker main goal is to make sure that **physics performance will stay stable wrt the current detector .**
  - We are going from a current detector where L1 raw data is extracted @100kHz to a system where the front-end should be able to extract two data streams: **trigger @40MHz and L1 raw @750kHz.**



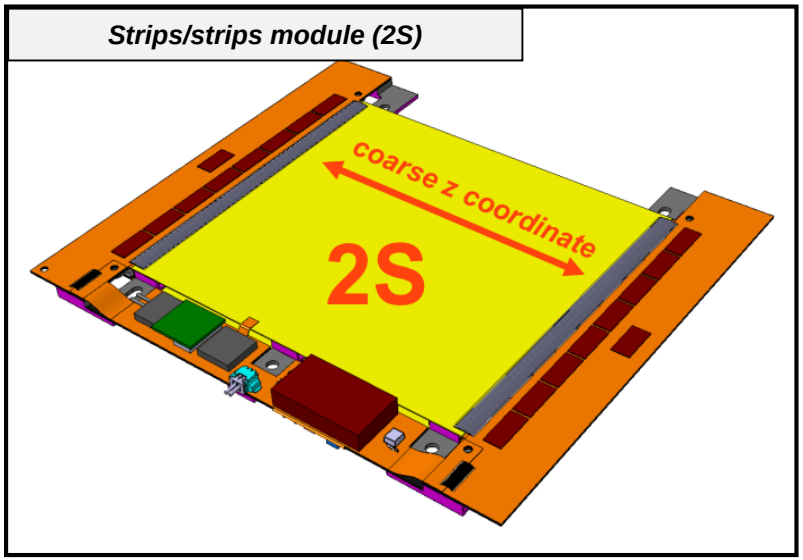


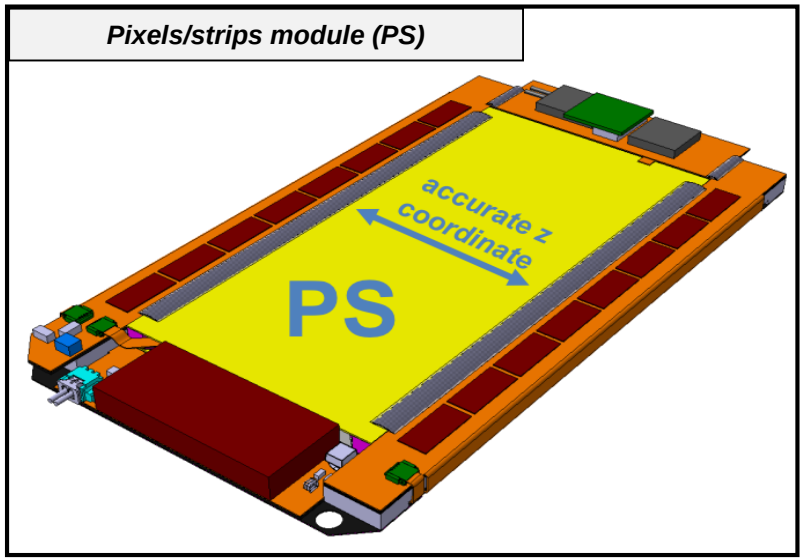
→ To improve the tracker you have to:
• Make it lighter & Increase it's granularity

→ To exploit it at 40MHz you have to:
• Extract data at this rate
• Analyze it within a very short latency

CIC chip is essential for this task

2 module types, 2 front-end flavors:

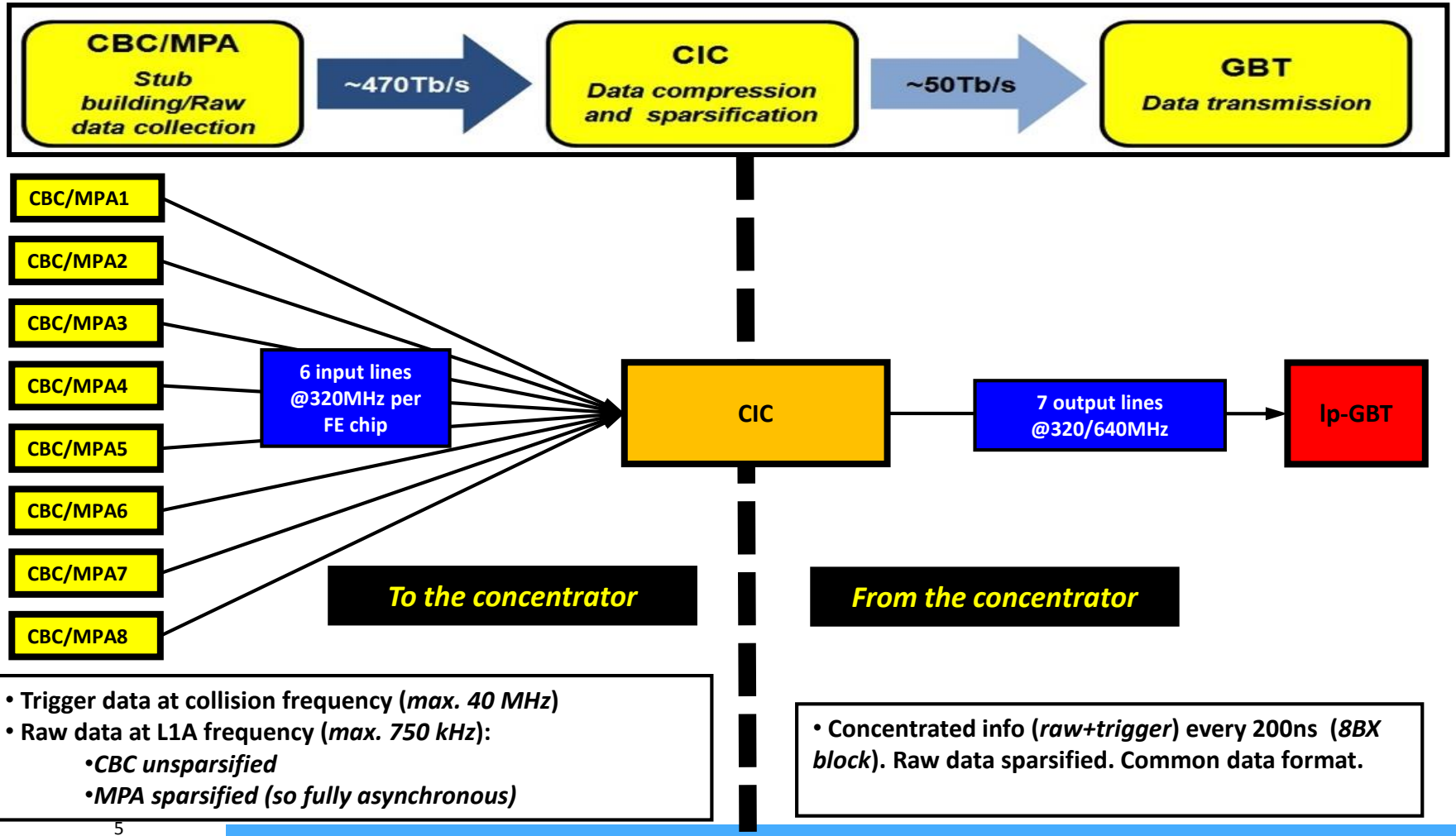




- PS modules are made of 2 different sensors, **pixels** (*1.5mm long strips*) and **strips** (*5cm long, as in 2S*).
- Each CIC is gathering the data of 8 FE chips. There are 2 CIC per module. Signal is transmitted for CIC to back-end via the lp-GBT.
- FE readout systems are slightly different (*different asics, different FE hybrids, different formats*). **Data format uniformization is provided by the CIC chip.**
- CBC/MPA/CIC chips sits on **FE hybrids**, lp-GBT on **service hybrid**.

CIC role in the readout chain

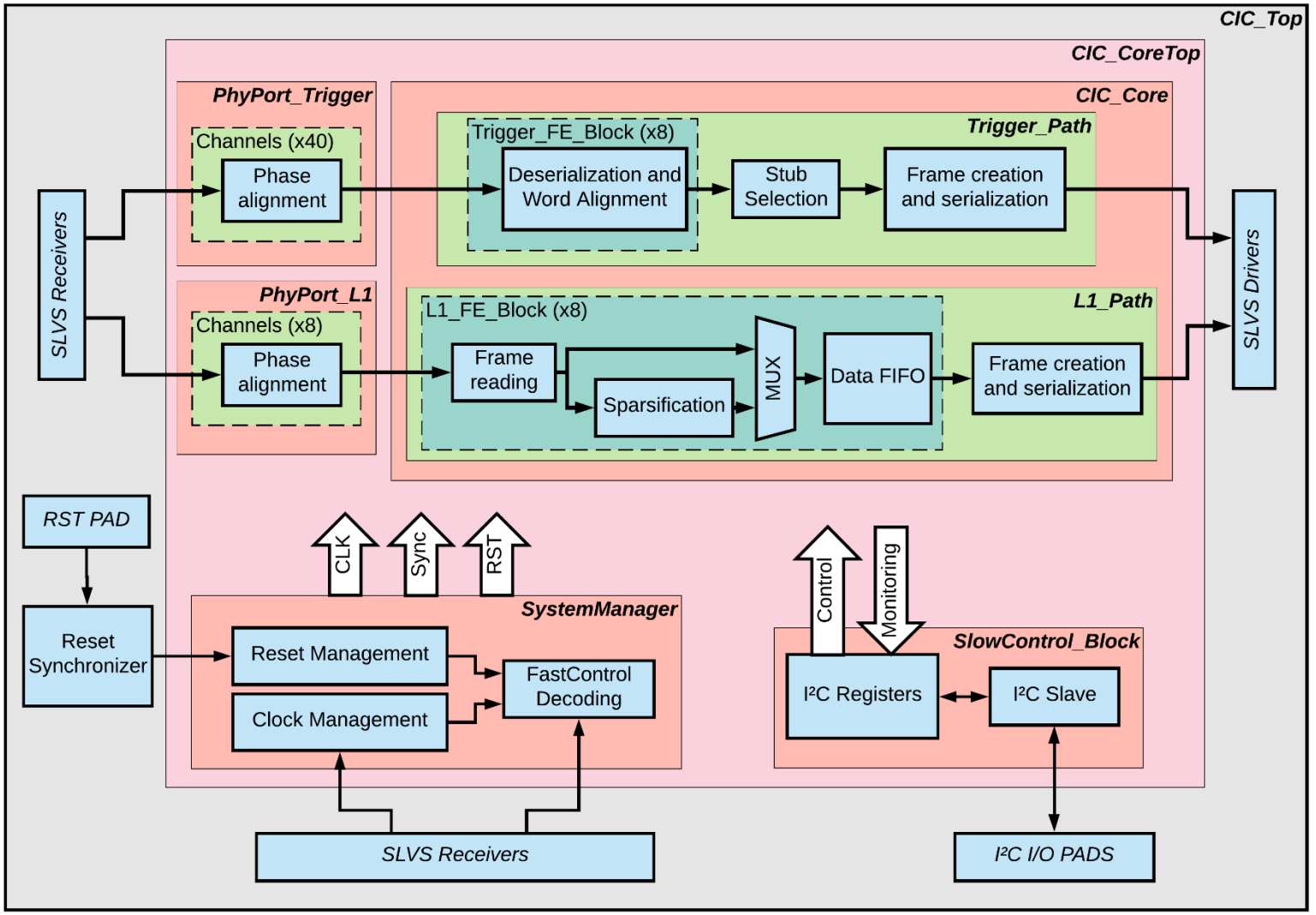
- CIC provides to the readout chain an extra factor 10 data reduction, by grouping data over time (8BX blocks) and space (8 input chips).



CIC main requirements

- **AIM:** *collect data generated by front-end ASICs, select and sort them, format them in an output data format that permits to minimize the data trigger losses and latency.*
- Must live on **two different FE hybrids.**
- Chip core must work at 2 different input voltages: **1.0 V** (PS) and **1.2 V** (2S)
- Receive input from 48 lines at 320Mbps with **2 different formats** (CBC for 2S module and SSA+MPA for PS module).
- Send output via 7 lines at 320/640Mbps into a **pre-defined data format**.
- **TSMC 65nm** technology.
- Placed and routed design using **standard cells** + **analog IPs** (analog macro in the *phase aligner* blocks).
- Memory triplication (SEU hardened design): will be available only in CIC2.
- Bare die (flip chip) with C4 bumps.

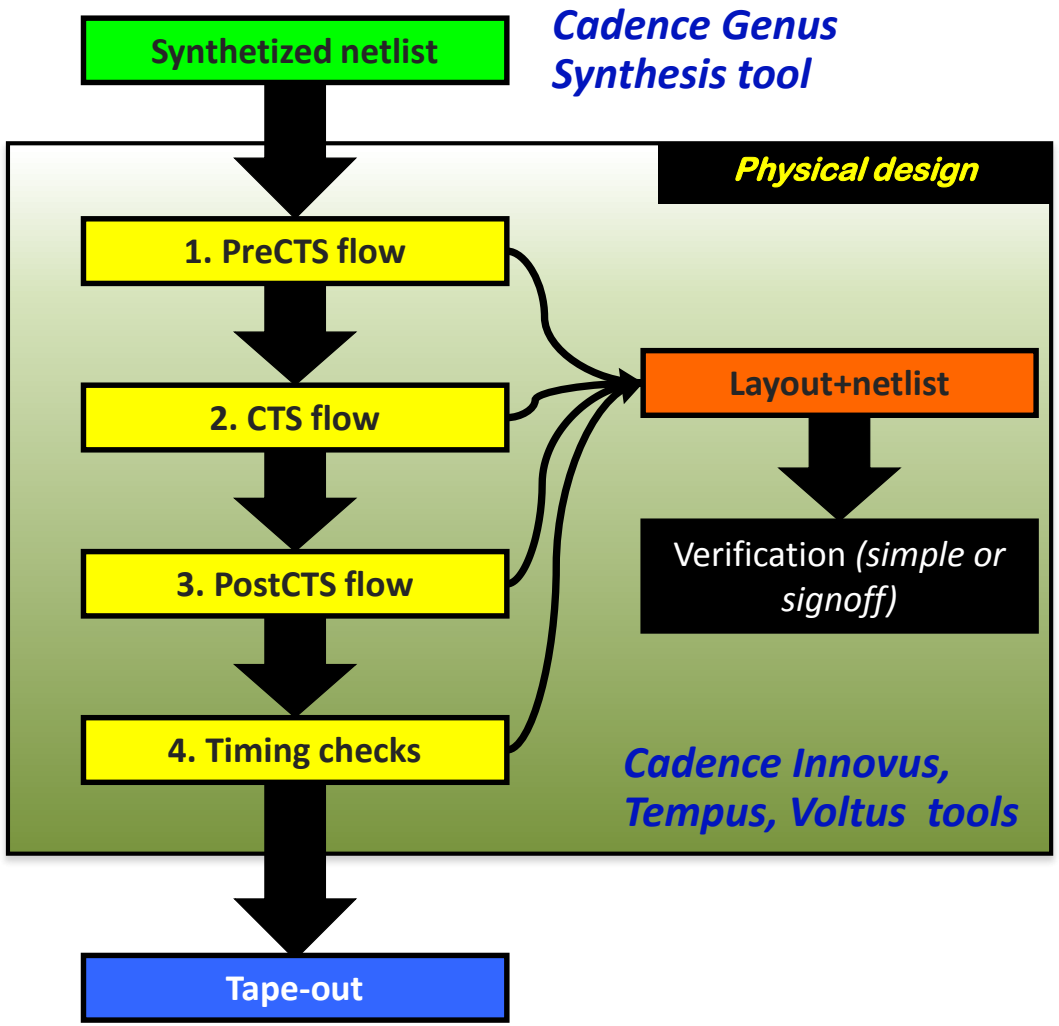
CIC simplified block diagram



CIC model

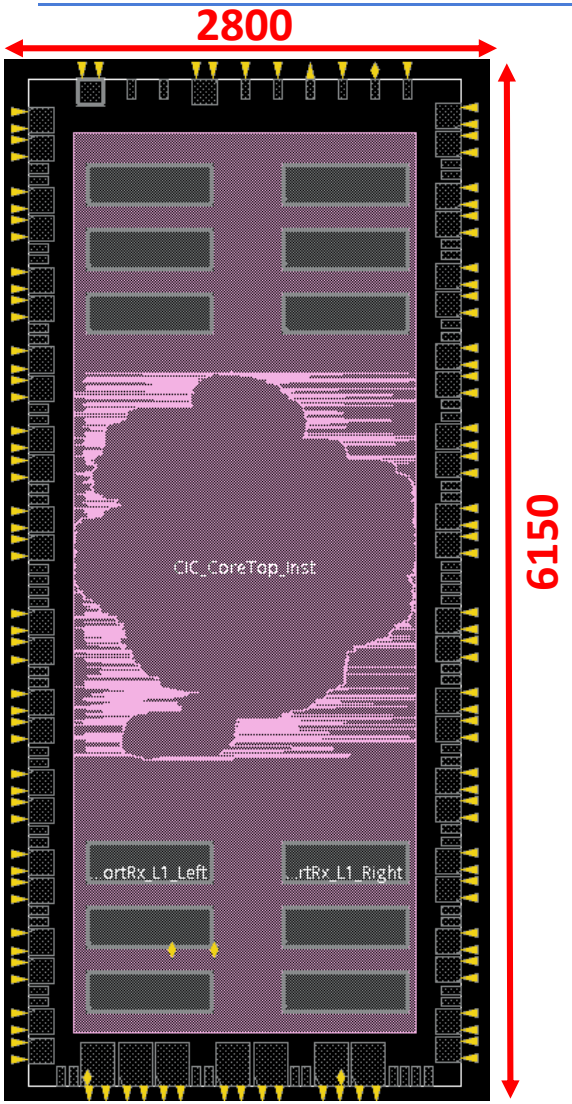
- CIC model written in **System Verilog** language
- Analog IP block called "**Phase Aligner**" (designed by SMU University) used at each input data channel incoming from the 6 lines from each MPA/CBC front-end. Phase alignment is required in order to synchronize the signal with the internal clock (320 MHz).
- The **CIC_Core** is based on two different data paths working in parallel and independently:
  - **Trigger data path**: treatment (deserialization, word alignment, stub selection and frame creation) of data payload produced @40MHz, the information necessary to the L1 track reconstruction system.
  - **L1 data path**: treatment (sparsification in the case of CBC, storing in a FIFO, frame creation) of raw tracker data. This data payload is sent on request each time an L1-accept signal is emitted.
- **SystemManager** block manages the clocks generations (40 MHz, 320 MHz, 640 MHz), clock gating, reset generations, command decoding from the fast control frame.
- **SlowControl** block manages the communication via I^2C protocol for control and monitoring of the system. It contains the I^2C slave (from CERN) and the internal slow control registers.

Digital design flow



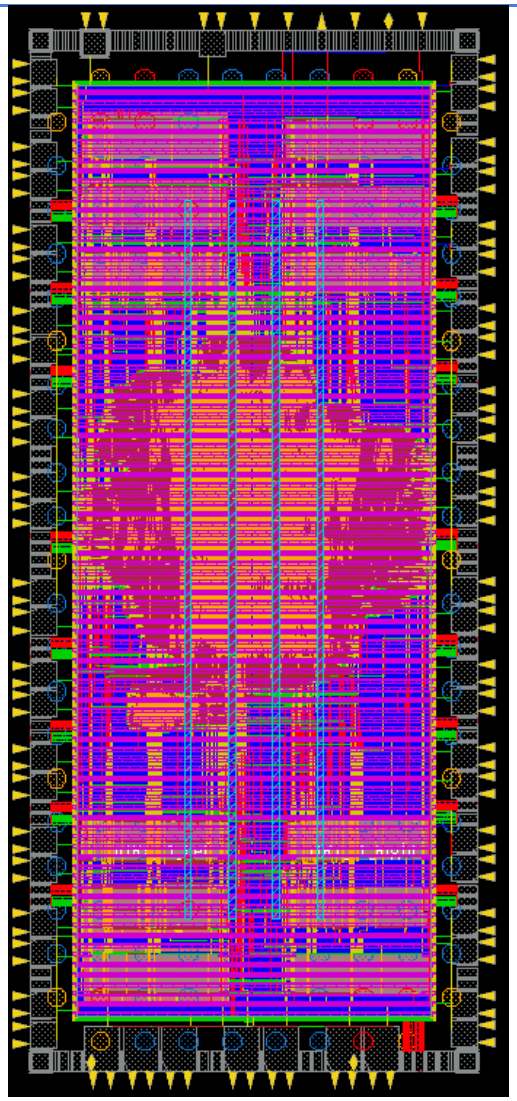
- The digital flow, based on a series of scripts, permits to reach the final file (**GDS**) for the Tape-out phase starting from the behavioral description of the architecture (**RTL**).
- Tape-out phase: final step before the ASIC fabrication.

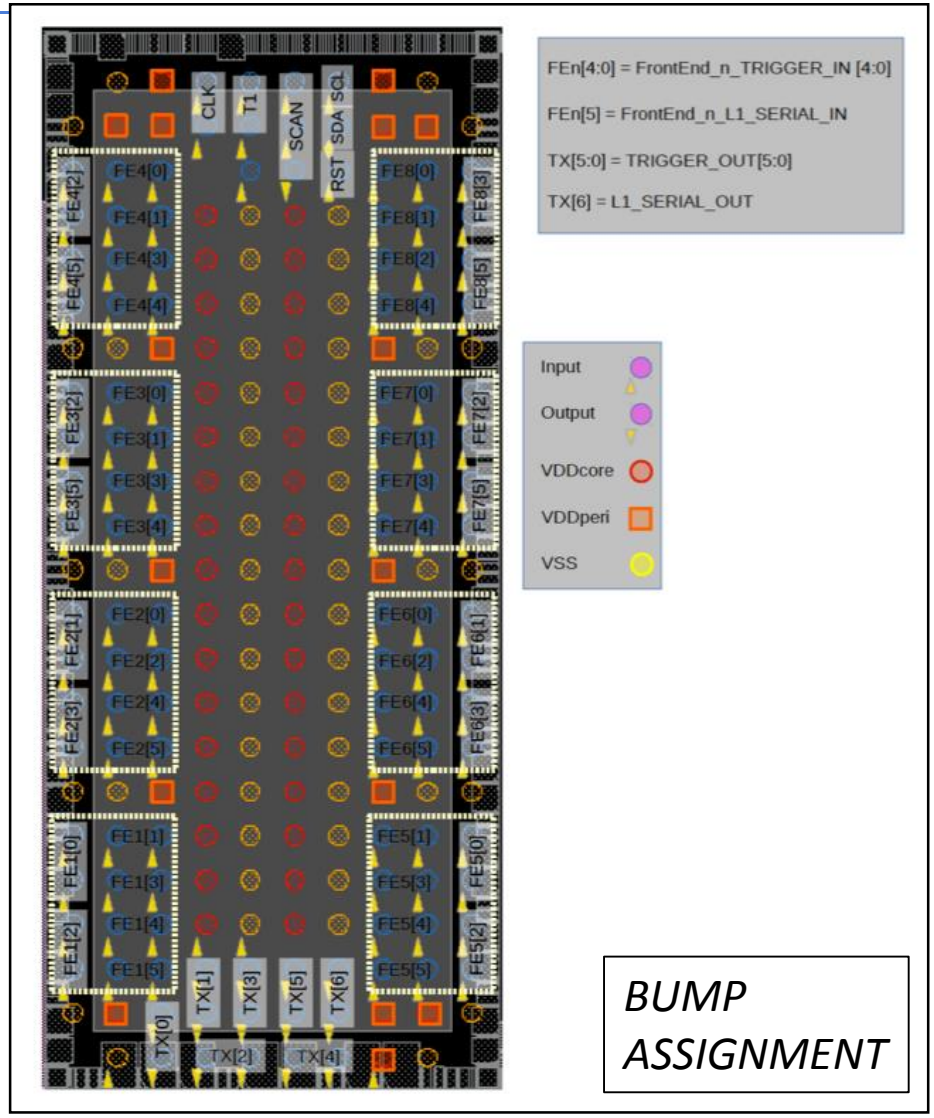
Physical design



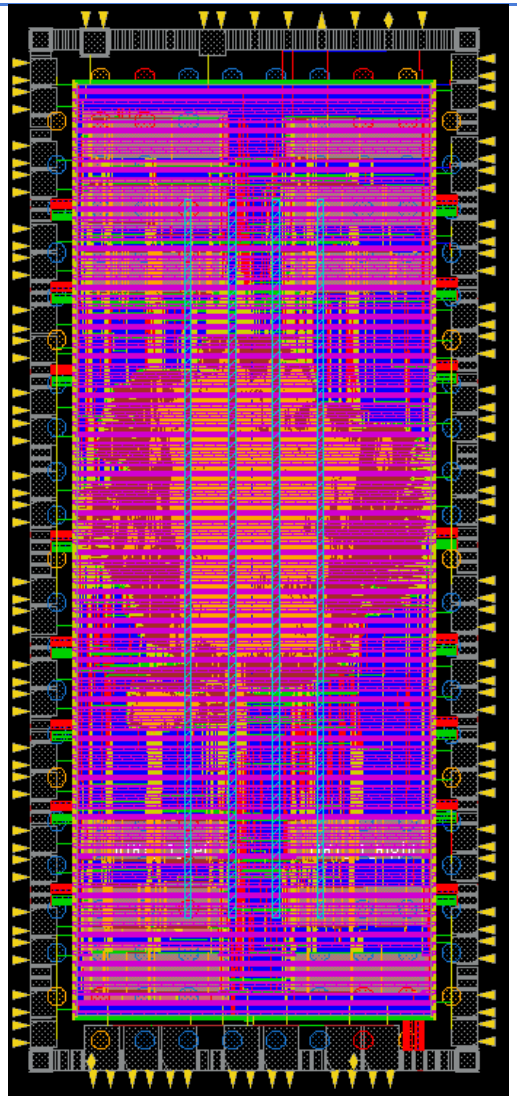
- Digital on Top implementation
- Die dimensions take into account bondable pad + seal ring (not shown in figure)
- Process TSMC 65nm LP 1p7m4x1z1u metal stack
- Wire bond with AP RDL (not shown in figure)
- **Periphery ring:**
  - 48 sLVS RX pads along the left and right sides (core+periphery supplies)
  - 7 sLVS TX pads on the bottom side
  - 2 sLVS RX + 7 CMOS pads on top side
- **PHY-ports:**
  - 2 PHY-port blocks phase-aligns 8 L1_IN bitlines wrt SYS_CLK
  - 10 PHY-port blocks phase-align 40 TRIGGER_IN bitlines wrt SYS_CLK
- **CIC_Core**:
  - Flat synthesis of trigger and L1 data-path, I^2C and Fast control blocks.
  - 8 Front-End blocks each containing a 16 words by 800b FIFO @40 MHz (22,6k cells).
  - **~372k standard cells**

Physical design





Physical design



- **Top level power routing:**
  - 15 vertical stripes in AP layer
  - 98 horizontal stripes in M7 layer
- **Periphery supply:**
  - The power routing of the periphery supply is being kept separate from the core
  - Radiation tolerant ESD protections (designed by SOFICS): used in periphery ring
- **Clock tree synthesis (CTS):**
  - Clock tree routed using M5 and M6

CIC power estimation

- Power budget @ PS module: **250 mW**
- Power budget @ 2S module: **300 mW**

- Power estimates (in mw) were processed for the complete chip (CIC_top), for the **worst corners** in 2 differents configurations. For the analog Phyport part estimations are used.

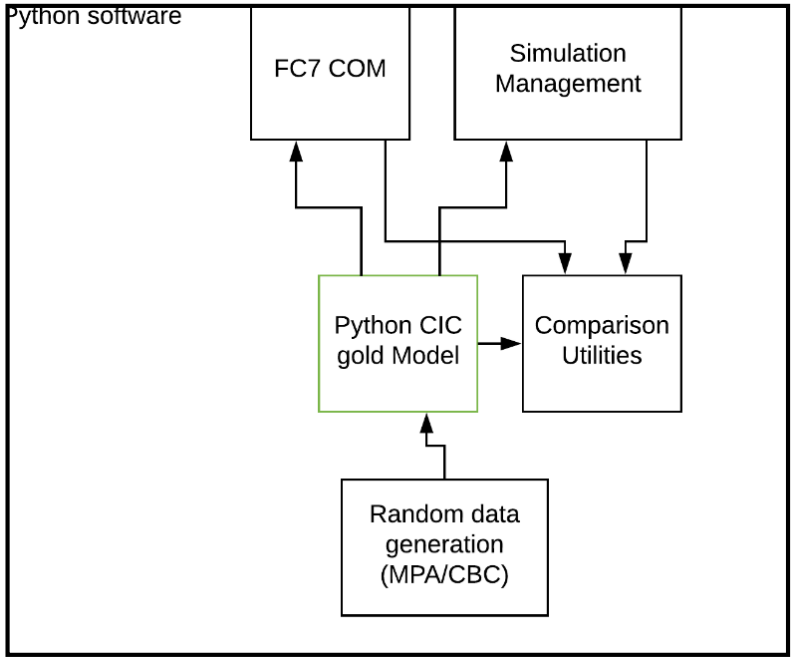
Corner		Startup phase (*PhyPort init,...*)			Running phase (*high input load*)		
		Digital	***Analog***	***Total***	***Digital***	***Analog***	***Total***
PS-like	1.1V/0° C	182	27	**209**	183	16	**199**
2S-like	1.32V/0° C	259	63	**322**	282	56	**338**

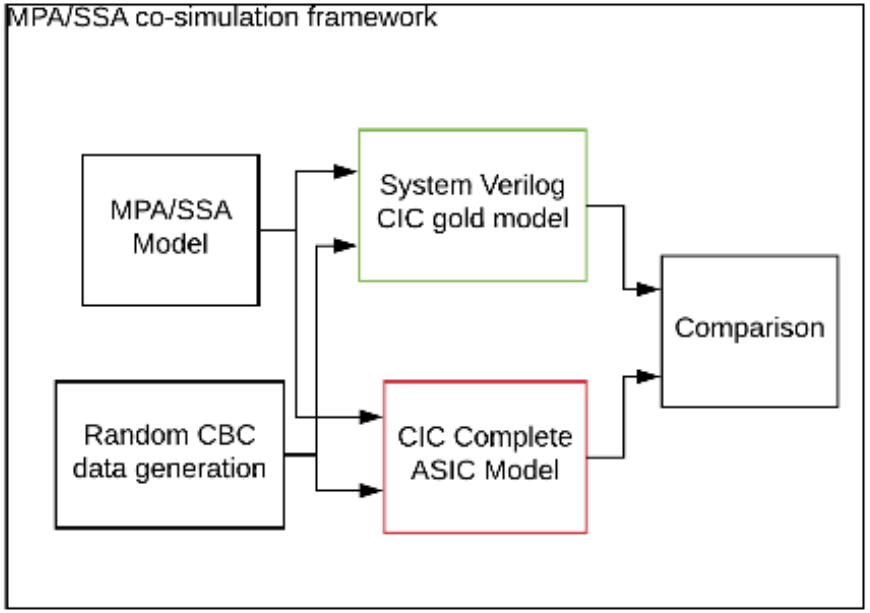
- This is before CTS (expect **30% increase** then), but **without any power-oriented optimization**. We will not further optimize the power budget for the CIC1.

CIC testbench

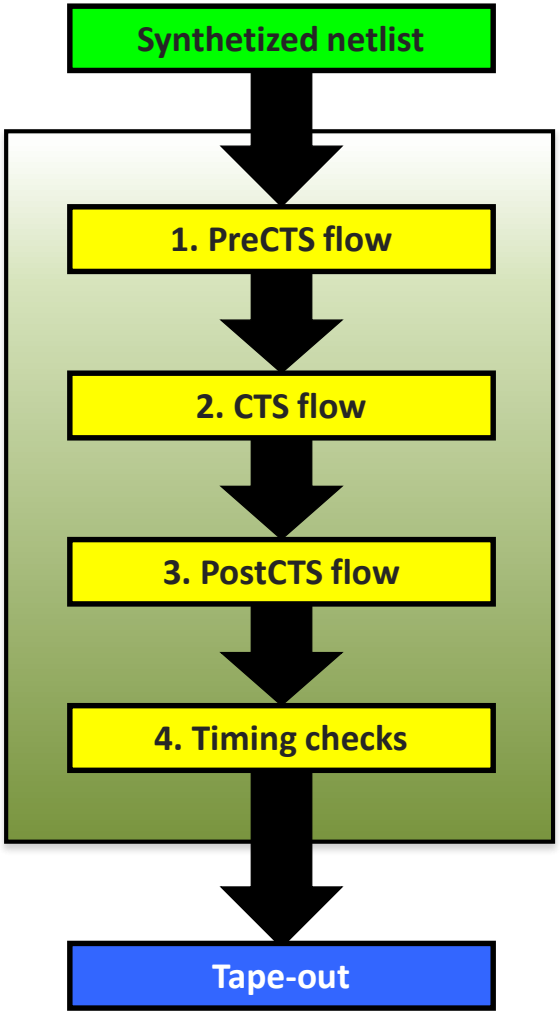
- A **standalone testbench** has been implemented in order to:
  - Check model functionality
  - Perform the comparison between data stream from CMS simulation environment with the CIC model output after the phase alignment and data treatment.

- **System level Testbench** for the validation of the full acquisition chain, developed at CERN





CIC status



full set of scripts exists: Constraints are ready at 80%.

Scripts exist: to be refined after latest RTL modifications.

To be revised: to include latest RTL modifications and recommendations from the design review.

Scripts are being defined right now.

To be validated.

Project planning (1)

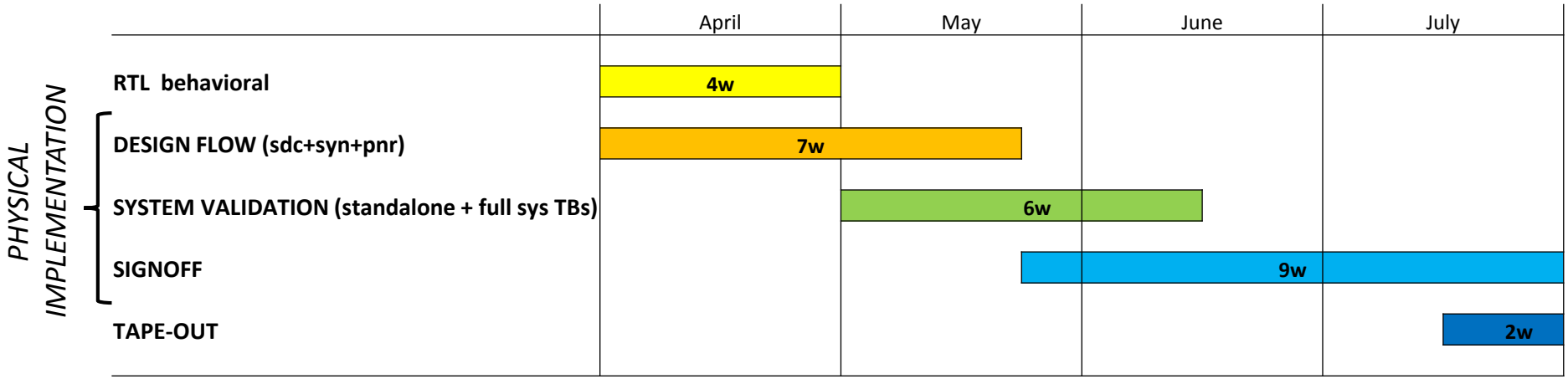
- This is the **first digital ASIC** design in TSMC 65 nm technology within MicRhAu
- As this is the last chip to be produced within the acquisition chain:
  - Must take into account all the flaws of the other ASICs (non-negligible impact on project planning).
  - 6 months delay accumulated along the year since Oct 2017:
    non-availability of external info (lib file of the CERN phyport obtained in Dec 2017, significant change of the form factor was required in Oct 2017, etc)

- **Complete redesign of the architecture during 2017**: structure, blocks etc were rewritten.
- Major work on the interfaces during the beginning of 2018 (SysManager block).

Project planning (2)

- At the end of 2017 two **design reviews** have validated the design.
- Chip size and I/O assignment can be considered as **final**, except for the CLK and T1 (*fastcontrol*) pins, which may have to be moved due to timing issues.
- Main missing elements are now the **ESD protections** for supply **core** pins to be placed inside the core area (*IP blocks to be provided by CERN*).
- Apart from minor modifications, the CIC1 Model can now be considered as **complete and functional**.
- **~100 prototypes** of CIC1 are foreseen to be produced
- We are therefore now planning the CIC1 run for **July 2018** if no external issue occurs:
  - PS module hybrid modification
  - System interface definition and validation
  - ESD protection availability

Timeline



Milestones:

- **Begin 2019**: Prototype test (CIC1+ 8 Front-End + FE-Hybrid).
- **July 2019**: CIC2 production.
- **Begin 2020**: Pre-production of FE assemblies starts (FEH, SEH, MaPSA).
- **End 2020**: Final ASIC production (30k units).
- **End 2022**: End integration of the tracker.

CIC team

➔ **L. Caponetto (IPNL)**: **technical coordination**, physical design

➔ **G. Galbit (IPNL)**: digital design, system test and CIC characterization testbench

➔ **B. Nodari (IPNL)**: block-level synthesis, physical design

➔ **S. Scarfi (CERN)**: system validation

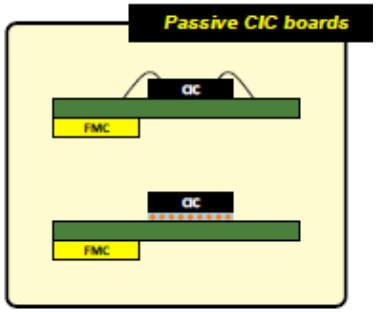
➔ **S. Viret (IPNL): scientific coordination**

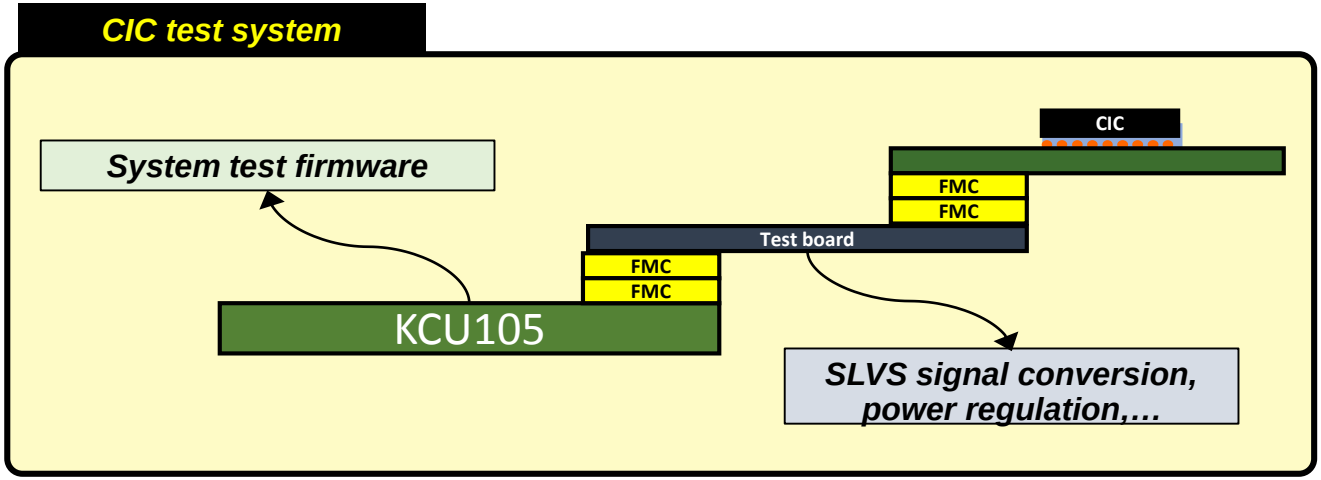
➔ In addition to that we can now count on the support from the CERN CMS TRACKER IC team, which has gained good experience in the TSMC 65 nm technology.

Back up

CIC test system

- CIC prototypes will be soldered on small passive PCBs and will be driven externally.
- 2 PCB flavors will be produced: **wire-bonded** and **soldered** (we will also order bumped CIC1 wafers).
- Necessary tasks are:
  1. Design and routing of the 3 specific board (test vehicle, test board, converter)
  2. Implementation of the test bench **firmware**
  3. Implementation of the test bench **software**
- The full system will use 3 boards:





➢ **C. Guerin & W.Tromeur** (IPNL) : CIC characterization testbench and boards development