R&D Time-to-Digital Converter TDC

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Pôle MicRhAu

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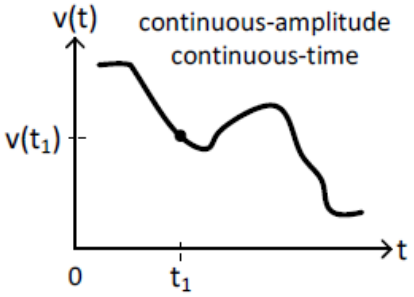
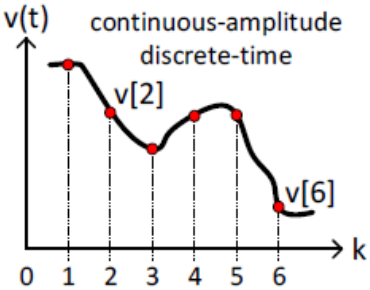
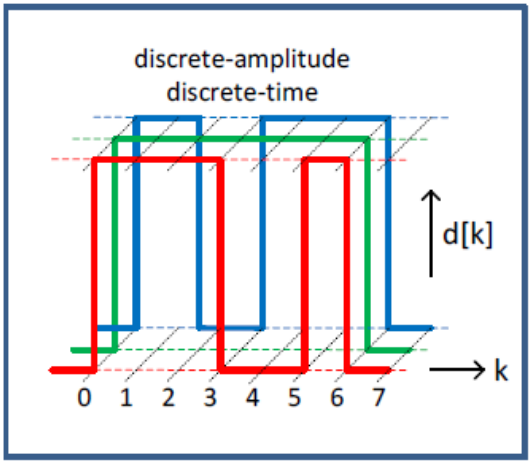
Plan

Plan

Information Carrier of an Electrical Signal

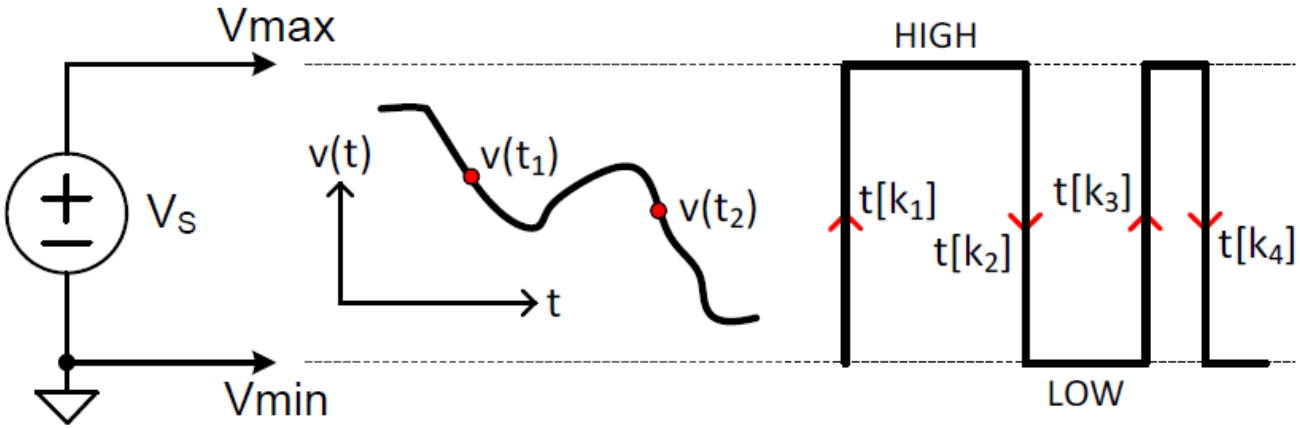






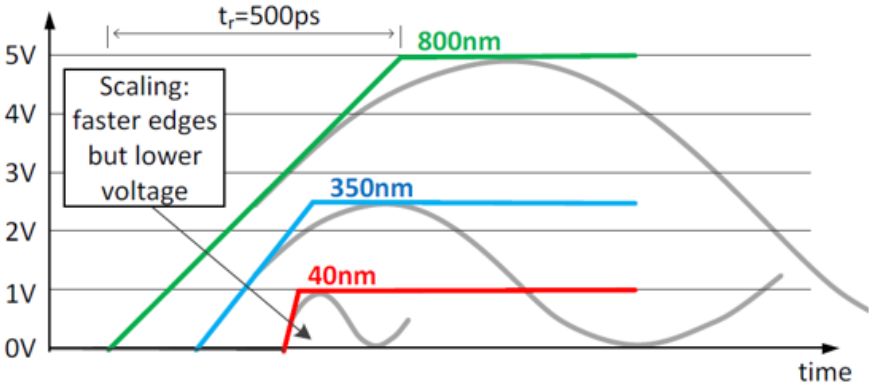
- The Electrical signal representations are well known and commonly used:
  - Continuous-amplitude and continuous-time (Analog signal)
  - Continuous-amplitude and discrete-time (Sampled analog signal)
  - Discrete-amplitude and discrete-time (Digial signal)
- Is this all? Can a signal be represented in other forms ?
- What about time ?

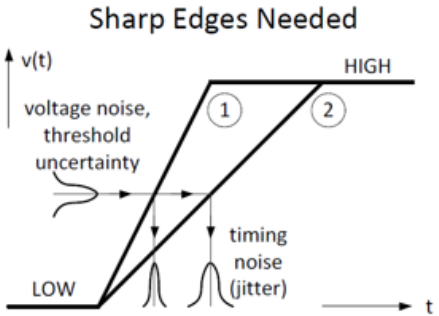
Time-Domain Signaling



- Instead of the amplitude, it is the time (i.e, timestamp) that carries the information t$[k_1]$
- R. Bogdan Staszewski (Professor, IEEE Fellow University College Dublin) : In deep-submicron CMOS process, a signal representation in time domaine will be more interesting than voltage domaine ([4] [3])

Technological Limitations

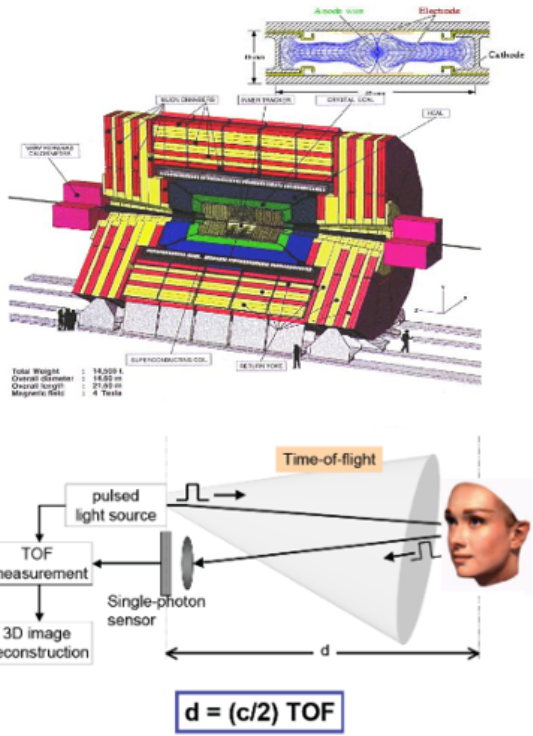




- In the past, the voltage resolution of v(t) was good (5V, 3.3V et 2.5V)
- But the circuit technology has been painfully slow (rise time $tr_{800nm} = 500ps$, $tr_{350nm} = 50ps$)
- Transition edge that carries the information needs to be sharp, otherwise the slow transition uncertaintly and timing jitter will worsen the timing signal.
- The new CMOS technologies are extremely fast (tr_{130n}=[20ps 50ps] tr_{90nm}=[10ps 20ps] but a low supply voltage (at or below 1.5V).

TDC Applications

- TDC applications in CERN HEP:
  - Drift time in gas based tracking (CMS, ATLAS)
  - Time Of Flight (TOF) interaction (ALICE)
- Medical imaging (Hadron Therapy)
- 3D Imaging (TOF), LADAR (Laser RADAR)
- Domaine of phase and delay synthesis (full -digital PLL)



Plan

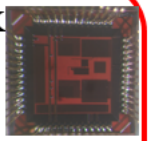
Time Line of TDC application in MicRHAU pole

ASIC

HODOPIC
Delay-line
S.Deng

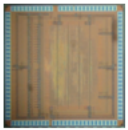
LSB=200ps
Resolution=700ps$_{RMS}$

TDC BRICK
Vernier RO
IBM 130nm



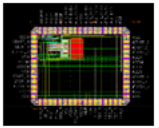
XOR standard cell
LSB=60ps over 1ns
Resolution=25ps$_{RMS}$

CRONOTIC
Vernier RO



32-ch, CMS_muon
LSB: 20ps target
Under test

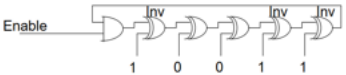
CRONOTIC2
Multi-detection de phase
LSB < 20 ps target
Resolution <2 ps$_{RMS}$
traget



2013 2014 2015 2016 2017 2018

FPGA

R&D, C. Girerd.
Vernier RO Cyclone III
Tuneable RO ➔XOR gate delay
LSB=10ps over 2.4ns range



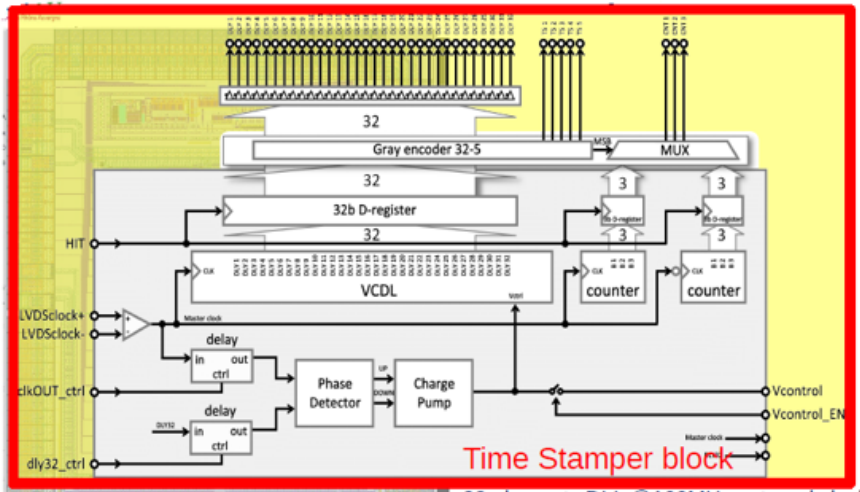
Tsinghua university for
RPC/MGRPC

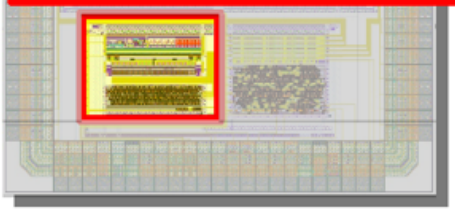
24-ch, Delay-line TDC
Resolution = 25 ps$_{RMS}$

CMS_muon
64-ch, TDC Cyclone V
Target
35 ps$_{RMS}$
with(Generator)
200 ps$_{RMS}$ With detector

HODOPIC Time stamper block

- Voltage Delay Locked loop (VDLL) for a Time stamper converter





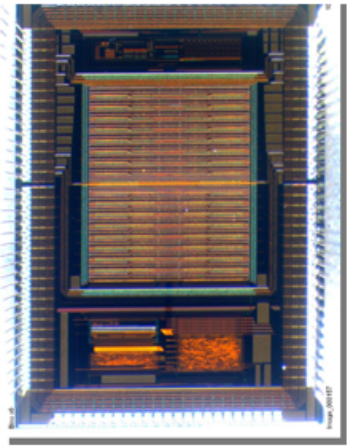
32 elements DLL @160MHz external clock (as in SCATS chip)

2x 3b counter provides 50ns time dynamic (as in IMOTEPAD chip)

5b Gray decoding of the 32b Voltage Controlled Delay Line

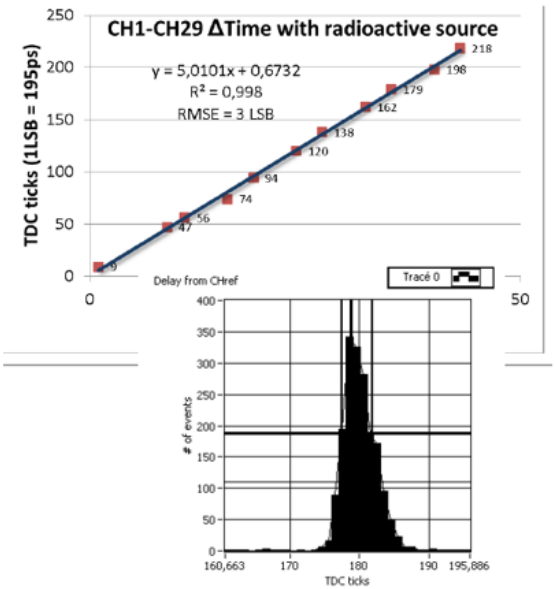
DLL architecture described in S.Deng PhD thesis

Readout of a beam hodoscope with time tagging



HODOPIC AMS 0.35um

HODOPIC Time stamper block



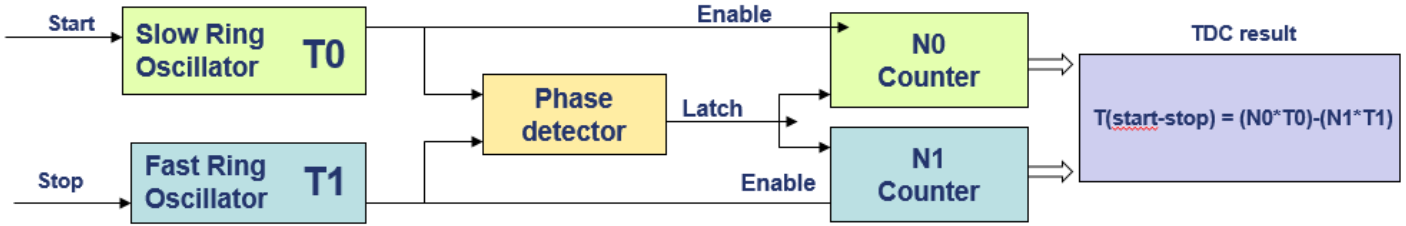
HODOPIC tests and measurements:

- **LSB =195ps**
- **Resolution (RMS) = 700ps = 3LSB**

- Advantage of the DLL :
  - High integration level by using standard digital CMOS
  - Sensitivity to environmental conditions is factored out by the self-calibration mechanism.
- Disadvantage of the DLL :
  - The time resolution is limited to the unit cell delay (td= 50ps ams 350nm)
  - For higher resolution, faster technologies must be used
- Another possibility to overcome the resolution limit: Sub-gate technique [1] [2]

R&D in TDC: Vernier technique (C.Girerd)

Beyond the limits of the technology: Vernier technique



The TDC time resolution is given by the frequency difference between oscillators : LSB= Ts-Tf

- In theory the resolution can be very small, as small as the frequency difference

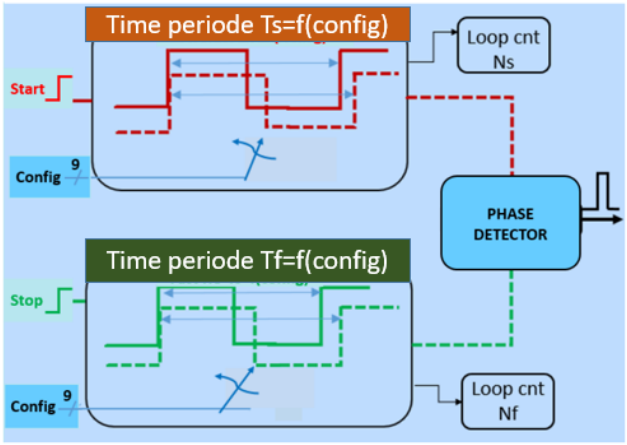
- Simple architecture: Low Area, low consumption, can implemented in standard cells

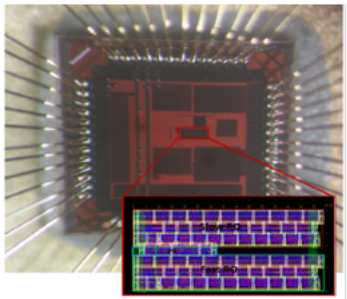
ASIC	[1] Youngmin Park Wentzloff	[2] Jianjun Yu
Process	65 nm	130 nm
LSB	1 ps	8 ps
DNL/INL	0.5/0.8	0.5/0.8

FPGA	[3] Sachin S. Junnarkar	C. Girerd
Process	ALTERA Stratix II	Cyclone III
LSB	11.8 ps (rms)	~ 10 ps
DNL/INL	0.5 / 1	-

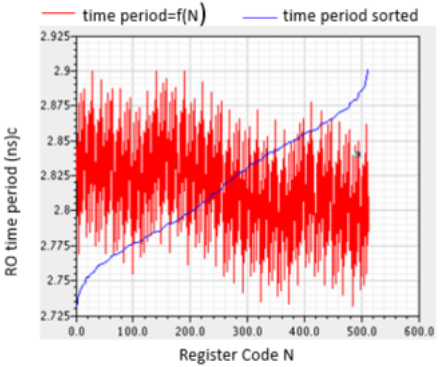
TDC BRICK for R&D

Tow Ring oscillators in vernier configuration





TDC IBM 130nm

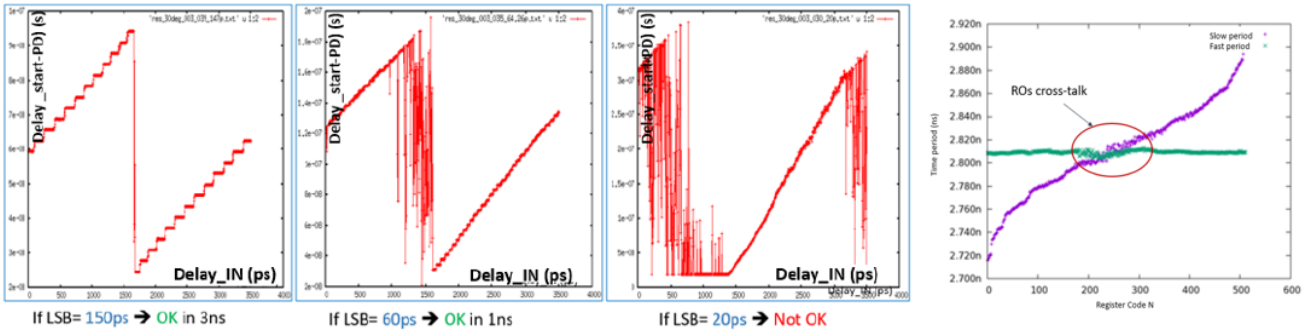


512 configuration Code for fine tuning
Frequency range [340MHz 370MHz]

- The frequency of each RO is adjustable thanks to 9-bit register
- The resulting LSB often called $\Delta t = T_{slow} - T_{fast}$ could be theoretically adjusted down to 10fs

TDC BRICK for R&D

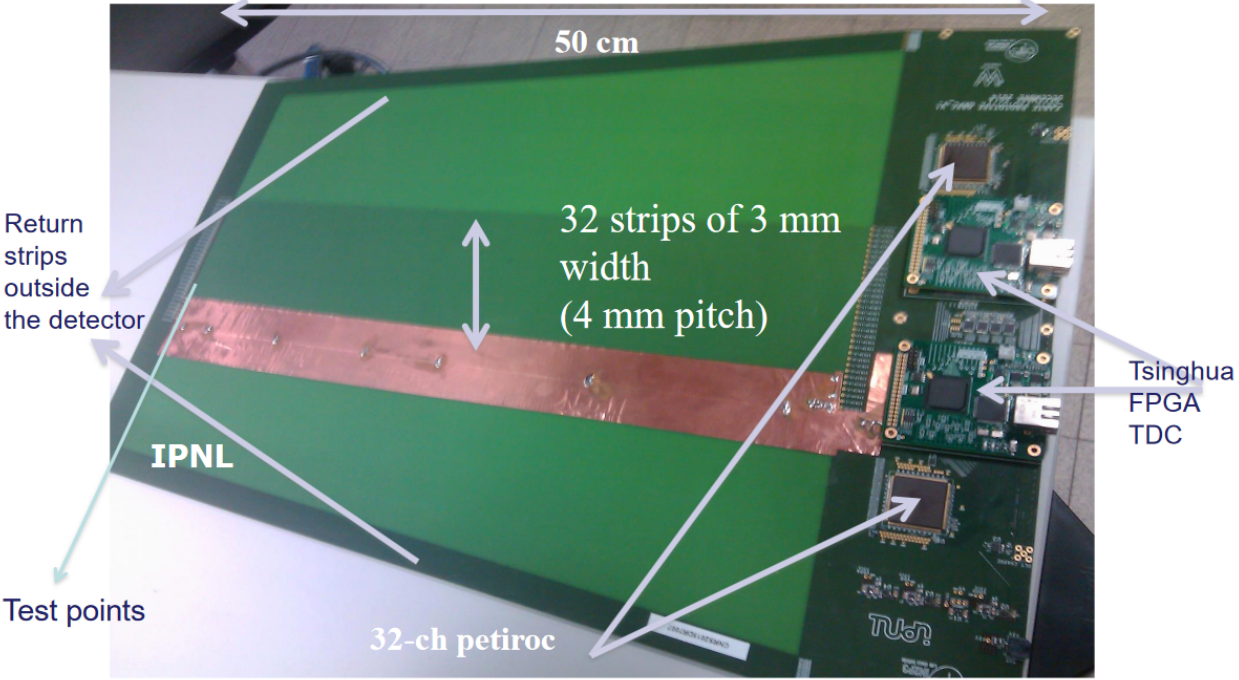
Measured (I/O) characteristic of the TDC for different LSB configuration



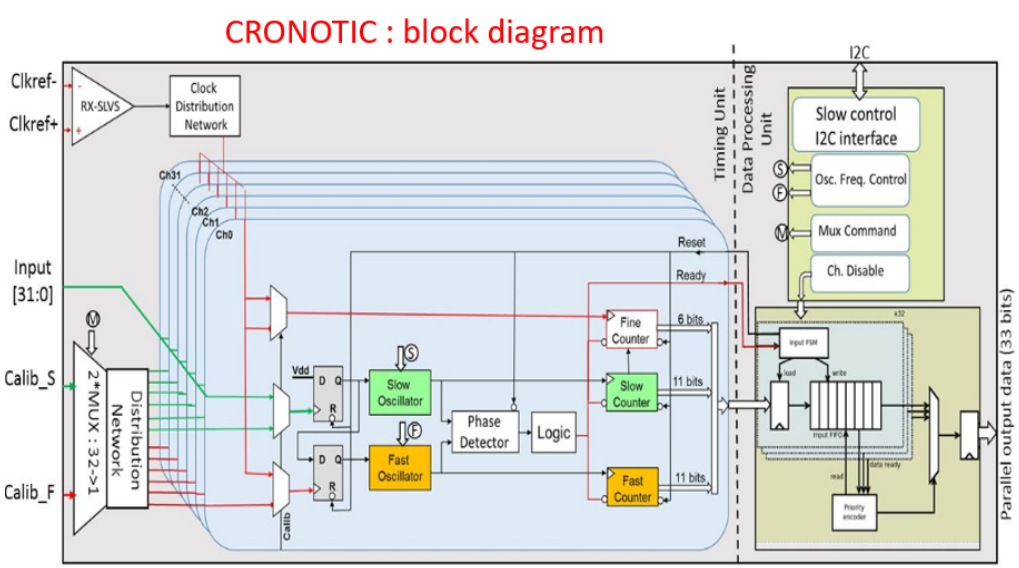
- Advantage
  - High integration level
  - Very good time resolution and dynamic range
  - Save silicon area and power
- Disadvantage
  - Accumulated timing errors
  - Coupling between the ROs
  - Calibration is done off-line

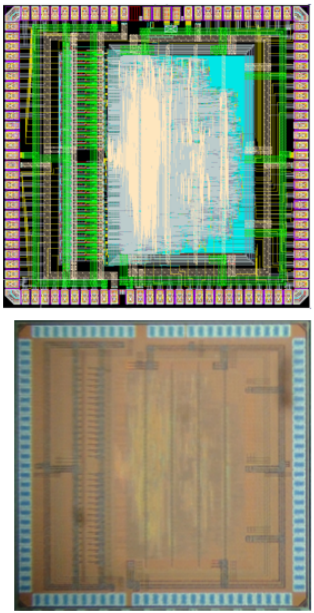
Electronics for Multigap CMS-GRPC detectors

A PCB was conceived to host : Pickup strips, 2 PETIROC, 2 TDC
A DAQ system was developed. The PCB is intended to equip large chambers



CRONOTIC

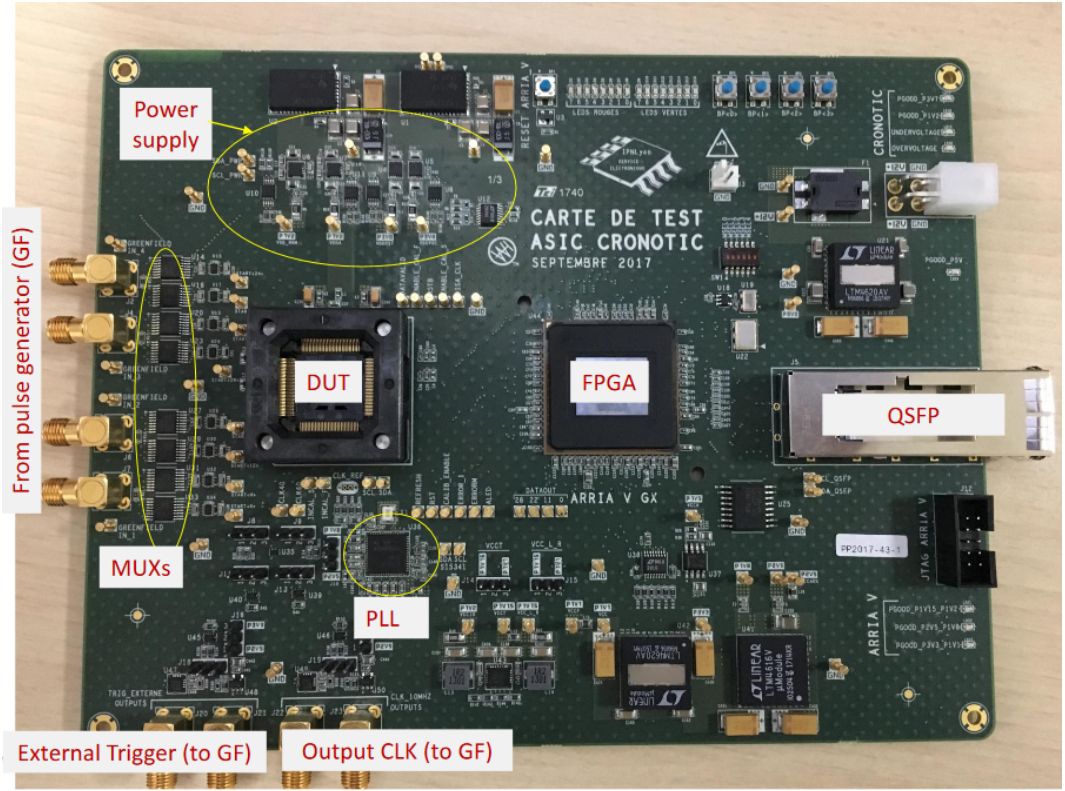




x32 TDC channels TSM 130nm

- Vernier Ring Oscillator with a single phase detector technique
- Standard cells used to build the Ring Oscillators(R.O)
- Tsmc 130nm process is chosen according to the technology used in the front-end electronics (PETIROC from OMEGA group)

CRONOTIC : test board

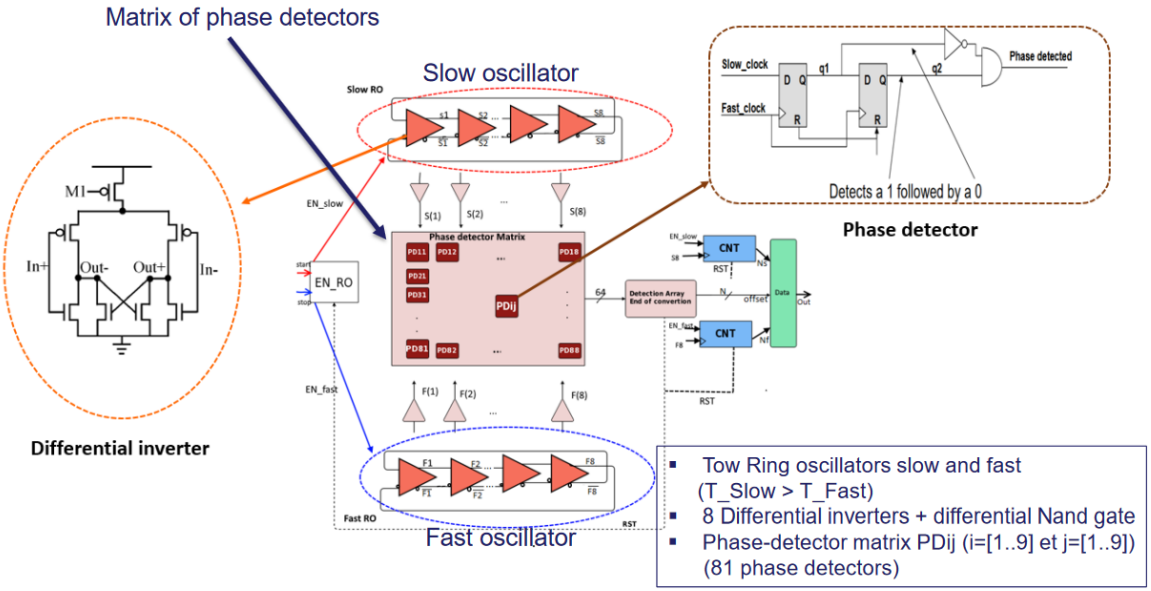


CRONOTIC : summary

- Preliminary results of CRONOTIC:
  - The configuration of the ASIC through the I2C link is working correctly
  - The digital processing part of the ASIC works (up to a frequency of 90 MHz)
  - Both the calibration and data acquisition modes of CRONOTIC work normally
  - Significant offsets were found on the value of the slow and fast oscillator periods (during calibration)
  - The slvs circuit operates at frequencies ranging from 100MHz to 900MHz

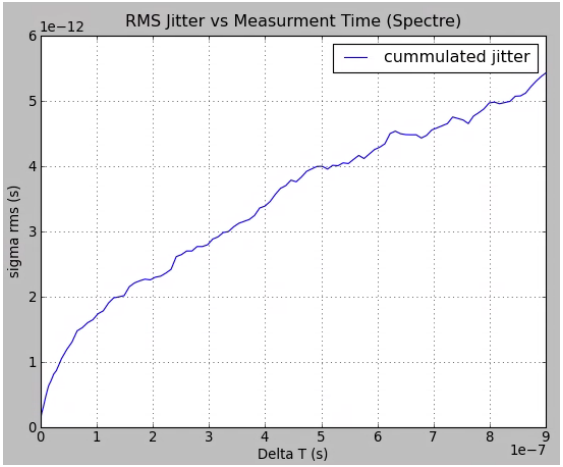
- Next steps:
  - Calibrate as precisely as possible the frequencies of the oscillators. This will allow to :
    - Study the cross talk between the 32 channels of CRONOTIC
    - Measure the resolution (Sigma) of CRONOTIC

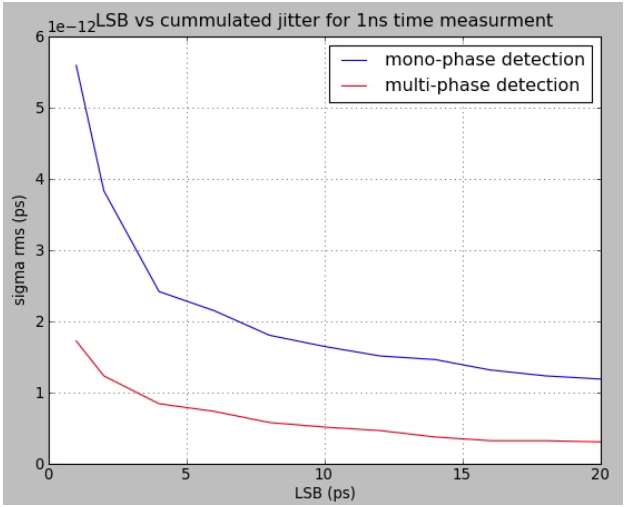
CRONOTIC2 R&D : Multi-phase detector TDC



- TDC LSB= T_{slow} - T_{fast} (same as signe phase detector TDC)
- Full custom Inverter cells are designed (Sharp edge, 22fs noise jitter simulation)
- Advantage of the multi-phase technique : reducing dead time, cumulted jitter

CRONOTIC 2: Simulation results

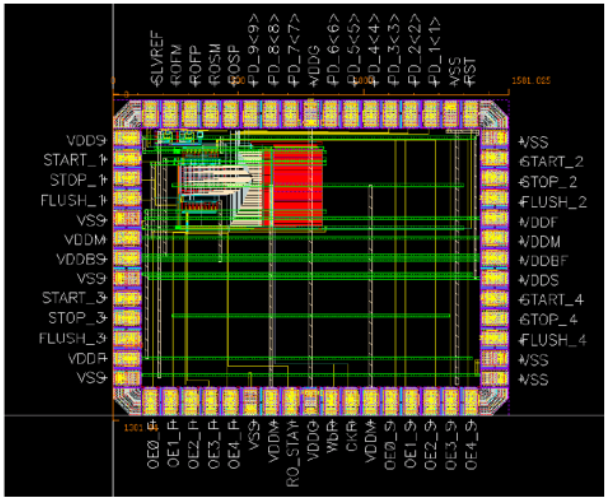




- Cumulated jitter σ_j (due to noise or any other source) is the most undesired side effect of the Ring oscillator
- $\sigma_j = K\sqrt{\Delta t}$:
  - K=cst proportional to the inverter noise jitter (22fs)
  - ΔT is the measurment time

- Dead time $\Delta t = \frac{DR}{LSB}$
- For an LSB=20ps and Dynamic range DR= 1ns :
  - $\sigma_{j_{simple}} = 3 \times \sigma_{j_{multi}}$

CRONOTIC2 : Layout of the submitted circuit



TDC **prototype** in Tsmc 130nm technology

- Frequency range[1GHz 1.5GHz] std= 75MHz thank to 5bit selection
- LSB range [1p to 214ps] std=20fs (simulation results)

- Demonstrate an architecture suitable for high-resolution TDC
- Observe the Ring oscillator behavior to imperfections and noise
- Highlighted the advantage :
  - Deat time, Cummulated jitter
- Disadvantage:
  - Digital processing, Power Consumption($I_{avg} = 34mA$ for both ROs mainly dominate by the matrix buffers)

Plan

Conclusion

- MicRhAu pole support strongly the TDC *R&D* activity in tsm130nm technology
  - Cronotic A Vernier RO TDC using single phase detector is under test:
    - Simplicity of digital processing unit, less power consumption, less area
    - cumulated jitter and dead time
  - Cronotic 2 A multi phase detector version of the TDC was designed and on fabrication:
    - less cumulated jitter and less dead time
    - complexity of the digital precessing unit, more power consumption , bigger area(power and area can be reduce with the matrix size)
  - Improved version of Cronotic will be submited affter the final testing (Cronotic, Cronotic2)
  - Combine Petiroc frond-end (OMEGA) and Cronotic in one ASIC for the CMS-RPC time measurement
  - Observe in real situation the advantage and drawback of a multi-phase technique and include improvement for a full and complete chip

Plan

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Thank You!