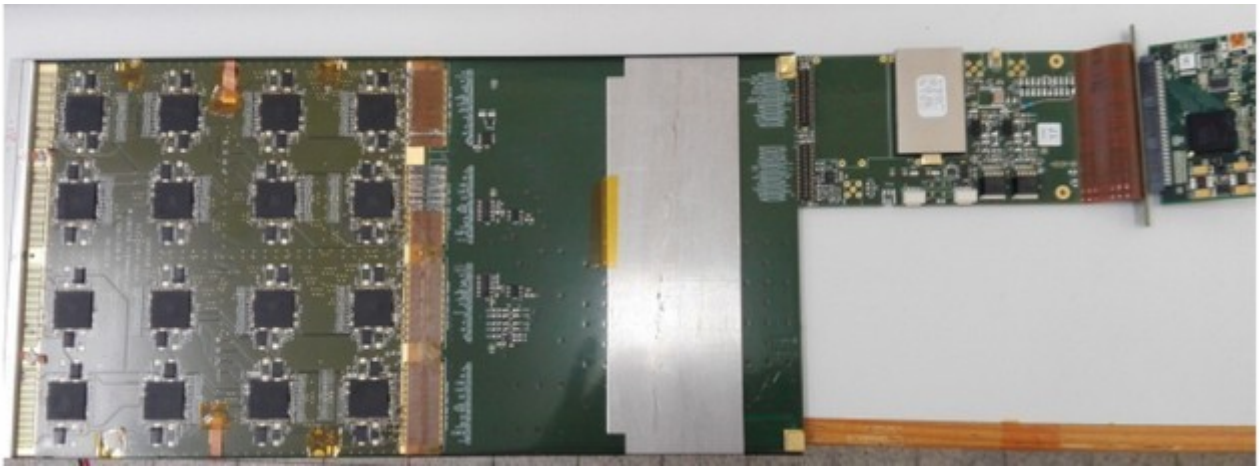
Operation of single slabs (TB2017)

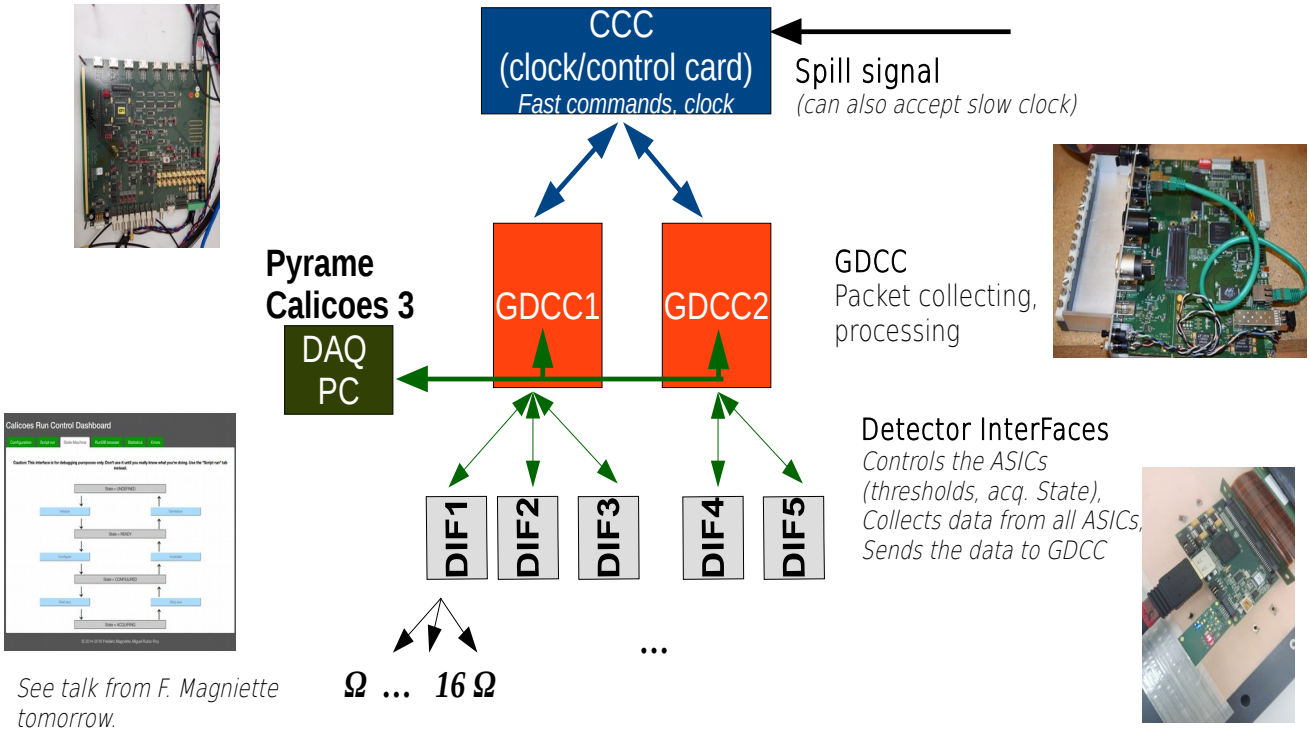
1 ASU (active sensor unit)

The entity of sensors, thin PCB (printed circuit boards) and ASICs (application-specific integrated circuits) is called Active Signal Units or ASU. An individual ASU has a lateral dimension of 18x18 cm 2 and has glued onto it 4 silicon wafers (currently with a thickness of 320 µm). The ASUs are equipped further with 16 ASIC for the read out and features 1024 square pads (64 per ASIC) of 5x5 mm. The readout layers of the SiW-ECAL consist of a chain of ASUs and an interface card to a data acquisition system (DAQ) at the beginning of the layer. This interface card, called SMB-VX (x=3,4 or 4b), also carries services as power connectors, test output pins, connectors for signal injection, etc. Currently, the technological prototype layers are built with the version of PCB called **FEV11** with 16 SKIROC (see DAQ section) in BGA packages mounted on top of it.



2 DAQ

A schematic view of the architecture of the DAQ can be seen in the following picture :



SKIROC (Silicon pin Kalorimeter Integrated ReadOut Chip) is the very front end ASIC designed for the readout of the Silicon PIN didoes. It consists of 64 channels that each comprises a low noise charge preamplifier of variable gain followed by two lines: a fast line for the trigger decission and a slow line for dual gain charge measurement. Finally, a Wilkinson type analogue to digital converter fabricates the digitised charge deposition that can be readout. Once one channel is triggered, the ASIC reads out all 64 channels adding a bit of information to tag them as triggered or not triggered. The information is stored in 15 cell deep phisycal switched capacitor array (SCA). This autotrigger capability is mandatory for ILC case since the accelerator will not provide a central global trigger. A key feature of the SKIROC ASICs is that they can be power pulsed to meet ILC power consumption requirements.

Every ASU of the SiW-ECAL prototype is equipped with 16 SKIROCs version 2. A new version, 2a, has been produced and will be used to equip new layers currently in production. The design of the subsequent chain of the data acquisition (DAQ) system is inspired by the ILC. Current DAQ consists of three modules which are designed to be generic enough to cope with other applications. The first module is the so called detector interface (DIF) which is placed at the beginning of each layer holding up to 15 ASUs. All DIFs are connected by single HDMI cables to the concentrator cards: Gigabit Concentrator Card (GDCC). The HDMI connection is used to transmit both slow control and data readout. One GDCC controls up to 7 DIFs collecting all data from them and distributing to them the system clock and fast commands. The most downstream module is the

clock and control card (CCC). The CCC provides a clock, control fan-out of up to 8 GDCCs and accepts and distributes external signals (i.e. spill signals).

The whole system is controled by the Calicoes and the Pyrame DAQ software version 3. The Pyrame framework provides basic blocks (called modules) of control- command or data acquisition. Calicoes is specific the im-plementation of these blocks for control-command and data acquisition of the SiW-ECAL prototype.

See references in folder DAQ for more information.
Please, visit also the CALICOES web page :
http://llr.in2p3.fr/sites/pyrame/calicoes/documentation/

3 Networking (to do)

TO DO.

4 Check the slab response.

Check the soldering points/ cabling /short cuts etc

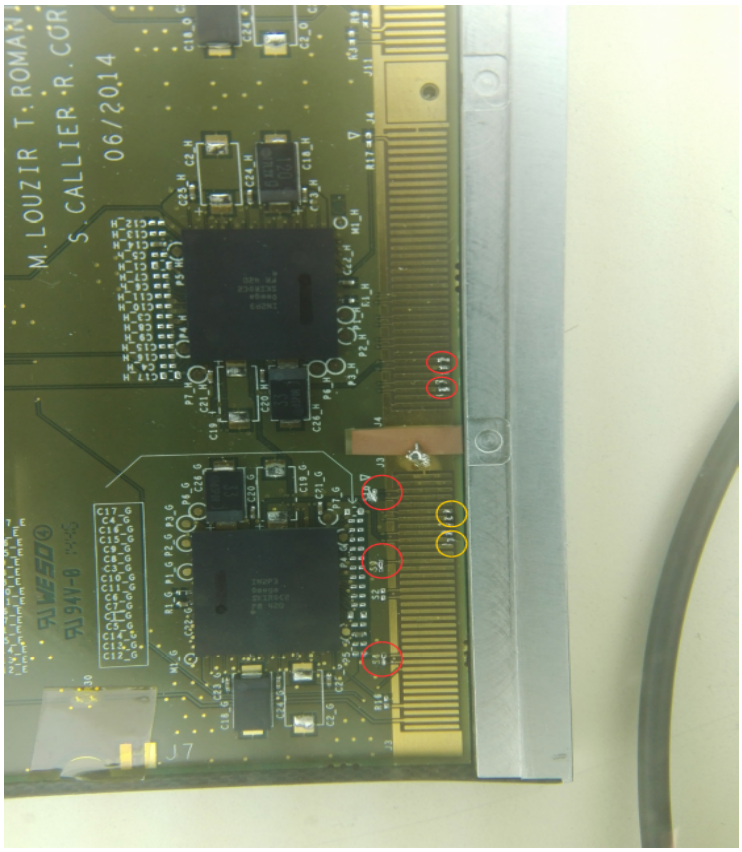
Turn around the slab and check soldering points in :

- DIF resistors (for slow control)

-HV (GND at SMB)

Turn slab around, open aluminim cover and do a check of soldering points in the base of the ASU :

- Pin pad number one (the lowest one in the picture)
  - S4, S9, S10
  - the pins 6 and 7 (from the top) and the 9-10 from the top.
    - ?? 100 % sure ??, (it is not clear in the picture if they are soldered or not)
- Pad numer 2 (the one in the top of the picture)
  - 3-4
  - 6-7
- The other two pads are symmetric.

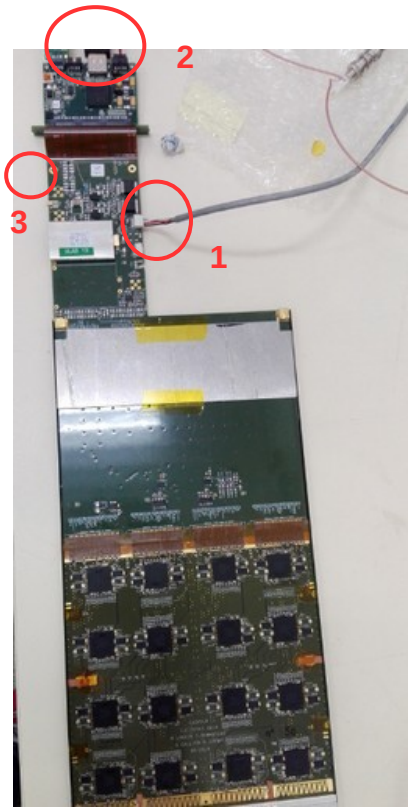


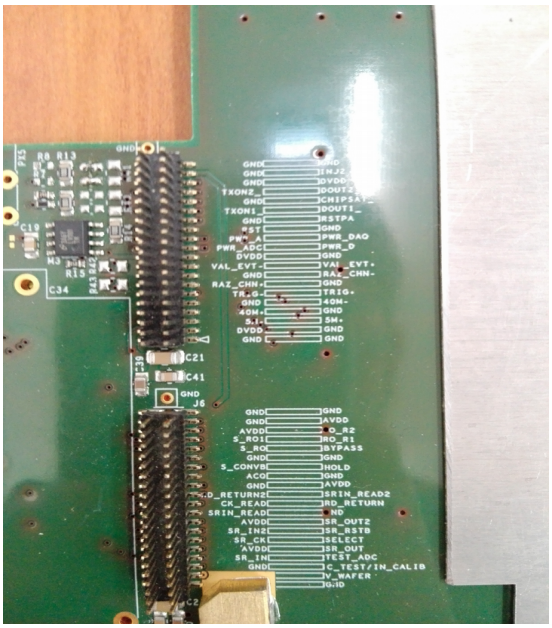
Electrical checks (NOT POWERED SLABS)		
		Comments
GND/PCB		check that it is gnd in every GND point
RESISTOR/DVDD		
SlowControl :		
S4-S16		check that are shorted between them in the last slab
SRIN-SROUT		check that are shorted between them in the last slab
Readout Return S9-S21		check that are shorted between them in the last slab
GND HV and bottom PCB		
No shortcuts between VDDA/VDD/GND		

Procedure for power up

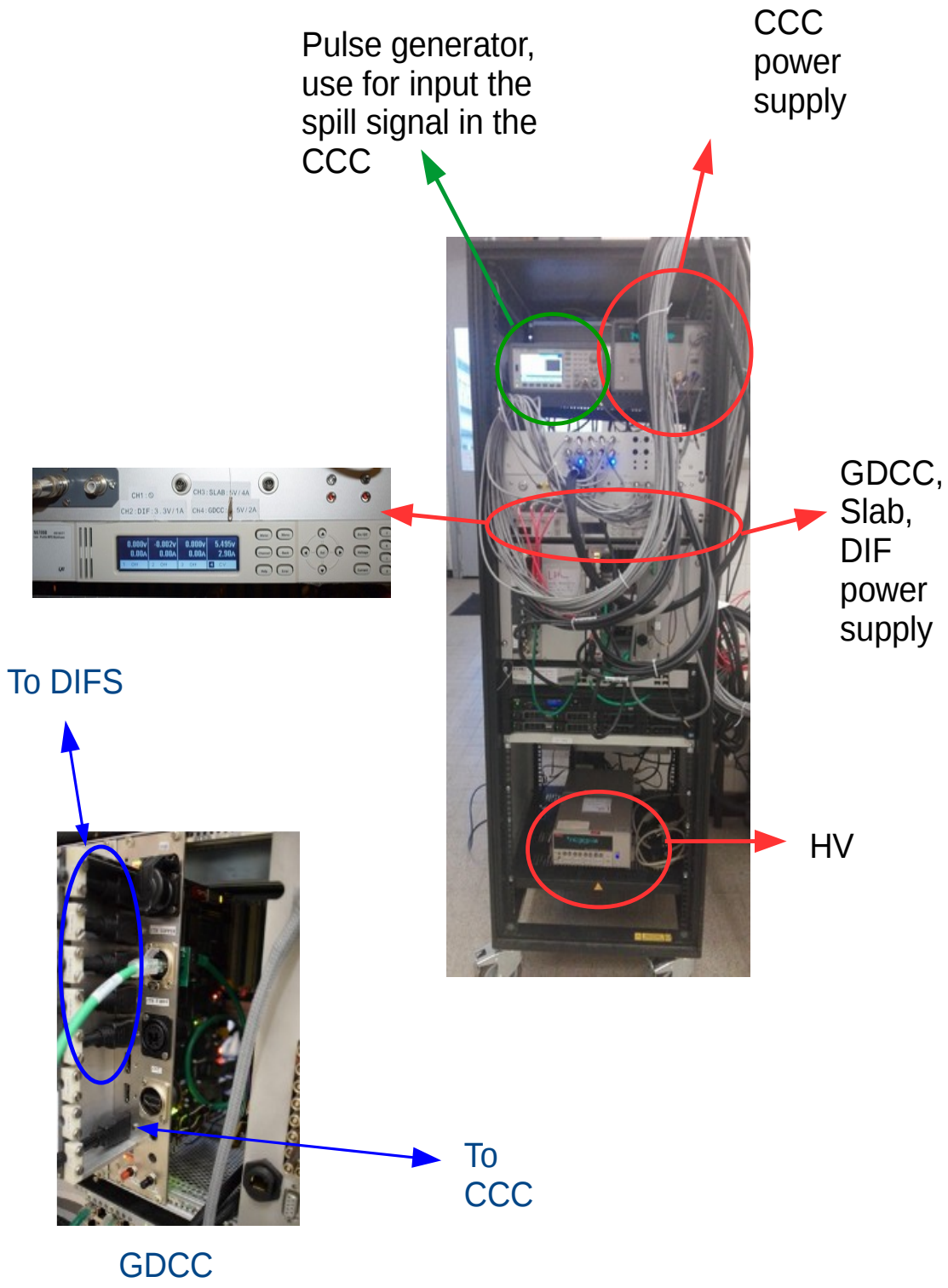
If a SMBV3 is used, the power of the DIF and the Slab is delivered through the slab itself using a single connectors and values of ~3.7V and 1-2 A of limit are used.

- Power the CCC (clock-control-card).
  - 3.3V, 5V and -5V with 1 A of limit.
- Power the GDCC (concentrator), the slab (AVDD, DVDD) and the DIF (in the same PS for the LLR rack used in beam test 2017)
  - channel 1 : LV DIF (2 in the picture) with 3.3V and ~ 2 A limit
  - channel 2 : slab power 4.5-5V, with 2 A limit (1 in the picture)
  - channel 3 : GDCC power 5V, with 2 A limit





See more about cabling + connectors information in the ASU folder.



Before powering the HV we should do some tests to check the power of the slab :

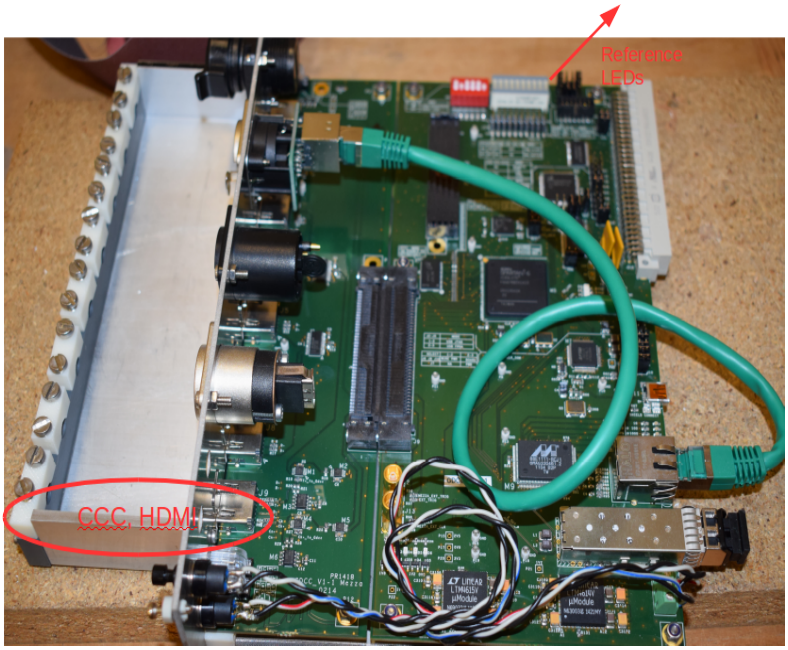
Electrical checks (Low Votlage on)		
		Comments
Green LED in SLAB		
BLUE LED light (DIF) blinking		
1.2V and 2.5V in J3 and J4 (DIF)		
VDDA		Should be 3.3. V
VDDD		Should be 3.3 V
Configure : RED LED blinks		Depends on the FEV&SMB version. If it blinks in some color it is already a good sign

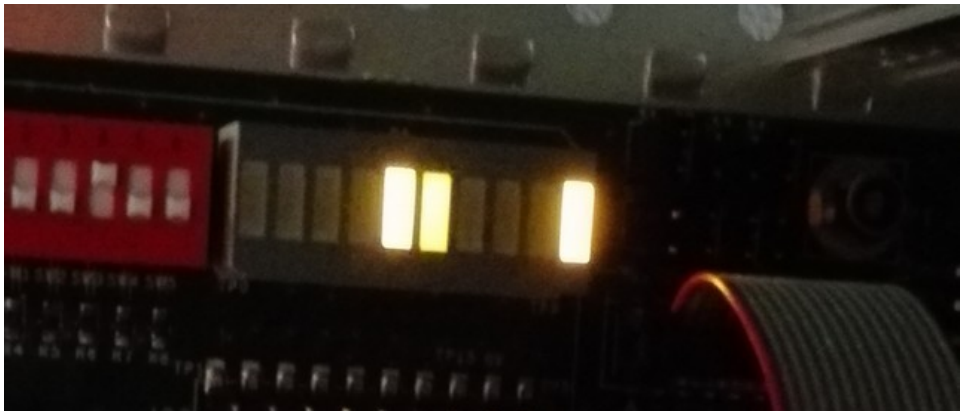
GDCC LEDs :

Last one is not blinking → connexion with CCC.

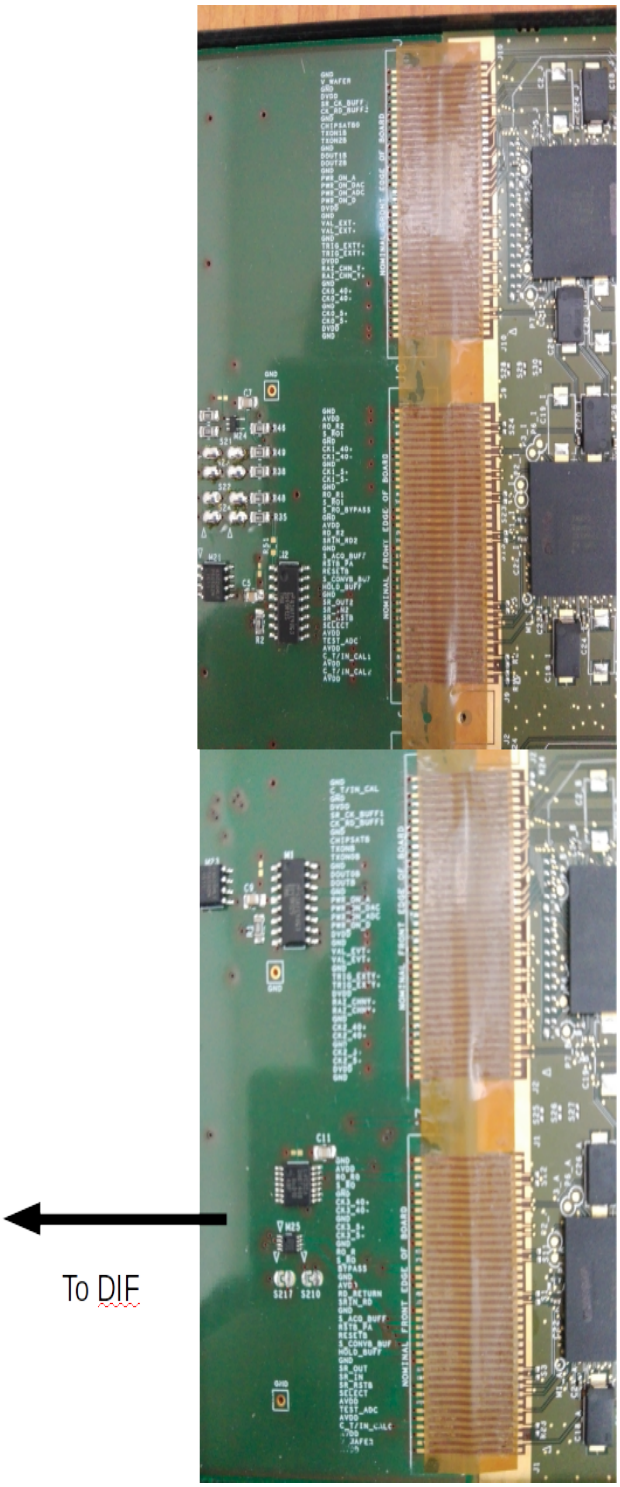
The 5th LED is blinking.

If the spill is connected, a new LED starts to blink at the spill frequency.





Some reference voltages: *see the following table and pins in the SMB 4 → they are equal at the end of the ASUs (FEV10,11,12)*



Pins	Ref values
VDDD	3.3 V
AVDD	3.3 V
SresetB	3.3 V
In calib	Ground (50 Ohm)
Wwafer	floating
Ctest	floating
testADC	floating

5 Start the data acquisition tests.

Assuming that the slab is well powered, we can start the tests with the DAQ software. Read the calicoes instructions in the top of this document before.

Go to the folder where the scripts are :

```
[root@llrcaldaq ~]# cd /opt/calicoes/standard/commissioning
```

Some key commands in terminal (can be also done in the gui explained in the Calicoes twiki) :

systemctl restart pyrame → restart the DAQ software

load_config_file.sh /opt/calicoes/standard/commissioning/slab_commissioning.xml → load the configuration file of the salb

initialize.sh → initialize the configuration files

configure.sh → send the configuration command to the slab.

invaldiate.sh → go from configured to initialized

deinitialize.sh → go from initialized to uninitialized.

start_acq.sh → start a simple data acquisition

stopacq.sh → stop the acquisition

The simplest test to be done is, in the terminal, being root user :

systemctl restart pyrame
load_config_file.sh /opt/calicoes/standard/commissioning/slab_commissioning.xml
initialize.sh
configure.sh
start_acq.sh

→ check that :

- the data is being taken (file frowing in /opt/calicoes/raw_data/)
- the orange and red LED lights in the DIF are blinking
- that inside the raw file, some spil and chip words are seen, (using the > *hexedit filename* command)

stopacq.sh

6 Typical errors and possible solutions:

1. No connexion with the GDCC → not link or similar error.
    1. Check the LEDs in the GDCC are ON (see next picture):
        1. If not → Reset or even power cycle the GDCC and wait to see them.
    2. Check the networking and the connexion of HDMI cables to the DIF and the proper assignment of them in the configuration file. Check also the MAC address of the GDCC and see if it is the correct one in the configuration file.
    3. Is the CCC on and the connected to the GDCC ? Is the spill generator connected to the CCC ?
2. Error of configuration during slow control loading→ bitstream is not arriving to the rocs and the DIF LED is red. This is most probably due to :
    1. Misconnexion between the SMB and the ASU
    2. Wrong power of the SLAB or the DIF.
    3. Check the voltages in the SMB and ASU foot and if are not correct, start Section 4 from the beginning.
    4. If the voltages are correct and the problem persists (we see that the DIF receives the slow control since it does a couple of orange blinks byut the slow control are not transferred) then we need to check the proper transmission of all signals (SR_IN, SR_OUT specially). Most probably is that some return lines are not properly closed.

7 HV ramp up.

- **HV should not be applied if the LV of the slab is not applied !**
  - Switch the power supply on and remove the zerochnk option
  - Set the limits of currents to 20-25uA and the limits of V to 100 V.
- **The currents should not be larger than few uA.** The usual values are 1-2uA for 4 wafers of Si-wafer of 325um
  - Select a value of 4 V and clic enter twice. Repeat until 10 V, checking always teh currents.
  - Clic « operation ». The Power supply is supplying current if the blue led of « operation » is on.
  - If with 10 V is okay (low currents), then you can go to 100V in steps of 10. But in principle, with a voltage of 10 V we can already do most of the basic test measurements. (100 V = optimal value for a Si-wafer of 325um)

The stabilization of the HV currents will take ~ 30-60 minutes. In the meanwhile, some short tests of the DAQ can be done (or even before ramping up the HV). See next section.

8 Noise commissioning

Test the single slab :

```
[root@llrcaldaq ~]# source test.sh SlabName type_of_run
```

where type_of_run is noise (only noise+scurves) or all (includes cosmic data taking).

If this is done, all the data is saved in : /home/data/testbenchLAL/Commissioning → **this is hardcoded in the configuration file and in the test_noise_signal.py script !!**

9 Useful links

Work in progress !!

TB2017 : https://twiki.cern.ch/twiki/bin/view/CALICE/SiWDESY201706

Commissioning : https://twiki.cern.ch/twiki/bin/view/CALICE/SiWDESY201706Commissioning