Electronics overview for AGATA

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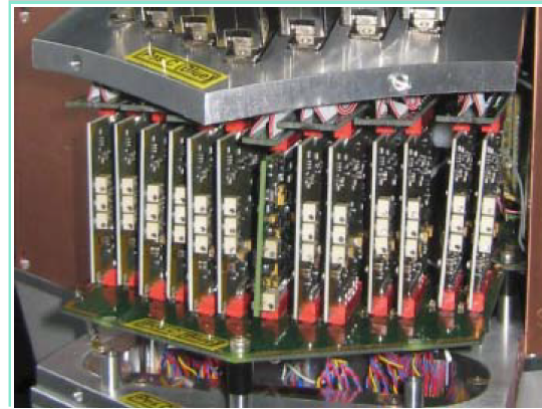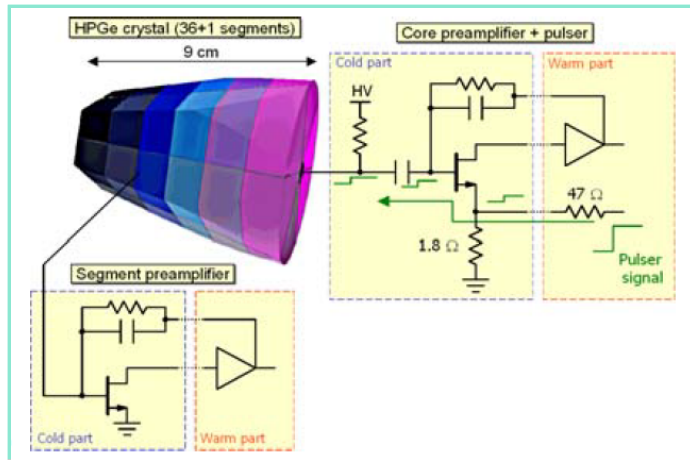ETSE - University of Valencia

IFIC (Valencia)

Outline

- AGATA Electronics Evolution
- Found issues
- Guidelines for R&D initiative
- On going Technical Proposal

AGATA Electronics Evolution

AGATA Preamplifiers

Core Preamplifier

Image taken from J. Gerl. *Nuclear Spectroscopy with AGATA*. NUSTAR Week, VECC Kolkata (India)

Cold and Warm Parts
  Cold Part (150 K)
    FET based charge amplifier
    Gain: 53 mV/MeV
  Warm Part
    Folded Cascode (10 V positive output range)

Energy Range
  180 MeV with TOT
  0.2 % Energy resolution

CORE and SEGMENT gains
  Single Core: 100mV/MeV
  Dual Core: 50 mV/MeV and 200 mV/MeV
  Segment Gain: 100 mV/MeV

Differential output
Time Over Threshold operation
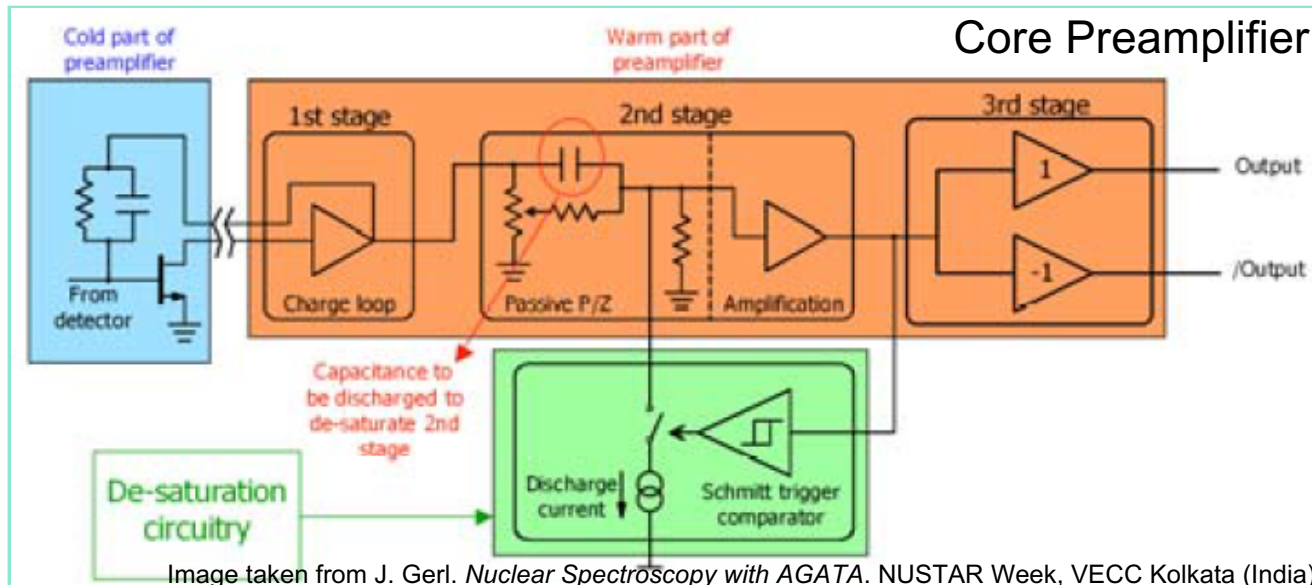**Fast Reset Circuitry**
Built-in Pulser for calibration

INFN-Mi, GANIL, Köln.

G.Pascovici et al., Low noise, dual gain preamplifier with built in spectroscopic pulser for highly segmented high-purity germanium detectors, WSEAS Transactions on Circuit and Systems 7 (2008) 470.

Outline – **AGATA Electronics Evolution** – Known issues - Guidelines for the R&D – R&D description

AGATA Electronics Evolution

AGATA Electronics Phase 0/Early1
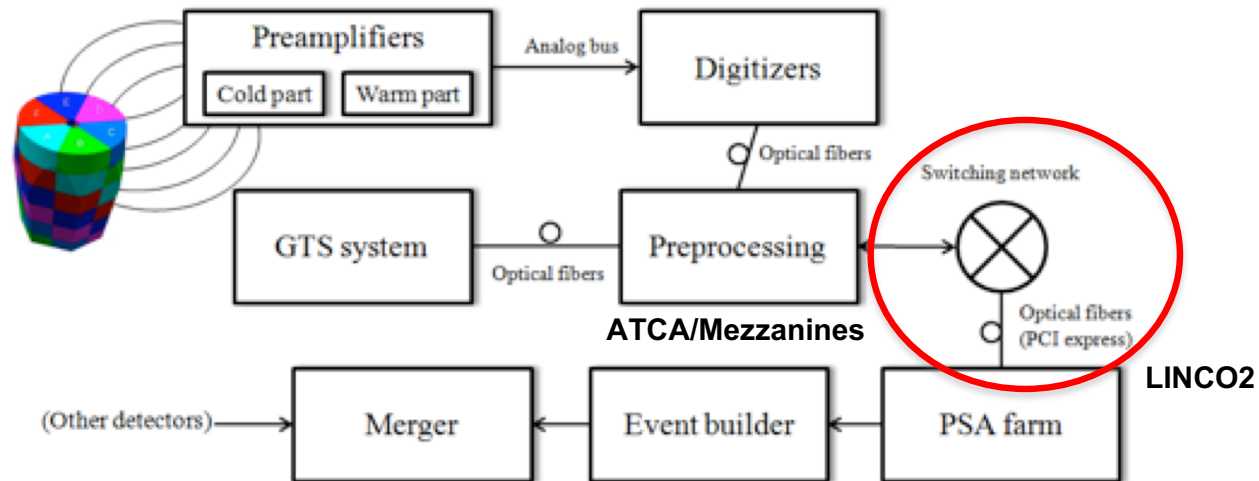
23 to 25 channels available
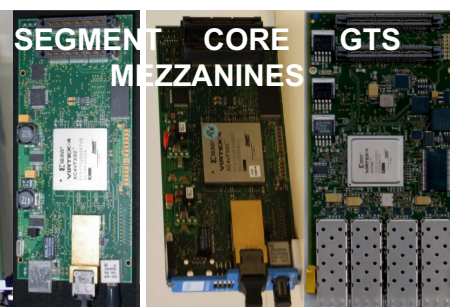
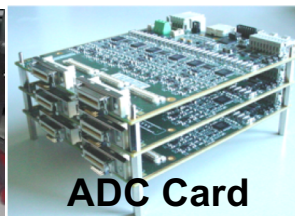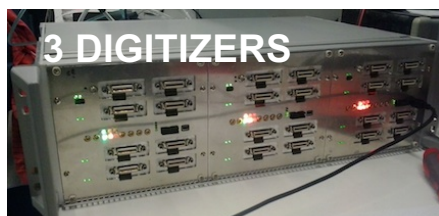IPHC Strasbourg Uni.Liverpool STFC Daresbury IPNO, CSNSM-Orsay INFN-Padova

AGATA Electronics Evolution

AGATA Electronics Advanced Phase 1

Up to 13 channels available

3 DIGITIZERS

ADC Card   Control Card   GGP Card
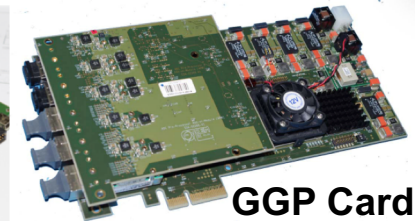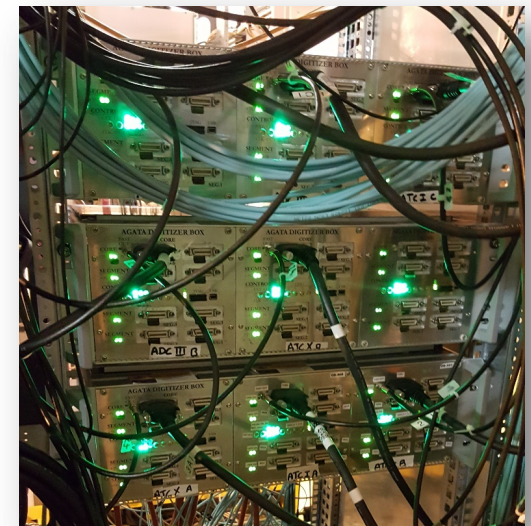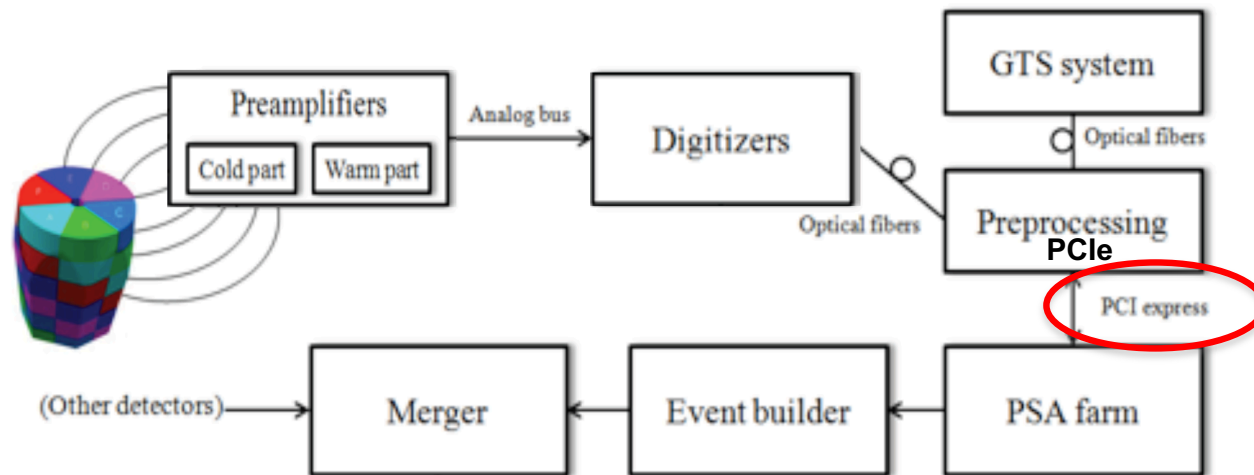
INFN-Milano INFN-Padova INFN-LNL IFIC-Valencia ETSE-Uni-Valencia

AGATA Electronics Evolution

Up to 38 channels available for AGATA
Up to 45 detectors by end of GANIL campaign

New production batch of Adv. Phase 1 electronics
10 channels + spares

We need to go to 60 channels

More Adv. Phase 1 channels?
New electronics?

Known issues

Several issues faced in AGATA Electronics evolution

At least:

- Component procurement due to obsolescence (transceivers, IC, …)
- Compatibility issues, i.e. GGP and workstations
- Difficulties in maintenance and repairing
- Costs
- …

We also need to think in view of AGATA Phase 2 (beyond 2020)

More Adv. Phase 1 channels? 😟
New electronics? 😄 ➡ Electronics R&D

Guidelines for the R&D

Recommendation of experts evaluation for Advanced Phase 1 (2012)

- **New R&D Phase to improve integration** and reduce data transmission using large number of optical links.
- **Model of FEE production with an R&D phase at least on every construction phase of AGATA**. This model also reduces considerably the maintenance costs since the expensive early electronics might be replace with time by cheaper newer one.
- **Compatibility with the existing electronics and with the GTS is considered a basic requirement.**

Guidelines for the R&D

FEE Group discussions identified the following lines of R&D

1. Possibility of **higher integration and power consumption reduction** in the AGATA **core and segment pre-amplifier**. Exploring the **ASIC technology** for the AGATA pre-amplifiers.
2. Possible **integration of the preamplifier and the ADC** in the spirit of the **Digital Pre-amplifier module**.
3. **Improvement in the Digitizer ENOB**
   - Using **16 Bit FADC's (or beyond)**
   - Using more **complex pre-processing algorithms** on the evaluation of the baseline.
4. Possibility of **higher integration in the Digitizer control Card** for remote settings of the Digitizing cards.
5. Pre-Processing improvements: considering the **possibility to integrate the pre-processing of a full cluster in a single card.**
6. Study of the **possibility to locate Digitizer an pre-processing electronics together in the neighbourhood of the AGATA Clusters**, using short links and avoiding long optical fibers.
7. **Improvements in the GTS protocol** increasing the **number of leaves** in the tree and possibly defining **"qualifier bytes"** for complex triggers.

Guidelines for the R&D

Lines of R&D cont'd

8. Development of the **Hardware and Software trigger processor** able to cope with the necessities of AGATA and all complementary instrumentation beyond Phase 1.
9. Exploring the **possibility of using Ethernet capacity**
   - To transfer data from experimental hall to the computer room **avoiding dedicated interfaces**.
   - **To remove customized cards** inside computer farm.
10. **Explore if some high level processing algorithm can be moved** from the FPGA to computer farm.

After **January 2016** Town Meeting on R&D for AGATA Electronics, the **AMB and ASC encouraged the development of a medium term solution for processing an ATC and with Ethernet readout**, while **long term developments with ASIC (Digital Pre-amplifiers)** shows technical difficulties that **need further development**.

On going Technical Proposal(*)

CSNSM (Orsay), ETSE – U. Valencia, IFIC (Valencia), IPHC (Strabourg), RAL (Daresbury), U. Milan, ...

Proposal objective: to build a scalable and stable Back End Electronics and DAQ (Electronic Data Acquisition) system for AGATA beyond phase 1 and track the best technical solutions for the full 4π array

Important aspects to consider

- Interface between front end electronics and servers should **not rely on any specific hardware interface**.
- Simplified and autonomous electronic modules to **ease maintenance** and **minimize impact of possible rework due to obsolete components** in future.
- **Highly integrated solution** to ease the installation in experimental area.
- **Readout** based on **high bandwidth network technology** (up to 10 Gb/s per crystal).
- **Stable and scalable architecture** of the AGATA BEE&DAQ architecture (for which the necessary performances must be fulfilled from 45 up to 180 crystals)
- **Modularity** to allow **for the use of new technologies** when available and suitable for the objectives of cost reduction and higher integration.

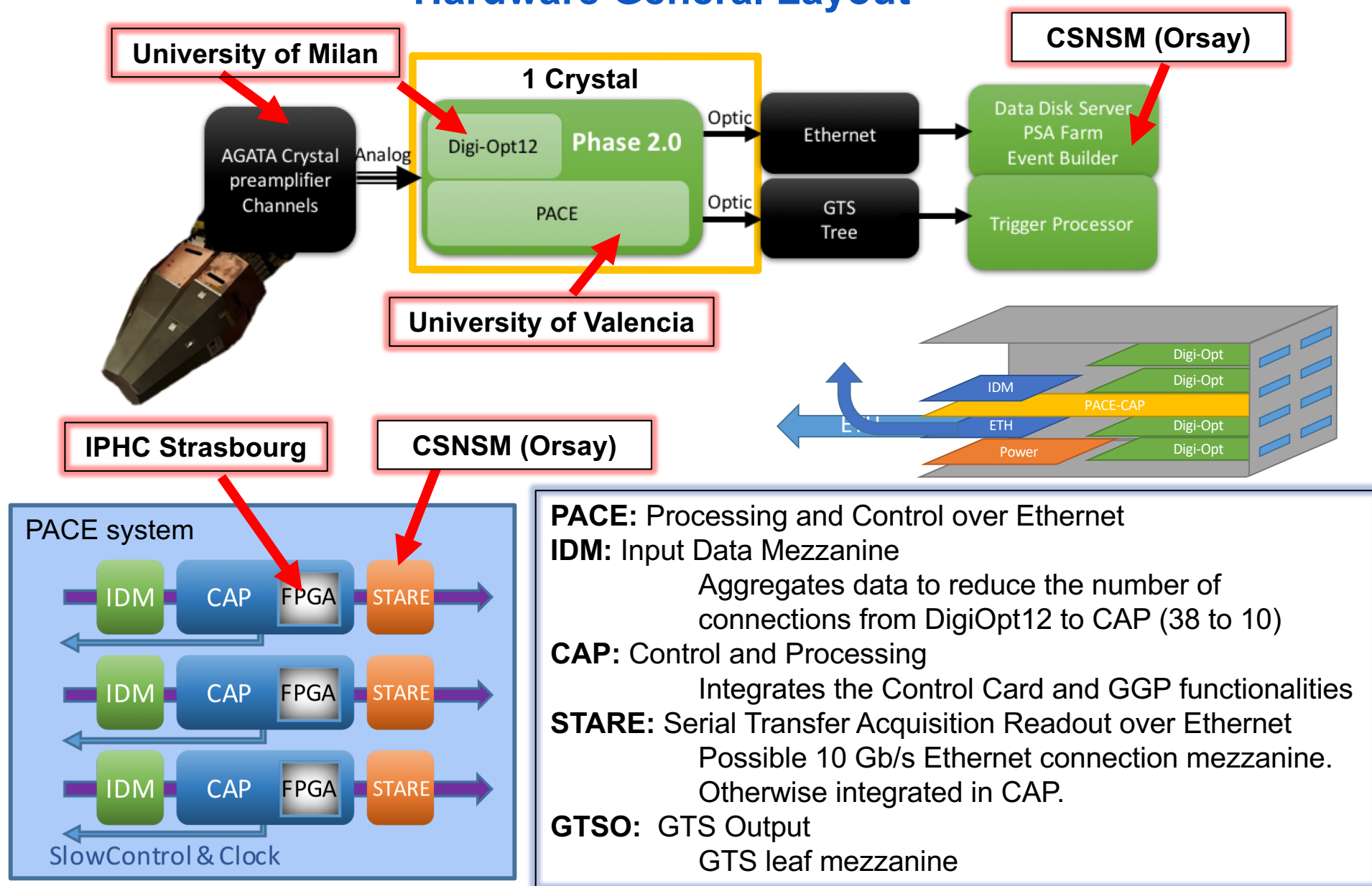(*) Information from the working document for the R&D on electronics for AGATA Phase 2.

Important aspects to consider (cont'd)

- **Maintenance** of the system **by external companies highly recommended** to insure it through the life of the experiment independently of man power fluctuations in the collaboration.
- **Possibility to have a portable version** to install them in Scanning area, Acceptance Test labs, Host labs for detector maintenance labs so that results can be compared using the same instrumentation between experimental area and labs.
- **Built-in self tests and built-in embedded software** so that the system can work **without network access to servers and complicated infrastructure**.
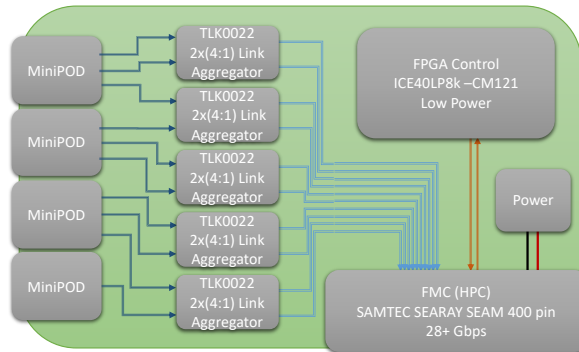
On going Technical Proposal
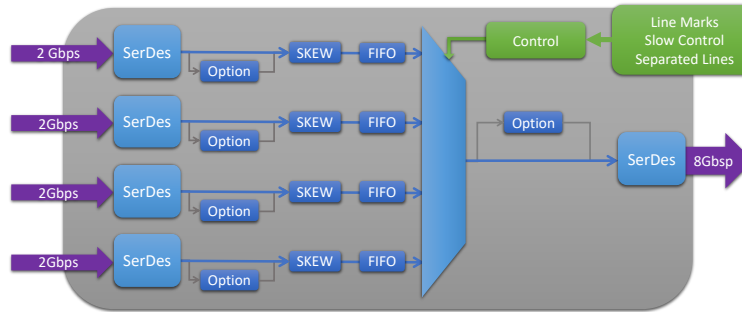
Hardware General Layout

PACE: Processing and Control over Ethernet
IDM: Input Data Mezzanine
  Aggregates data to reduce the number of connections from DigiOpt12 to CAP (38 to 10)
CAP: Control and Processing
  Integrates the Control Card and GGP functionalities
STARE: Serial Transfer Acquisition Readout over Ethernet
  Possible 10 Gb/s Ethernet connection mezzanine. Otherwise integrated in CAP.
GTSO: GTS Output
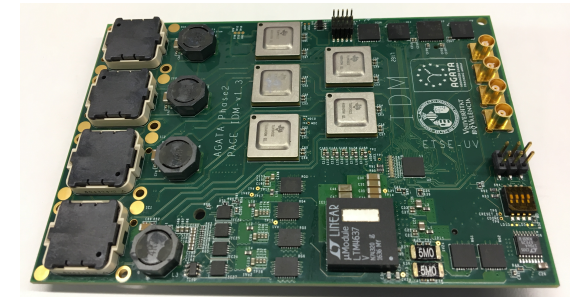 GTS leaf mezzanine

Input Data Mezzanine
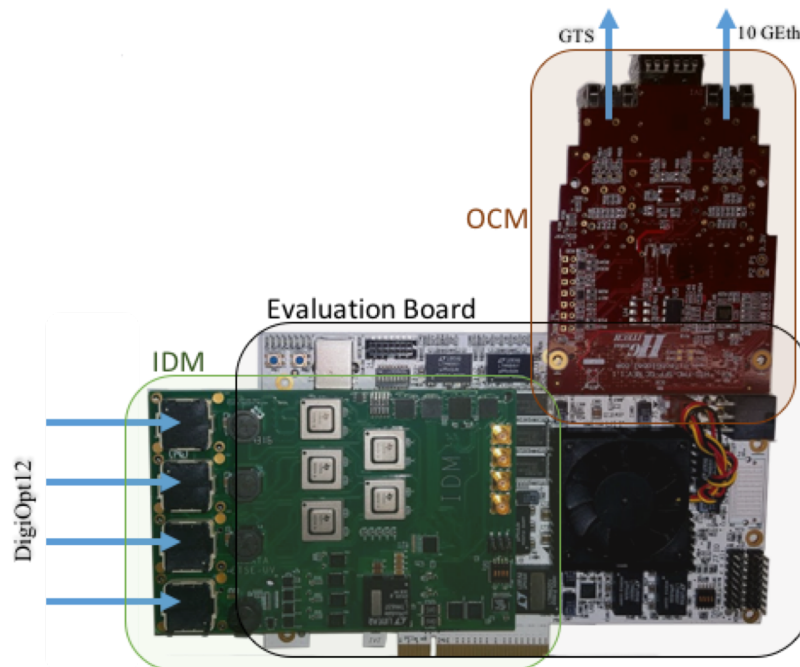

Block Diagram

Functional Block Diagram

IDM prototype

HiTech Gigabit FMC

HiTech Kintex Ultrascale KCU115

IDM Testbench

Firmware General Layout

Firmware should integrate the **functionalities** of
- current **Control Card and GGP**
- and **others** interesting for the physics, system maintenance, etc.
  - **pre-processing algorithms**
  - **oscilloscope mode**
  - …
- several ip's to develop

We need to fix the FPGA platform for the development

Software General Layout

May need development but still under discussion

Thank you for your attention