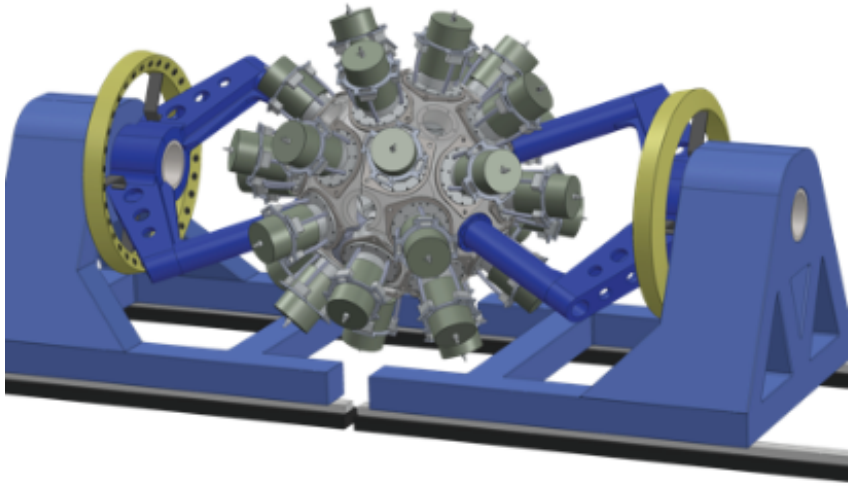
Second AGATA-GRETINA Tracking Array Collaboration Meeting

GRETA ELECTRONICS I

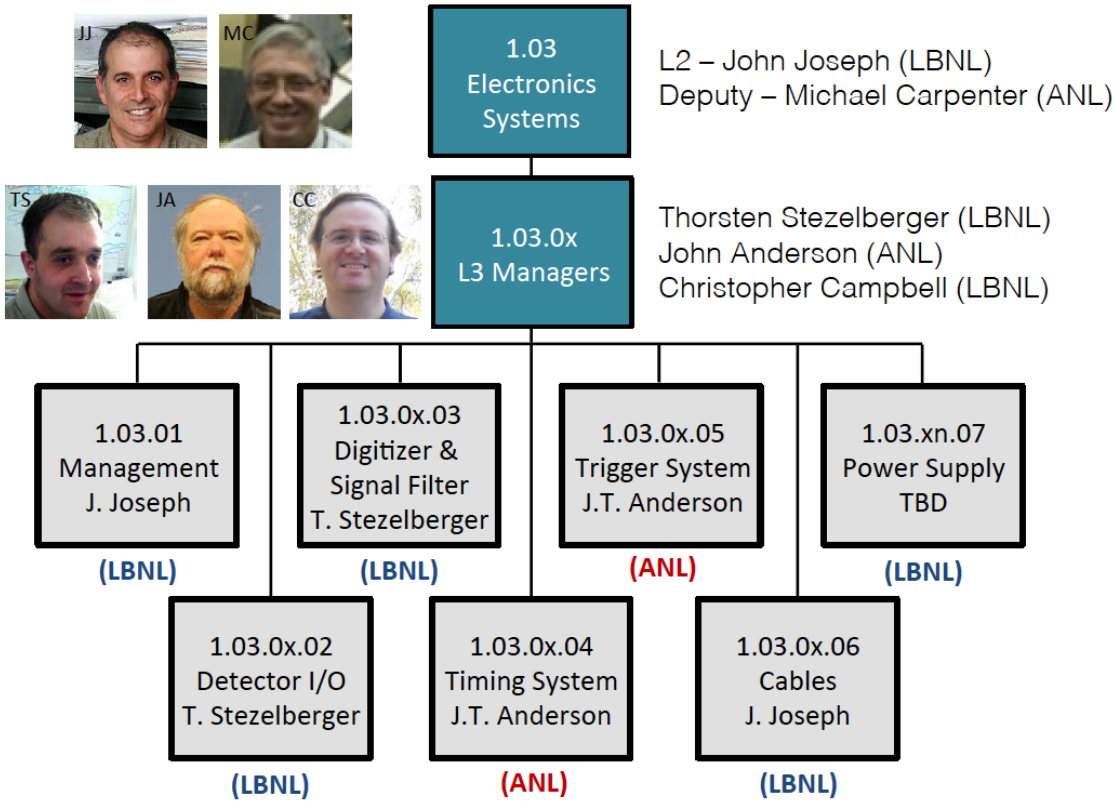


MICHAEL P CARPENTER
Physics Division
Argonne National Laboratory

April. 4-6, 2018
CSNSM – Orsay
Orsay, France

OUTLINE OF TALK

Overview of Electronics conceptual design for GRETA
- Digitizer
- Signal Filter Board
- Trigger and Timing System



ELECTRONICS REQUIREMENTS

Electronics System Requirements

- Deliver digital signal processing electronics to instrument 30 Quad Detector Modules, capable of digitizing detector preamplifier signals at 100 MHz sampling frequency, over a dynamic range up to 25 MeV, maintaining the intrinsic detector energy resolution of < 2.5 keV (FWHM) at 1.33 MeV.
- Ensure integral (differential) non-linearity ≤ ± 0.01% (1%) as measured in the final energy spectrum with a nominal gain of 0.3 keV/channel over 10 MeV.
- Ensure synchronous ADC sampling across the array.
- Provide a global time stamping mechanism to allow event reconstruction including external detector systems.
- Provide real-time energy and timing filters and waveform windowing.
- Provide a trigger system capable of producing a fast trigger output (< 500 ns) to auxiliary detectors, identifying physics events for readout and incorporating trigger inputs from external detector systems.

ELECTRONICS DESIGN CONSIDERATIONS

Existing GRETINA digital signal processing boards (ADC + FPGA filter) do not meet the full GRETA requirements for

- Increased data rate and throughput needs
- ADC linearity performance

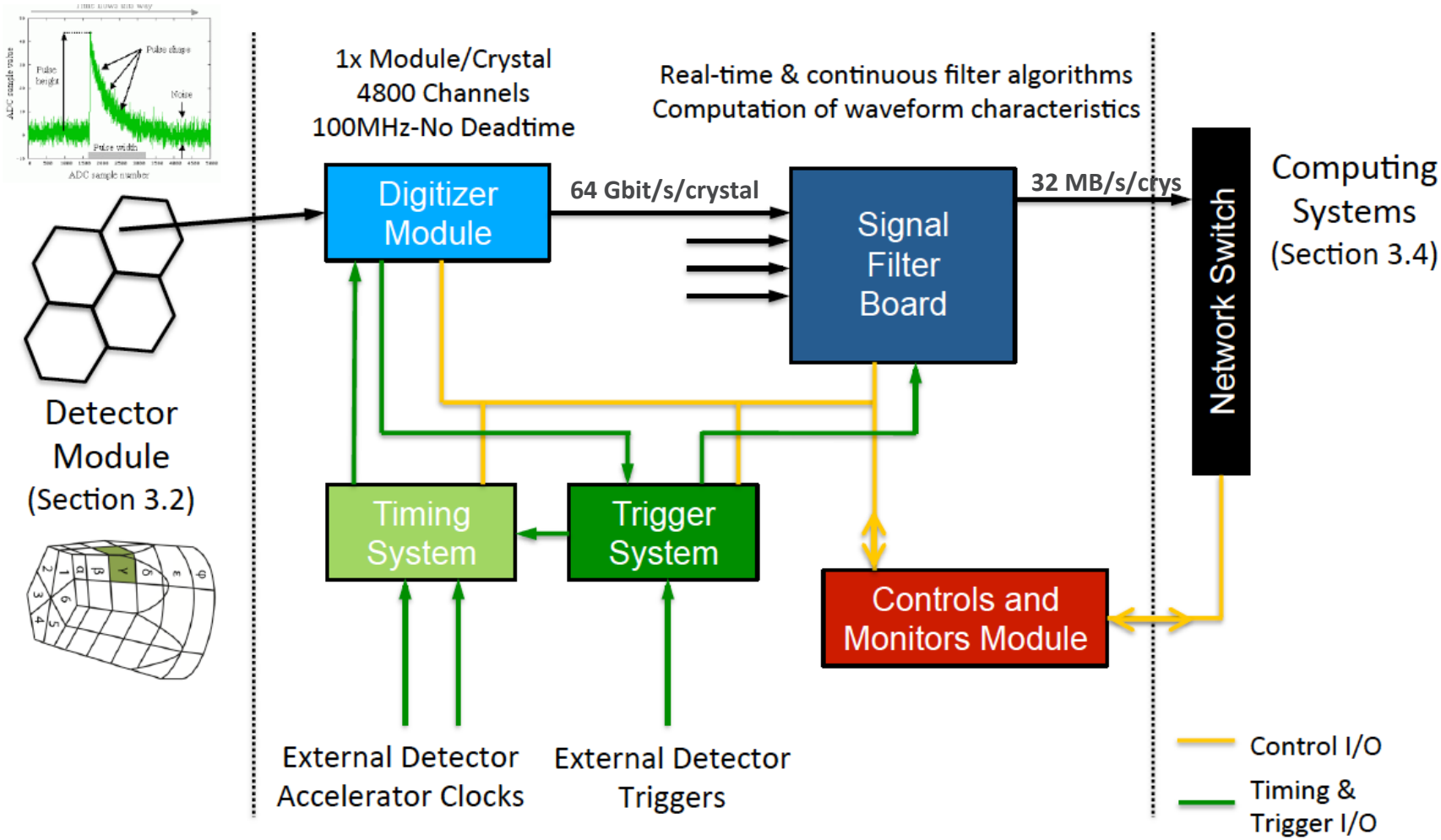
Trigger and timing systems based on the GRETINA approach is a proven and scalable option for GRETA.

Today's components provide significant gains in performance and motivate a new design.

GRETA approach - separate digitizer and signal filter functionality into two boards to allow us to

- Place digitizers close to detector module
- Enable upgrade of (commercial) signal filter boards

PROPOSED CONCEPTUAL DESIGN



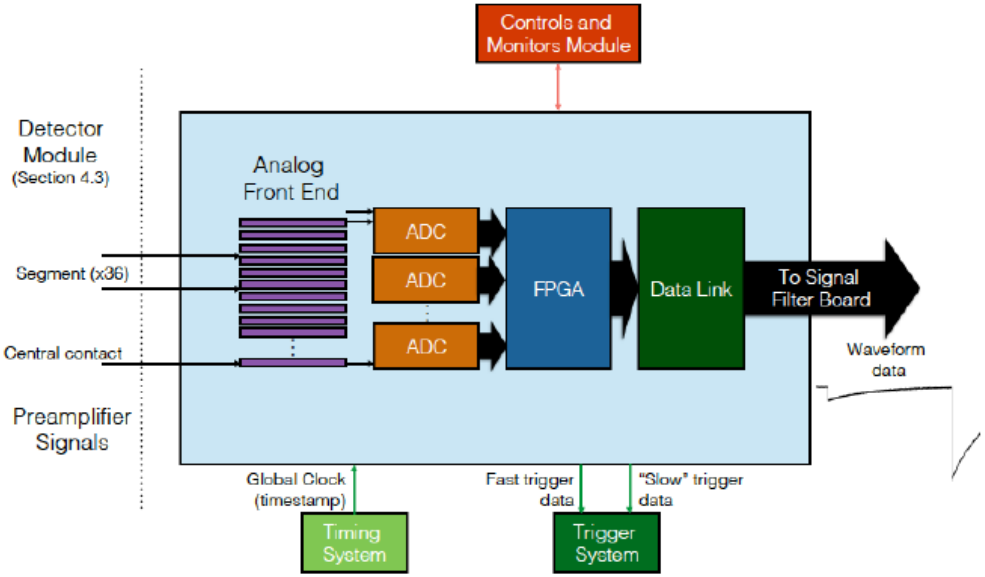
DELIVERABLES FOR ELECTRONIC SUBSYSTEM

- Digitizer Modules & Interface Box
  - Instrument all segments and central contacts for 120 crystals
- Signal Filter Boards
  - Data Processing for 120 crystals
- Trigger System
  - Trigger decision for GRETA & external detectors
- Timing System
  - Synchronous timing for all
- Key Interfaces
  - Detector Modules
  - Computing Systems

Utilize lessons learned on GRETINA in all new designs

DIGITIZER MODULE DESIGN

LBNL – T. STEZELBERGER



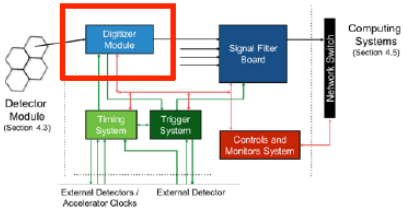
- Digitizer Module
  - Compact and low-power ADC components with good linearity performance
  - High-bandwidth fiber links for high data transfer rate to meet throughput requirements
  - Provide "fast" and "slow" trigger information to the array trigger system

Design will allow digitizer to be placed as close as possible to the detectors, minimizing transmission length of analog signals.

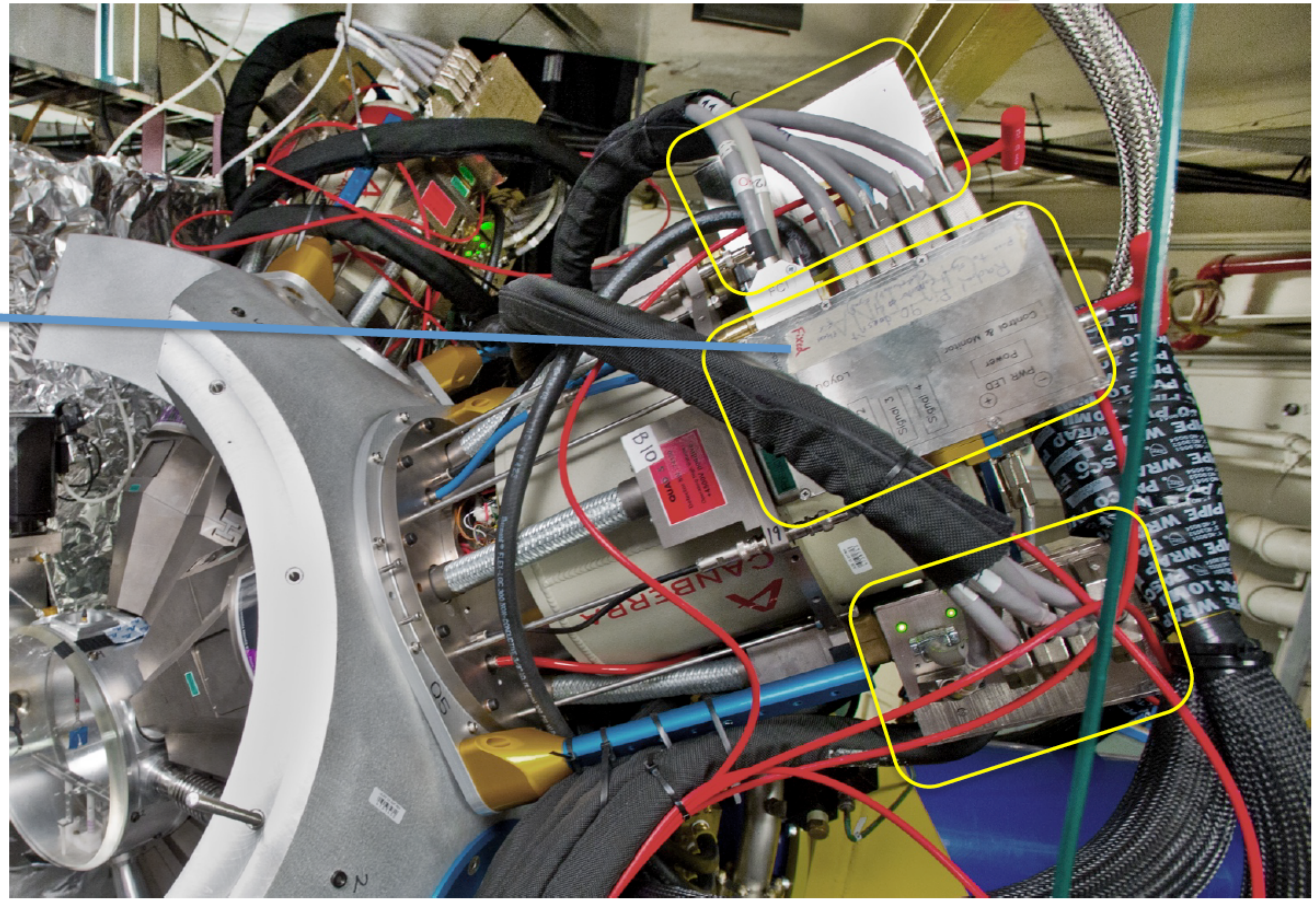
- Identified as the most challenging ES Subsystem
- Design starts early & ~30% of ES Design budget
- Schedule provides a full year + contingency for design of the Digitizer Module

LOCATION OF ADC BOARD

Digitizer Modules will be located at current "Radiall Box" location



"Radiall Box"



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ADC FOR GRETA

Requirements for Candidates

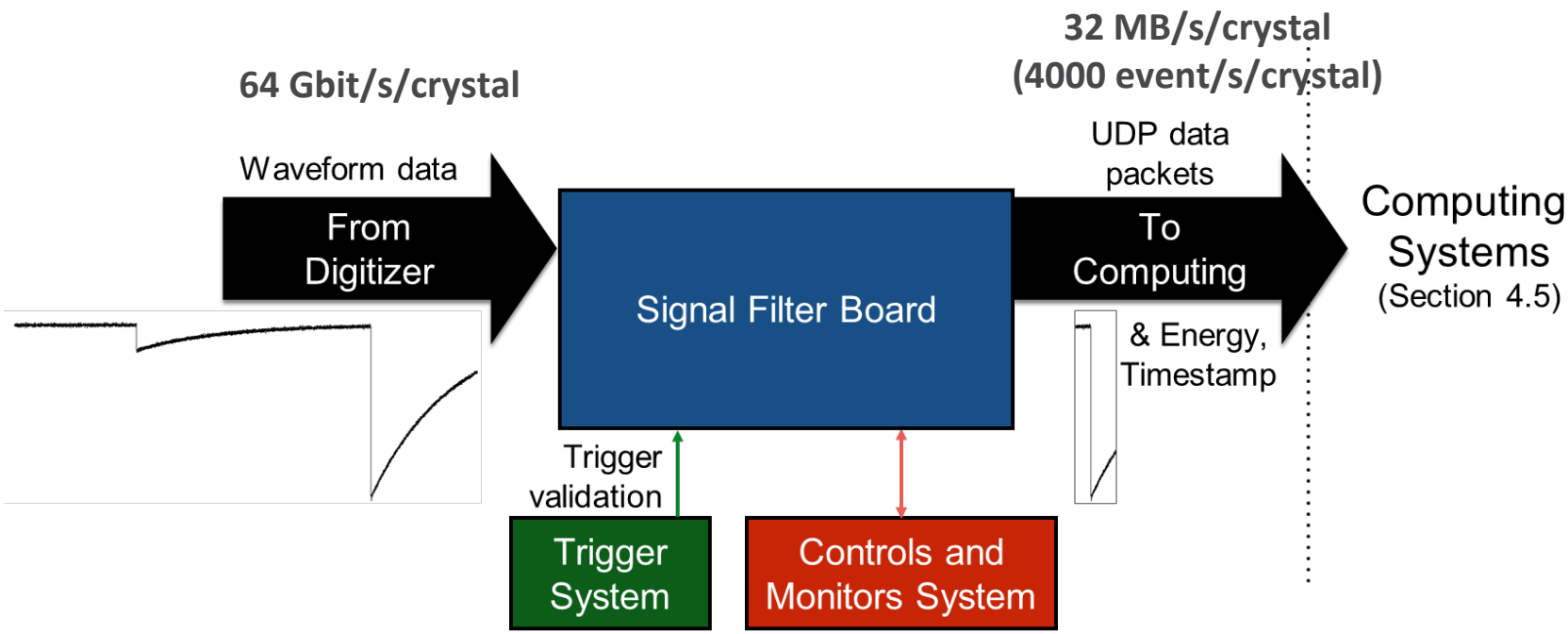
(Based on GRETINA experience)

- >= 14 bit (Up to 25MeV)
- >= 100MSamples/s
- Low power
- Package Size

- We identified 3 Candidates

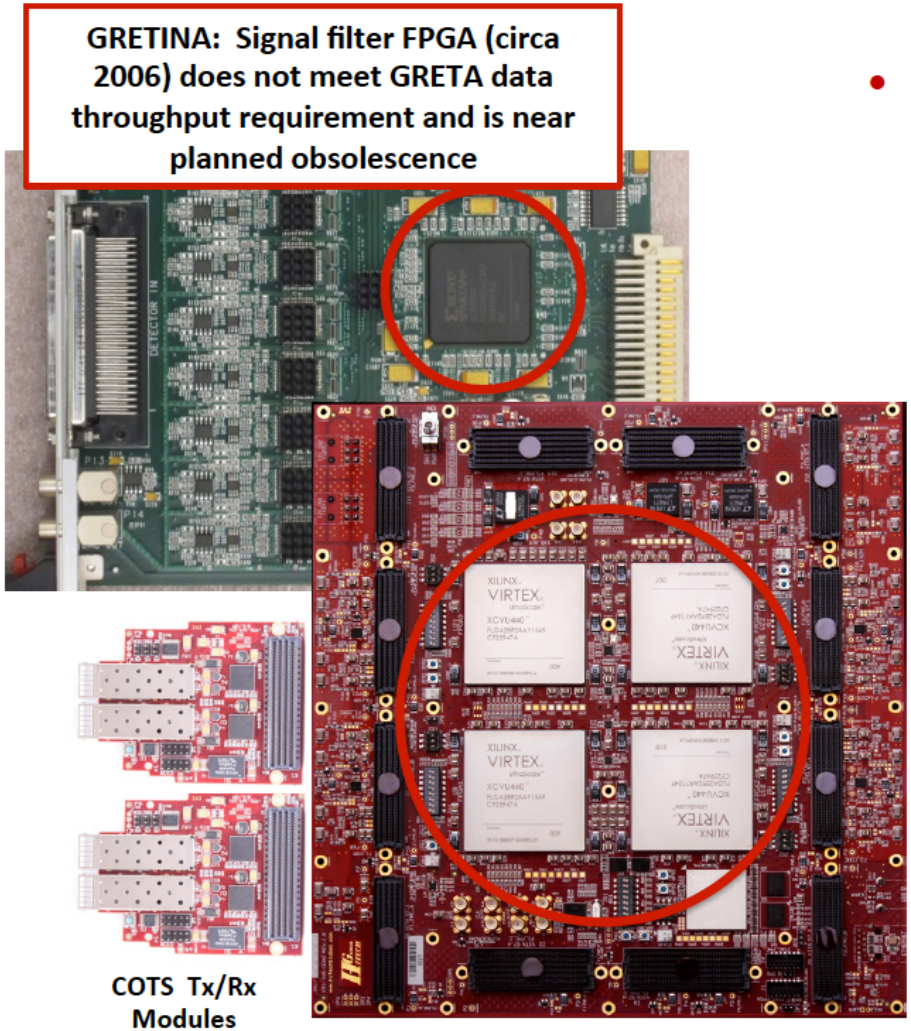
  (16 bit / 100MSamples/s)
  - AD9655
  - AD9653
  - LTC2194
- We compared the ADCs
  - One of the ADCs looks promising (LTC2194)

SIGNAL FILTER BOARD



- Filter Board receives the entire output from digitizer
- Compute filter for all ADC data streams
  - Event time
  - Event energy
- Package “Validated Events” and transmit to computer cluster
- Upgradable !!!

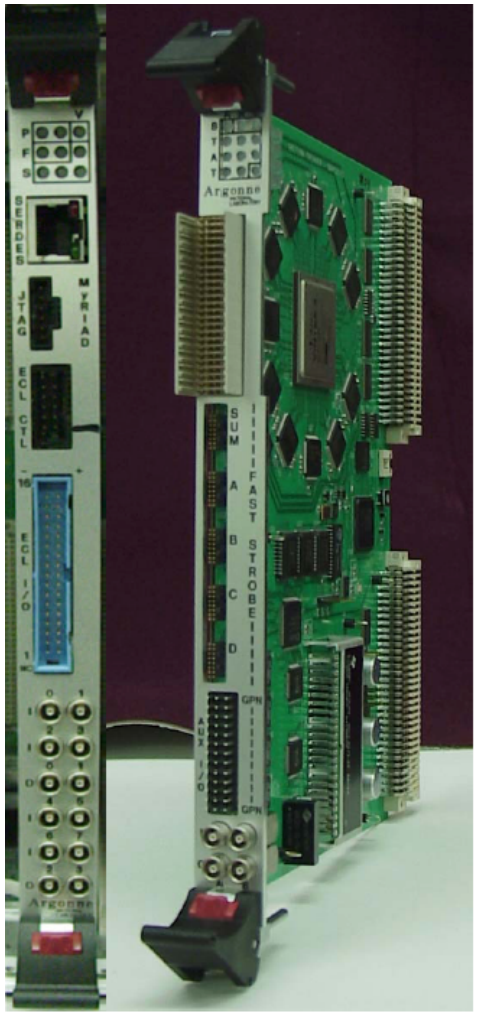
SIGNAL FILTER BOARD
LBNL – T. STEZELBERGER



Example of COTS with 4 FPGAs per Module
Possible to implement 1 Detector Module per Board

- Signal Filter Board
  - Commercial-off-the-Shelf (COTS) hardware
  - Scalable design
  - Meets the data throughput requirement
- Utilize existing GRETINA VHDL code base as launching platform
- ~20% of ES Design Budget
  - Use of COTS hardware
    - Reduces fabrication risk
    - Provides upgrade path
  - Allows Firmware development independent of Digitizer development

TRIGGER SYSTEM DESIGN
ANL – J. ANDERSON

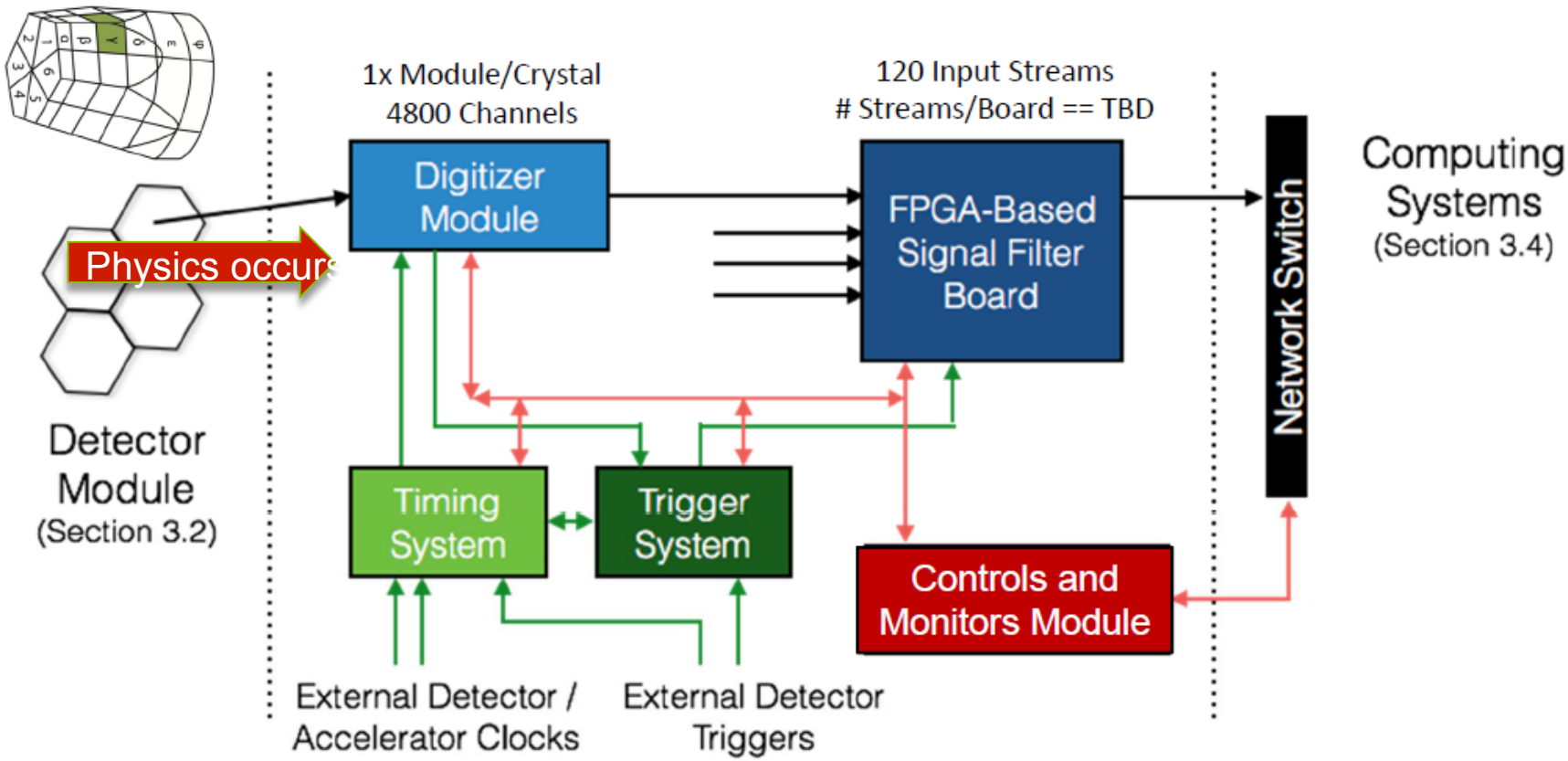


DGS & GRETINA Hardware

- New GRETA designs will leverage years of hardware and algorithm experience gained from use in GRETINA and Digital Gammasphere applications
- Scope requires moderate development work to adapt current hardware to GRETA conceptual design
- Triggers could be generated by GRETA *e.g.* crystal multiplicity or total detected energy **and/or** by ancillary detectors

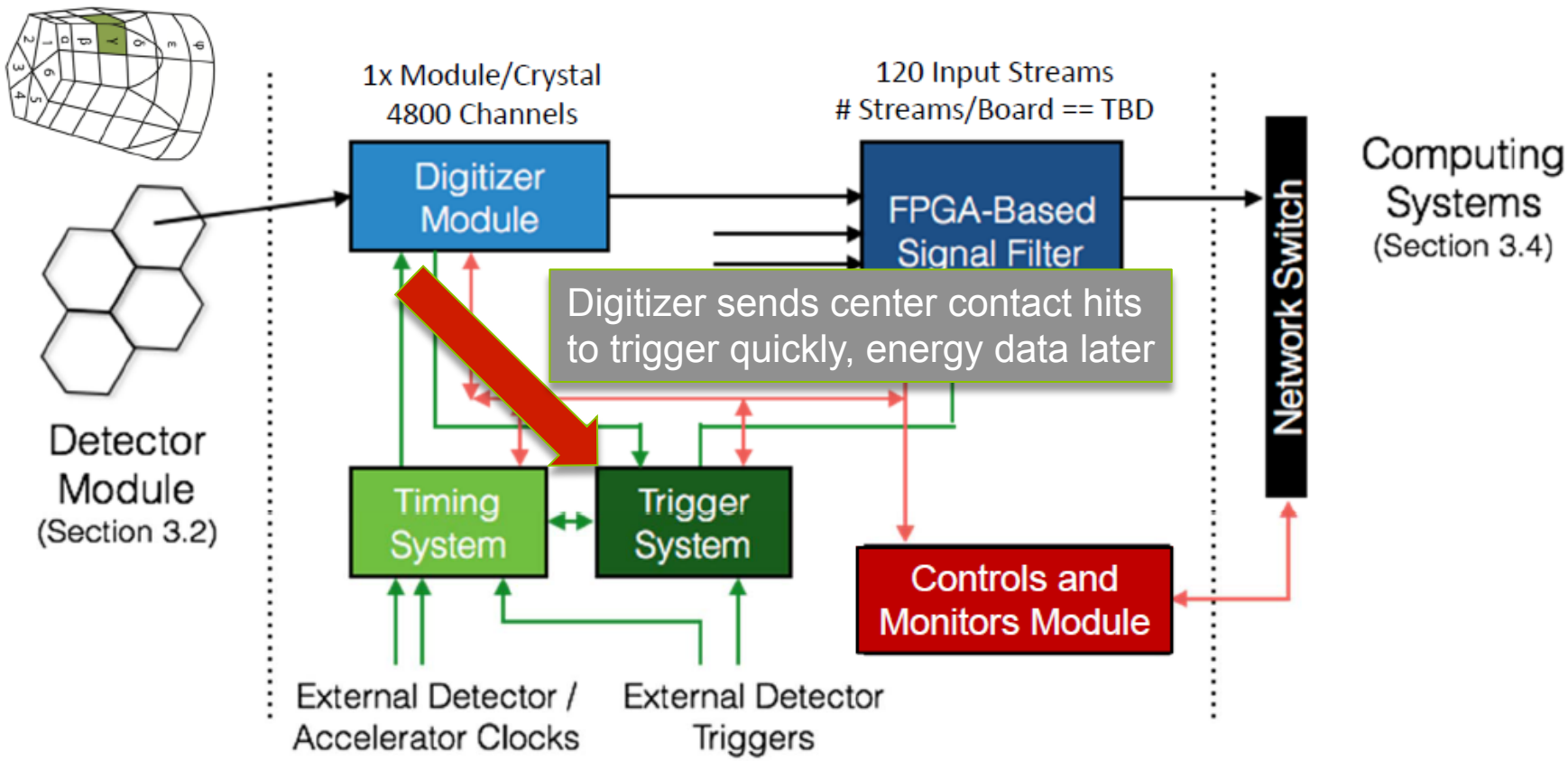
The conceptual design meets the required trigger rate of 4000 validated events/crystal/sec

Triggering Architecture for GRETA



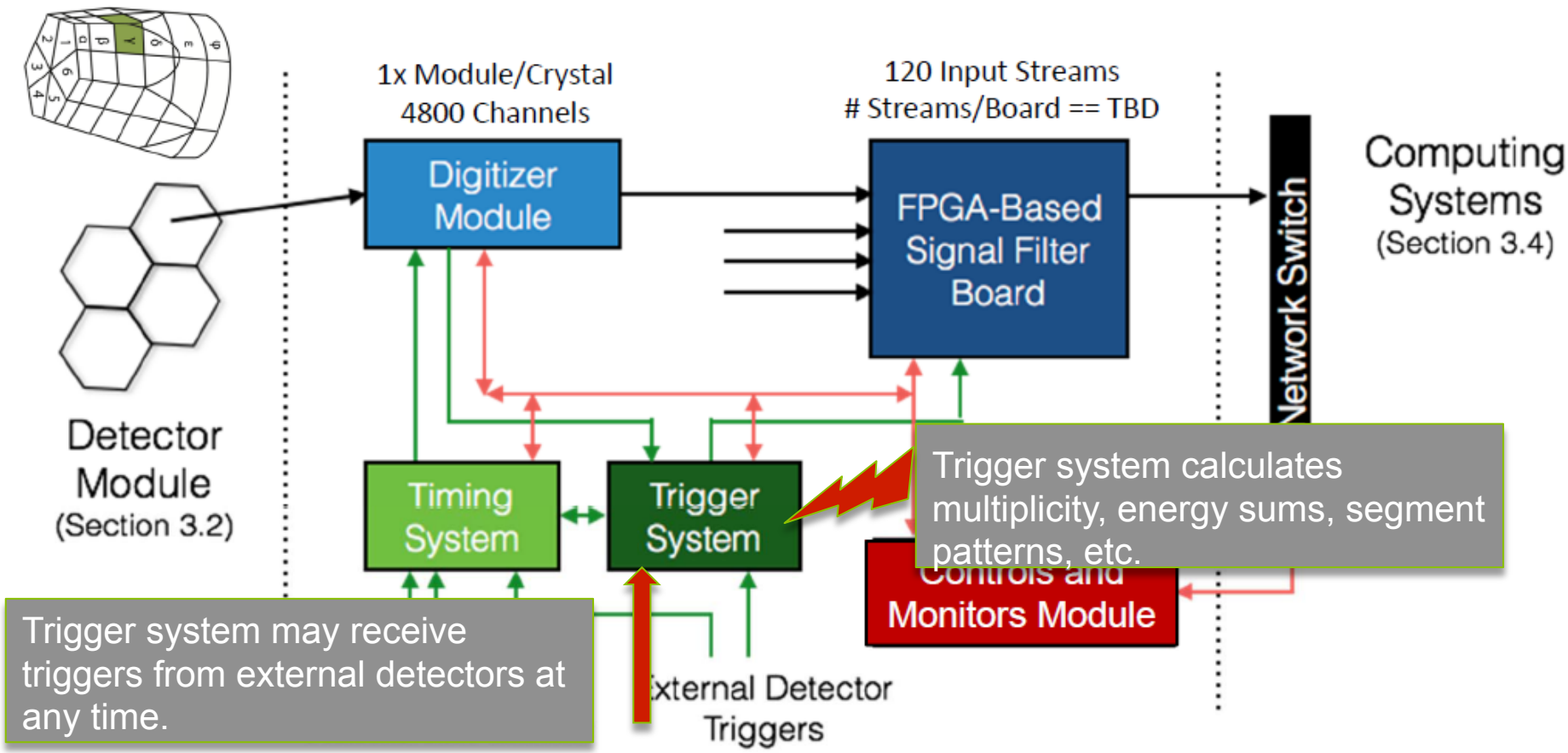
Gamma interactions within the detector generate analog signals that are digitized by the digitizer module. Discriminator logic looks for edges.

Triggering Architecture for GRETA



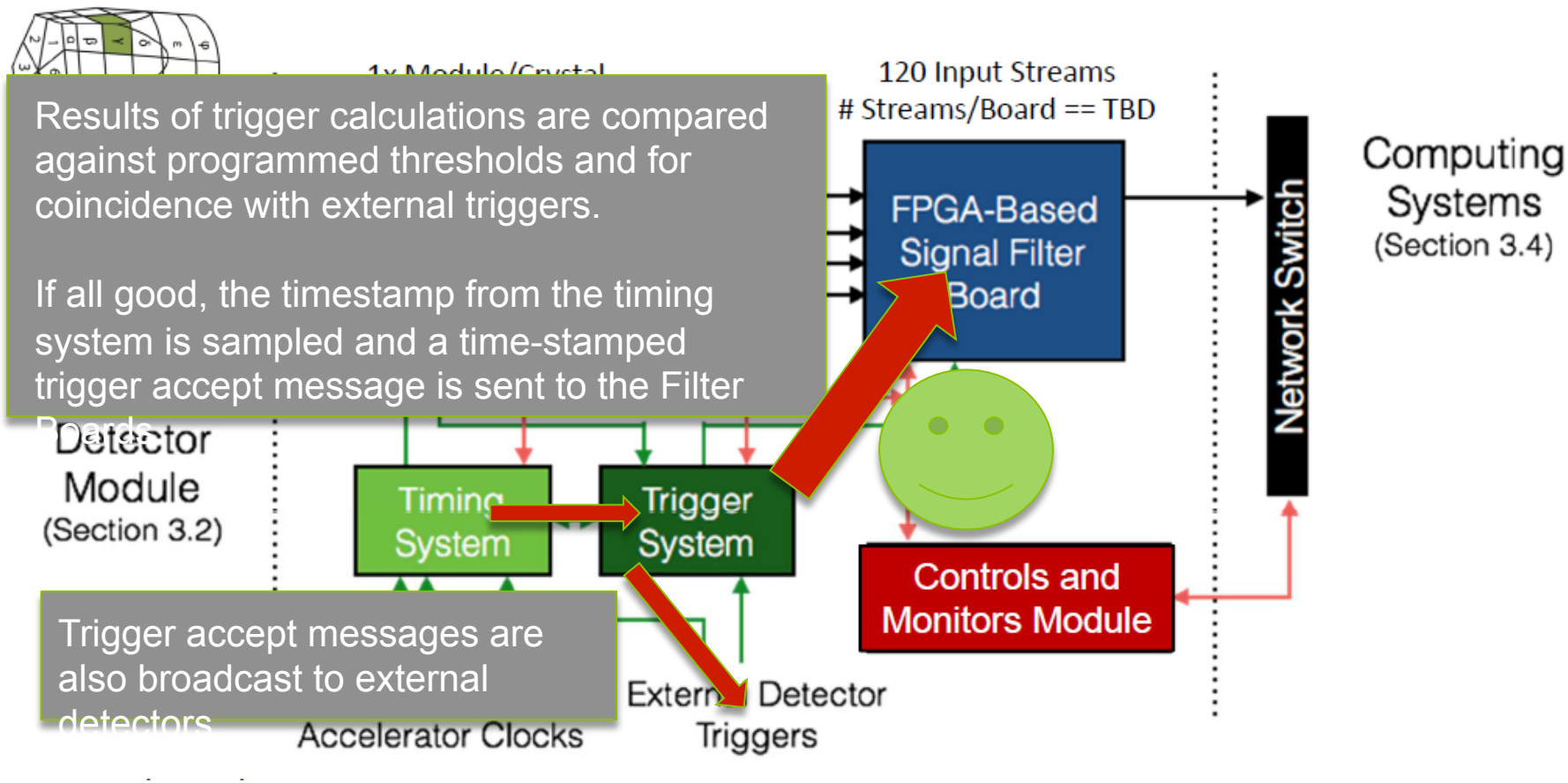
Discriminator firings are reported promptly to the trigger. Coarse energy sums, segment patterns, etc. are also provided, but at some delay.

Triggering Architecture for GRETA



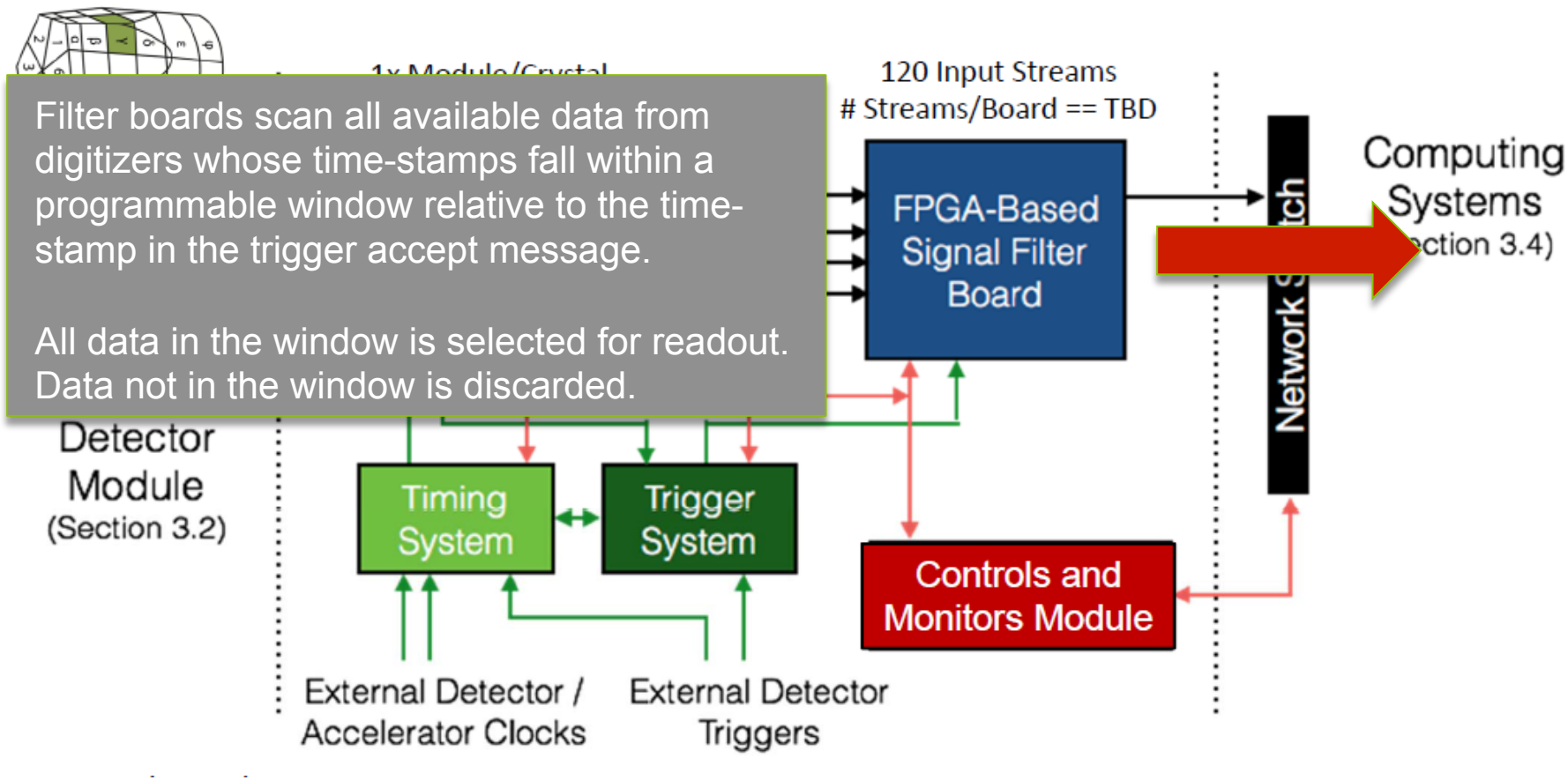
The trigger continuously monitors internal and external trigger conditions at all time, running up to 8 parallel triggering algorithms.

Triggering Architecture for GRETA



Each enabled trigger algorithm can independently send one trigger accept message every 2 microseconds (500kHz). FIFOs for trigger accept messages allow each algorithm to support burst rates up to about 5MHz.

Triggering Architecture for GRETA

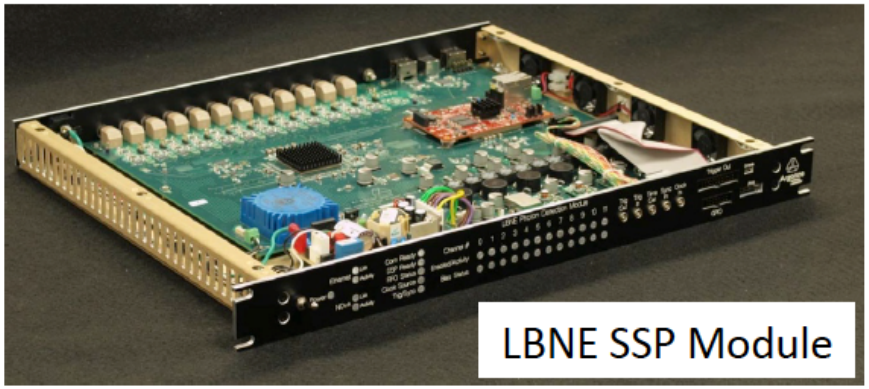


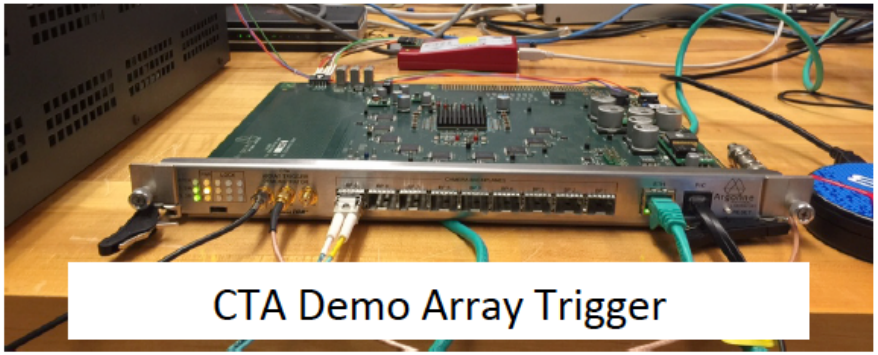
Filter boards scan all available data from digitizers whose time-stamps fall within a programmable window relative to the time-stamp in the trigger accept message.

All data in the window is selected for readout. Data not in the window is discarded.

Formation time of fast multiplicity triggers is ~500ns. Other algorithms vary but typically solve in 1-2us. The filter board holds possibly selectable events for much longer to allow for coincidences with external detectors.

TIMING SYSTEM DESIGN
ANL - J. ANDERSON


LBNE SSP Module


CTA Demo Array Trigger

GRETA

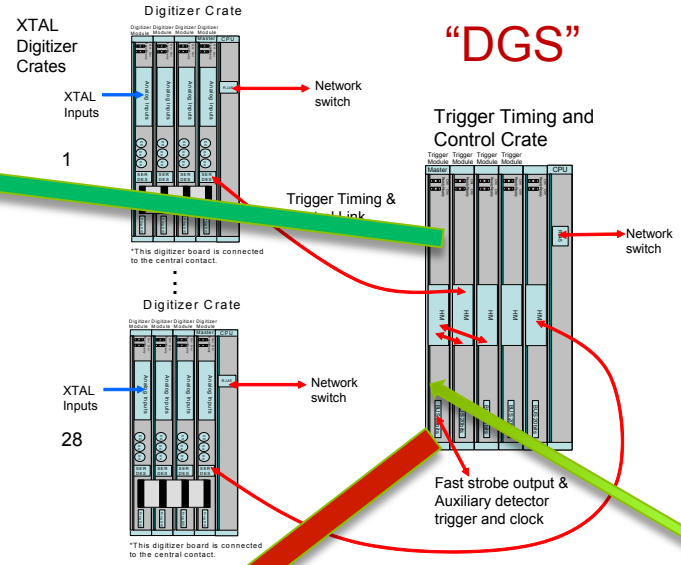
Form factor similar to LBNE SSP; Self-contained "pizza box"

Board design similar to CTA (Cherenkov Telescope Array) Demo

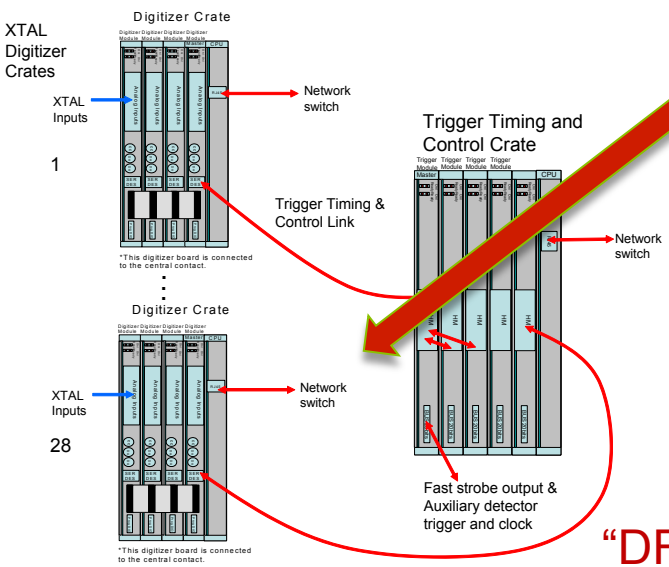
- Leverage timing design from GRETINA trigger module, plus experience gained in design of other systems for LBNE and CTA.
- Utilize existing Digital Gammasphere code base as launching platform.
  - Add jitter cleaner, GPS & TDC capability from other systems
- Timing system is master clock of GRETA, generating clocks and timestamps
- Timing system interfaces with accelerator, GPS, other detectors and trigger system to synchronize all operations

TIMING SYSTEM AS USED IN DIGITAL GAMMASPHERE

The MyRIAD module in an external detector's DAQ latches the DGS timestamp when local triggers occur



The RF clock from the accelerator is connected to the master trigger. A firmware TDC measures the sub-clock timing of the RF relative to the system clock.



The master trigger of one system may use the clock from the master of another system just like router triggers use the clock of their master trigger.

ALL FEATURES DIRECTLY APPLICABLE TO GRETA DESIGN

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THANKS FOR YOUR ATTENTION

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