sPMT HV Splitter status

Pablo Walker*

*On behalf of the PUCC JUNO group

SPMT Internal Electronic Review, Bordeaux

March 8 2018

Outline

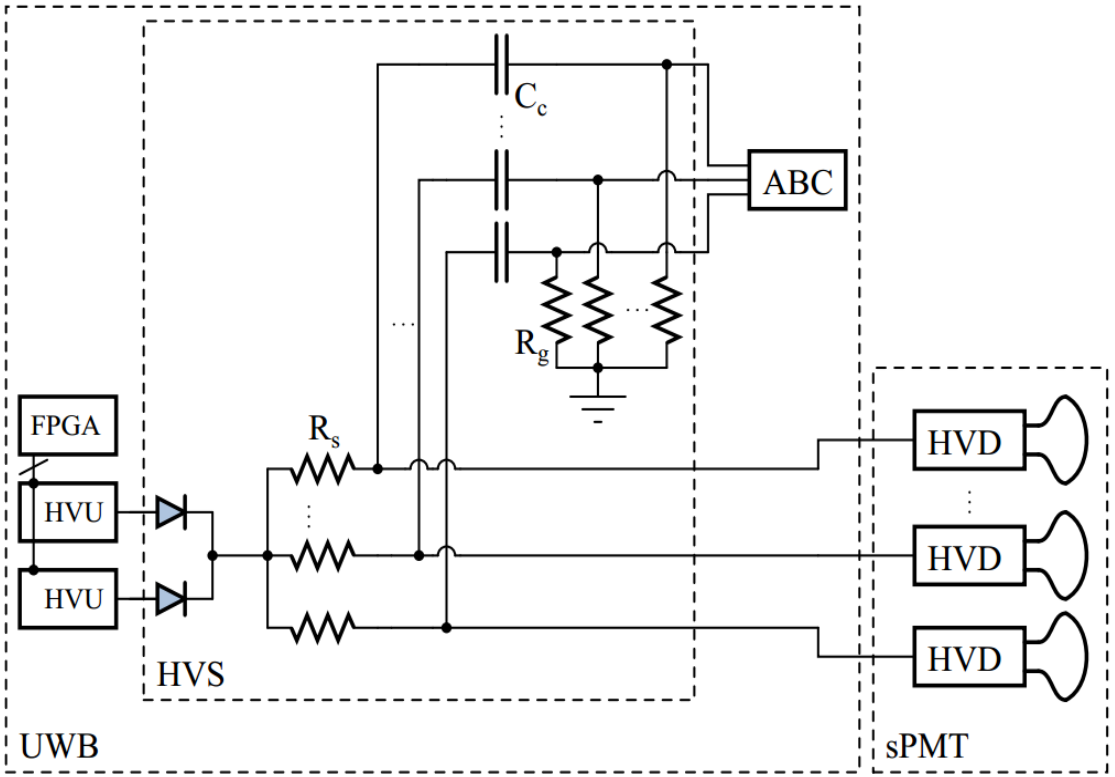
- sPMT splitter board design
- HVS prototype
- Design constraints subject to change

SPMT SPLITTER BOARD DESIGN

High Voltage Splitter (HVS): Problem definition

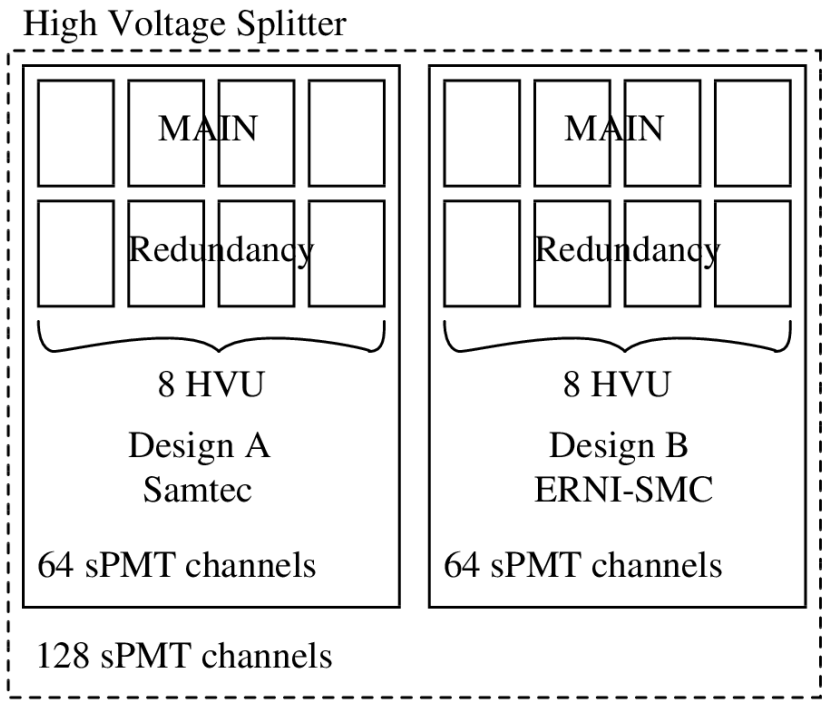
The HVS function is twofold:

- To serve as a **motherboard** for the HVU's and distribute the HV bias to a large number of sPMT's
- To **decouple** the HV bias from the AC signal coming from the sPMT's



HVS system-level specs

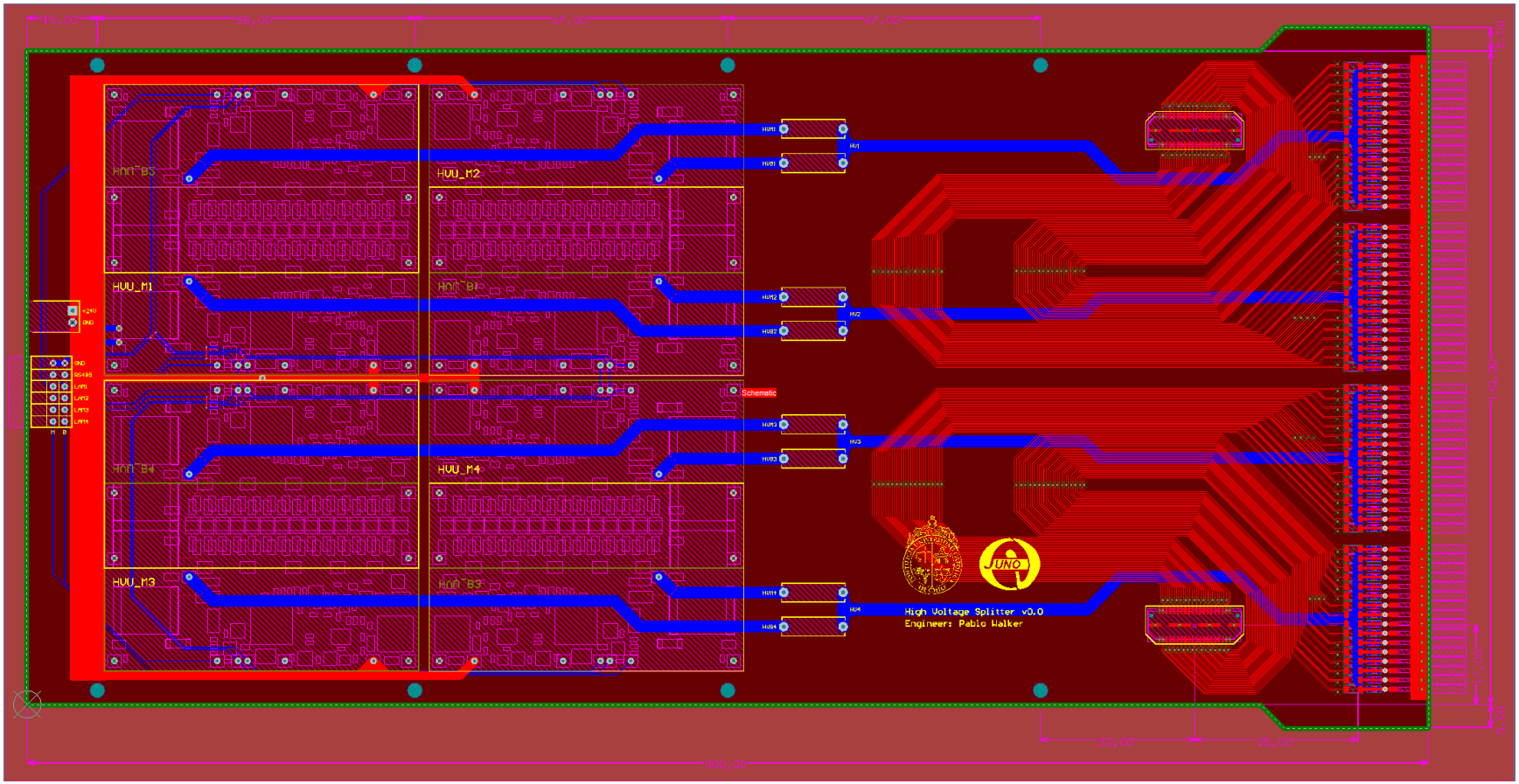
- 128 sPMT channels per UWB
- The current design of the HVS system consists of two board designs (A and B), **64 channels** each
  - Options for SAMTEC and ERNI connectors
- **8 HVU's** on each board
  - 4 for bias and 4 for redundancy
  - Each HVU will bias 16 sPMT channels
- The two HVS board, HVU's and ACB form a **board stack**.



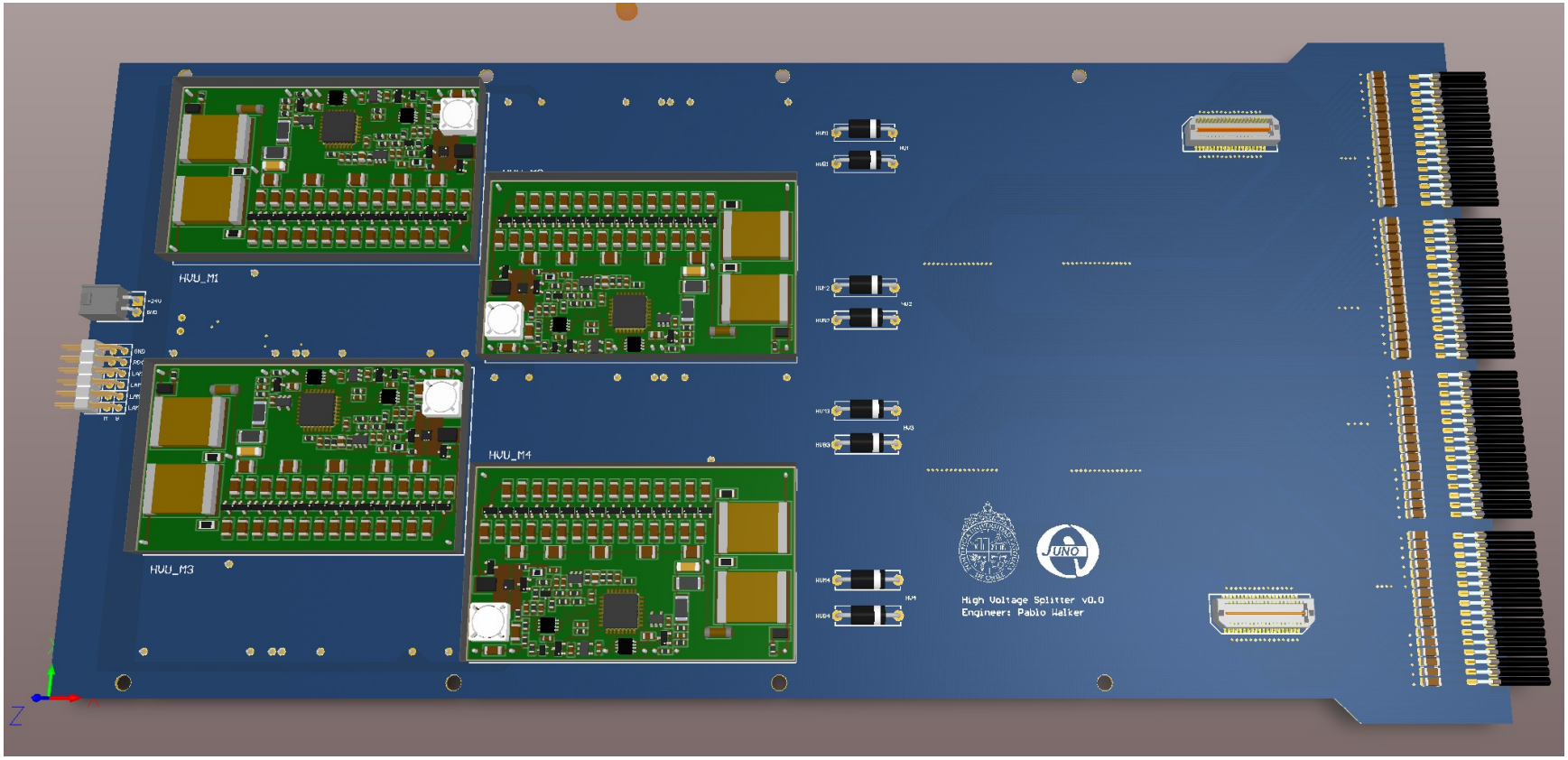
HVS – Current Design

- **Two different board designs**, each with two connectors for **32 channels each**, to match the position of the connectors on the ABC board in the board stack
- The sPMT channels are connected to the board via **direct soldering of RG-178 coaxial** cable
  - We considered 1.8-mm cable diameter
  - Changes in this value will most likely result in changes in the dimension of the board
- The **HVU's are mounted** both on top and on the bottom of the HVS board
  - This allows to keep the design to be approximately of the same dimensions as the ABC board
  - However, this adds to the vertical dimension of the board stack
- The boards have **4 metal layers**
- The physical dimensions of the boards are **150mm x 330mm**

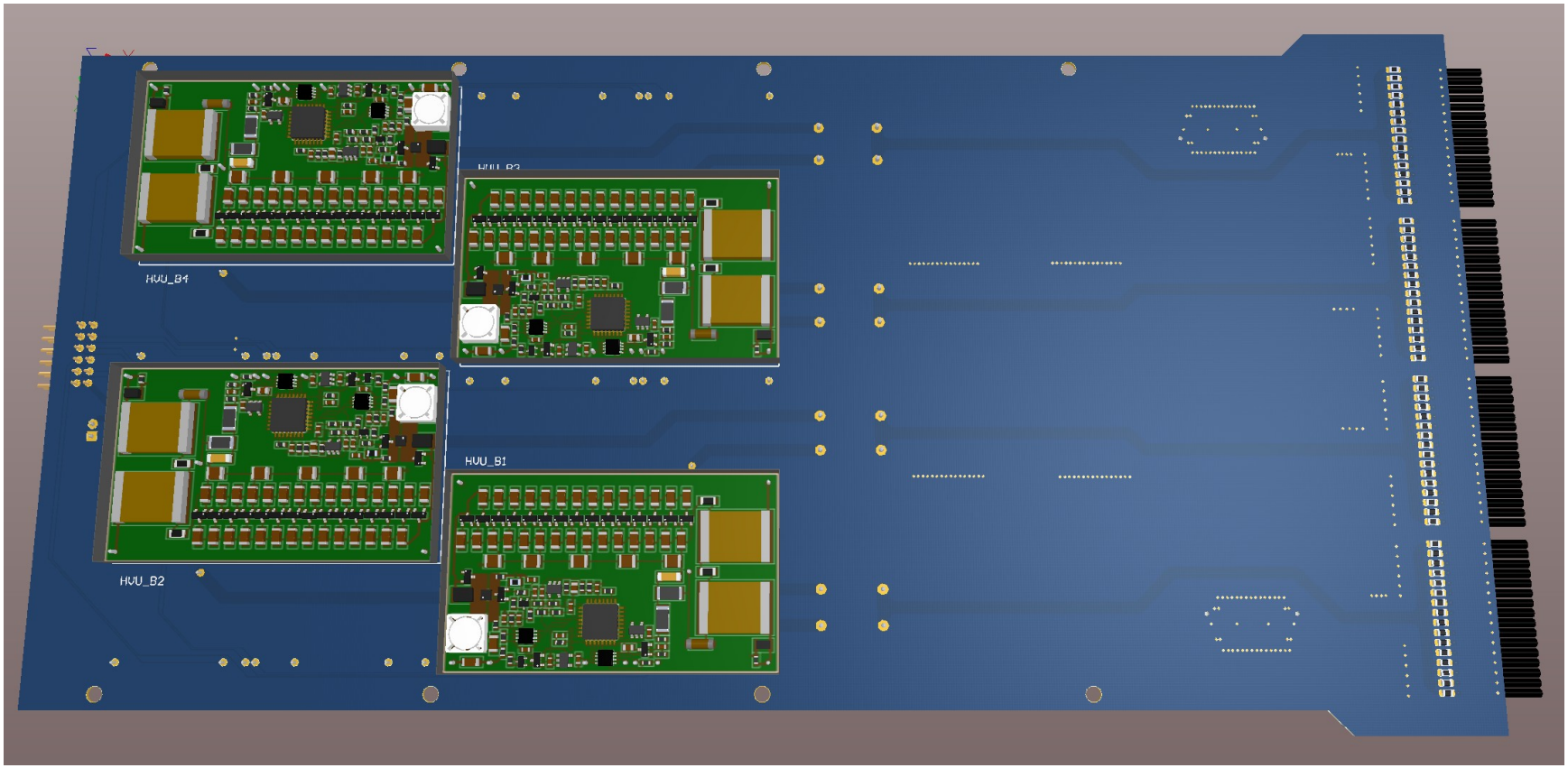
HVS_A v0.0 (Samtec): Layout



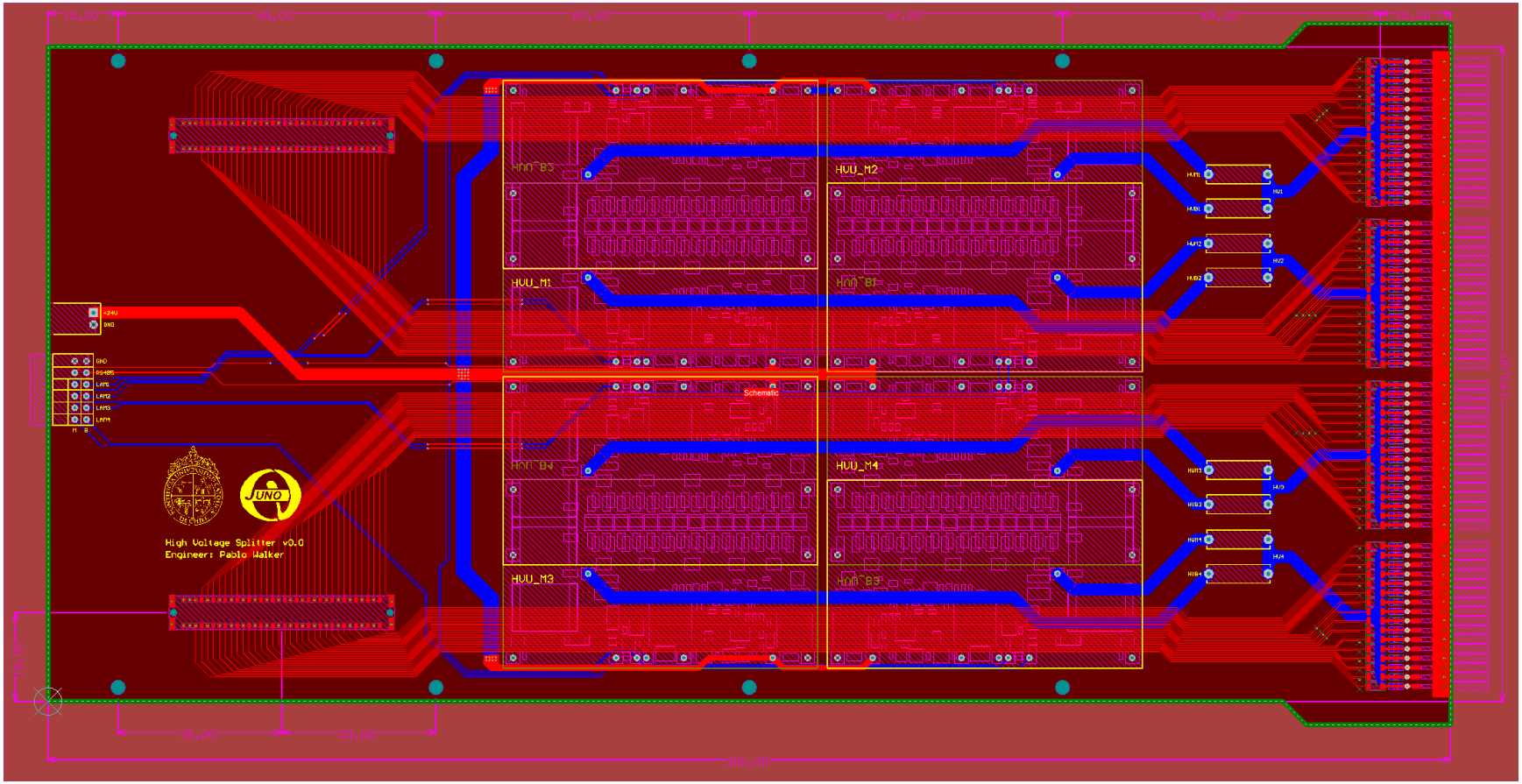
HVS_A v0.0 (Samtec): 3D Top view



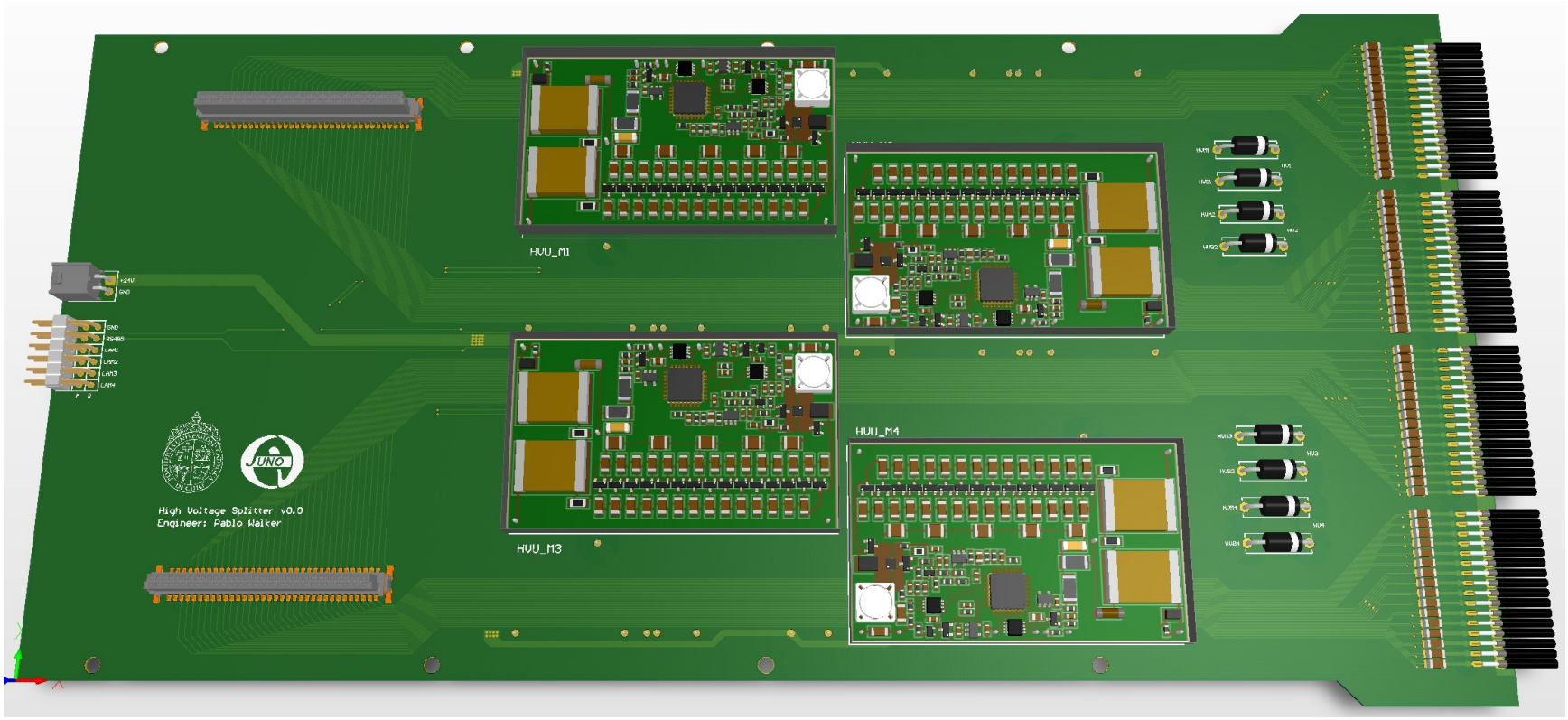
HVS_A v0.0 (Samtec): 3D Bottom view



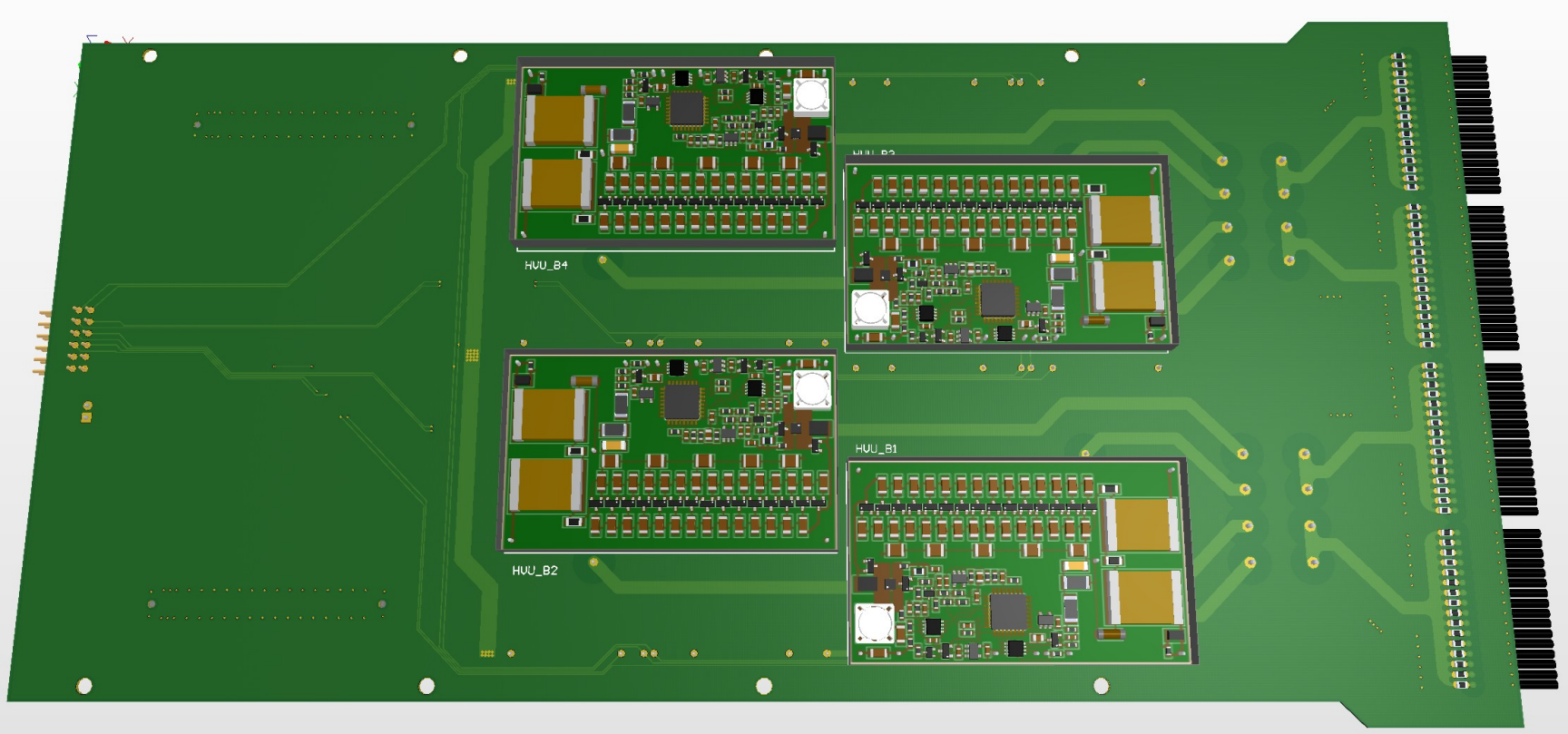
HVS_B v0.0 (ERNI): Layout



HVS_B v0.0 (ERNI): 3D Top view



HVS_B v0.0 (ERNI): 3D Bottom View



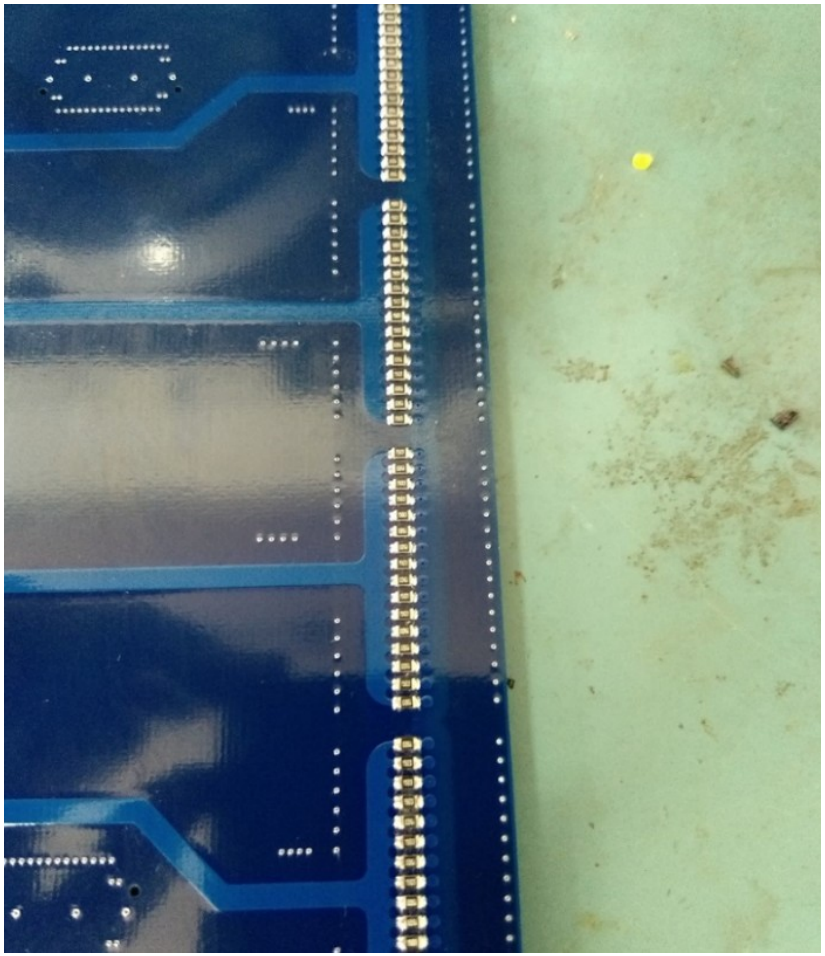
HVS PROTOTYPE

HVS – Prototype: sPMT testing

- By September we need to be able to test the sPMTs from the Factory at Dongguang.
- Two tet stations must be operational by then: One with 128, and another with 16.
- In order for things to be operational in China by September, we need them to get to France first.
- We plan to deliver at least 3 HVS prototypes by June/July: one for 128, one for the remaining 16, and another one for spare.

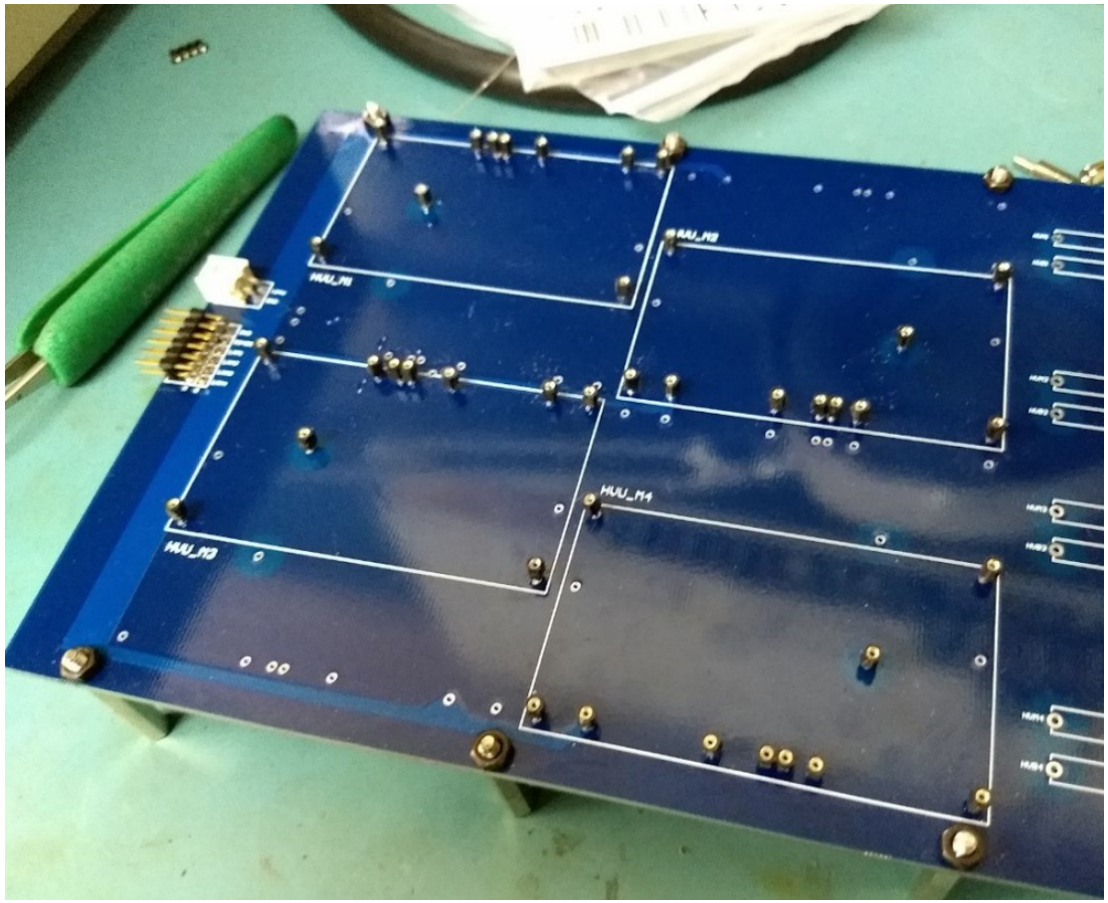
HVS – Prototype

- A prototype for the **two board designs** has been fabricated and the tests are on the early stages
  - Test for shorts to ground
  - continuity test in a selected group of tracks



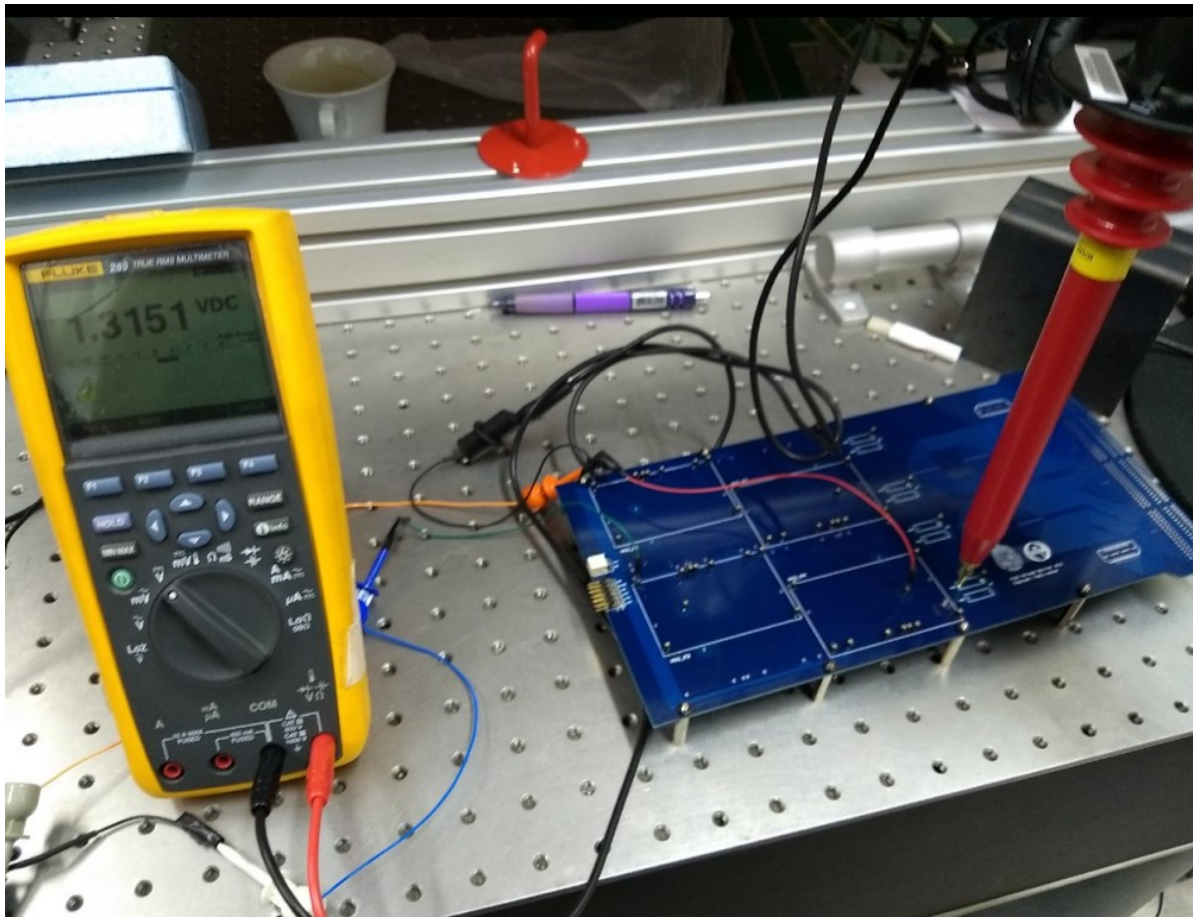
HVS - Prototype

- Partial soldering of **board A** (Samtec) is completed
- Female headers were used for the pins of the HVU's, to allow for easy connection and testing.



High voltage tests

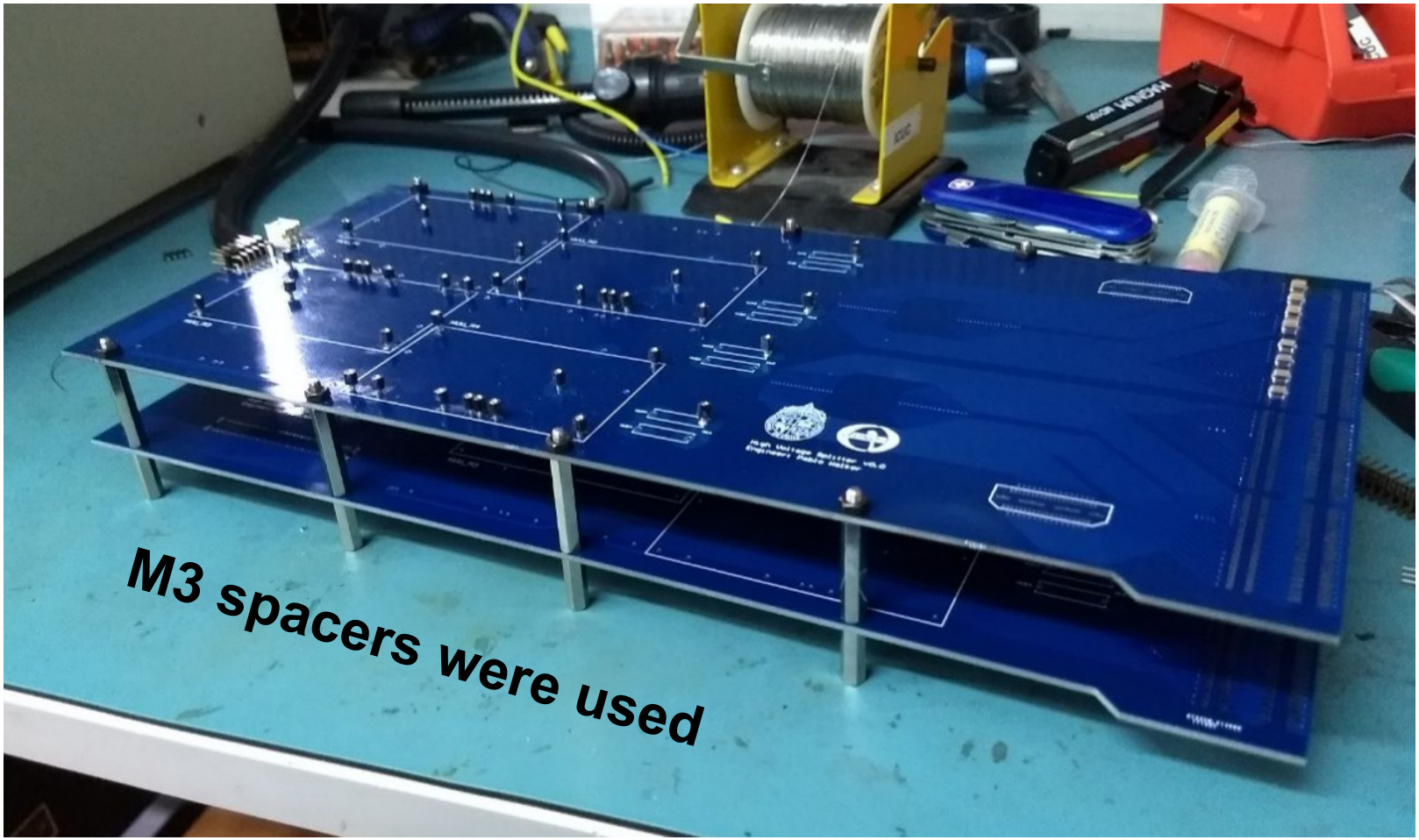
- Connection to HV (~1300VDC) on board A to test for current leak and arcs
  - All HV tracks were tested
  - Adjacent HV channels were connected to GND to simulate worst-case scenario
  - No current was observed in any of the tests



Functionality tests

- The decoupling functionality was tested on a selected group of tracks for low voltage bias
  - No problems were observed
  - More comprehensive tests are still pending
- We currently lack the equipment to formally test for crosstalk

Board stack concept



DESIGN CONSTRAINTS SUBJECT TO CHANGE

Design constraints subject to change

- Some of the hardware that interfaces with the HVS have been subject to, or are in discussion of, changes.
- Next are listed some of the changes that have the potential to change the current HVS design.

Design constraints: RG178 diameter

- Diameter of RG178 cable is increased from the standard 1.8mm to a custom 2.1mm.
- With everything else remaining constant, this would mean a 19.2mm size increase in the HVS design.
- The dimensions of the board would change from 330mm x 150mm → 330mm x 170mm

Design constraints: HVU design

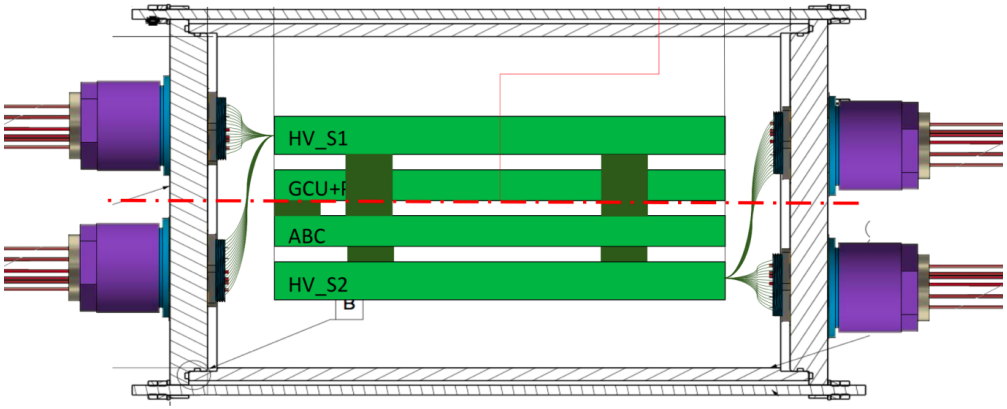
- Change in the HVU design to integrate with the evolving LPMT design.
- New design has three HV channels per board.
- Discussions have been had with the Russian colleagues, and that they have confirmed that in principle it would be possible to keep the old HVU design.
- We are expecting 50 HVUs with the old design to be ready by ~May.
- Not clear yet if the HVS should migrate to the new design, or stick with the old one. We will look into our options carefully.

Design constraints: HVU address and logic

- The HVU comes with a fixed RS485 address from the fabrication.
- Reconfiguring the address of 3200 HVU is no small task.
- One potential solution is to add local logic to the HVS (uC).

Design constraints: UWB endcap-connectors

- The UWB endcap interfacing connector distribution is subject to change. A two endcap (figure) distibution is being discussed.
- For the current HVS design, it was considered that all the connectors were located in a single endcap.
- This determines the orientation of the board, given that the RG178 cables point toward the connector.



Acknowledgement

We thank the PUCC team for all the hard work:

Angel, Pedro, Beda, Michael, Agustín

THANKS FOR YOUR ATTENTION