The ABC readout board introduction

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APC - Astroparticule et Cosmologie

Outline

Context

ABCv0

Summary

Context

Requirements

Need to develop a compact, high channel density building block for JUNO

- Process with analog electronics signals from small photomultipliers
- Remotely setup acquisition, performing signal conditioning (accommodating signal dispersion, etc.)
- Acquire, readout and store resulting digitized outputs without any data lose
- Instrument up to ~ 25.000 channels by groups of 128 (easier to handle)
- Modular and flexible architecture, including custom logic and huge buffering resources
- Compatible with GCU through a industry standard, high bandwidth interface
- Possibility to programmatically include advanced features and dedicated functionality
- Locally / remotely reprogrammable

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Based on 16-channels, software controlled, CatiROC ASIC
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First steps
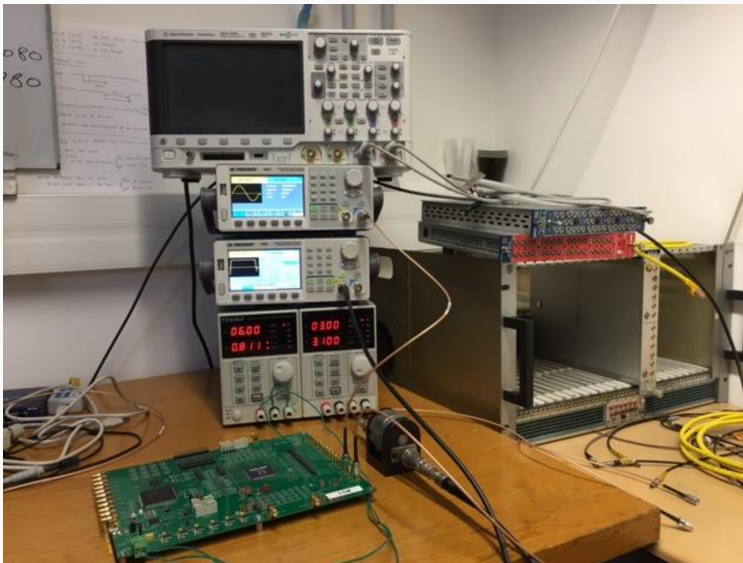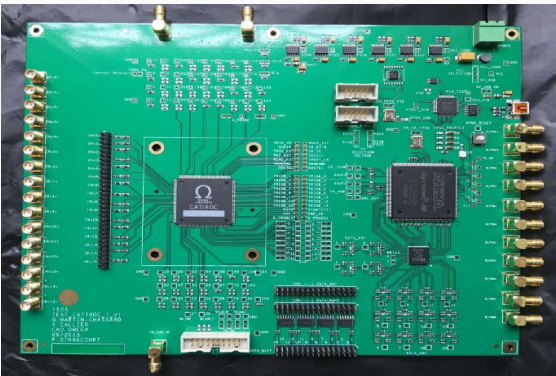
In lab testing with omega test card

A. Fully understanding CatiROC ASIC using Omega test board

Development of firmware and software
In lab testing with PMT
Data analysis (timing, etc.)
Online visualization (histogramming, etc.)

B. Based on feedback, design of a new board: ABCv0

Adaptation to Juno requirements
Inclusion of programmable logic

C. ABCv1 will come later on ...

ABCv0

ABCv0 ... features

Basic features

Massive trigerless driven data flow

Completely independent channels

8 CatiROC asics
128 channels
Xilinx Kindex 7 FPGA
FMC for GCU interfacing
Four 32 lines connectors
Inspection lines for debugging
JTAG programming
40 MB/s USB2 interface

Advanced features

Fully software controlled System

Huge amount of programmable logic
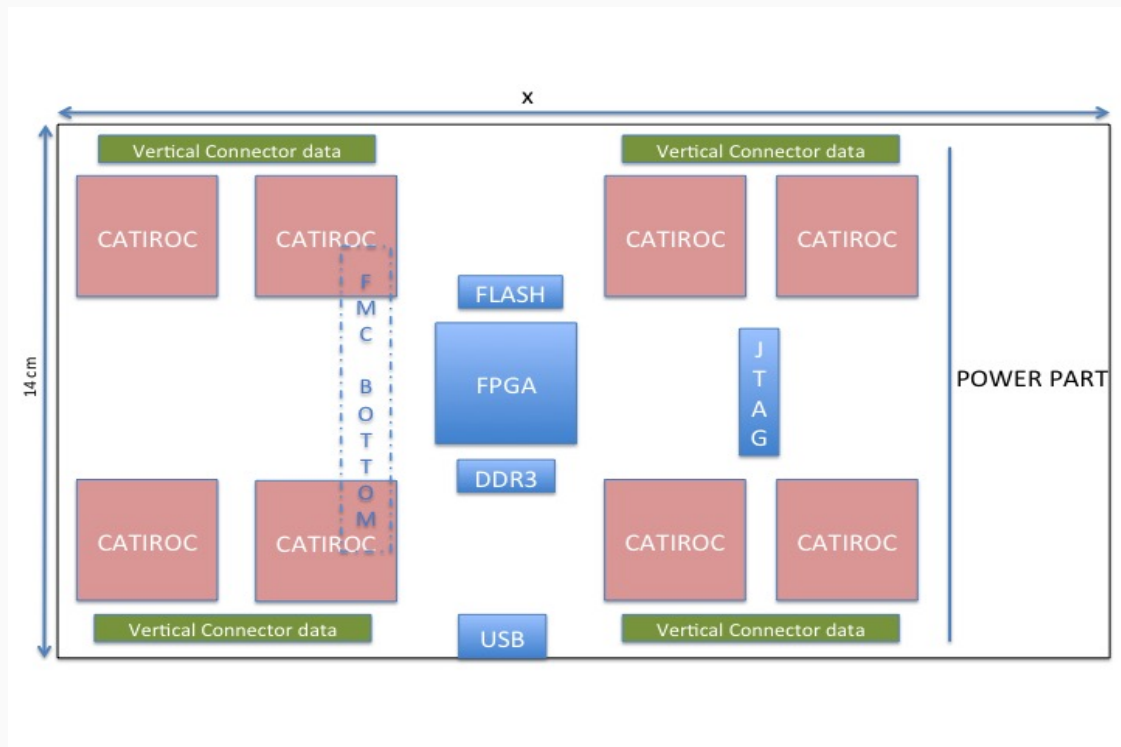
Dead timeless (almost) dead time monitoring
2 GB DDR3 (*supernova burst buffering*)
S-Curve computting for noise monitoring
Discriminator output TOT measurement
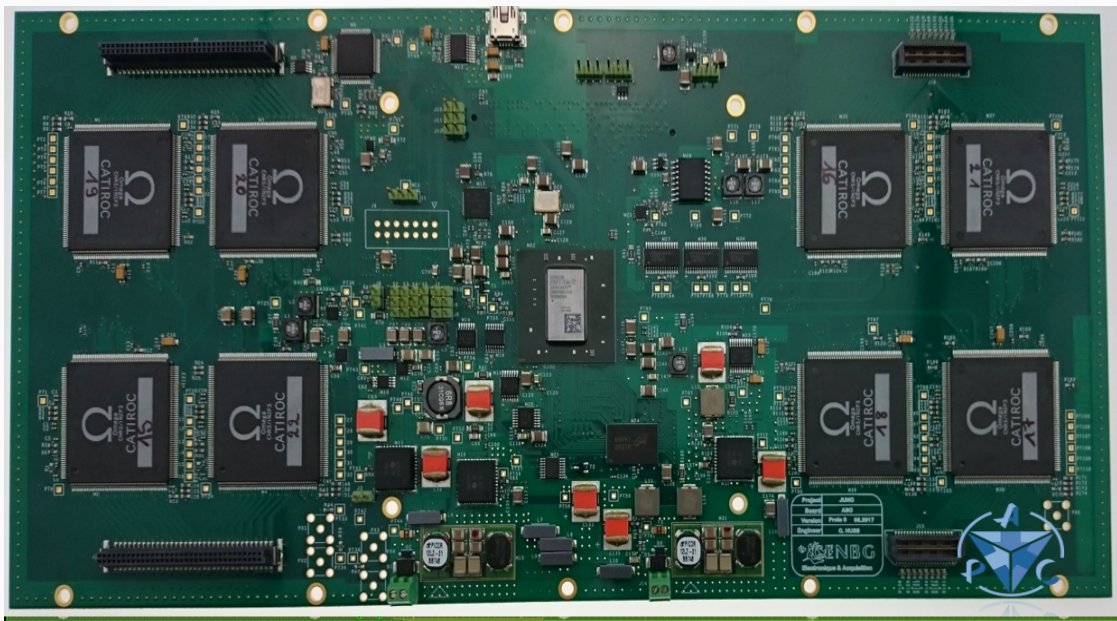
FPGA handles communication and ASIC setting up / data readout

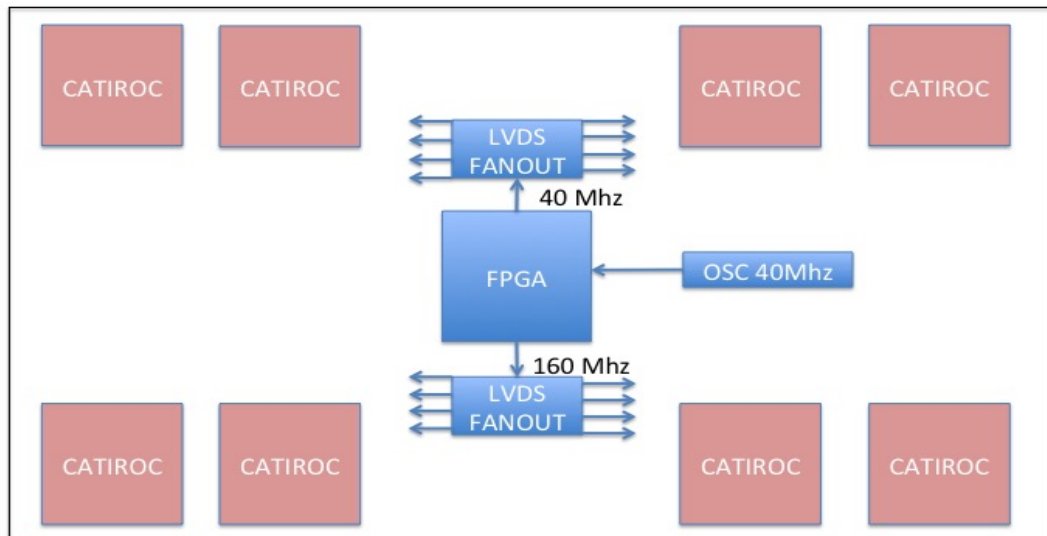Best of two worlds: full custom asic and programmable logic fpga

Collaboration between several IN2P3 laboratories: more than one year of joint development

All 128 discriminator outputs are brought to the FPGA for processing

ASIC 40/160 MHz clocks : identical delay
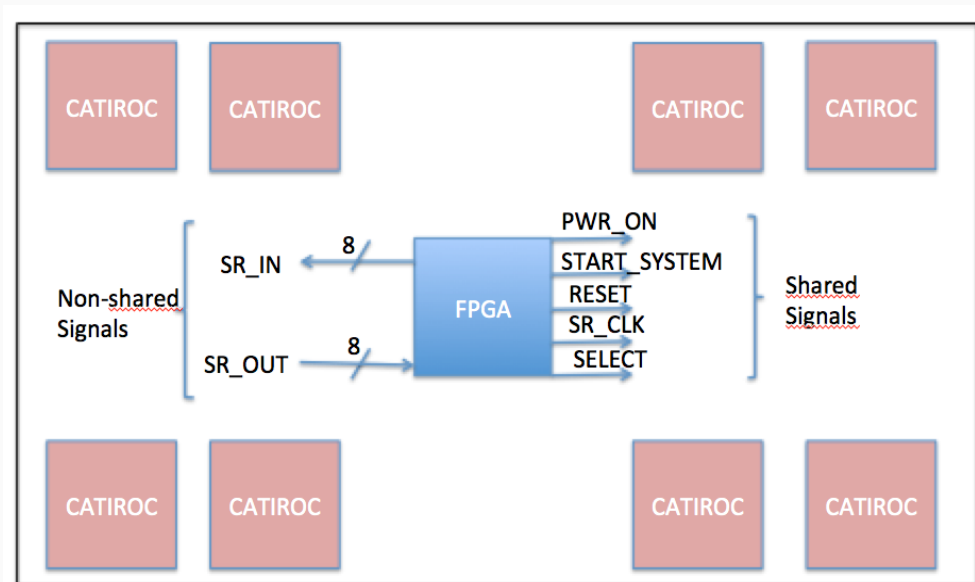*Always* provided by fpga : FPGA/ASIC time stamps are identical

Source clock : Board local oscillator / GCU

ASIC 40/160 MHz clocks

All ASICS are power on / reset / started at same time

Slow control Star topology

Avoid daisy chaining (in case of failure of one ASIC)

Summary

ABCv0

Summary

- All channels are synchronous
- Events are numbered and time stamped
- Charge, time and gain information
- Additional 'fake' events from discriminator output

... refer to next talks for more details !