ATLAS detector upgrades and performances

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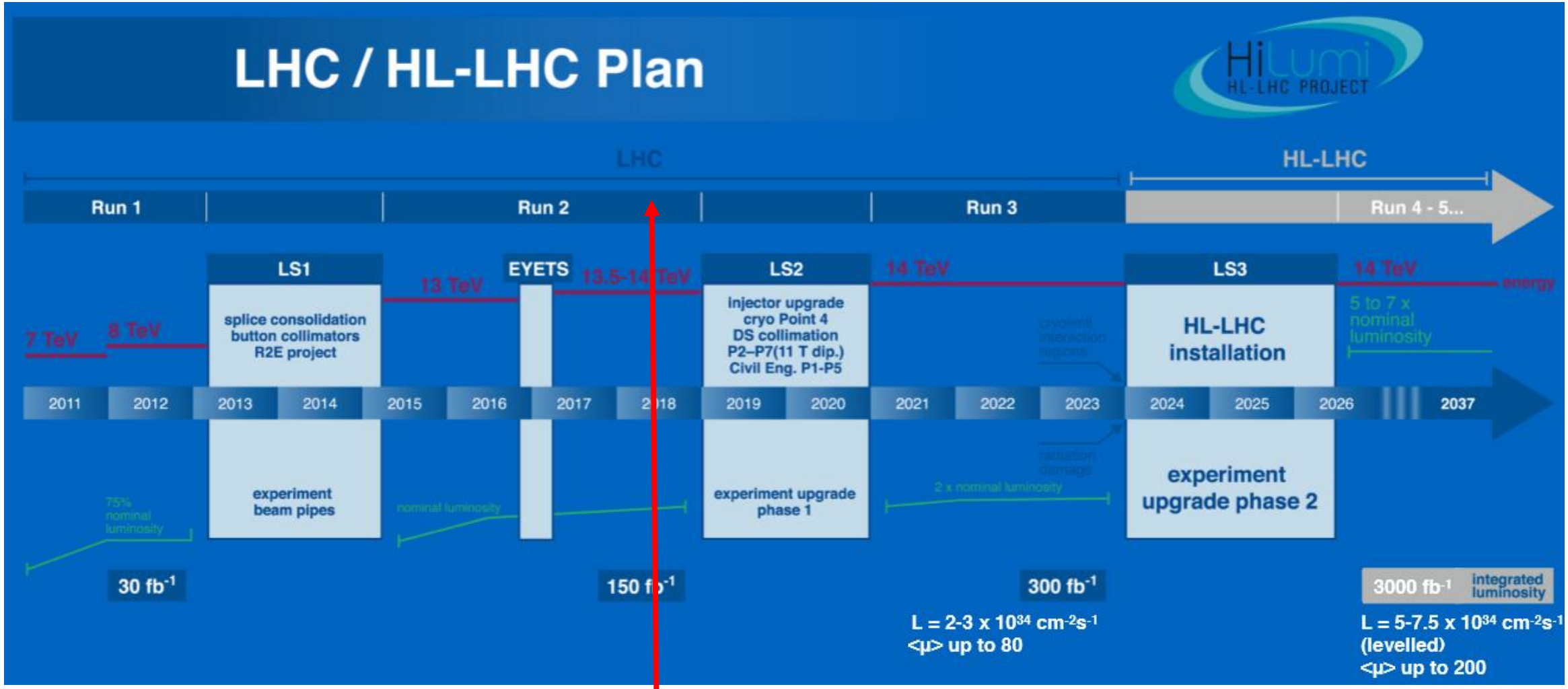
Upgrades timeline

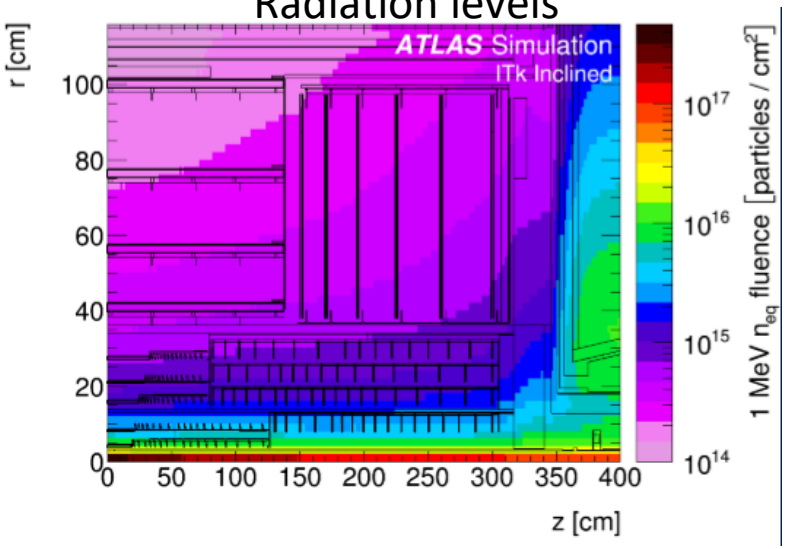


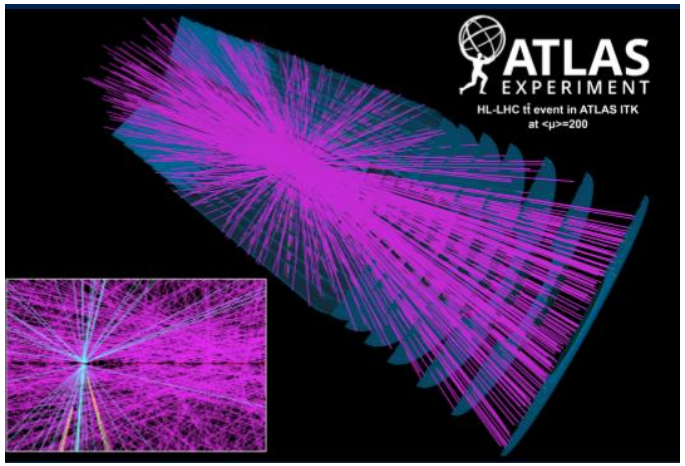
Today

Context of the upgrades

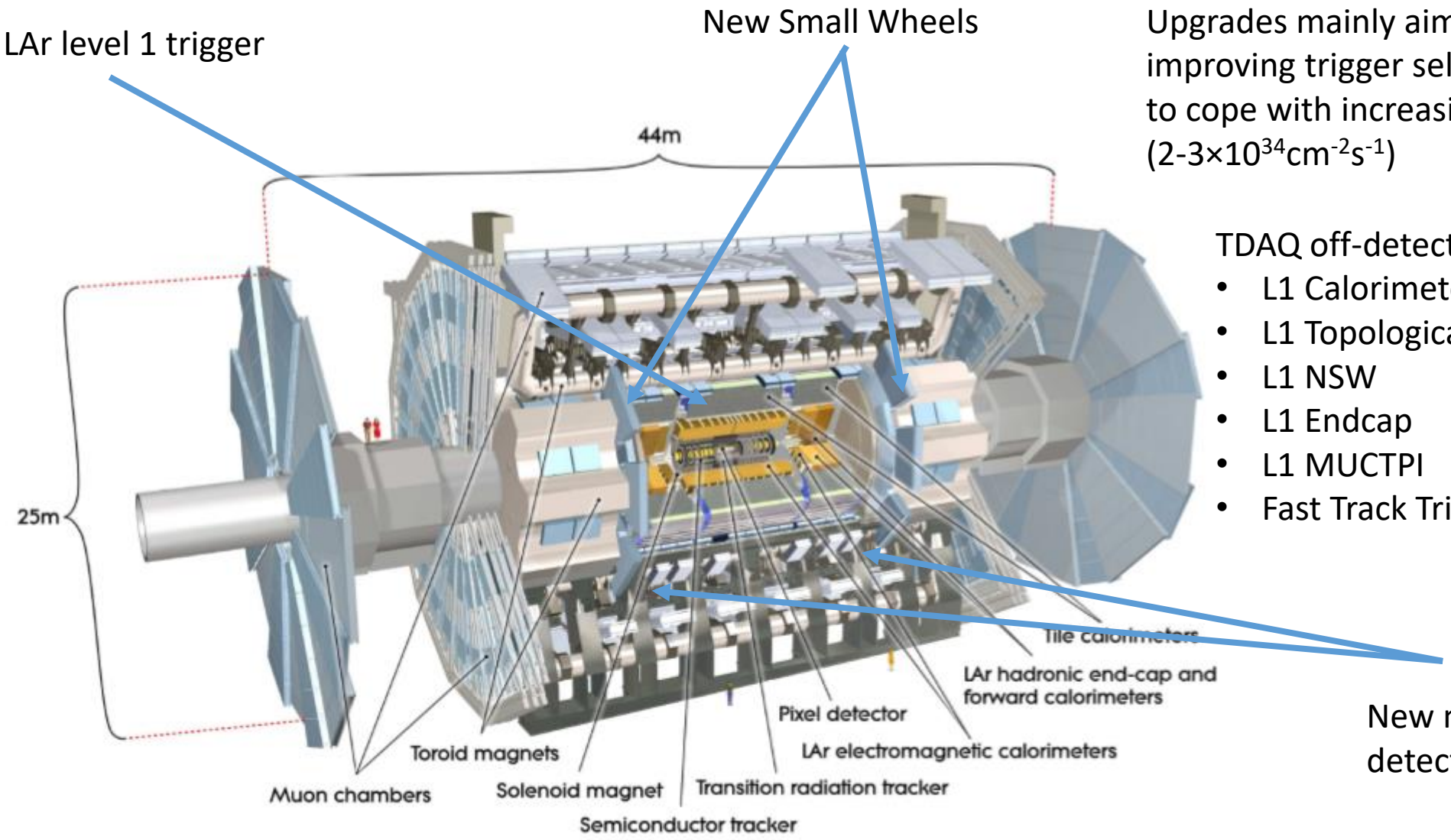
- Increasing the inst. luminosity is the only way of beating (temporarily) the $\sqrt{t}$ factor in increasing the range for new physics
- Detector upgrades are mainly oriented towards :
  - Radiation tolerance : present detector qualified only up to 1000 fb^{-1}, need to stand up to 10^{16} neq/cm^2-10 MGy
  - Improving trigger selectivity, to avoid bandwidth saturation
  - Keeping detector physics performance similar to today in high pile-up conditions (peak levelled luminosity up to 7.5×10^{34} $cm^{-2}s^{-1}$, $<\mu>\approx200$)
  - Bring in new information for better trigger/reconstruction (timing)
  - Increasing acceptance coverage where possible
  - Keep electronics up to date; some parts are obsolete (> 15 years old !) and cant be manufactured/maintained on the long term

Radiation levels





ATLAS Phase-I upgrades (LS2, 2019-2020)



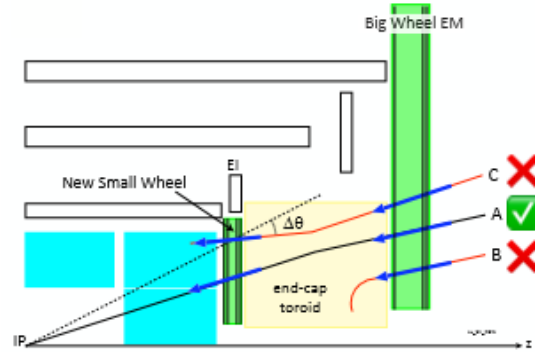
Upgrades mainly aim at improving trigger selectivity, to cope with increasing luminosity ($2\text{-}3\times10^{34}\text{cm}^{-2}\text{s}^{-1}$)

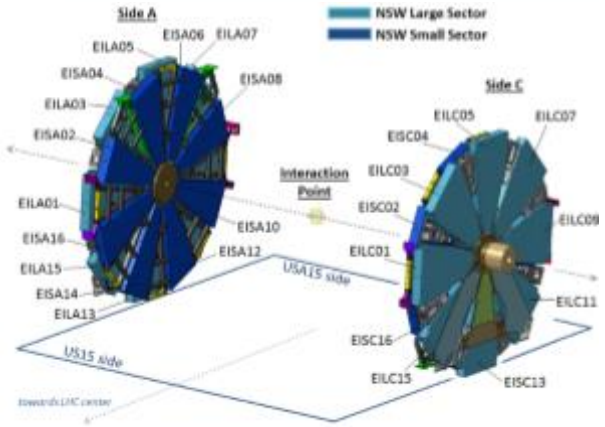
TDAQ off-detector electronics

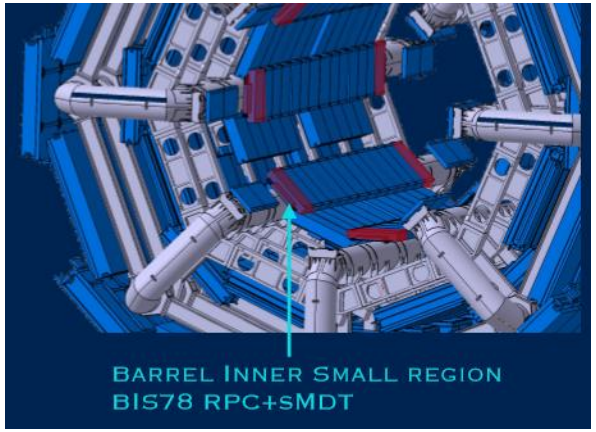
- L1 Calorimeter
- L1 Topological
- L1 NSW
- L1 Endcap
- L1 MUCTPI
- Fast Track Trigger (FTK)

New muon RPC detectors

New Small Wheels and BIS78







Intended to reduce muon fake rate in endcap region
Coincidence between end-cap chambers and NSW

Strong requirements on NSW measurement precision :
- 1 mrad on track direction
- 100 μ on track position

5m radius wheels covering 1.3<|η|<2.7, each wheel has :
- 2 external sTGC quadruplets used as trigger chambers,

BCID assignment and track direction measurement
- 2 Internal MicroMegas quadruplets for tracking (< 100 μ resolution)

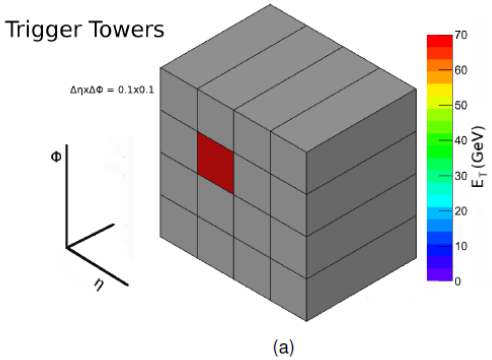
16 new RPC + replacement of
16 MDT by sMDT to cover 1.0<|η|<1.3

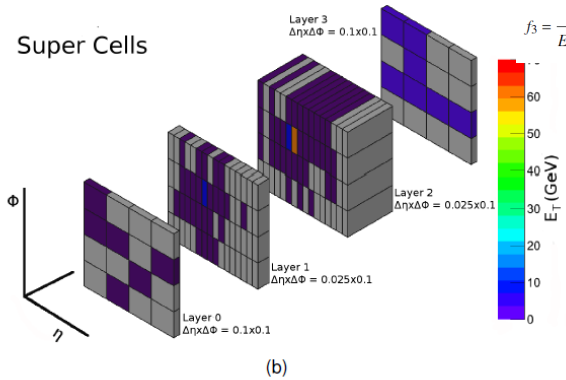
Same technology will be used for
Phase-2 Muon upgrades

L1 trigger rate for inst. Luminosity 3×1034 cm-2s-1

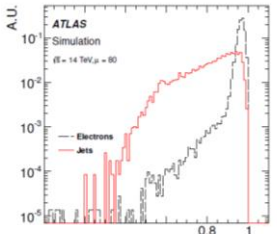
L1MU threshold (GeV)	Level-1 rate (kHz)
$p_T > 20$	60 ± 11
$p_T > 40$	29 ± 5
$p_T > 20$ barrel only	7 ± 1
$p_T > 20$ with NSW	22 ± 3

L1 Calo trigger upgrade



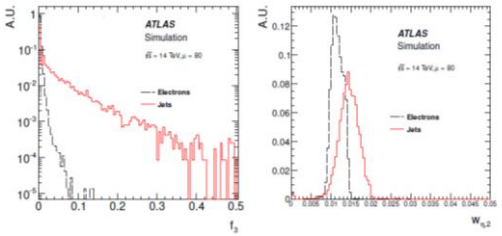


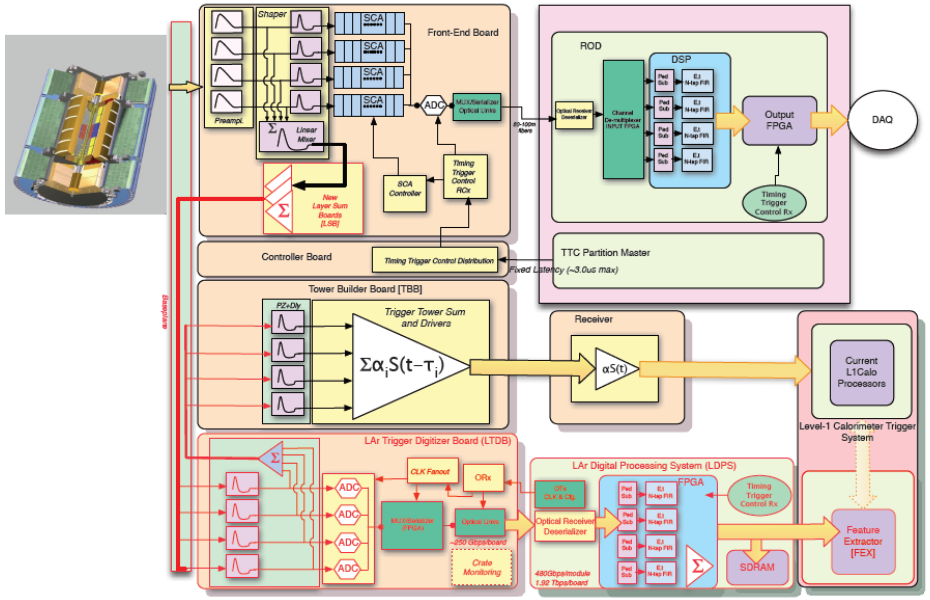
$$R_\eta = \frac{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.175\times0.2}}$$



$$f_3 = \frac{E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.2\times0.2}}{E^{(1)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.}}$$

$$w_{\eta 2} = \sqrt{\frac{\Sigma\left(E^{(2)}_{\mathrm{T}}\times\eta^2\right)_{\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}} - \left(\frac{\Sigma\left(E^{(2)}_{\mathrm{T}}\times\eta\right)_{\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}}\right)^2}$$

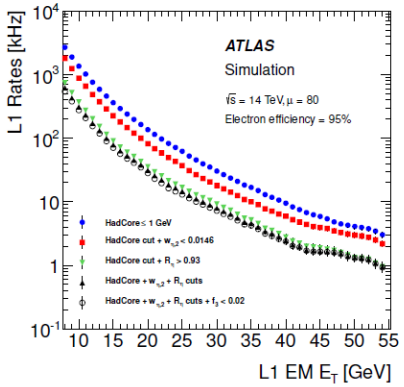


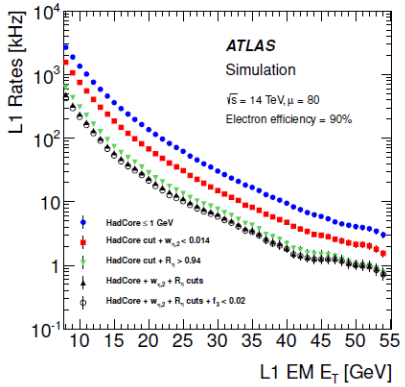


Shower shape estimators can only be built with :

- Layer information
- Fine granularity

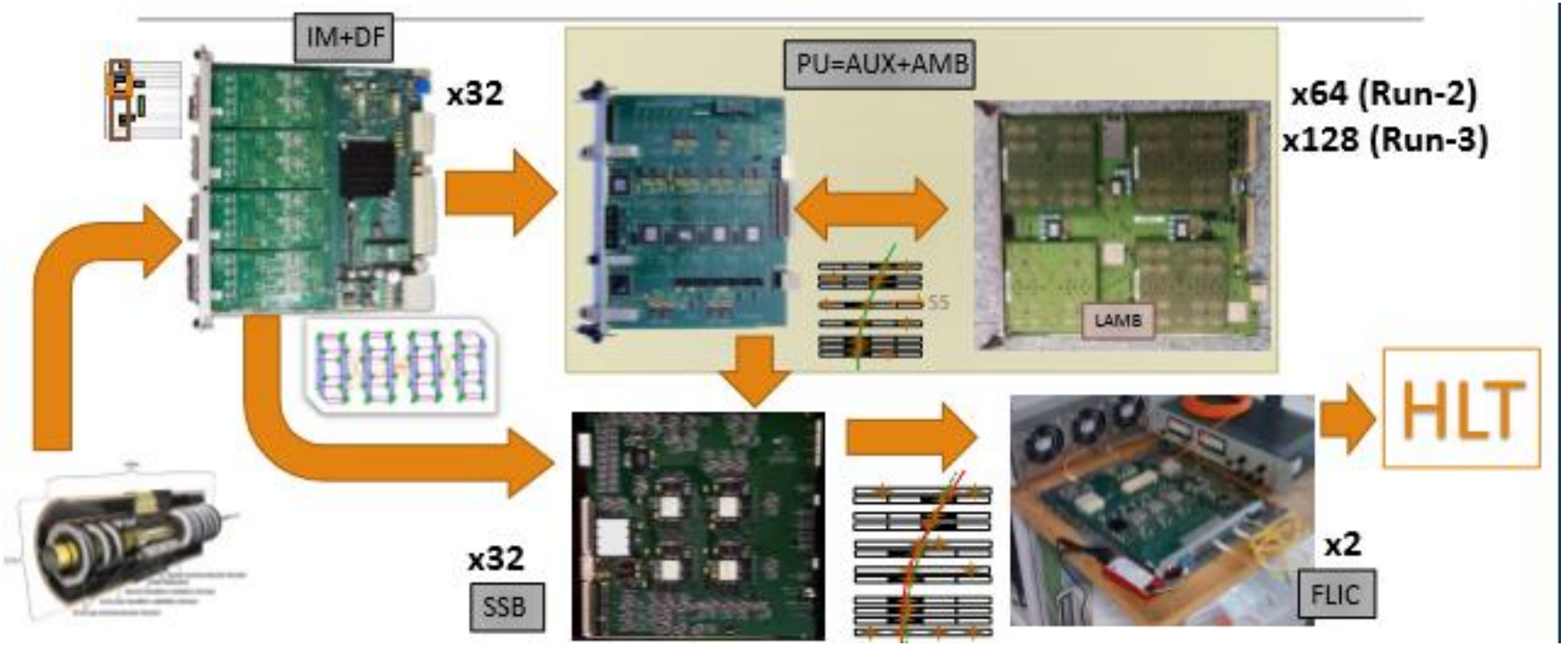
→×10 more signals w.r.t. present system





On-board 12-bit digitization at 40 MSPS
Present analog trigger system kept as backup

FTK



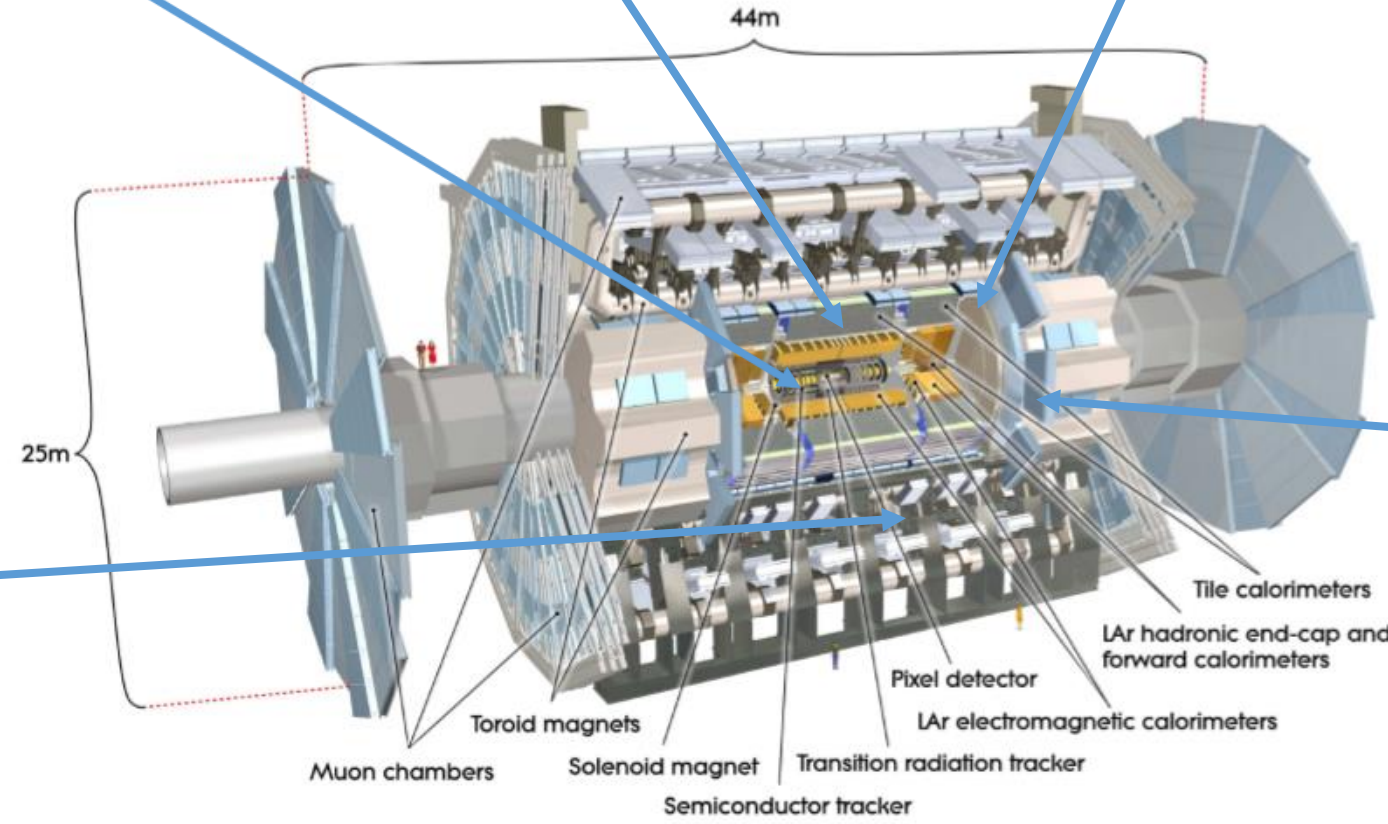
- Real time tracking for all events accepted by L1 trigger (no RoI), provided to L2
- Pipelined custom hardware : First stage (pattern recognition), Second stage Track fitting)
- Efficiency > 90% for Pt>1 GeV, latency < 100 µs
- 8192 associative memory custom chips, > 1000 FPGAs

ATLAS Phase-2 upgrades (LS3, 2024-2026)

New Inner Tracker, all Silicon
Coverage increased to η=4

New LAr Readout

High Granularity Timing Detector (HGTD)
Adds timing information in LAr endcap acceptance



Muon high η tagger
(under study, probably even later than LS3)

New muon chambers
in barrel region

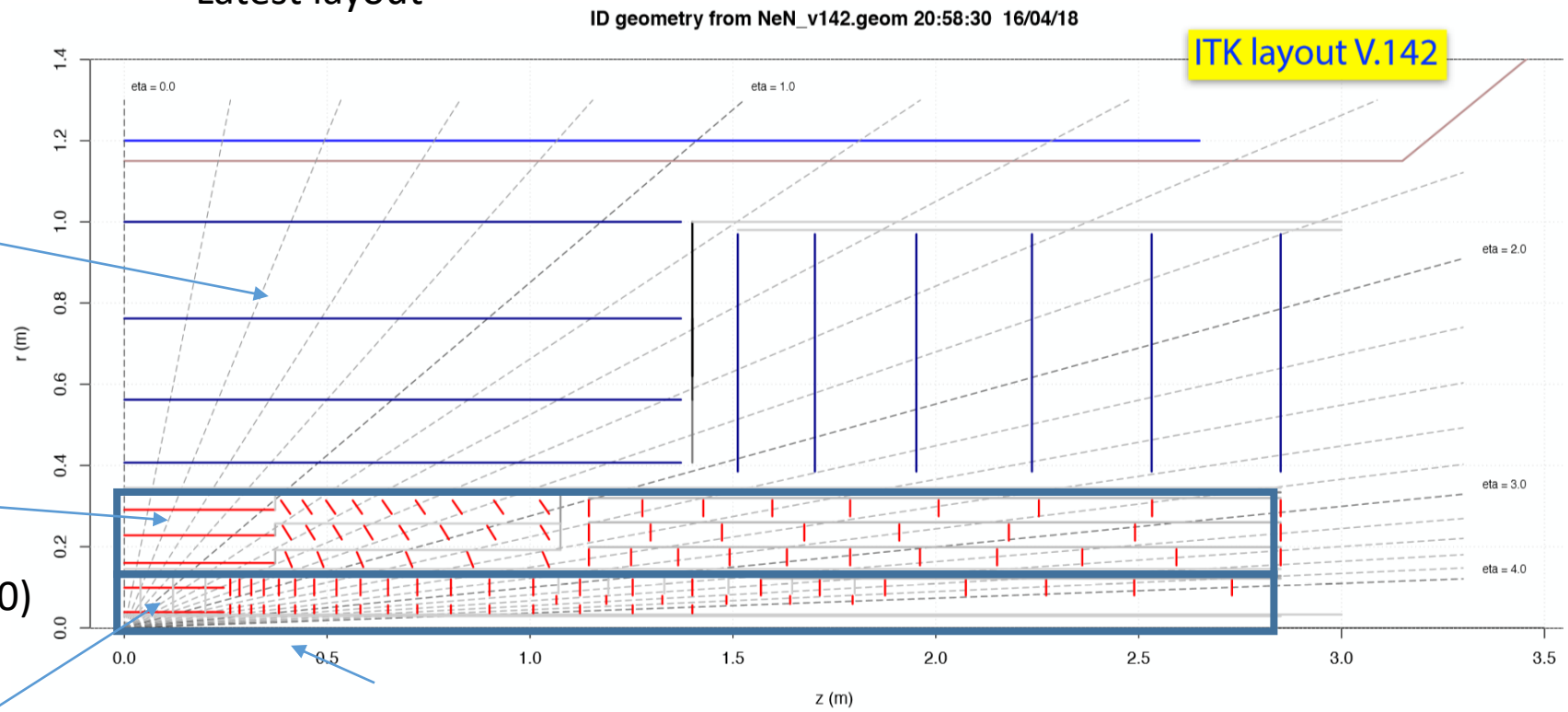
+ Complete redesign of TDAQ off-detector electronics

ITK

Replaces present tracker (IBL, Pixels, SCT, TRT)
IBL/Pixels/SCT not validated up to 3000 fb-1
TRT occupancy will reach 100%

Major change to the ATLAS detector !

Latest layout



Strip layers

Outer pixels (layers 2..4)
Barrel : cylindrical shells
End-Caps : Inclined quad modules
Planar technology
CMOS MAPS option for barrel layer 4
Pixel pitch under study (25×100 or 50×50)

Inner pixels (layers 0..1)
Barrel : cylindrical shells
End-Caps : coupled rings (three types of rings)
Planar and 3D technology
Pixel pitch under study (25×100 or 50×50)

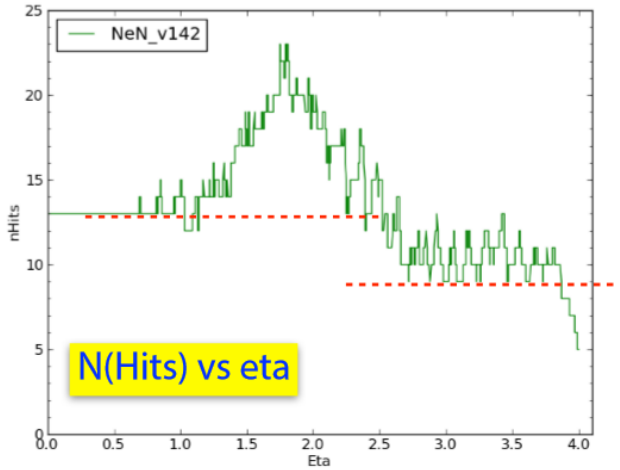
TDR published for the strips, under preparation for pixels

- Coverage up to η=4 (2.5 in present Inner Detector)
- ≈60 M channels, i.e. 10 times than today detector
- Total material budget ≈2 times lower than today detector

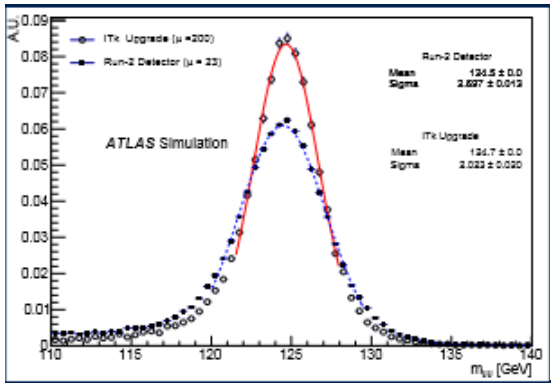
ITK Performance

Equal or better performance than present detector, in a much more difficult environment
>99% efficiency for muons with Pt>3 GeV, >85% efficiency for pions/electrons > 1 GeV, fake rate < 1%

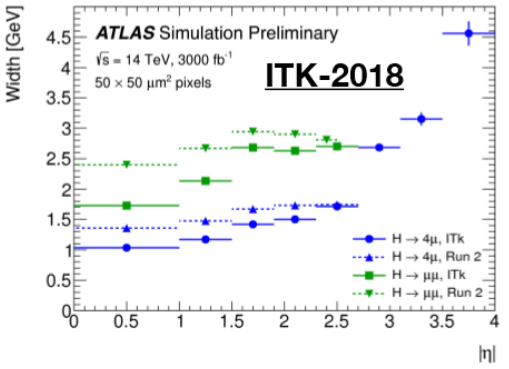
IDRes fast simulation performance studies

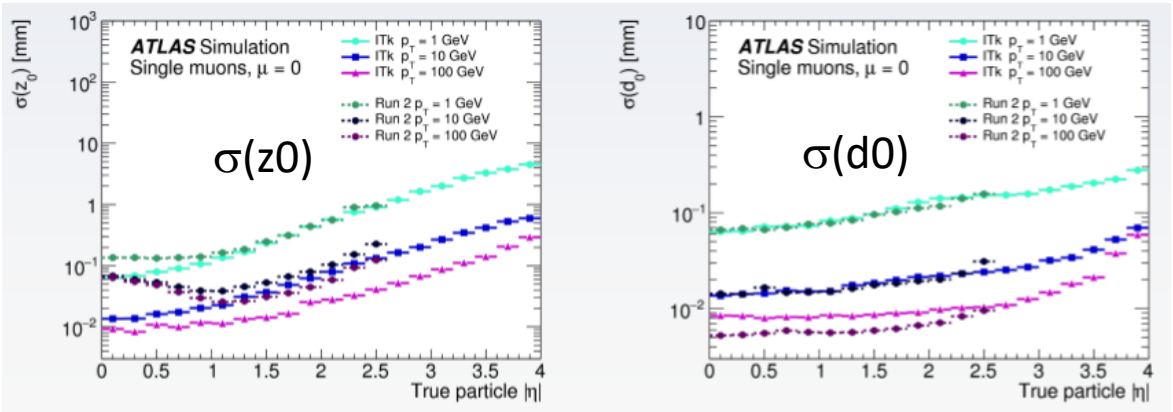


Signal resolution for H→μμ

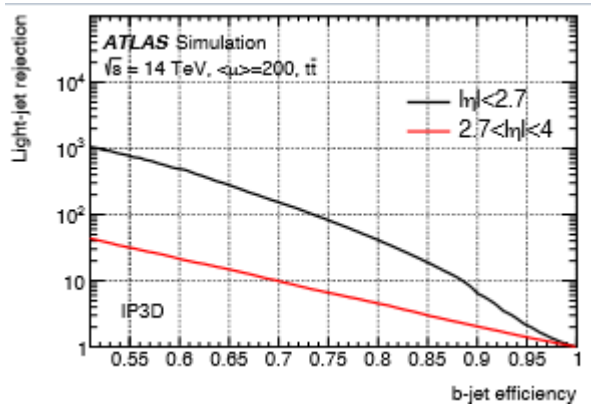


Signal resolution for H→4μ

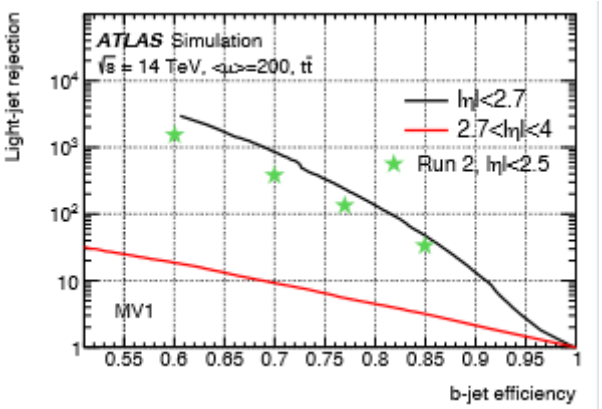




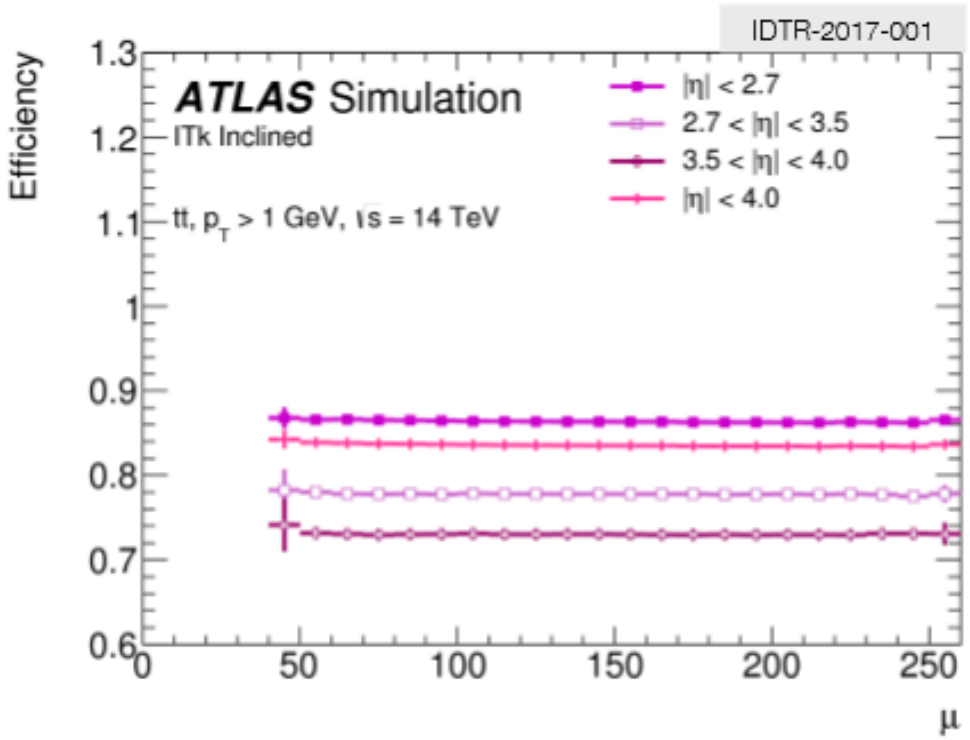
IP3D b-tagging perf. (ttbar)



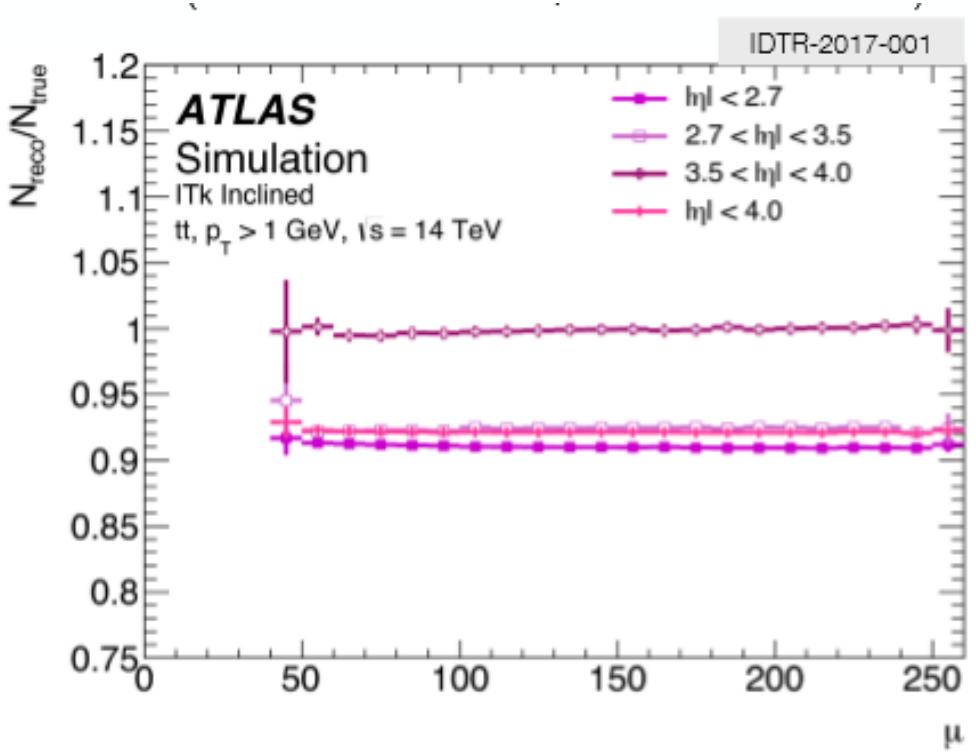
MV1 b-tagging perf.



ITK performance : <μ> dependance

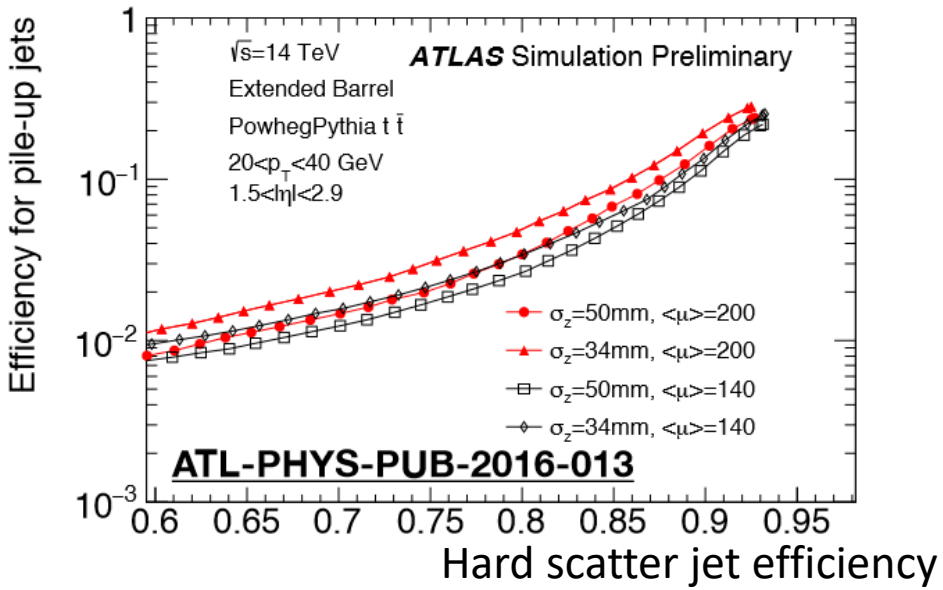


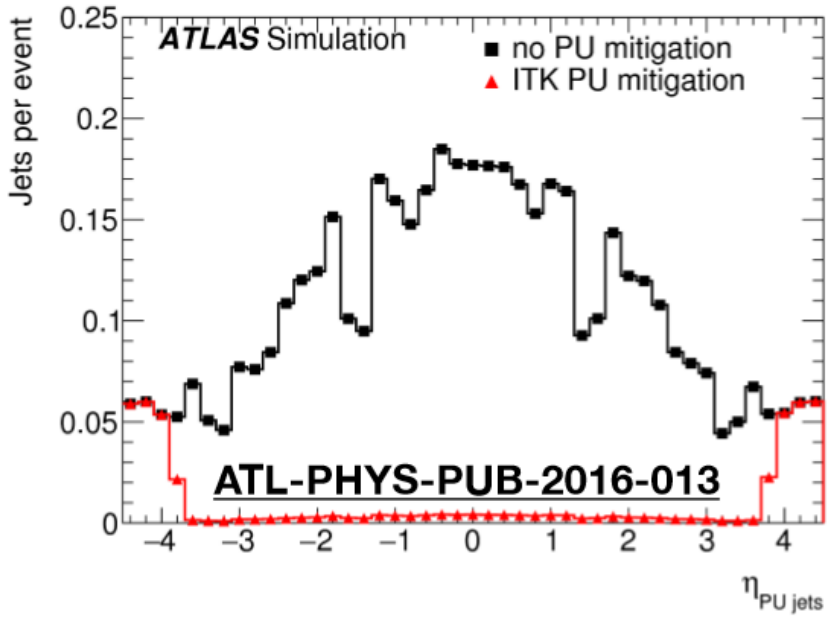
Tracking efficiency almost unchanged up to <μ>=250 for all η regions



Fake rate independant of <μ>, no problem with fakes up to <μ>=250

Jet/Vertex association





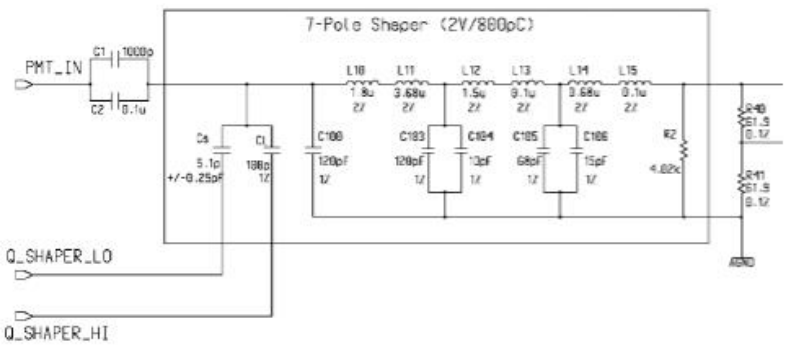
At <μ>=200,
the average number of pileup jets with pT>30 GeV per event is around 3

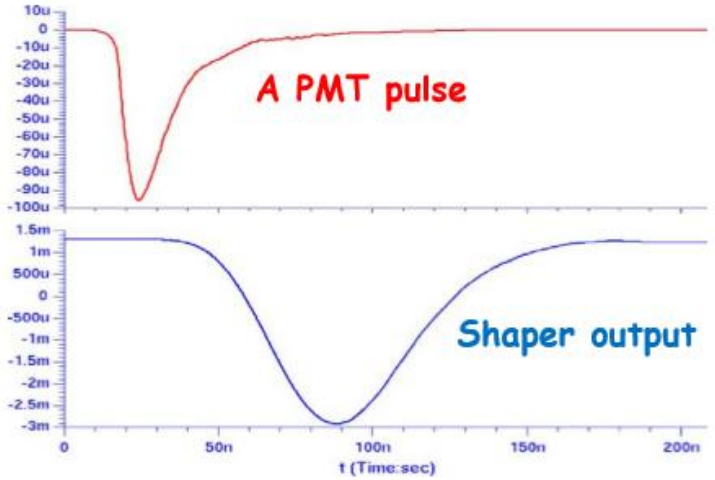
Track to vertex association is used to mitigate pileup

Tracking coverage to |η|<4 greatly reduces the number of pileup jets, achieving 2% pileup jet efficiency for 86% hard scatter jet efficiency for 20<pT<40 GeV

Tilecal : 3-in-1 Front-End signal processing

- Optimized version of the present version of the 3-in-1 board, option chosen to be implemented for the upgrade
- Seven pole shaper circuit (only passive components)
- Transforms the PMT pulse into a gaussian pulse, amplitude proportional to PMT signal total charge

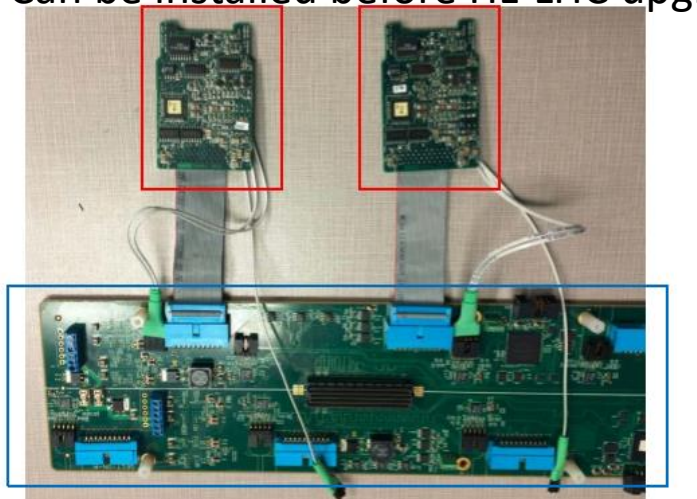




Upgrade digitization : 12 bits (COTS) ADC instead of 10 bits

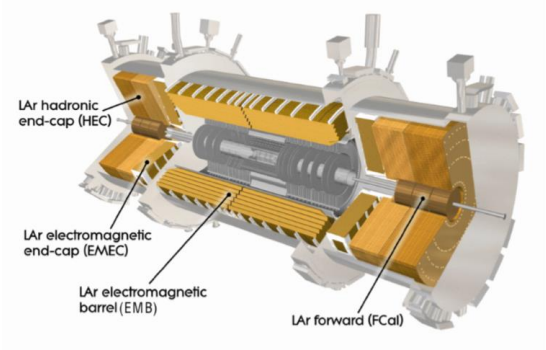
Compatible with present analog trigger (no longer used for Phase-2)

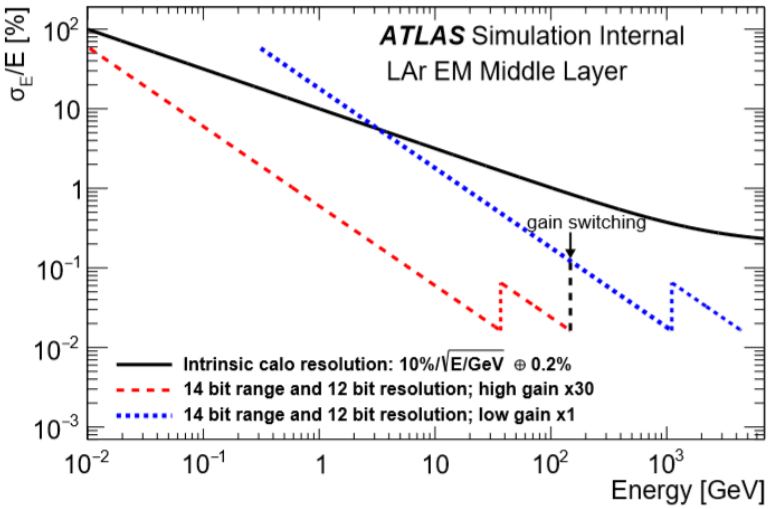
Can be installed before HL-LHC upgrade



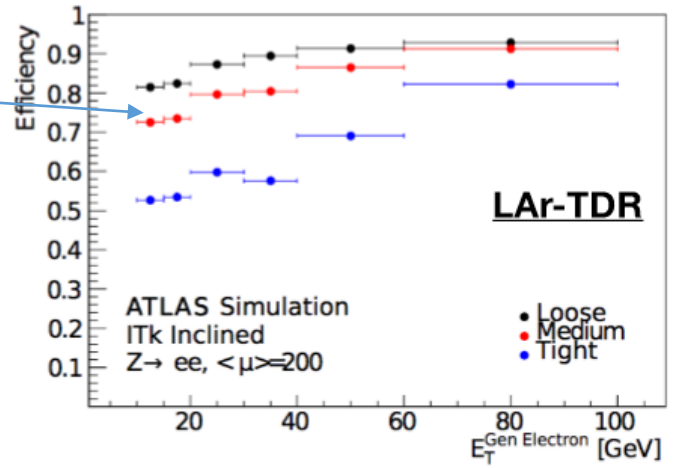
- Validated performance prototypes
- Slow integrator channel (used for Van Der Meer scans and Cs calibration) has very good sensitivity

LAr calorimeter Phase-2 upgrade

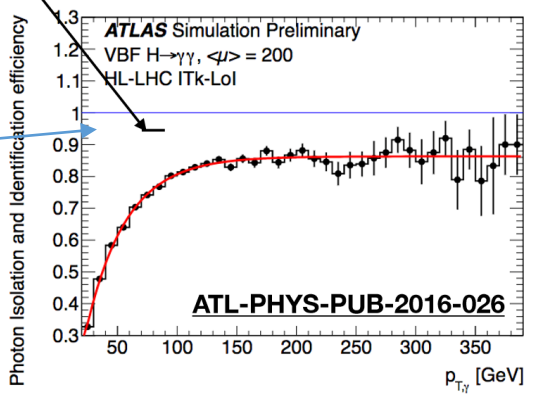




- Electrons
  - Rejection of light jets ranges from 600 to 3000 for the Loose to Tight working points
  - Mutivariate techniques should improve performance (as for Run-2, factor 2 to 6)
  - Reduced ID material reduces Bremsstrahlung and conversions
- Photons
  - Cut-based ID should be improved in the future using more elaborate techniques



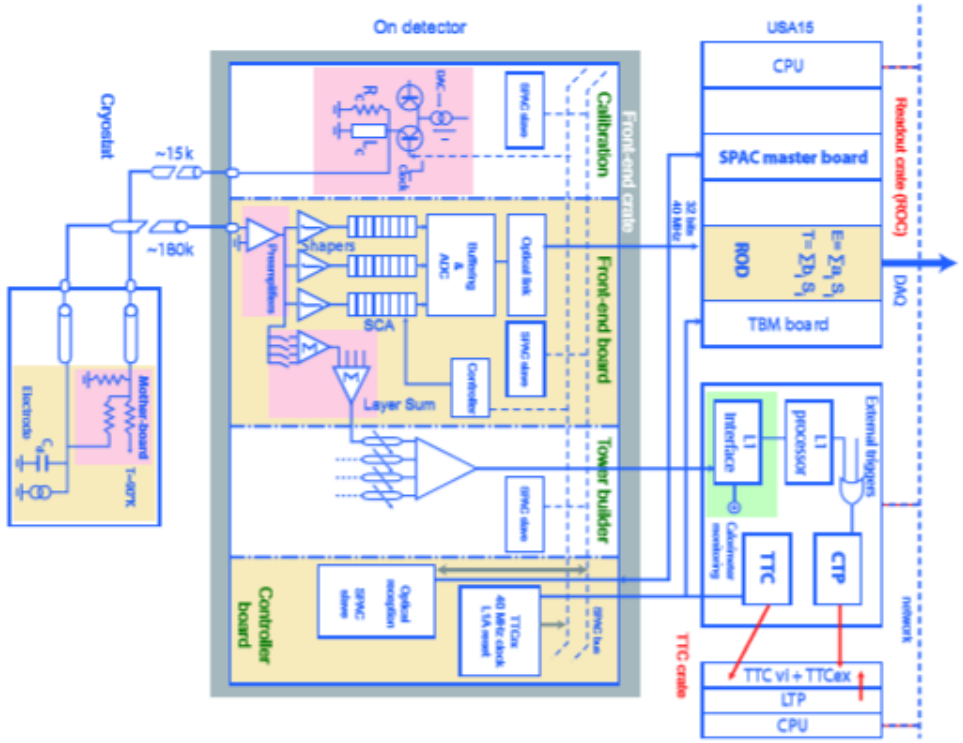
2015 Performance



- Analog dynamic range : 16-17 bits
- Keep present analog processing philosophy : preamplifier + CR-RC2 bipolar shaping. Add adjustable shaping time constant
- Change digitization scheme from three gains/12 bits ADC to two gains/14 bit ADC (12 bits ENOB)
- All data digitized at 40 MSPS, sent off-detector for all bunch crossings→ full granularity available for trigger decision
- No on-detector pipelines

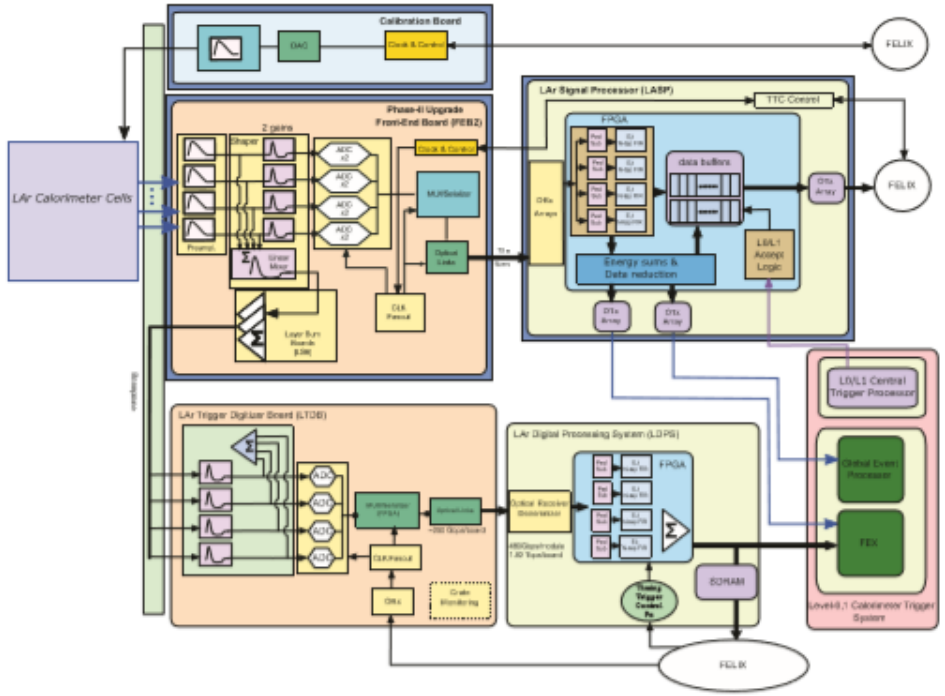
LAr Calorimeter readout system architecture

Present readout system



- Analog trigger sums
- Replaced in Phase-1 by digital trigger board (LTDB), with improved granularity
- Shaped signal stored in analog memories
- Digitized and sent to back-end after L1A decision

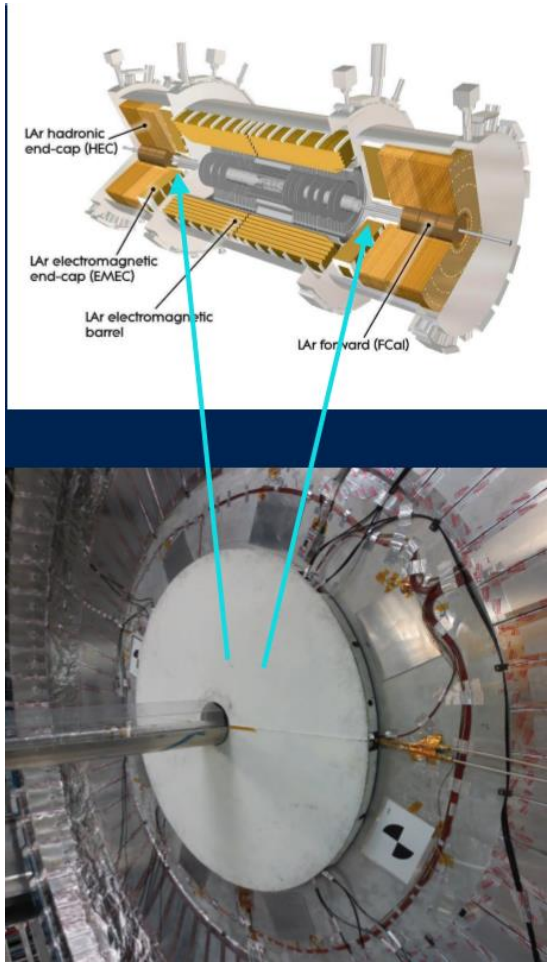
Phase-2 readout system

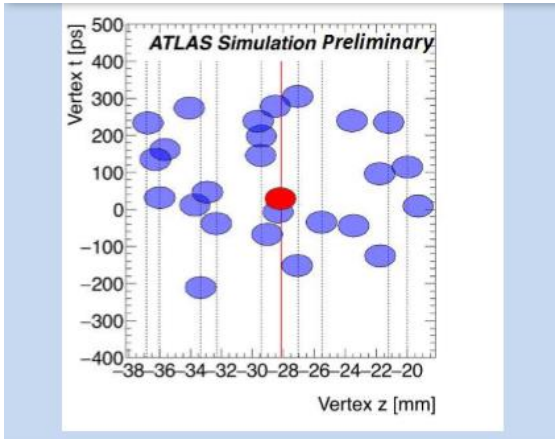


- Phase-1 LTDB trigger board still present, as Level-0 trigger and coarse (backup) readout system
- Shaped signal digitized on the fly and sent directly to Back-End

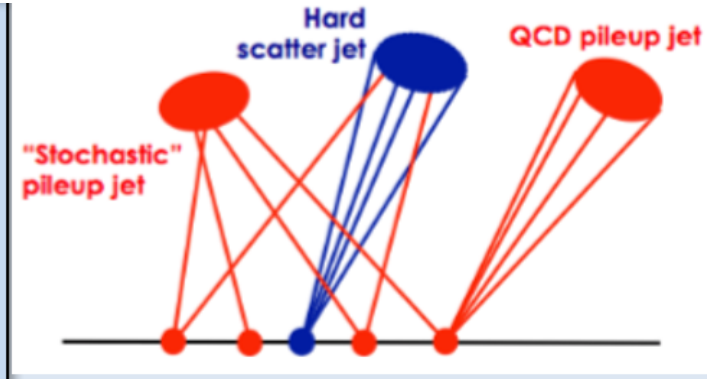
High Granularity Timing Detector (HGTD)

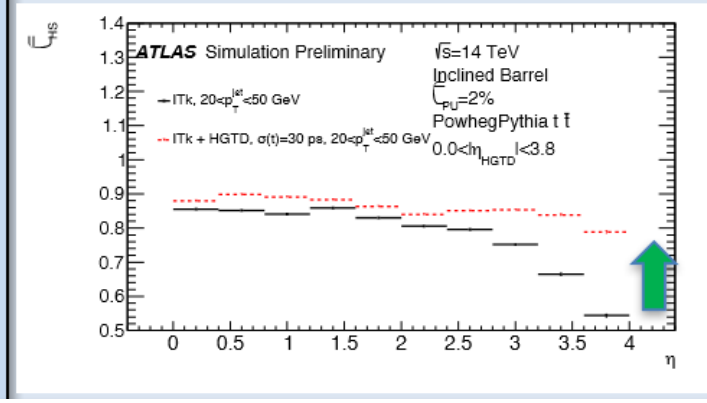
η Coverage : 2.4-4.2 (11 cm to 65 cm)
60 mm thick detection layer (LGADs)
Time resolution < 50 ps





- Performance of jet-vertex tagging techniques degrades with merging of vertices
  → Limited performances at high |η|, related to the worse z_0 track resolution
- The merged vertices can be resolved using timing information of the tracks from the HGTD
- *The performances of jet-vertex tagging techniques are improved at high |η|*





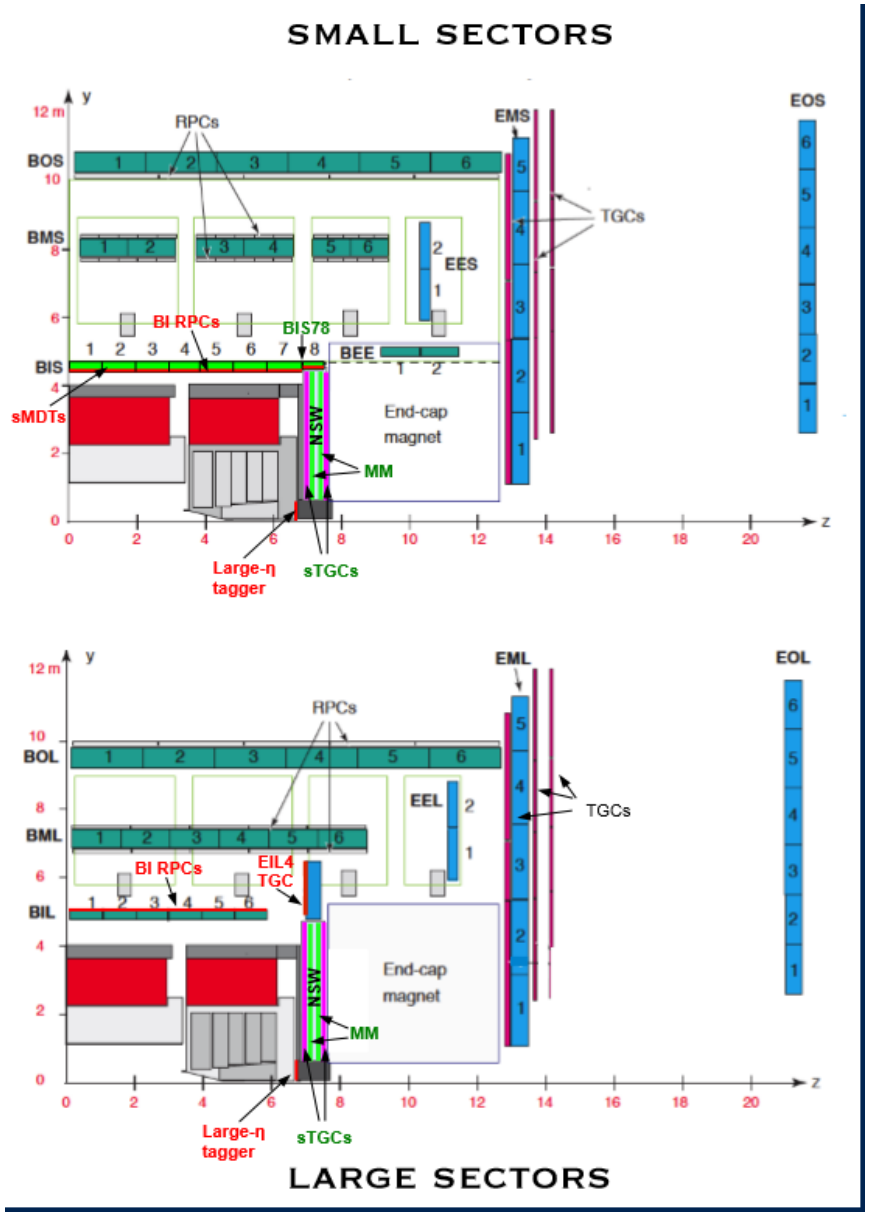
Muon system Phase 2 upgrade

- Reduce trigger fake rate over complete acceptance (barrel/end-cap)
- Increase geometrical coverage of the barrel region

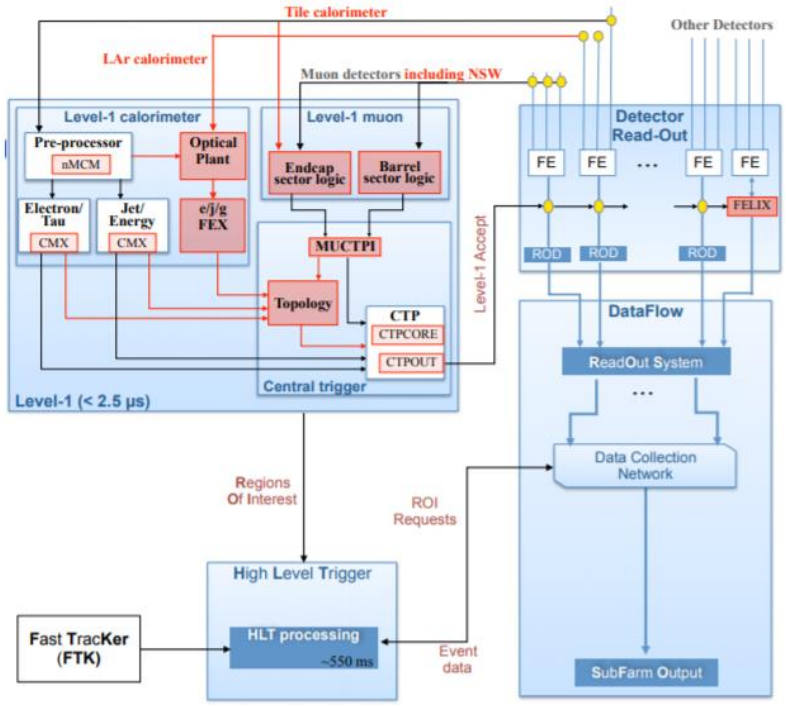
- New detectors
  - BIS MDT replaced by sMDT+RPC
  - New RPC mounted on top of existing BIL MDT

  - TGC EIL4

  - Large η tagger :
    - CMOS MAPS and various flavours of MicroMegas under study
    - Granularity needed : 1 mm^2 to 10 mm^2



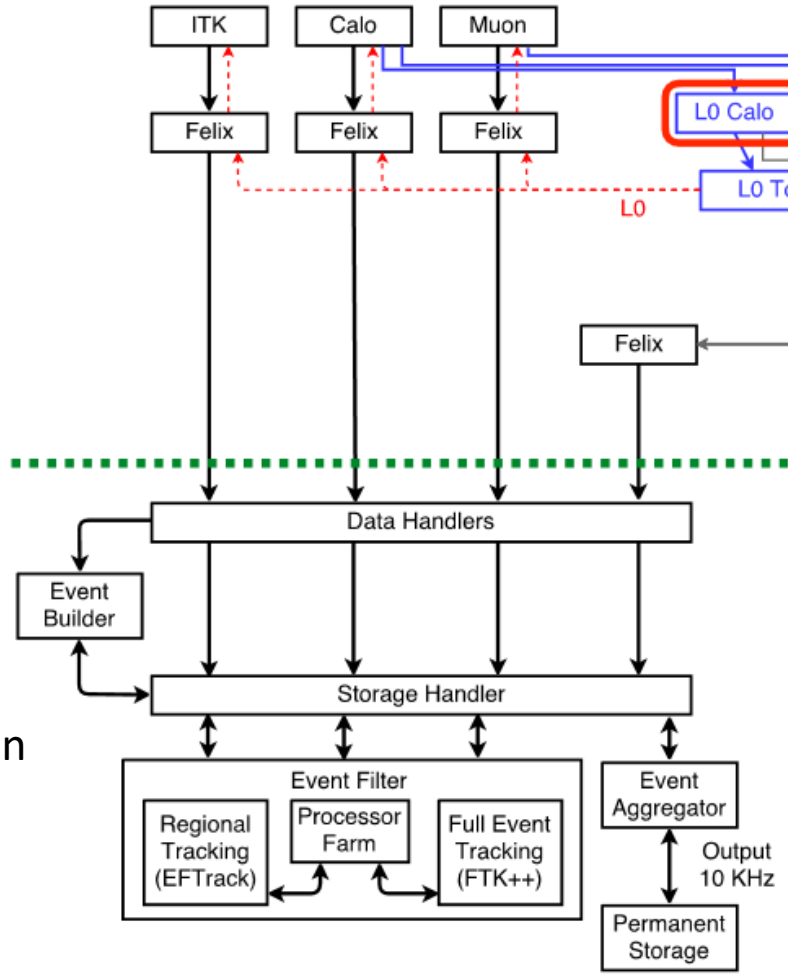
TDAQ Phase-2 Upgrade



Present L1 latency : 2.5 µs
Decision built from reduced granularity information
L1 rate : 100 kHZ

L2 rate : 3.5 kHz
L2 processing time : 40 ms
L2 seeded by RoI from L1

HLT rate : 200 Hz



Hardware Trigger

Level-0 trigger

1MHz / **10µsec**

CALO + MUON

40MHz → 1MHz

Full event information available to hardware L0

Conclusions

- ATLAS upgrade projects are targeted at making most benefit from luminosity increases
  - Detector performance in terms of resolution, background rejection similar or better than today detector
  - Calorimeter performance will benefit from material reduction induced by ITK
  - HGTD will provide new handles against pile-up
  - Particular attention given to minimize effects of pile-up (ITK, HGTD)
  - In addition, further gains to be expected from development of new algorithms