

3rd Workshop on LHCb Upgrade II

LAPP, 22 – 23 March 2017



A High Granularity Timing Detector for the Phase II Upgrade of the ATLAS experiment

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ON BEHALF OF THE ATLAS HGTD COMMUNITY



Annecy – March 22nd, 2018

Overview

Introduction

HGTD System

Sensors

Integration

Physics

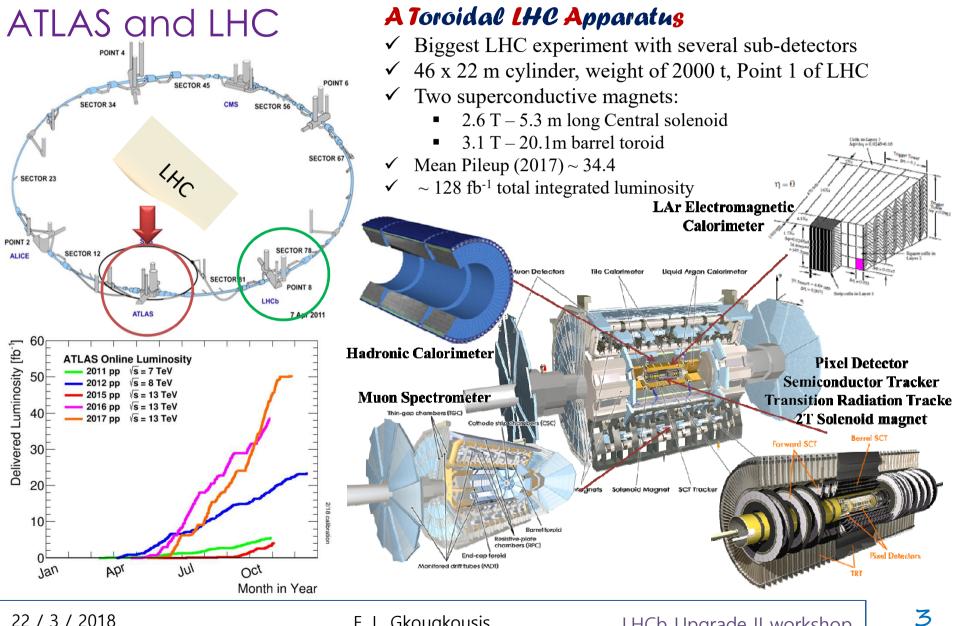
Luminometer

Schedule

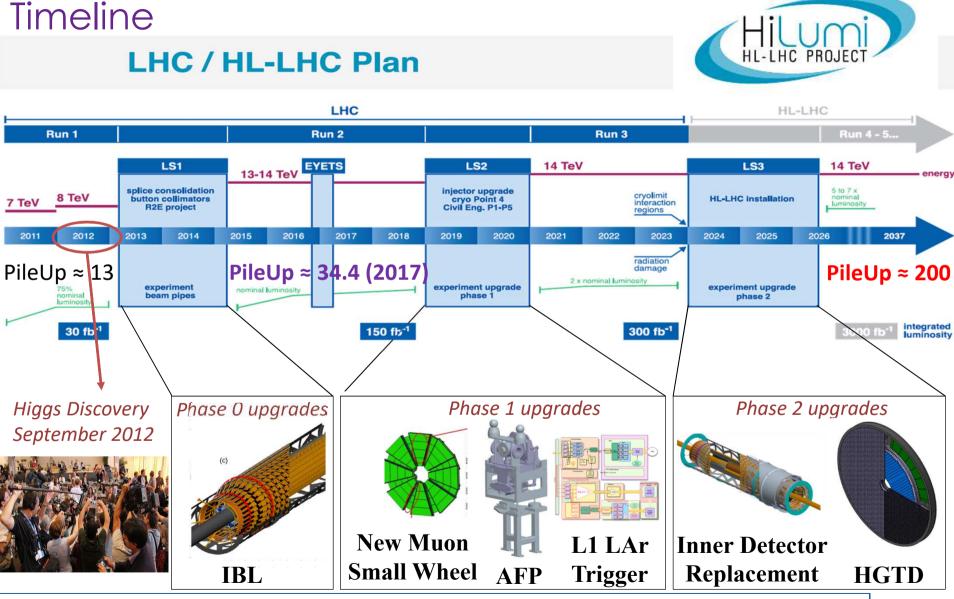
Conclusions

- ATLAS and HL-HLC
- Geometry and design
- Low Gain Avalanche Diodes
 - Electronics and services
 - Physics and Performance
 - Online and off-line luminosity estimation
 - Timeline and resources
 - Conclusions and Outlook

Introduction



ATLAS Phase II Upgrade



HL-LHC Conditions

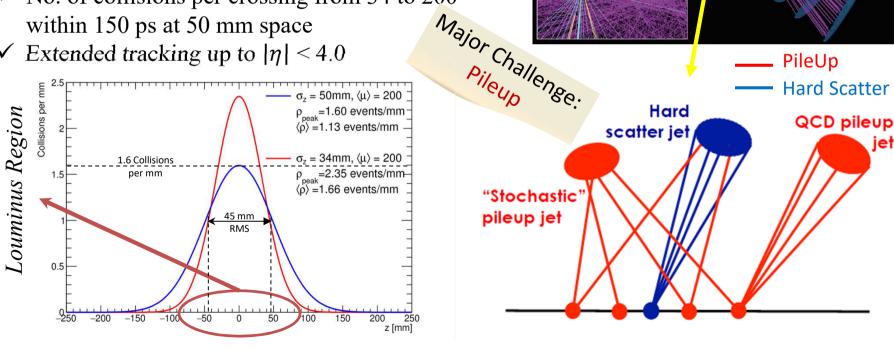
Pileup density

Luminosity

- ✓ Phase I: $< 2.2 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1} (300 \text{ fb}^{-1})$
- ✓ Phase-II : 7.5×10^{34} cm⁻²s⁻¹ (4000 fb⁻¹)

Conditions

- ✓ 14 TeV center of mass energy beam 6000primary tracks per event
- \checkmark No. of collisions per crossing from 34 to 200 within 150 ps at 50 mm space
- ✓ Extended tracking up to $|\eta| < 4.0$



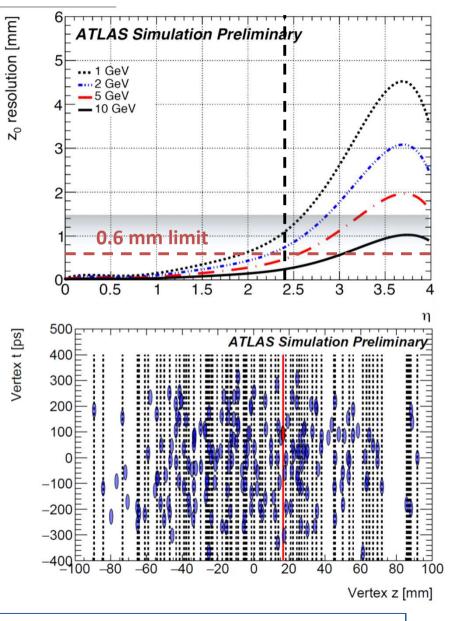
HL-LHC Conditions

Vertex Resolution

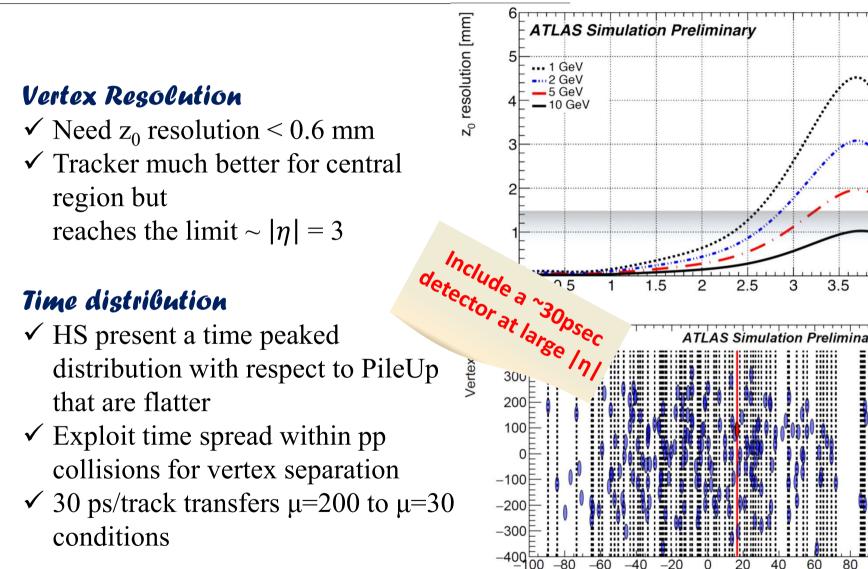
- ✓ Need z_0 resolution < 0.6 mm
- ✓ Tracker much better for central region but reaches the limit ~ $|\eta| = 3$

Time distribution

- ✓ HS present a time peaked distribution with respect to PileUp that are flatter
- ✓ Exploit time spread within pp collisions for vertex separation
- ✓ 30 ps/track transfers µ=200 to µ=30 conditions



HL-LHC Conditions

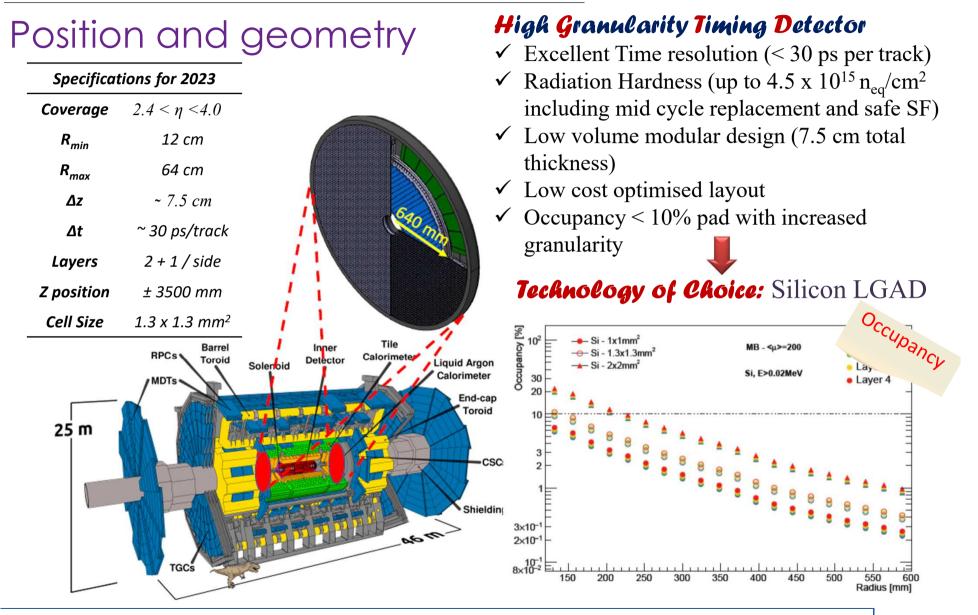


100

Vertex z [mm]

7

•HGTD System

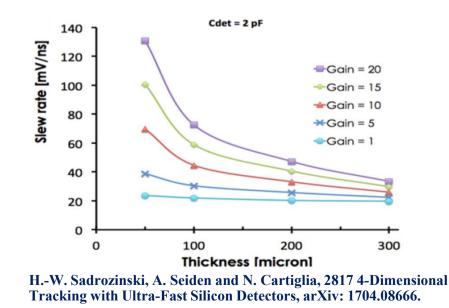


• Sensors

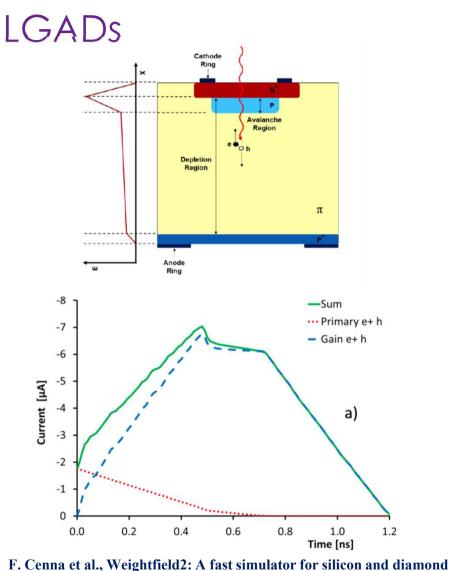
Timing Concepts TDC_{bin} V_{thr} lrise σ^2_{elec} $\overline{S/t}_{rise}]_{RMS}$ /NConversion **Jitter** Time walk time $\left[\frac{V_{th}}{S/t_{rise}}\right]_{RMS} \propto$ Where: S signal dV N noise $\left[\frac{dt}{dt}\right]_{RMS}$ V_{th} CFD threshold $\frac{t_{rise}}{dV/dt} \approx \frac{1}{dV/dt}$ \mathbf{t}_{rise} rise time Jitter [ps] Test Bench using Ctest pulse Jitter at 10 fC Simulation: LGAD pulse Simulation: Ctest pulse Dependence on Japacitance 20 2 3 7 5 6 Cd [pF]

 $\sigma_{tot}^{2} = \sigma_{elec.}^{2} + \sigma_{Landau}^{2} + \sigma_{Clock}^{2}$ Fast time resolution:

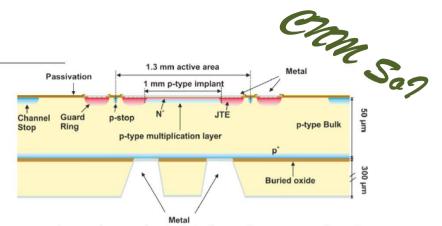
- ✓ Maximize slope (large fast signals)
- ✓ Correct time walk with Constant fraction discriminator
- ✓ Minimize noise to minimize jitter
- ✓ Estimated clock jitter ~ 5 ps
- \checkmark Thin silicon sensors with internal gain



• Sensors

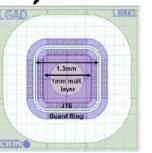


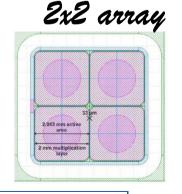




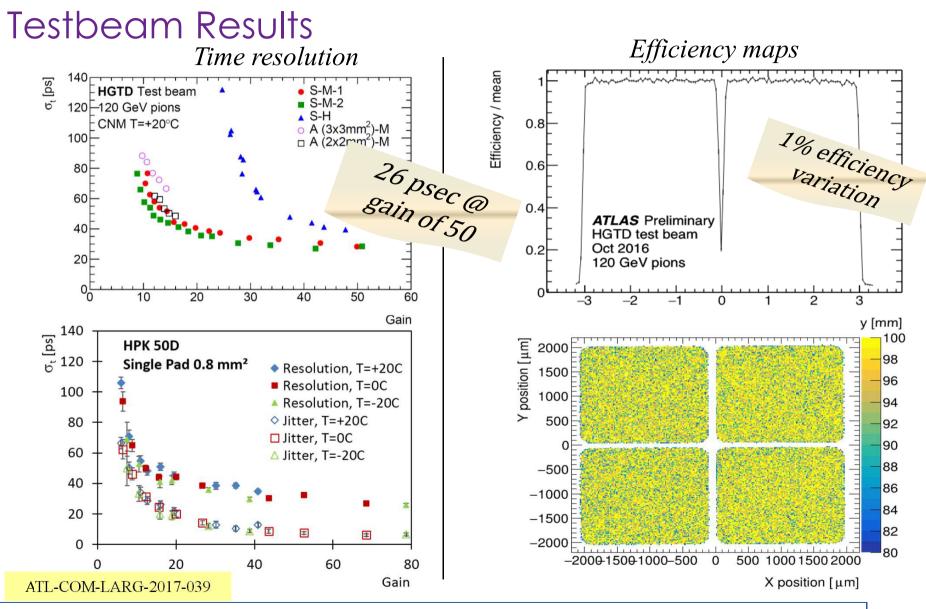
- ✓ Developed and initial R&D productions at CNM (Barcelona)
- ✓ Secondary p implant introducing moderate gain HPK, CNM, FBK produced sensors
- ✓ 50 μ m thickness on 250 μ m support wafer
- ✓ Different implantation doses including Gallium and Carbon
- ✓ Various structures including:
 - ✓ Pad diodes of $1.3 \text{ x} 1.3 \text{ mm}^2$
 - 2×2 arrays of 1 x 1 mm² pad

Single Diode

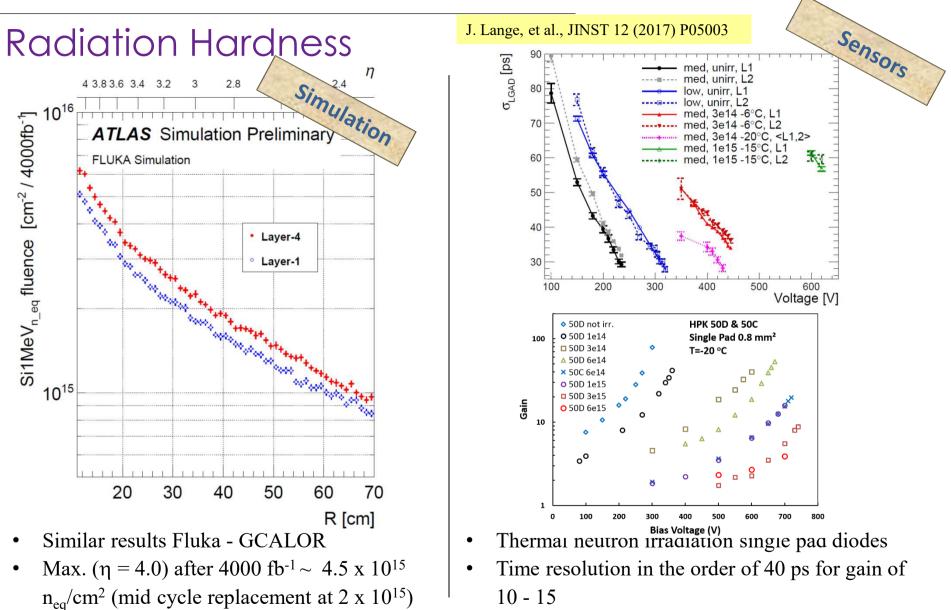






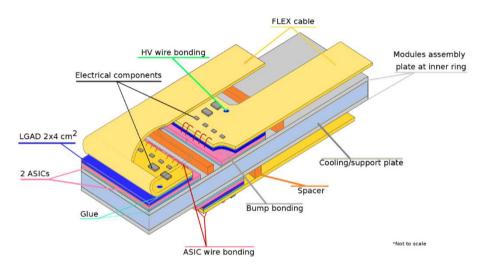


• Sensors



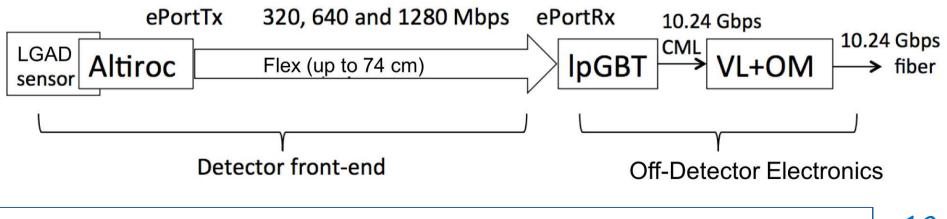
Integration

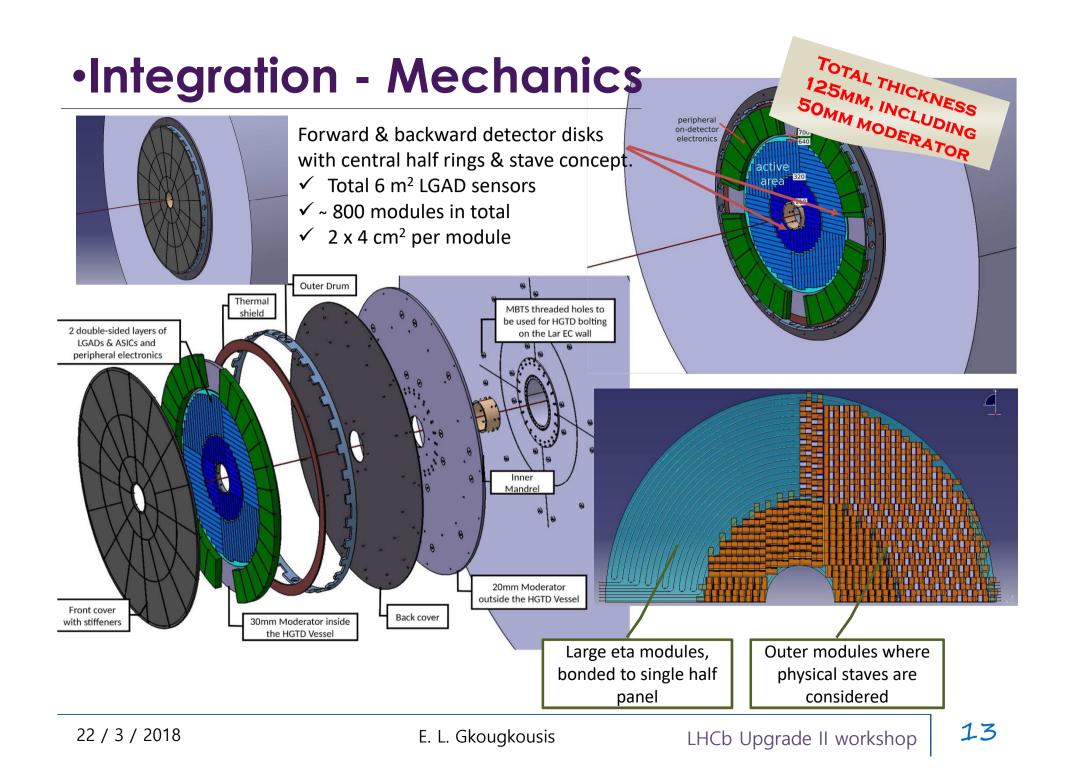
ASIC and Signal extraction



ATLAS LGAD Timing Integrated ReadOut Chip (ALTiRoC)

- ➢ 2 x 2 cm die, TSMC 130µm technology
- > Bump-bonded to $2 \times 4 \text{ cm}^2$ sensors
- Single pixel readout, 225 channels/ASIC
- Readout Rate:
 - > 1 MHz detailed hit info after L1
 - 40 MHz number of hits on outer radii for luminosity estimation
- > 25 ps estimated time resolution
- Wire-bonded to capton flex

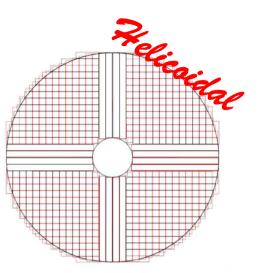


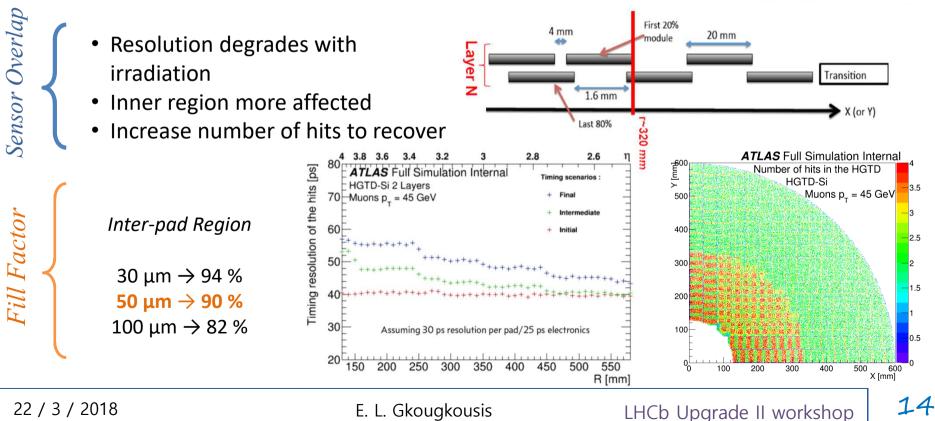


Integration

Layout Optimization

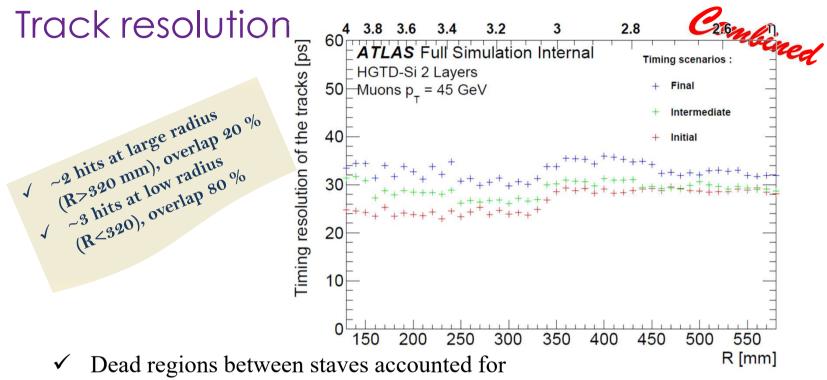
Efficiency		Geometry	
Events with 0 hits	0.7 %	Longest Stave	546 mm
Fraction of events at x or y = 0	52 %	Coverage	91.8 %
		18 staves per quadrant	





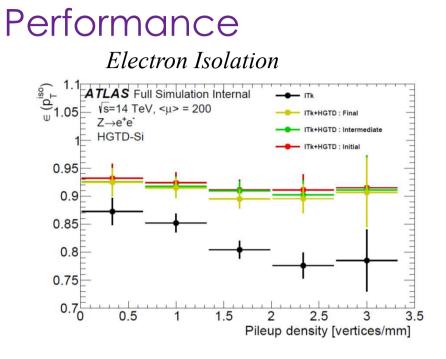
Stave layout

Physics and Performance



- 4 mm for 80 % overlap
- 16 mm for 20 % overlap
- ✓ Track resolution always < 40 psec
- ✓ 3 different timing scenarii
 - Initial : 30 psec per pad and 25 psec for electronic
 - ➤ Intermediate : timing resolution after 2000 fb⁻¹ (with inner layer replacement)
 - ➢ Final : timing resolution after 4000 fb⁻¹

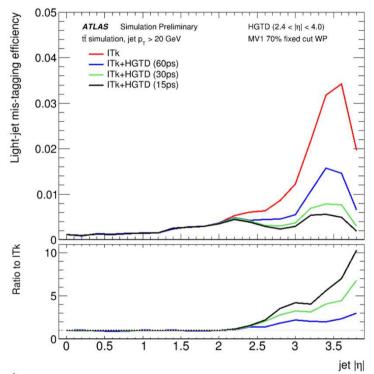
Physics and Performance



- ✓ 2 layers/side with overlap
- ✓ Average efficiency ~93% at all cases
- ✓ ITk only average efficiency ~83%

Performance plots currently been updated for new geometry

B-tagging performance



- 100% Efficient does not use η parametrization nor fill factor
- ✓ Initial assumes 30psec across the whole detector
- ✓ Slight degradation between initial and final, though larger loss from hit efficiency

Physics and Performance

Some EW channels

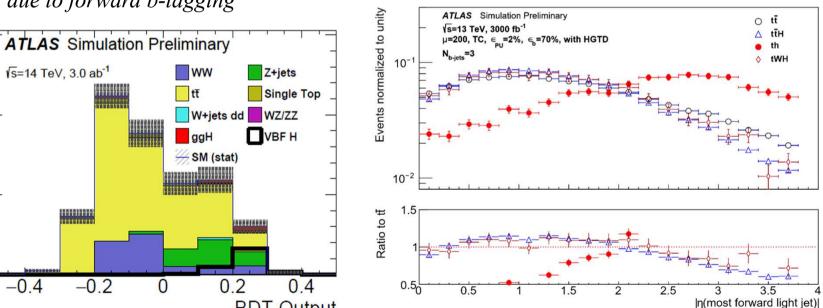
 $qqH \rightarrow qqWW^* \rightarrow qq + ev_e \mu v_\mu$

- 8% relative improvement
 - 43% background rejection
 - 3% PU efficiency \geq
 - BDT analysis \triangleright
 - Top dominated background *due to forward b-tagging*

 $tH(\rightarrow bb)$

11% relative improvement

States -



٢

-0.4

Events

3000⊢

2000

1000

E. L. Gkougkousis

BDT Output

VBF processes

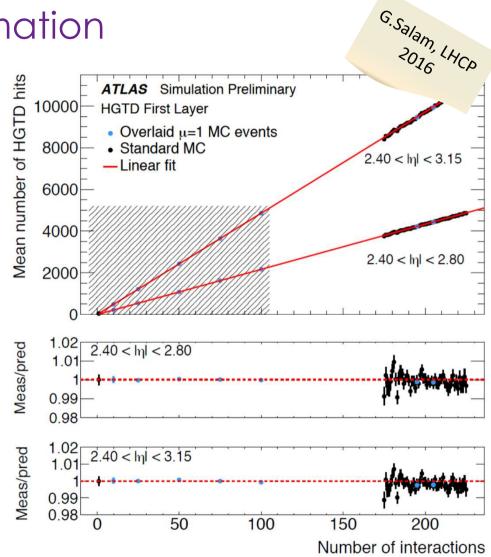
under investigation

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•HGTD as Luminometer

On line and off-line estimation

- linear dependence of number of hits on number of interactions
 - Count hits in the region of 320 mm < R < 640 mm</p>
 - 0.1% expected statistical uncertainty for 1 sec integration time
 - Low systematics
 - Out of time sideband subtraction
 - Hit count per ASIC and BCID
 - On-line Estimation
 - 40MHz readout for real time estimation
 - Provide per BCID interactive estimate
 - Total latency of 440 ns (100 ASIC+ 340 ns fiber)



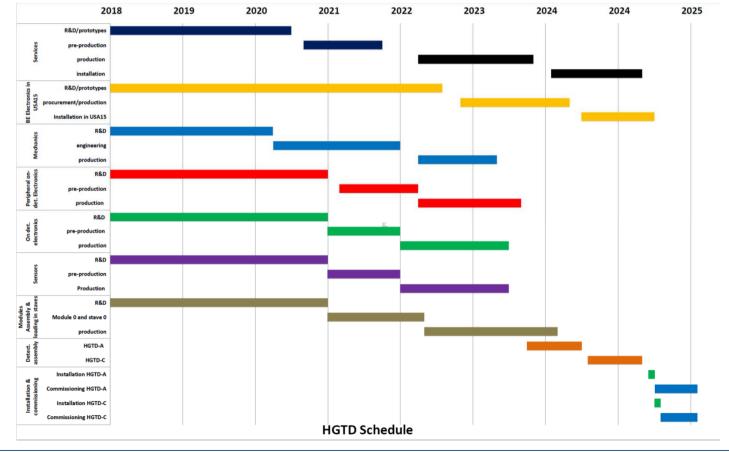
Schedule

Important mile-stones

- ▶ 2018 2020:
- ▶ 2021 2024:
- ▶ 2025 2026:

Sensor, ASIC, electronics and services RnD Fabrication and module assembly





Conclusions and Outlook

Sensors, ASIC, Integration and Radiation Hardness

So far....

Physics

- $\checkmark\,$ Very promising results for pileup rejection in the high η region where VBF and exotics will benefit
- \checkmark High jet single purity for invisible searches

Sensors

- ✓ 26 ps time resolution for single un-irradiated 1.3mm² diodes
- $\checkmark~99\%$ uniformity with low inefficiencies in the inter-pad regions
- ✓ Operations up to 6e15 n_{eq} /cm², meeting the radiation hardness requirements
- \checkmark Any timing degradation due to early breakdown

Integration

- ✓ First ASIC prototypes successfully assembled at IFAE and tested in HGTD September CERN testbeam
- ✓ Validate full ASIC design and expect first prototype at the last quarter of 2018

