Monolithic Active CMOS Pixel Sensors: ASICs with Integrated High Precision Particle Detection

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Contents

- Introduction on Monolithic CMOS Pixel Sensor (CPS)
- On-going R&D relevant for high luminosity pp collisions
- *Remarks/Questions addressing the specific case of the LHCb tracker*
- Summary & Outlook

SOURCES : Talks at TWEPP-17, Hiroshima-17, CERN Workshop on Instrument. Techno. (16.03.18), LHCb meeting (16.03.18) SLIDES : Ch. Parkes, M. Needham, W. Snoeys, T. Kugathasan, D. Wiedner, H. Pernegger, ...

Origin of CMOS Pixel Sensors

- CMOS Pixel Sensors are derived from ASICS

 Application-Specific Integrated Circuits
 - ASICs populate every day's life: e.g. credit cards,
 - PC, cell-phones, cars, washing machines, ...
 - \Rightarrow industrial mass production item (world revenue \sim several 100 billions USD/year)
 - key element: MOSFET transistors & conductive traces
 printed in **Silicon** (usually)

- C.M.O.S. = Complementary Metal Oxyde Semi-conductor
 - widespread technology for constructing integrated circuits used in microprocessors, microcontrollers, memories, etc.



Substrat type P pour MOSFET canal N Substrat type N pour MOSFET canal P



CMOS Technology

- CMOS fabrication mode :
 - * μ circuit lithography on a substrate sliced from a crystal ingot (or *boule*)
 - * proceeds through reticules (e.g. 21x23 or 25x32 mm²) organised in wafers

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CMOS Pixel Sensors: Main Features

- Prominent features of CMOS pixel sensors :
 - high granularity \Rightarrow excellent (micronic) spatial resolution
 - $_\circ\,$ signal generated in (very) thin (15-40 μm) epitaxial layer
 - $\hookrightarrow\,$ resistivity may be \gg 1 k $\Omega\cdot cm$
 - $_\circ\,$ signal processing $\mu\text{-circuits}$ integrated on sensor substrate
 - \Rightarrow impact on downstream electronics and syst. integration (\Rightarrow cost)
- CMOS pixel sensor technology has the highest potential :
- ⇒ R&D largely consists in trying to exploit potential at best with accessible industrial processes
 - → manufacturing param. not optimised for particle detection:
 wafer/EPI characteristics, feature size, N(ML), ...
- Read-out architectures :
 - 1st generation : rolling shutter with analog read-out (twin-well)
 - 2nd generation : rolling shutter with // read-out & end-of-column discrimination (twin-well)
 - 3rd generation : data driven read-out with in-pixel discrimination (synchronous/asynchronous)



Quadruple-Well

Motivation for Using CMOS Pixel Sensors

- CPS development triggered by need of very high granularity & low material budget
- Applications exhibit(ed) much milder running conditions than pp/LHC
 - \Rightarrow Relaxed speed & radiation tolerance specifications
- Increasing panel of existing, foreseen or potential application domains :
 - Heavy Ion Collisions : STAR-PXL, ALICE-ITS, CBM-MVD, NA61, FOCAL,
 - ∘ e⁺e[−] collisions : ILC, BES-3, ...
 - Non-collider experiments : FIRST, NA63, Mu3e, PANDA, ...
 - High precision beam telescopes adapted to medium/low energy electron beams :
 - \hookrightarrow few μm resolution achievable on DUT with EUDET-BT (DESY), **BTF-BT (Frascati)**, ...
 - $_\circ~$ RECENTLY: high rate pp collisions $\Rightarrow~$ addressing the pb of speed and radiation hardness

Evolution of Radiation Tolerance and Hit Rate Capability

	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n _{eq} /cm²]	10 ¹²	10 ¹³	<10 ¹²	10 ¹⁵	10 ¹⁶	10 ¹⁵⁻ 10 ¹⁷
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad
Hit rate [MHz/cm ²]	0.4	10	<0.3	100-200	2000	200-20000

Alpide Sensor

MALTA & Monopix & Atlas Pix Sensor

- Evolution of process characteristics:
 - starting material: epitaxy thickness and resistivity
 - o doping profile: from twin-well to quadruple well with burried N-doped brane
 - feature size and nb of Metal. Layers
- Today's accessible CMOS processes allow considering pp collisions at LHC
 - \hookrightarrow market drives CMOS technology in a direction complying with HEP needs

Radiation Tolerance Achieved by 2013 (AMS-0.35 process)

Reminder: radiation tolerance may be enhanced in various ways: sensing node density
 (= pixel pitch), operating temperature, epitaxy resistivity & depletion, signal processing speed, etc.

Main Components of the Signal Processing Chain

- Typical components of read-out chain :
 - AMP : In-pixel low noise pre-amplifier
 - Filter : In-pixel filter
 - **ADC** : Analog-to-Digital Conversion : 1-bit \equiv discriminator
 - Zero suppression : Only hit pixel information is retained and transfered
 - Data transmission : O(Gbits/s) link implemented on sensor periphery
- Read-Out in general data-driven:
 - Synchronous: clock distributed over pixel array \Rightarrow Power consumption !
 - Asynchronous : no clock running over pixel array \Rightarrow increased design complexity ?
- Trade-off between conflicting parametres:
 - \rightarrow pixel dimensions (precision, sensing node density), speed and power, ...

 \rightarrow exploit relaxed constraints to privilege the most demanding ones !

• Thin sensitive volume \Rightarrow small signal \Rightarrow VERY LOW NOISE signal processing circuitry

Various In-Pixel Circuitry Approaches

- Monolithic CPS integrate the complete signal creation and processing chain :
 - ⇒ SPECIFIC GLOBAL OPTIMISATION for each dedicated application
- Sensing Node \equiv key element
- Large electrodes

Small electrodes

- + μ -circuits inside coll. well
- + shortened drift distance
- + extended lateral depletion
- sensing node capacitance
- \Rightarrow ENC, gain, signal rise, power
- risk of X-talks betw. digital & analog $\mu {\rm C}$

- + $\mu\text{-circuits}$ outside coll. well
- + small capa. \Rightarrow high SNR, fast signal
- + separate ana. & digi. μ circuits
- sizeable drift distance
- \Rightarrow calls for process modif. (rad. tol.)

 "Burried" electrodes (SOI)

- + $\mu\text{-circuit}$ & sensing node in separate layers
- + adaptable sensitive vol.

⇒ special design to overcome radiation induced charge build up at interfaces

TowerJazz 180 nm Modified Process

- Modified process developed in collaboration of CERN with TJ foundry, originally developed in context of ALICE ITS
- Adding a planar n-type layer significantly improves depletion under deep PWELL
 - Increased depletion volume \rightarrow fast charge collection by drift
 - better time resolution reduced probability of charge trapping (radiation hardness)
 - Possibility to fully deplete sensing volume with no significant circuit or layout changes

Granular Monolithic CPS for LHC pp Running Conditions

Chip name	Technology	CE Size*	Pixel size [µm ²]	R/O architecture	Staust	
aH18	AMS 180nm	Large	56 × 56	Asynchronous	Measurements	
Malta	TowerJazz	Small	36 × 36	Asynchronous		
TJ Monopix	180nm	Small	36 × 40	Synchronous	Submitted	
LF Monopix	LFoundry 150 nm	Large	50 × 250	Synchronous		
Coolpix		Large	50 × 250	Synchronous	Measurements	
LF2		Large	50 × 50	Synchronous		
10mm * CE Size = Collection Electrode Siz Image: Collection Electrode Siz Image: Ce Size Image: Ce Size Image: Ce Size Image: Ce S					mm ²	
ATLAS Pix 8	MuPix	MONO	PIX, LF2 & COOLPIX	MONOF	PIX & MALTA	
AMS 180 nr	m	Lfound	dry 150 nm	TowerJa	azz 180 nm	

ATLAS Inner Tracker Upgrade Phase 2

Specifications for the ATLAS Inner Tracker Upgrade Phase 2 (HL-LHC)

	ALICE-LHC	ATLAS-HL-LHC	
		Outer	Inner
Required Time Res. [ns]	20 000	25	
Particle Rate [kHz/mm ²]	10	1000	10 000
Fluence [n _{eq} /cm²]	>10 ¹³	10 ¹⁵	10 ¹⁶
lon. Dose [Mrad]	0.7	50	1000

- ✓ Time resolution: fast collection by drift (<< 25 ns) → larger depletion
- ✓ High particle rate: short dead time (< 1 us)</p>
- ✓ Tolerance to non-ionizing radiation (displacement damage):
 fast collection by drift to decrease signal charge trapping probability → larger depletion
- ✓ High Q/C for power optimization:
 - High Q : less charge sharing (small cluster) → larger depletion
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Large CPS Fabricated Recently for the ATLAS Inner Tracker

Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers :MALTA & TJ-Monopix

MALTA

Asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix. No clock distribution over the pixel matrix -(power reduction)

TJ-Monopix

Synchronous readout architecture. Uses the well-established column drain readout architecture (experience from LF-Monopix design)

? Dead time ?

Test Results of Investigator Pixel Array Prototype

High-Voltage Monolithic CMOS Pixel Sensor

- High Voltage Monolithic Active Pixel Sensors
- HV-CMOS technology
- N-well in p-substrate
- Reversely biased ~85V
 - O Depletion layer
 - Charge collection via drift
 - Fast <1 ns charge collection</p>
 - Thinning to < 50 μ m possible
- Integrated readout electronics

by Ivan Perić I. Perić, A novel monolithic

pixelated particle detector implemented in high-voltage CMOS technology Nucl.Instrum.Meth., 2007, A582, 876

HV-CMOS: Test Results of MuPix-7 and -8

- First large scale sensors : MuPix-7 and MuPix-8:
 - process: AMS-H18
 - triple well, no epitaxy
 - $_{\circ}\,$ thinned to 50 μm
 - light doping substrate:
 - $ho \sim$ 20/80 $\Omega \cdot$ cm for MuPix-7/-8
 - $_{\circ}\,$ depletion depth: \simeq 9/15 μm for MuPix-7/-8

0.85

0.8

0.75

0.7

0.65

0.6

0.55

0.5

- \circ pixels : 80 x 81 μm^2
- $_{\circ}\,$ fluence: 1.5 $\cdot 10^{15} \mathrm{p/cm}^{2}$ (CERN-PS)
- $_{\circ}~T_{\it op}\sim 10^{\circ}C$????
- response to 4 GeV e^+ (DESY) 0.95
- non-ion. radiation tolerance
 after 1 yr of anealing

LHCb Tracker: Non-Uniform Radiation Load over Detection Area

- Smallest radii:
 - radiation hardness is a priority
 - ATLAS oriented CPS may be appropriate
- Medium and Large radii:
 - radiation hardness is much less demanding
 - o how to exploit this relaxed requirement ?
 - power saving becomes the priority:
 - pitch > 50 μm complying with good det. eff. (small pixels may be grouped in larger super-pixels)
 - reduce in-pixel current?
 - etc.

Time Remaining for Dedicated Sensor Realisation

• 2 different time scales

- o for 2026 : how much can one depart from designs currently under development ?
- o for 2031 : time sufficient to develop a specific sensor, possibly based on new CMOS technology & concept

System Integration Aspects

Prominent performances driving parametres for high-resolution trackers

- track finding in dense environnement
- track momentum reconstruction (impacts track origin rec.)
- track origin (esp. for high P), if material budget low
- rejection of secondaries from interactions in det. material (esp. if detector material shrinks with new tracker)
 - \rightarrowtail detector radiography
- track pointing to ECAL (electron-photon separation) and HCAL (neutral hadron showers)

Double-sided detection modules

 improves track reconstruction (against ghosts), pointing resolution (upstream and downstream), momentum reconstruction, station spatial resolution (30 %) and alignment

- redundancy alleviates impact of detection inefficiencies (esp. after irradiation)
- possibility to combine two different sensors (< 1 ns timestamping ?)
- BUT: doubles power consumption and increases moderately (true ?) the material budget

CONCLUSION and **OUTLOOK**

- \sim 20 yrs of Monolithic CMOS Pixel Sensors development for charged particle detection
- \rightarrowtail achieved maturity allows addressing very demanding running conditions & large detection areas
 - \Rightarrow relevant technological approach for pixelated trackers of O(100) m $\hat{2}$ (R&D still needed !)
- Each application calls for specific design(s), guided by realistic, comprehensive, MC simulations, accounting for global yield & system integration aspects
- On-going R&D expected to establish the possibility to realise monolithic CPS combining

< 10 μm resolution, timestamping < 25 ns & high rad. tol. (10¹⁵n_{eq}/cm², 100 MRad)

- Are these sensors suited to the most exposed parts of the LHCb tracker ? \Rightarrow MC simulations should tell
- Which benefits would follow from relaxing the rad. tol. requirement on the design, to derive a sensor optimised (power !) for less exposed & largest surface of the tracker ?
- Reduced material budget associated to CPS \rightarrow double-sided stations may be of significant advantage
- Perspectives:
 - smaller feature size \Rightarrow faster & more complex (low power) circuitry for signal conditionning & transmission
 - stacked layers incorporating \geq 3 CPS / station module (\equiv mini-tracker)

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\Rightarrow MONOLITHIC CMOS PIXEL SENSORS OFFER A PROMISING FUTURE FOR LHC TRACKERS