Data Sheet **BANDGAP01**

FEATURES

Generic bandgap voltage reference
Typical voltage reference value of 572 mV
Typical power supply voltage: 1.2 V, but also evaluated at 1.5 V
Temperature drift from 0 to 70°C: 1.6 mV
Drift with power supply voltage from 1.1 to 1.2V: 1.5 mV
Current consumption: 490 μA
Technology TSMC CMOS 130nm

BRIEF DESCRIPTION

BANDGAP01 is a Building Block designed using the TSMC 130nm CMOS technology through the PDK distributed by Cern.
BANDGAP01 is based on a xx architecture and it is fitted with a start-up function.
BANDGAP01 is ready for being directly implemented in any analog or mixed 130nm-TSMC ASIC.

APPLICATION

DC Voltage reference with temperature and power supply voltage drifts compensation.
DC biasing inside analogue and mixed ASIC.

TYPICAL APPLICATION CIRCUIT

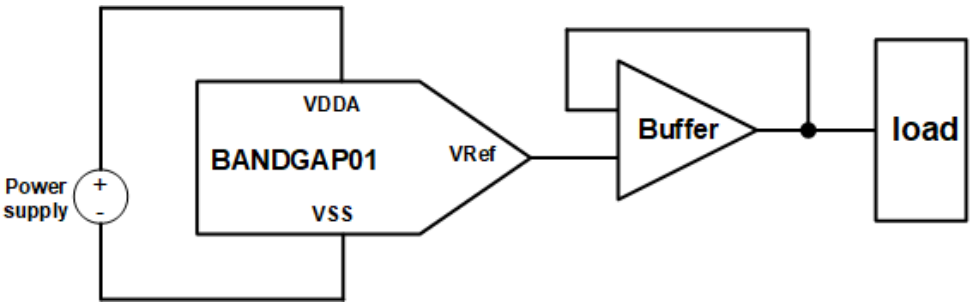

Figure 1: Typical application schematic

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REVISION HISTORY

10/17 - First version A

DETAILED DESCRIPTION

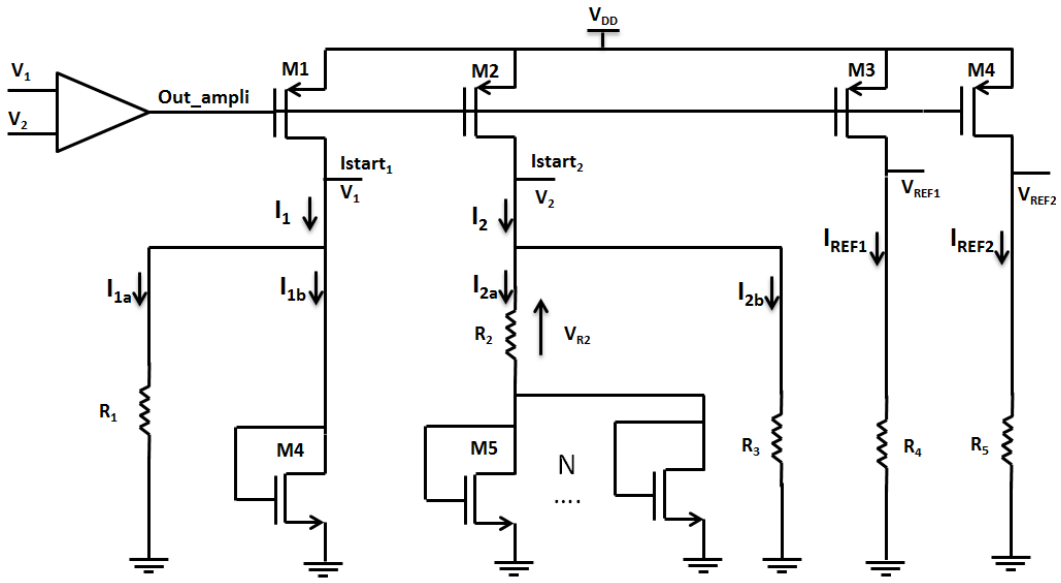

Figure 2: Architecture of the block

Compared to a conventional BGR circuit, this block presents two originalities. The first one concerns the use of a startup circuit which is embedded inside the self-biased amplifier circuit. Therefore the system doesn't require any external signal. The proposed startup circuit will be detailed further below.
The second singularity of the proposed BGR is that the diodes implemented inside the conventional CTAT are replaced by NMOS transistors working in a weak inversion region. In such operating mode, the NMOS transistors exhibit a threshold voltage limited to 300 mV, while the conventional diode threshold is above 600mV. Therefore, the use of NMOS transistors biased in weak inversion region presents a major interest to design high-quality reference circuit operating at low power supply voltage, using pure CMOS process.

Important note: in the proposed build block *bandgap01*, only one reference output voltage is delivered, VREF2, it means that VREF1 is not implemented.

The structure of the proposed BandGap reference circuit is shown in Fig. 2, where VREF2 corresponds to a voltage reference value of about 570 ,mV. The circuit is based on the topology proposed in [1] where two currents, proportional to CTAT and PTAT, are generated by only one feedback loop. All PMOS transistors M1:M4 have the same dimension and their gates are all connected to the amplifier output; hence, the currents I1, I2, IREF1 and IREF2 are equal. VR2 is the forward voltage difference between the transistors M4 and the N transistors M5. These transistors work in weak inversion. The resistors R1 and R3 have the same value.
The BGR circuit presents two possible operating points: the first one is for a biasing current equal to zero, and the second one with the current equal to the value given by equation 13. Therefore, it is necessary to use a startup circuit to impose a correct operating point. In this work, we propose a dynamic startup circuit (Fig. 3) which doesn't require any external Power On Reset signal (POR). The Startup circuit works as follows. When the power is switch on, the amplifier output voltage is low which places M6 grid-source voltage high so that the transistor delivers a maximum current through M7 and M8, making voltage at the resistance R6 close to power supply. Therefore, transistors M9 and M10 deliver currents called Istart1 and Istart2. Once the amplifier is in the steady state and correctly polarized, the current generated by the transistor M6 is too low to polarize transistors M9 and M10 through the resistor R6. M9 and M10 are then pushed into the cut-off region and the startup system is automatically turned off.

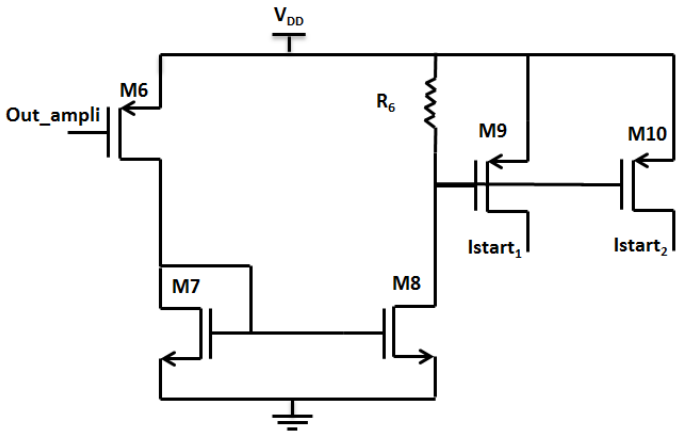

Figure 3: Startup circuit

LAYOUT

The layout of the bandgap is represented in Fig. 4. Its size is limited to 190 μm x 80 μm. Power is distributed thanks to horizontal rails on top and bottom sides, using metal1 layer and metal2 layer for VSSA and VDDA respectively. Output reference voltage VREF2 is accessible on the right side through a metal2 layer connection.

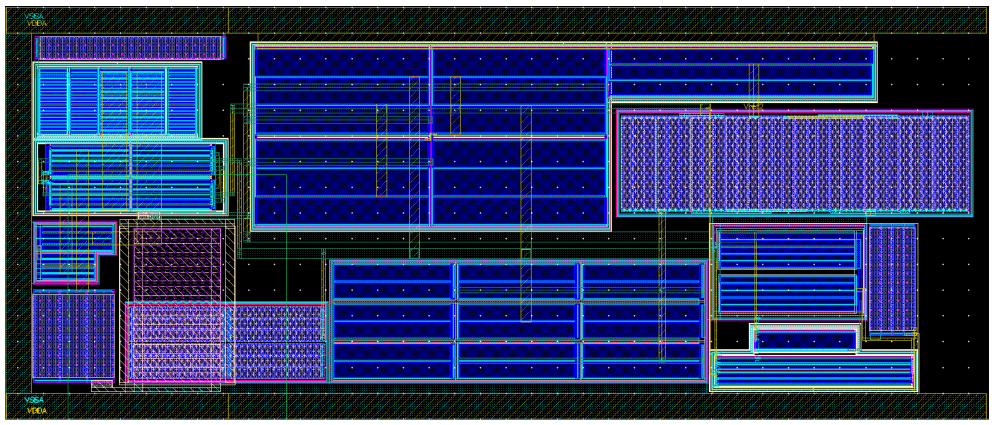

Figure 4: Physical implementation of the bandgap

SIMULATED PERFORMANCE

1.2V power supply (VDDA)

Parameter	Conditions	Min	Typ	Max	Unit
Output impedance R_{OUT}			27 k		Ω
Temperature drift ΔV_{temp}	from 0 to 70°C		1.6		mV
Supply Voltage drift ΔV_{VDDA}	from 1.1 to 1.3 V		1.5		mV
Output noise	Integrated rms noise from 1Hz to 1GHz		2.5		mV
Mismatch variation (Std Dev)	Random sampling method at 27°C		8.5		mV
Process variation (Std Dev)	at 27°C				mV
Startup efficiency versus mismatch variation	Low-Discrepancy sampling method at 27°C		97		%

Table 1: Specifications summary

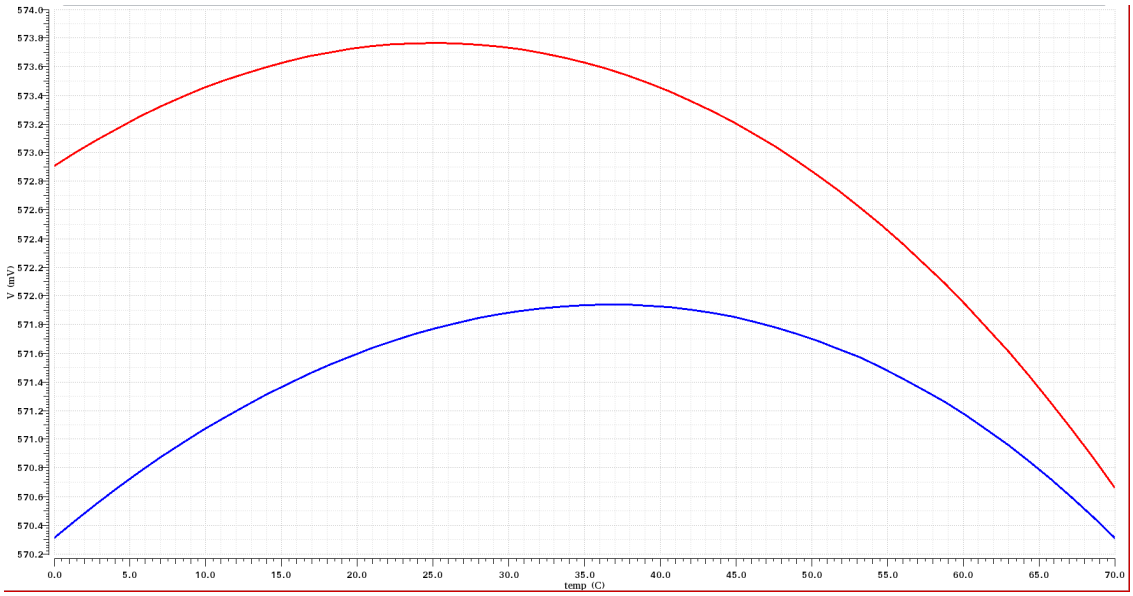

Figure 5: Reference voltage variations with temperature at 1.2V (blue) and 1.5V (red)

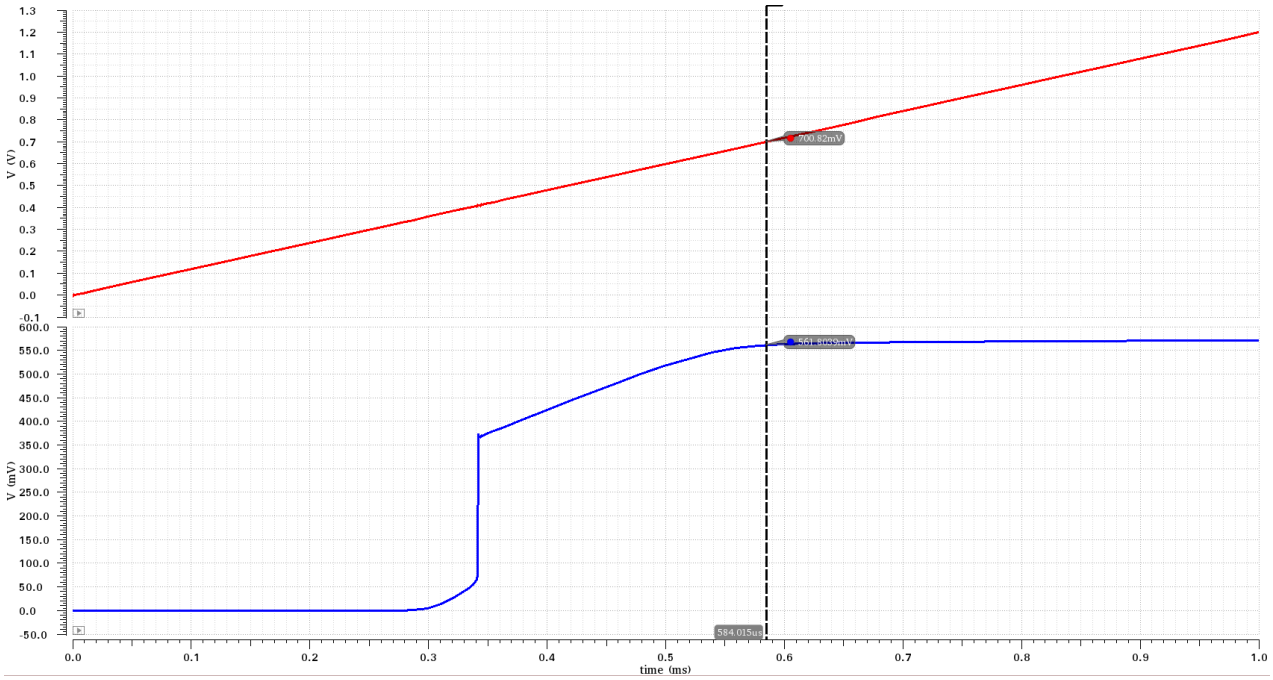

Figure 6: Variation of the output voltage (blue) with a ramping power supply voltage VDDA (red).

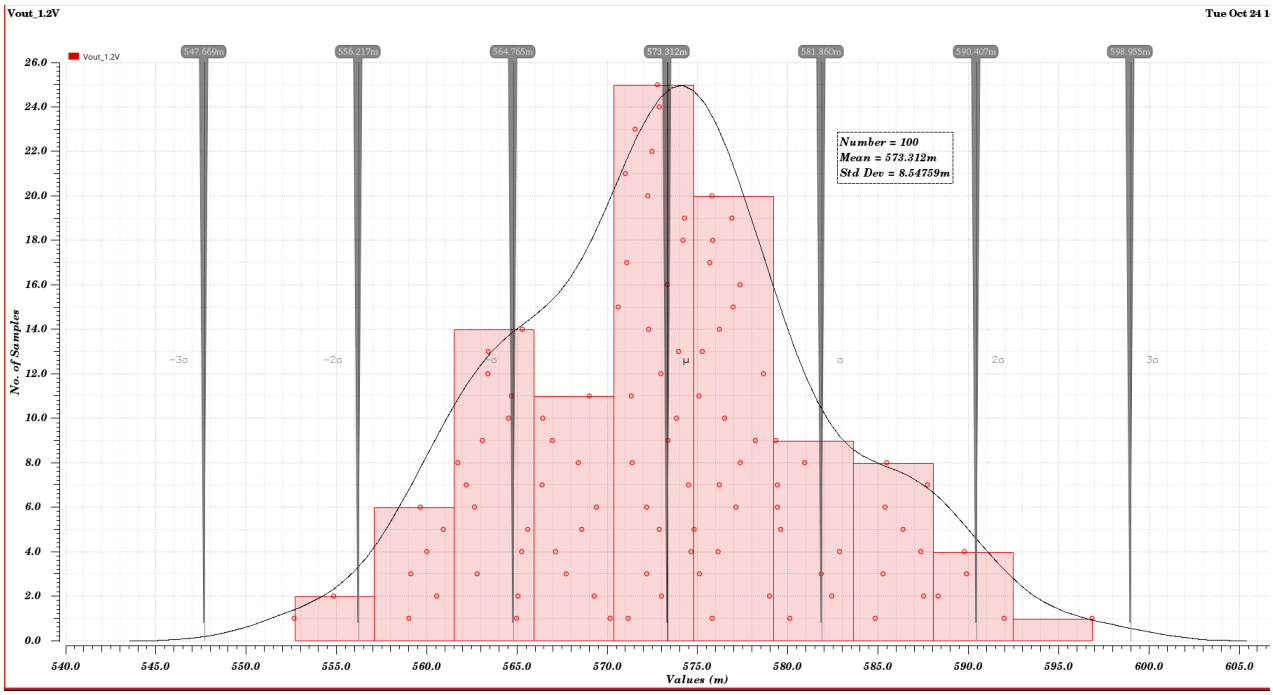

Figure 7: Distribution of the output voltage at the end of the startup period with mismatch variation.

MEASURED PERFORMANCE

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{DD}	1.2 to 1.5 V
Temperature Range	
Operatingjunction	-40°C to 125°C
Storage	-65°C to 150°C
Soldering Conditions	To Be Determined

Table 2: Absoulte maximum ratings summary

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

REFERENCES

References

[1] B. Hironori, et al., A CMOS Bandgap Reference Circuit with Sub-1-V Operation;, IEEE Journal of Solid-State Circuits, vol. 34, No. 5, pp. 670-673, May 1999.

NOTES