November'15 test beam analysis

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Contents

Many further details on this analysis may be found in the presentations at data analysis meetings (`https://indico.in2p3.fr/event/13195/` etc. - use arrow buttons in the top left to navigate from Dec'15 to May'16) and at the ILD ECAL meeting in February 2016, `https://agenda.linearcollider.org/event/6973`

The data have been analyzed by Kostya Shpak and by me. In particular, Kostya has studied:

- the **transverse fractal dimension** approach to distinguish electromagnetic and hadronic showers proposed in M. Ruan, D. Jeans, V. Boudry, J.-C. Brient and H. Videau "Fractal Dimension of Particle Showers Measured in a Highly Granular Calorimeter" Phys. Rev. Lett. 112, 012001. Up to now this approach was applied only to Monte Carlo

data. Here, it can be used even with the incomplete ECAL, even one layer is sufficient.

- So-called "square events". In such events many cells at the sensor periphery are fired and the event looks like a "square". They are produced due to a capacitive coupling between a guard ring and the periphery pixels by a big energy deposition at the guard ring. The latter is a special electrode at the sensor periphery which smooths the electrical field at the sensor edge. It ensures a high voltage stability and low dark currents of the sensor. Due to technological reasons, in the current design the guard ring potential is not fixed but floating. Therefore, a big charge at the guard ring may fire many peripheral pixels via the capacitive coupling. In the physical SiW ECAL prototype tested in 2006–2011 the sensors had the simplest guard ring with one segment. In the newer sensors of the technological prototype, 2 or 4 segments are used. This reduces the capacitive coupling and the probability of the "square events". Kostya has estimated this probability in the data when the beam shooted at the center of FEV-10,11, ie. at the corner of 4 sensors. **One "square event" per a few thousand of normal events was observed.** Note also, that Hamamatsu HPK company has a "know-how" to produce promising sensors without the guard ring. They should be tested in the future. One detector with such sensors was available in June 2016, but was not tested due to noise problems.

- **Data corruption** in the DAQ due to various reasons.

On the other hand, I have concentrated on the characterization of the detectors and the efficiency measurement, described in more detail in the following.

1 Pedestal calculation.

It was found that the pedestal calculation is much less trivial than expected. It was known from 2013 that the pedestals should be calculated per channel and per memory (every channel has 15 memories, called "SCA", so that the chip can accept up to 15 events in one ILC spill). The pedestals in different SCA memories for the same chip are different.

Another complication comes from the fact that there might be events with "negative" (ie. below pedestal) ADC values. It was found that in such events many channels might become negative, and negative signals in

the same chip are 100% correlated. Therefore, all events with any negative signal in the chip should be removed from the pedestal calculation.

Finally, there is one more complication. It was known from 2012 that the triggered event in "bunch crossing" clock window BX may be followed by "retriggers" in BX+1, BX+2, BX+3, ... The probability of retriggers increases with lowering the trigger threshold and in higher noise conditions. When lowering the trigger threshold, the spontaneous retriggers may start to dominate the data stream and this finally puts the limit on the allowed threshold. In fact, in June 2016 in 6 layers even with high thresholds (290 compared to the nominal 230) the retriggers dominated the physics at the rate of 100 : 1. Equivalently, this was interpreted as high noise conditions. In one layer retriggers were acceptable, however, even at the threshold of 230.

In November 2015 the retriggers were acceptable in all 3 readout detectors. Surprisingly, I have found that the pedestals in FEV-10,11 have two different positions depending on whether or not the event is followed by the retrigger. Ie. the pedestal "knows" whether the chip will produce the retriggers. The MIP position before a pedestal subtraction is, however, rather insensitive to the following retrigger. Ie. the retrigger biases the pedestal but not the MIP. Based on these observations, the correct pedestal is extracted only from events not followed by the retriggers. This was a new observation, not known for FEV-8. The splitting between the pedestal positions for the cases with and without retriggers, was significantly different between 3 studied FEV10,11 boards.

In the end, the pedestals were calculated per channel, per SCA memory in the events without any negative signals and not followed by retriggers. After that the resulting pedestal spectra finally became Gaussian, as shown in Fig. 1 for about 1000 channels in one detector. What was important is the absence of the right pedestal tail above Gaussian. One can see an excellent separation of the pedestals and the MIP signals, showing a very good potential of the SKIROC chip.

2 More on retriggers.

Another interesting and unexpected feature of retriggers we have discovered together with Christophe De La Taille. It was found that the retriggers represent in fact one very long event. Namely, in one merged macro-event (with all BX, BX+1, BX+2, ... combined):

- quite often all 64 channels are triggered. In fact, sometimes the macro-

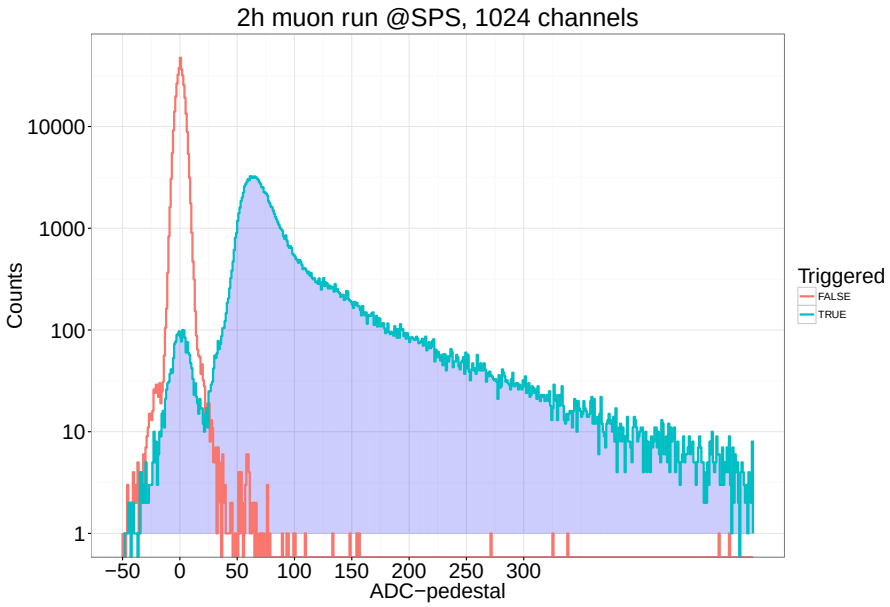

Figure 1: ADC spectra accumulated in all channels of one detector during two hours muon run. Triggered and non-triggered data are shown separately. A peak at zero for triggered data is produced by spontaneous retriggers (which always have zero signal).

event can continue further, and then all 64 channels might be triggered twice or even three times;

- if only 64 channels are triggered, normally, every channel triggers once and only once. This happens in (roughly) 1 μsec, a very long time for the fast SKIROC chip (one BX is 0.4 μsec in the current prototype).

Unfortunately, the reason of retriggers is not understood at the moment. Spontaneous retriggers limit the chip stability and the trigger threshold (provoking instabilities, like happened in June 2016, especially when the chips start to "talk" to each other in the board and the retrigger from one chip can continue in the other). The amount of retriggers is upredictable and different from board to board. Even in "normal" conditions like in November 2015 the retriggered data may occupy about 50% of events, this is another negative side of this effect.

3 Beam spot.

The typical beam spot accumulated in one muon run is shown in Fig. 2. 2.2% of 3x1024 channels have been masked. In particular, channel 37 in all chips is always masked (the reason why it is different from the other channels is not understood).

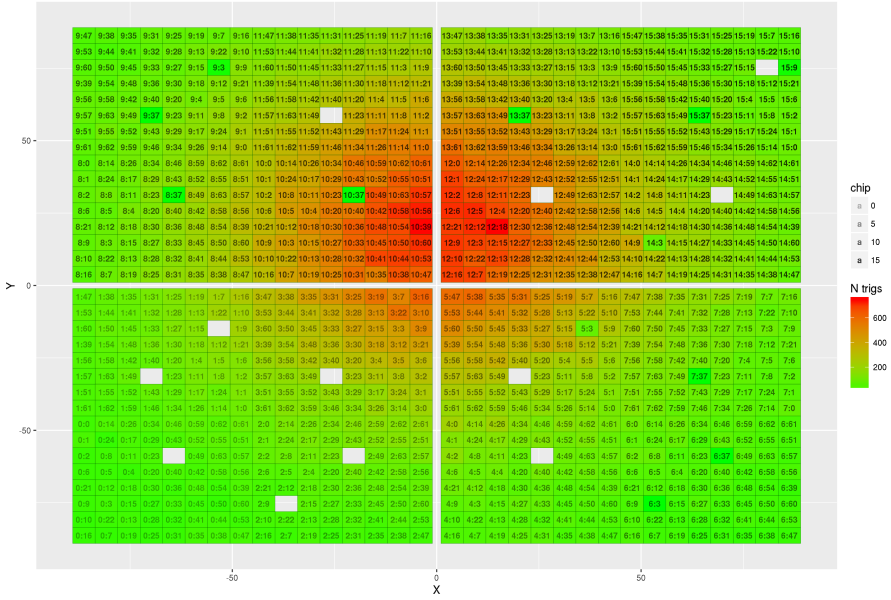

Figure 2: Beam spot in one of three detector layers (other two are similar)

4 Pedestal time stability.

For this study I used 19 muon runs, 2 hours each, mainly taken at night. The results are shown in Fig. 3. Only the pedestal spectra (per channel and per SCA memory) with at least 25 events are analyzed. All channels and SCAs are averaged in each chip (maximally, average over 64*15 = 960 numbers). Every point is one run and one chip, 19x16x3 = 912 points in total. Evolution of average pedestal position is shown with respect to chronologically first run. The problematic channels (#37 and #45-47 in chips 1,9 with double peaks) are excluded. The boxes contain 25%...75% quantiles (ie. excluding 25% lower and 25% upper points), lines above and below extend to the last point within 1.5x box height, outliers beyond are shown by black.

Three detectors are shown in three columns, raws represent groups of four chips in each detector. Different colors distinguish runs accumulated in different conditions. In particular, one can see that the pedestals around November 14 in the left column deviate by more than 1% of a MIP. They have been accumulated with different spill clock settings ("short spills"), this will be discussed in detail in the next subsection.

Without "short spills" the RMS of measured pedestal variations is about 0.5% of a MIP.

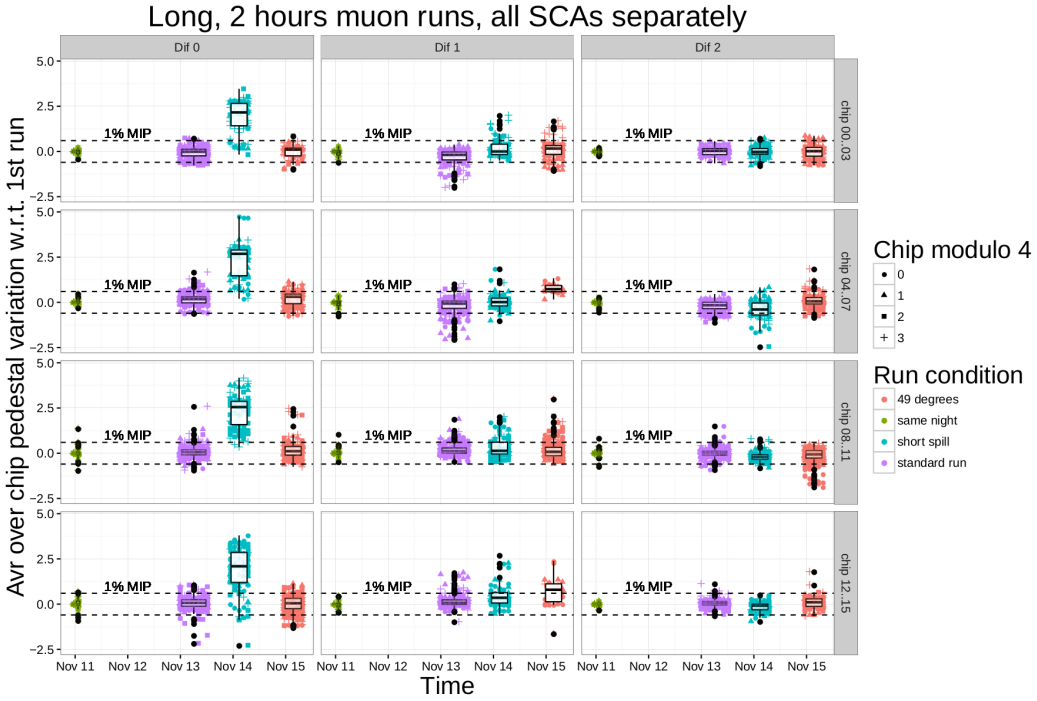

Figure 3: Time stability of the pedestals measured during all muon runs (mainly taken at night). Every point represents an average over one chip in one two-hours run (912 points in total). Columns (rows) represent layers (group of four chips in the layer). ±1% MIP interval is shown by dashed lines. Boxes include 50% of middle points.

5 Pedestal drift after power ON in power pulsing.

In the current design, ILC collides bunch trains during 1 msec and then stays idle for 199 msec. The latter long period is used to readout the data stored in SKIROC. To save power and simplify the cooling, the front-end electronics is then switched off. This is called "power pulsing".

In the muon runs with low muon intensity, to accumulate higher statistics we normally recorded data during 200 msec and used 50 next msec for readout. Such 4 Hz "spills" of 250 msec each have been optimized to reduce a data corruption (at 5 Hz we had problems in the last 16th chip, while with less than 50 msec readout time we had problems in the formation of correct "spill" blocks of data in DAQ).

In some runs, I have proposed to use "short spills": 2.5 msec of data taking and 247.5 msec for readout. Such conditions are closer to ILC and on the other hand, they allow to uniquely code the "bunch crossing" 2.5 MHz (400 nsec) clock number in 12 bits only available in SKIROC. In fact, the front-end electronics is switched on after the start spill signal, but then there is a "waiting period" for stabilization, to allow all transition processes to finish. The bunch clock counting starts after 0.9 msec, but the real data taking starts after 1.4 msec. Ie. the first data appear at about BX = (1400 - 900) msec / 0.4 msec = 1250 and continue until BX = (2500 - 900) / 0.4 = 4000. Such 2.5 msec spill window with $1250 \leq \mathrm{BX} \leq 4000$ have been chosen to fit to 12 bits BX range, up to 4095.

In 2013 the "waiting period" was shorter by about 0.5 msec. It was found that the pedestal level drifts for about first 0.3 msec, and then it was increased as described above.

The pedestal deviation with "short spills" in one layer in Fig. 3 left may indicate that some transitional processes are still ongoing. To study this effect, I have averaged all muon runs with short, 2.5 msec spills, and all 1024 channels of one layer. The result is shown in Fig. 4. There is a significant deviation in one layer with possibly slow drift towards zero. This slow drift needs a further investigation. In principle, since the slope is small, such a deviation may be not problematic for ILC, as it can be properly measured in the "true" ILC spill conditions. This is true only if the effect is always the same and stable in time (no strong dependence on the power supply etc.; to my knowledge, the reason why the pedestal shift is larger in one of three PCBs is unknown).

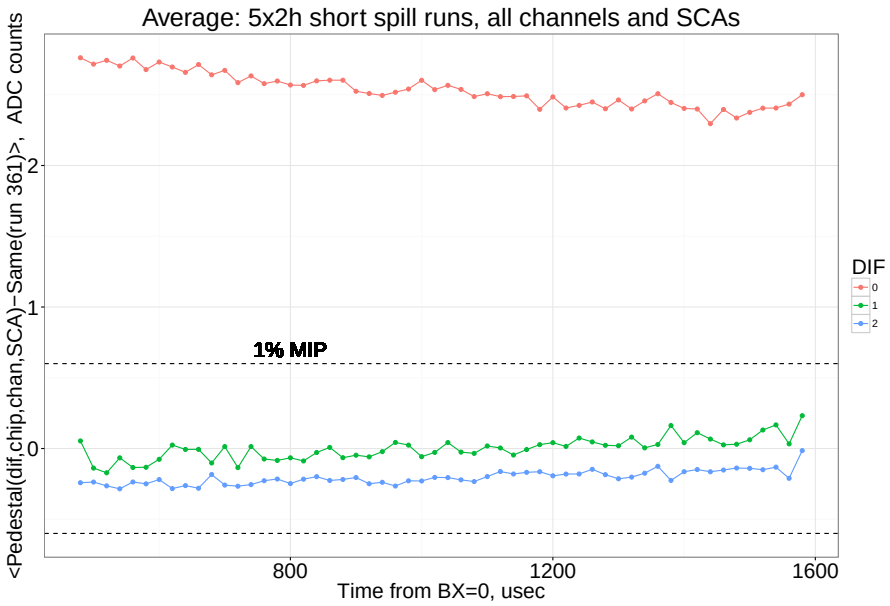

Figure 4: Pedestal drift after power ON in power pulsing, averaged over one layer.

6 Signal over noise ratio.

In November 2015 we selected the SKIROC gain "optimal" for a signal-over-noise (S/N) ratio. Nominally, for the highest dynamic range, the SKIROC feedback preamplifier capacitor should be 6 pF. It can be varied programmatically, however, and about twice better S/N can be achieved with 1.2 pF. This value was used during all November 2015 tests. This gives 5 times higher gain, meaning that the dominating noise at nominal 6 pF comes not from the preamplifier (!) but from further stages in SKIROC.

1.2 pF are thus optimal for the MIP signal which has the most probable value at about 65 ADC channels. Fig. 5 shows the ratio (MIP / RMS of pedestal spectrum). Note, that every histogram entry is obtained from one spectrum with at least 100 events (pedestal spectra are taken per channel, per SCA and per run), so this plot summarizes a huge statistics on about 3000 channels over a long period. One can see that in average S/N = 17-18, which demonstrates an excellent potential of the SKIROC chip. Also note, that pedestal RMS does not reflect the retrigger instabilities, as SKIROC has a trigger line separated from two (high and low gain) preamplifiers.

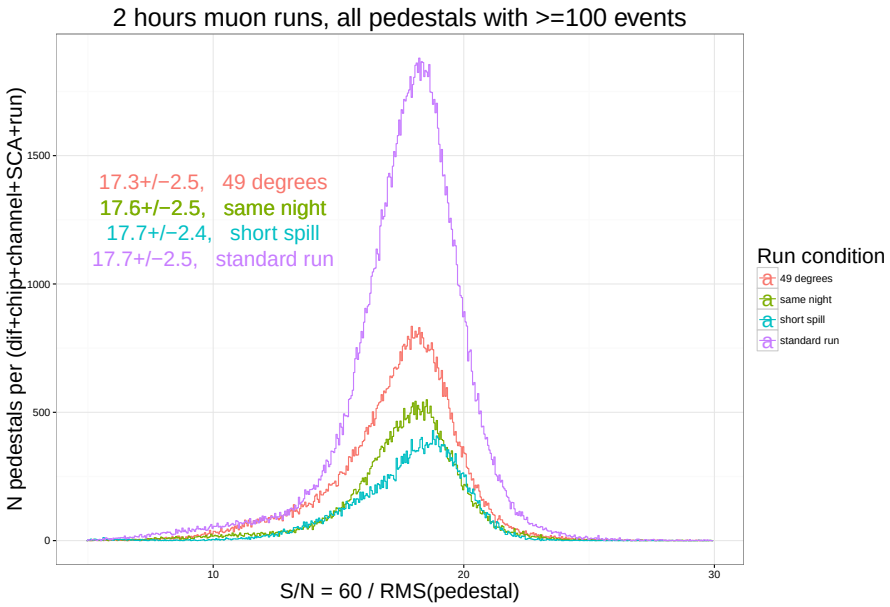

Figure 5: MIP signal over pedestal RMS ratio.

7 One layer average efficiency

The efficiency is determined in two 150 GeV muon runs. Two layers in coincidence are used as the "offline trigger", while the remaining layer efficiency is studied. Since the timing in any two layers may be shifted by maximum one bunch crossing (BX) clock period (400 nsec), the coincidence is detected if BX1 = BX2 or BX1 = BX2 ± 1. This is required both in the trigger and for the layer to be efficient. Since muons hit ECAL almost perpendicularly, for the trigger coincidence the hit pixel is required to be the same in both layers, ie. the hit coordinates x1=x2, y1=y2. For the layer to be efficient this requirement is relaxed to x3=x1 or x1 ± 1 and the same for y (this changes almost nothing: increases the efficiency by 0.1% or so).

Retriggers in BX+1, BX+2, ... (following the muon in BX) are removed. The pixel is defined to be hit (for both the trigger and for the efficiency definition) if it has a SKIROC trigger flag and has ADC - pedestal $>$ 20 ($>$40 for the trigger). Average pedestal RMS over all channels is 3.5 with the standard deviation of ±1.5 ADC channels. For simplicity, it is also required that there is only one hit in each of the two trigger layers (to avoid showers from 150 GeV muons; the tungsten absorber was installed for these runs, we did not take the risk to remove it since the setup was fragile because

of temporary DAQ interconnections with springs).

There is one more complication: the inefficiency in the central chips could be due to the limited SKIROC memory. To exclude this possibility it is required that the chip whose efficiency is studied, has at least one remaining empty memory in the end of the spill.

The bad channel 37 is also always excluded. There is also a tiny fraction of events with corrupted DAQ data where the SKIROC memory is greater than 15. Such events are also removed. The probability that the pixel becomes efficient due to a random noise is negligible.

What remains is mainly the inefficiency due to the SKIROC trigger threshold. For these two runs it was set to the "nominal" value of 230. The efficiency in three layers is shown in Fig. 6. The outliers with the efficiency lower 80% are shown by red points. The efficiency is high except in chip 14, layer 3, which will be discussed later. The overall fraction of outliers is 2.9%, it is dominated by this problematic chip.

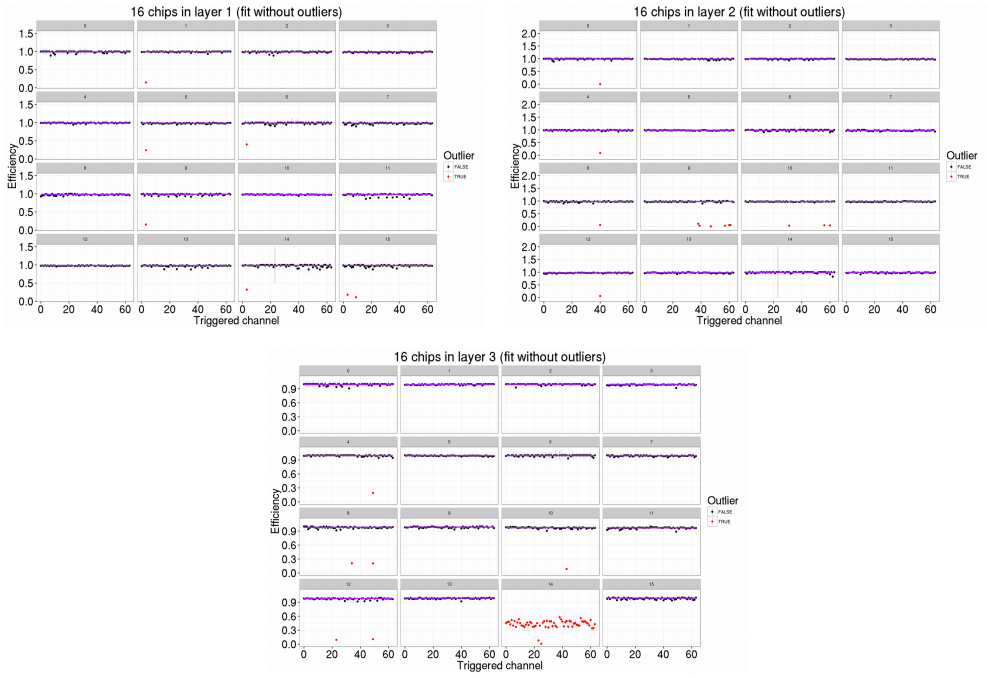

Figure 6: Average efficiency of all channels in three layers in 16 chips. Outliers with efficiency lower 80% are shown by red.

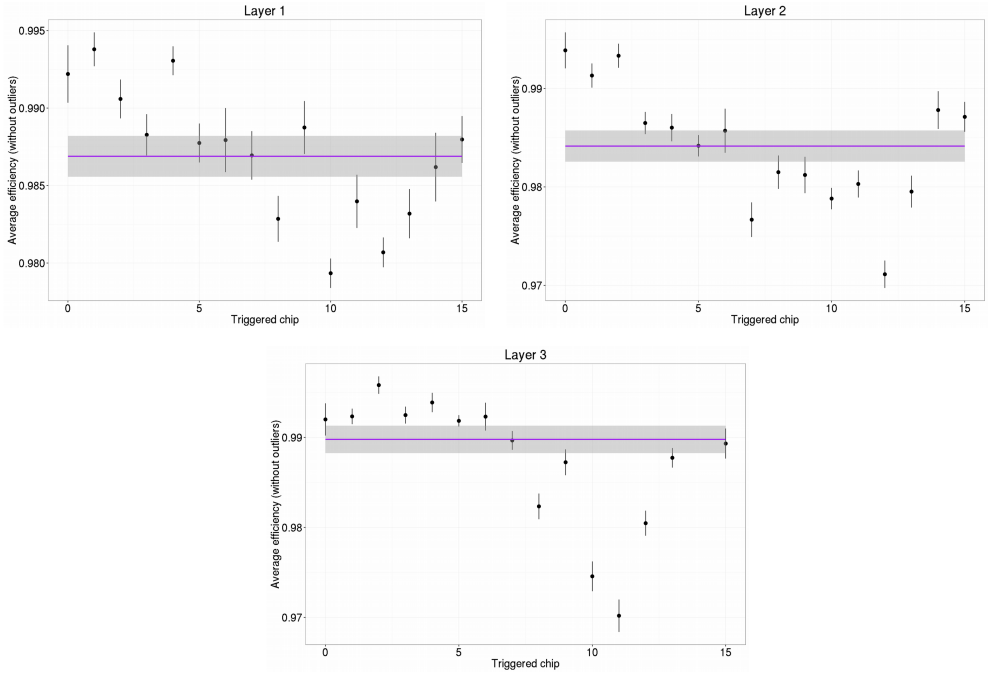

Figure 7: The efficiency averaged per chip excluding outliers.

Fig. 7 shows the average efficiency per chip excluding outliers. It is in the range 98 – 99%.

For simplicity, I do not treat separately the masked channels. If it is masked in the studied layer, but not in the trigger layers, the event appears as inefficient. This is one of the reasons of outliers. Note, that positioning of the channels in all layers is the same, the channel 37 is masked in all chips by default, so it is absent both in the trigger and in the studied layers. The fraction of other masked channels ($\neq$37) is only 0.6%. Also, I do not exclude the boundary cells and the cells close to masked. Therefore, very rarely, due to not perfect alignment, the muon can be in the trigger acceptance but outside the acceptance of the studied layer. This small effect also mimics (increases) the inefficiency. Note however, that at the detector boundaries the statistics is small, and the statistical errors are taken into account in the efficiency averaging.

Fig. 8 shows the efficiency versus the SKIROC memory number (SCA) used in the trigger. Between the two layers, the maximal SCA is chosen.

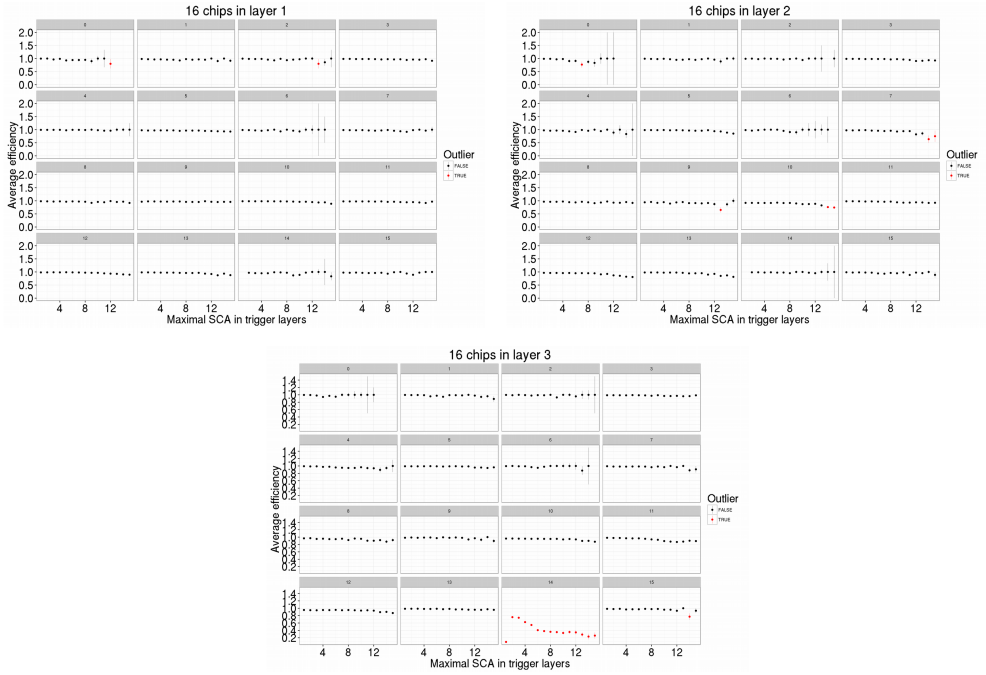

Figure 8: Efficiency dependence on max(SCA1,SCA2), where SCA1,2 are SKIROC memory numbers in two trigger layers.

Note, that due to different level of noises, the SCAs in different layers are different, but correlated. It is interesting, that the bad chip 14 in layer 3 has low efficiency when maximal trigger SCA = 1, 4,5, ... It is not clear why this chip is so different from the others.

Fig. 9 and Fig. 10 show X-Y efficiency maps and the occupancy distributions of trigger muons (not necessarily detected), respectively. The problematic chip 14, layer 3 with low efficiency (on the right above the central line) also reduces the number of triggers in the other two layers.

8 Uniformity of channel responses to muons

One of the main advantages of the silicon detector over scintillator is a much better uniformity across the channels. This makes the calibration much easier and reduces the systematics. As an illustration, Fig. 11 left shows the

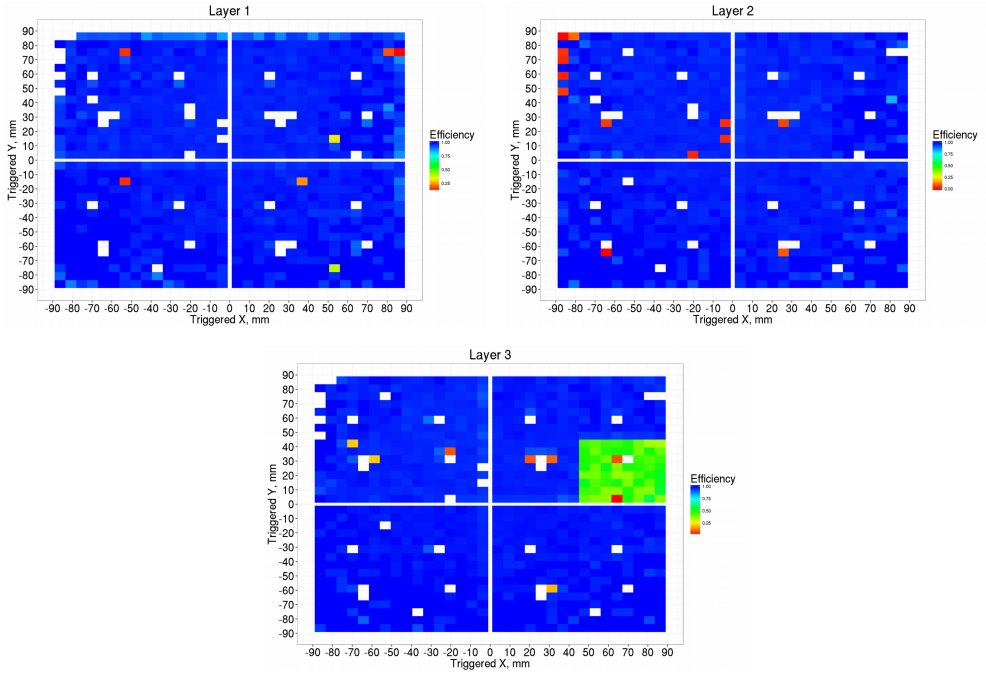

Figure 9: X-Y efficiency maps.

truncated mean of the dE/dx distribution in all channels in 9 muon runs with standard spill settings and the normal muon incidence. The relative variation, RMS / mean = 6.4%. The truncated mean, a simple approximation of the most probable value, is defined as shown in Fig.11 right, among 57% of the lowest pedestal subtracted ADC values above 40. It was required that 100% corresponds to at least 50 events, therefore due to the limited muon statistics at the corners, only 83% of all channels were calibrated in this way (we did not perform a position scan since the setup was very fragile).

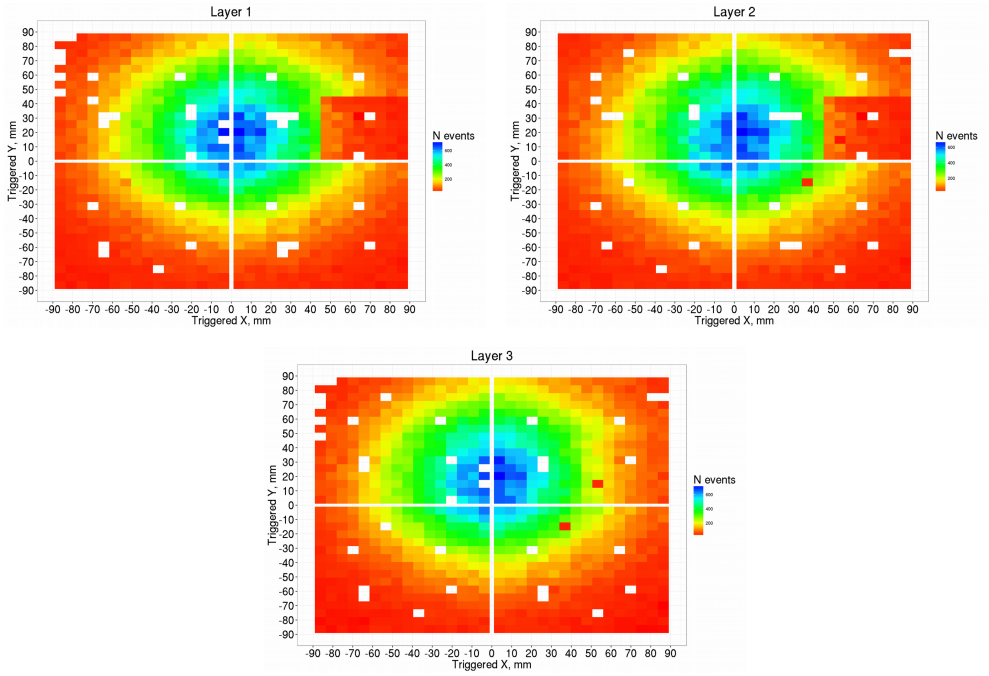

Figure 10: X-Y occupancy distributions of trigger muons.

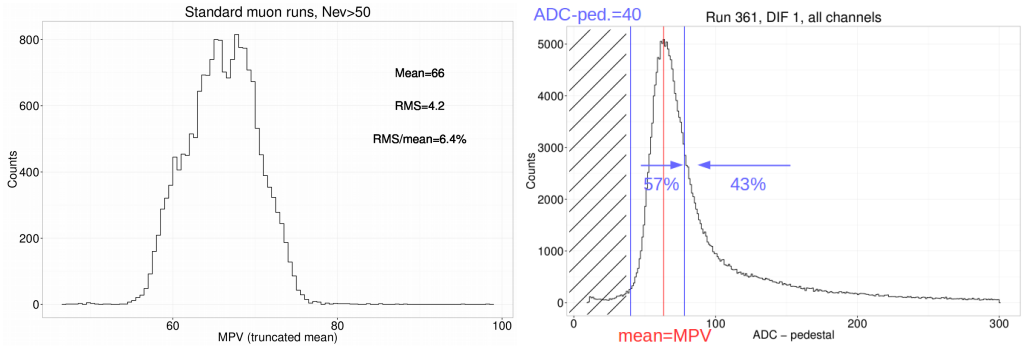

Figure 11: Left: the most probable dE/dx value measured in 17 682 spectra using a simple truncated mean method in 9 muon runs. Right: definition of the truncated mean as the average of 57% lowest ADC pedestal subtracted values above 40.