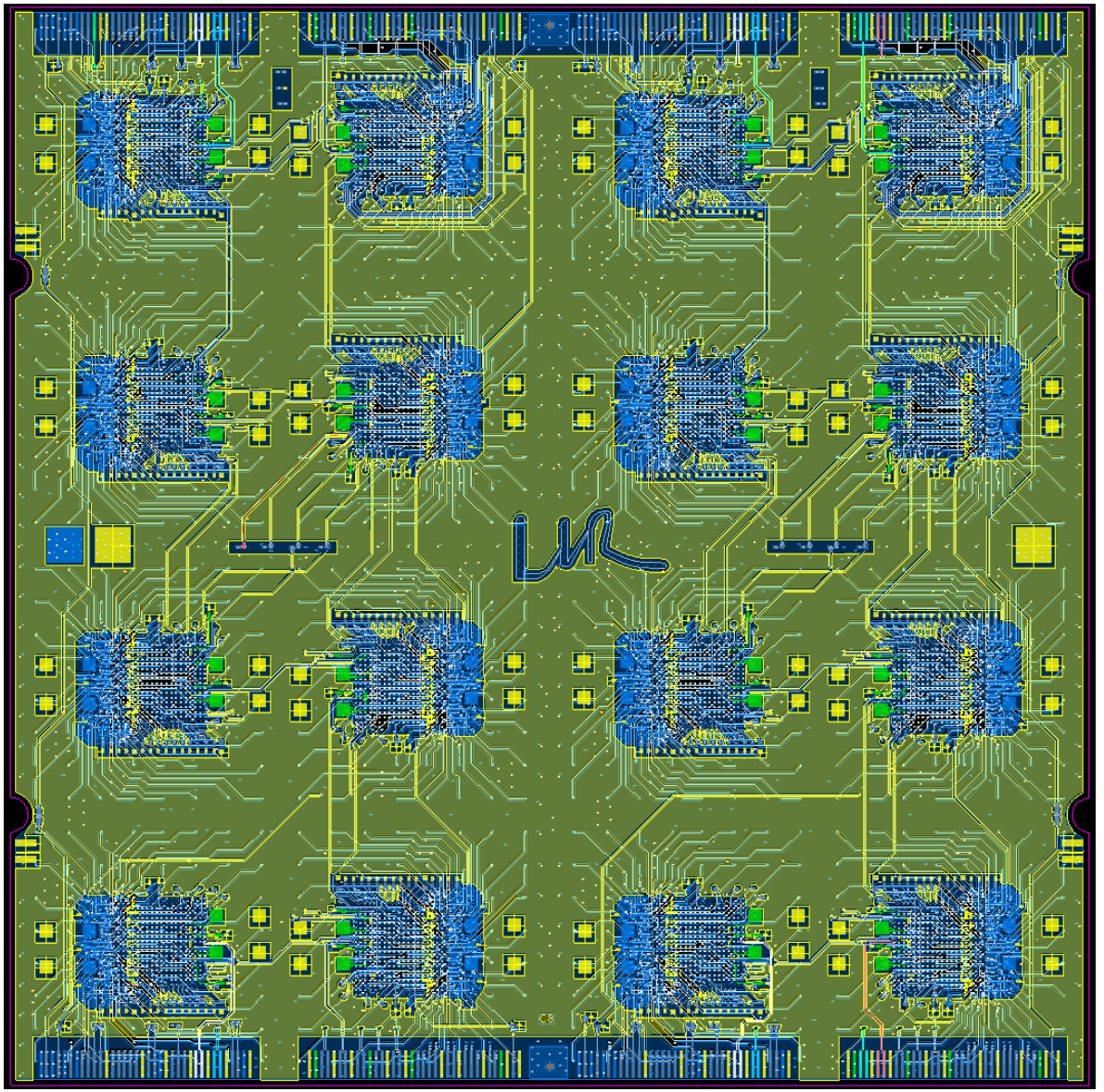
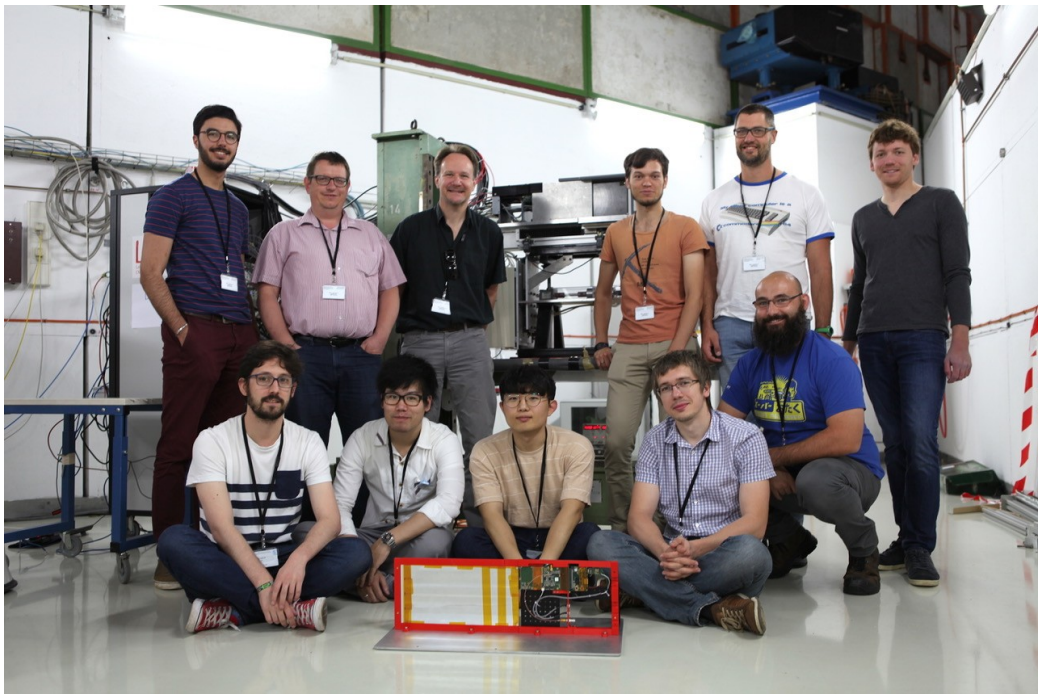


Enhancing SiW-ECAL short slabs

Frédéric Magniette

Beam-test of July 2017 a complete success

- Very quick setup
- No major technical issue
- Full of good data in all positions and all energy
- Shower profiling
- Nice signal over noise ratio
- Full of time for main physics program and extras (45°angle, magnetic field)



The ECAL short slab as it exists is a complete success

Why changing the design ?

- Some details remains annoying and can be improved by new design
  - Reduce the number of masked channels
  - Reduce retriggering and plane events effects
  - Suppress noise conduction by mechanical structure
  - Use the new chip Skiroc2a
  - Make the detector easier to interface with AIDA
  - Secure the DAQ to avoid data corruption and mis-classification
  - Get temperature/data correlation
  - Reduce the heat production

Calorimeter for ILC

The plan

- After meeting with all the project experts
- A plan with 17 tasks has been written
- Handled by three teams:
  - Omega
  - Kyushu
  - LLR
- Objective : try to get one new slab for 2018 beam-tests

1. Reducing masked channels systematics

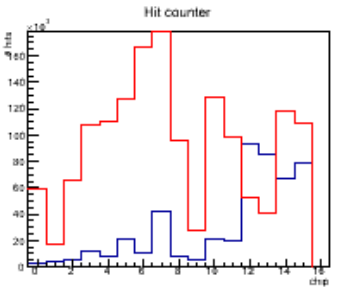
Desc: A substantial part of the channels are masked systematically, probably due to noise induced by the FEV design. For example, the channel 37 is always masked. This is probably a systematic of the basic block of the layout.

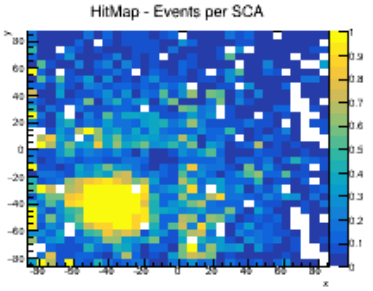
Todo:

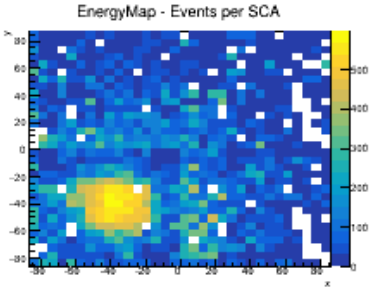
- Study of the layout vs the systematically masked channels
- Redesign the FEV layout

Who:

Omega team + LLR team







Status:

Kick-off meeting + first studies in progress

2. Separate the analog power supply

Desc: The first stage of the preamplifier needs an isolated power supply to avoid noise. New power supplies should be named VDDA and VDDI (this one is for preamp).

Todo :

- Change the schematics of the SMB to integrate a new regulator to split VDDA
- Find an available pin on the SMB-FEV connector
- Change the FEV schematics for this double supply
- Make a new layout

Who :

Omega team + LLR team

Status :

Kick-off meeting + first study in progress

3. Change the data routing on the chained FEV

Desc: The data readout follows a Z path on the FEV. If they are chained, the last readout has to be driven all along the slab to the dif. If the slab is long, it is too far for onboard driver. We need to change this readout path to be an U.

Todo :

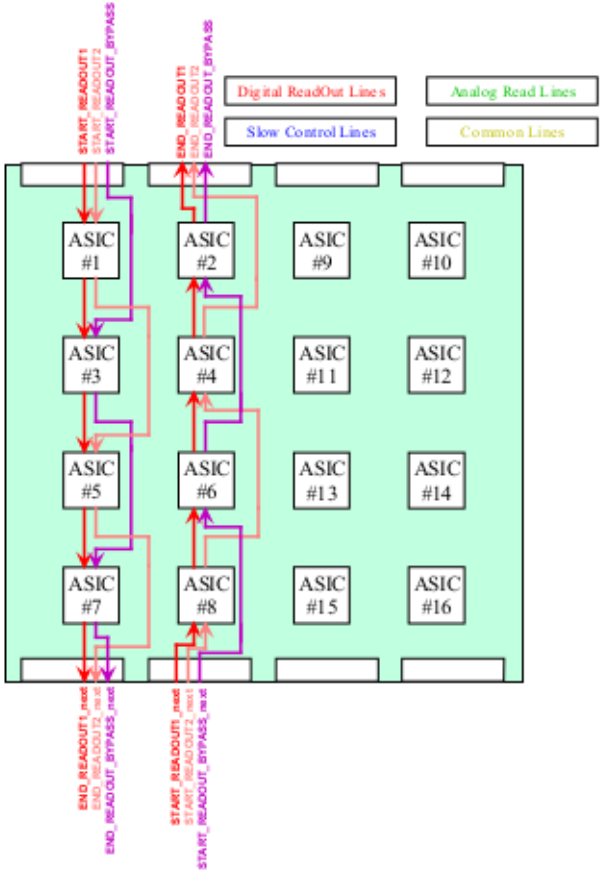
- Change the schematics of the FEV to reflect this change
- Modify the software to reflect this new order in skiroc id

Who :

LLR team + Omega team

Status :

Principle plan has been designed by Omega team



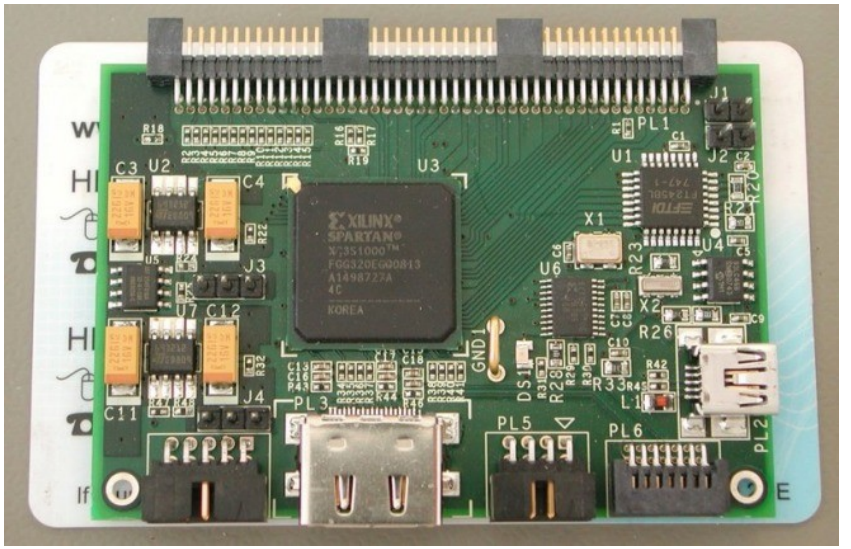
4. Change the sampling in the DIF

Desc: The data corruption is not negligible in the DAQ. This could come from a bad sampling in the DIF.

Todo :

- Parametrize the samping in DIF (phase)

- Make tests to check correlation between samping and data corruption



Who :

LLR team

5. Change fast clock frequency

Desc: The nominal frequency for the fast clock should be 40MHz (Skiroc spec.). It is now 50Mhz.

Todo :

- Check if it is possible to change the frequency on the CCC
- Qualify the DAQ for 40Mhz

Who :

LLR team

Status :

A 40Mhz CCC has been produced from old CCC. The DAQ read-out but data is corrupted

6. Cut the fast clock during acquisition

Desc: The fast clock can cause some noise during data acquisition. It has to be vetoed during this phase. This could be done inside the DIF by a nand on acq signal (or externally an enable driver on the SMB). This nand should be synchronized on the clock.

Todo :

- Study SMB vs DIF solution
- Implement of the choosen solution

Who :

LLR team

Status :

DIF solution has been studied and seems to cope with requirements

7. Using UDP protocol

Desc: The UDP protocol will secure the data transmission by enabling the interruption model in the Linux kernel.

Todo :

- Produce or find_and_test an UDP VHDL block
- Integrate this block in GDCC
- Modify the software to accept both ethernet and udp packets
- Qualify the DAQ with UDP

Who :

LLR team

Status :

A UDP block has been designed but still need enhancements

8. Getting unique ID and temperature from SMB

Desc: There is a Dallas DS2432 chip on the SMB providing temperature probe and unique id accessible through one wire protocol.

Todo :

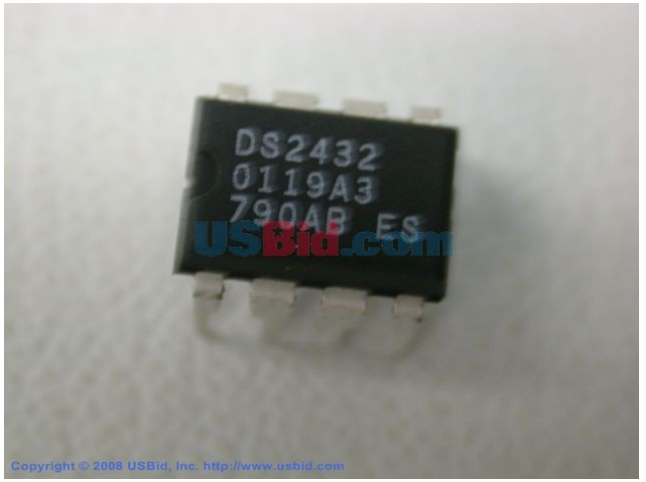
- Integrate the one wire VHDL block inside the DIF
- Add a block transfer command in the DIF to access this informations
- Modify software to extract the slab number from the unique id and integrate this value in the data

Who :

Kyushu team (firmware) + LLR team (software)

Status :

Kick-off meeting and time planning



9. Spill number propagation through CCC

Desc: The spill number is actually just a counter inside the DIF. This is not enough for combined runs. We need to get spill number from outside on the CCC (for example TCP or UDP on Mainz CCC). Then the spill number has to be transmitted to GDCC and DIF (via fast commands or block transfer commands). This spill number has to be integrated in the data in the DIF.

Todo :

- Find a way to get this value on the CCC (ethernet or input pin)
- Propagate it to GDCCs and DIFs via fast commands
- Implement fast command control block in DIF to integrate spill nb in appropriate register
- Modify software to handle break of monotony in spill number

Who :

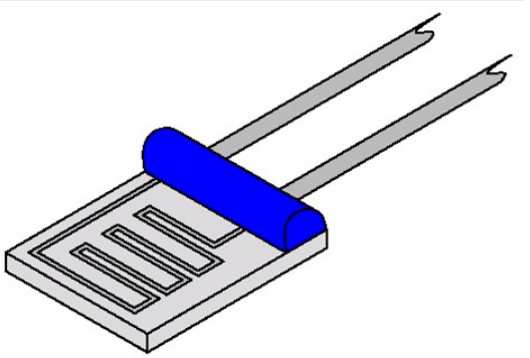
Kyushu team (firmware) + LLR team (software)

10. Probing the temperature in real-time

Desc: To understand the leakage current fluctuation, we need a temperature monitoring in realtime. At least one slab should be equiped with temperature probes to measure this fluctuations. The probes should be PT100 glued on the slab. The connection to the probes will be done by floating wires not to disturb the FEV design.

Todo :

- Design a temperature reading system



Who :

unaffected

11. Remove the adaptation clock resistor

Desc: 4 100ohm resistors adapt the clocks on FEV. They are added by hand at lab. It could deliver a lot of heat (to be verified). The FEV should work without it on short slabs but it is necessary for long slabs.

Todo :

- Measure the temperature and the consumption current
- Remove the resistor on a short slab and check the result.
- Add an imprint on the FEV
- Add it to the BOM

Who :

LLR team

12. Improve the SMB design and cabling

Desc: Some components on the SMB has not been integrated to initial design.

Todo :

- Integrate the 440Ω flying resistor in the schematics and layout
- Remove the RL filter for analog and digital power supply (presently bypassed by a strap)
- Add the link between SRIN2 and P16 (presently done by a strap)
- Add the big capacitor in the SMB BOM (take care to contact PCB-capa)

Who :

LLR team

13. Improve the FEV design and cabling

Desc: On FEV, straps are connecting the partitions. They should be replaced by 0Ω resistors or by press fit contactor

Todo :

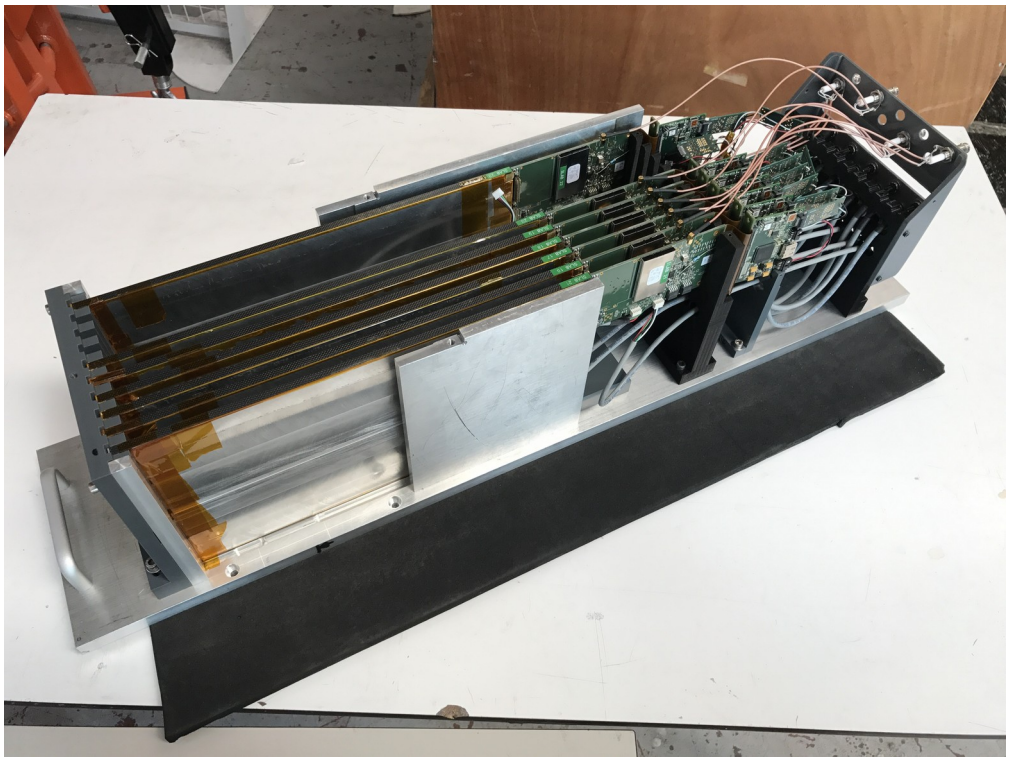
- Study the two solutions and choose one
- Change schematics and layout to reflect the choosen solution

Who :

LLR team

14. Isolate the end of the slab

Desc: The end of the slab expose an aluminium part that conducts noise through the base plate of the detector. A study has to be done to understand how the noise go through (conduction). A new piece has to be done in plastic to replace this aluminium piece in future slab.



Todo :

- Study the noise conduction on current slabs (time study vs bcid coherent noise)

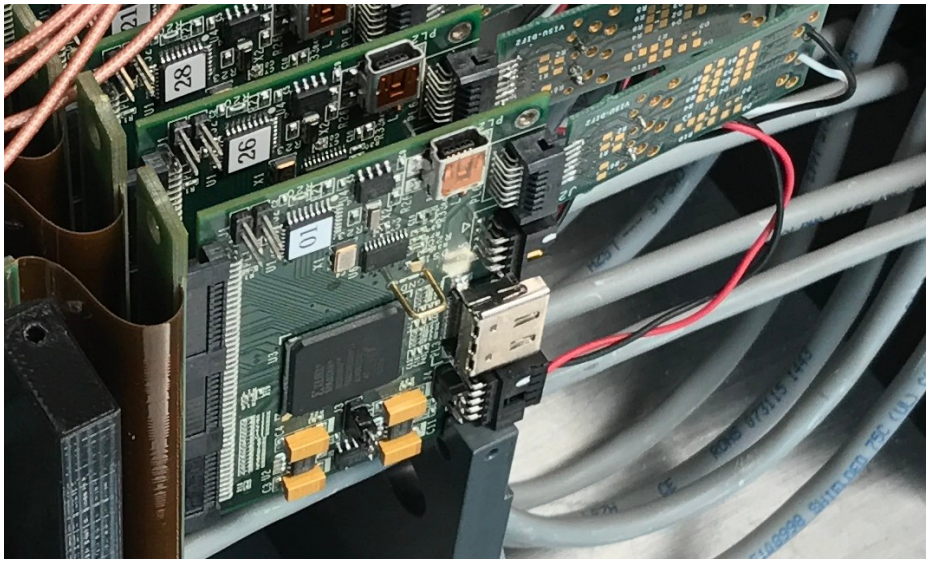
- Make a new version of this piece in plastic

Who :

LLR team (mechanics) + unaffected (noise study)

15. Change the power supply connector of the DIFs

Desc: This connector is in bad shape on almost all the DIF. It has to be changed as fast as possible. On another hand, this connector is really not reliable. Thus it is necessary to change the model.



Todo :

- Study available connectors to find a replacement (for example milligrid 2mm / clip with keyed connection)
- Recable all DIFs with the choosen connector
- Change all corresponding cables

Who :

LLR team

Status :

A new connector coping with requirement has been found

16. Adapt the FEV to skiroc2a

Desc: The decoupling capacitors are not the same for skiroc2 and skiroc2a. A study has to be done to determine the optimal values.

Todo :

- Study the optimal values
- Change the BOM of FEV to reflect this choose.

Who :

LLR team

17. Organise the code and documentation avaibility

Desc: The documentations and the codes are splitted on different repository and forge. Except the Pyrame/Calicoes project, no codes are in version management systems. None of these resources are available easily for the project crew. The idea is to deposit codes, schematics, layouts and docs in some git repository made accessible for any project member. A commit policy has to be written and diffused in the project in order to avoid unconsistant add-ons.

Todo :

- Setup a repository
- Migrate all codes and docs to it
- Give access to all project members

Who :

LLR team

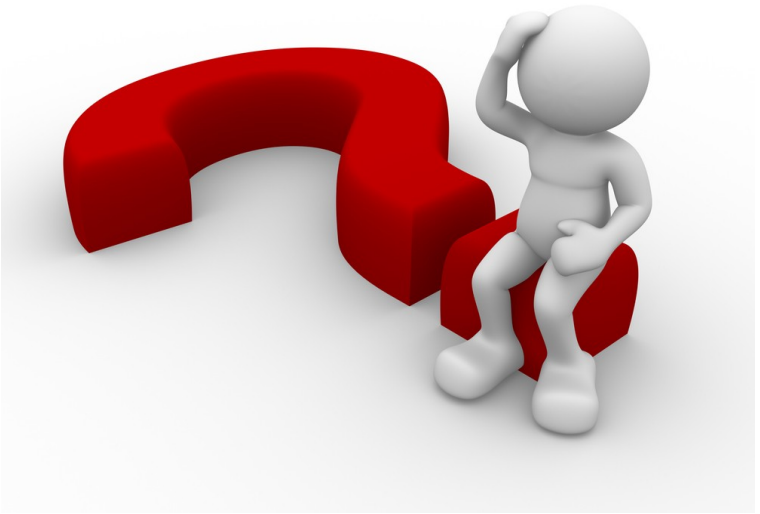
Status :

The repository has been created and populated for DIF code

Participation Call

- This program is very ambitious and the time slot is short
- Some task are unaffected
  - Noise study
  - Real-time temperature measurement
- If you are interested by these task, let me know
- For all other tasks, we are open to collaboration

Any questions ?



For any other questions
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