Retriggering analysis (etc.)

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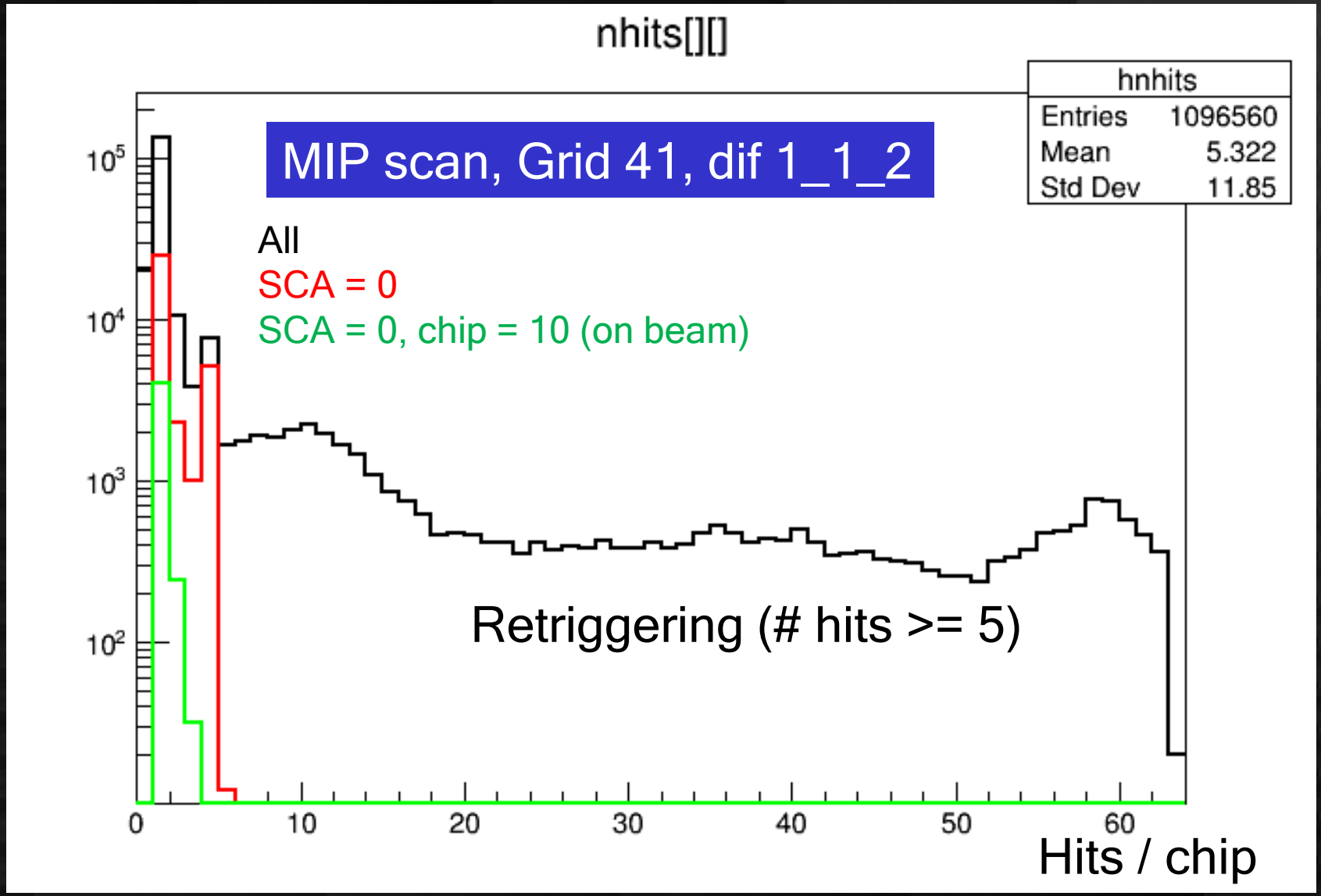
of hits


nhits[][]
hnhits
Entries 1096560
Mean 5.322
Std Dev 11.85
MIP scan, Grid 41, dif 1_1_2
All
SCA = 0
SCA = 0, chip = 10 (on beam)
Retriggering (# hits >= 5)
10^5
10^4
10^3
10^2
0
10
20
30
40
50
60
Hits / chip

of events (Grid 41, dif 1_1_2)

	All events	SCA = 0	Chip 3 or 10 (on beam)	Other chips (not on beam)
Empty event (0 hits)	20509 (9.5%)	10	13824 (11.7%)	6685 (6.8%)
Normal event (1-4 hits)	157589 (72.8%)	33595	102152 (86.8%)	55437 (56.1%)
Retriggering (>= 5 hits)	38517 (17.8%)	20	1756 (1.5%)	36761 (37.2%)
Total	**216615**	**33625**	**117732**	**98883**

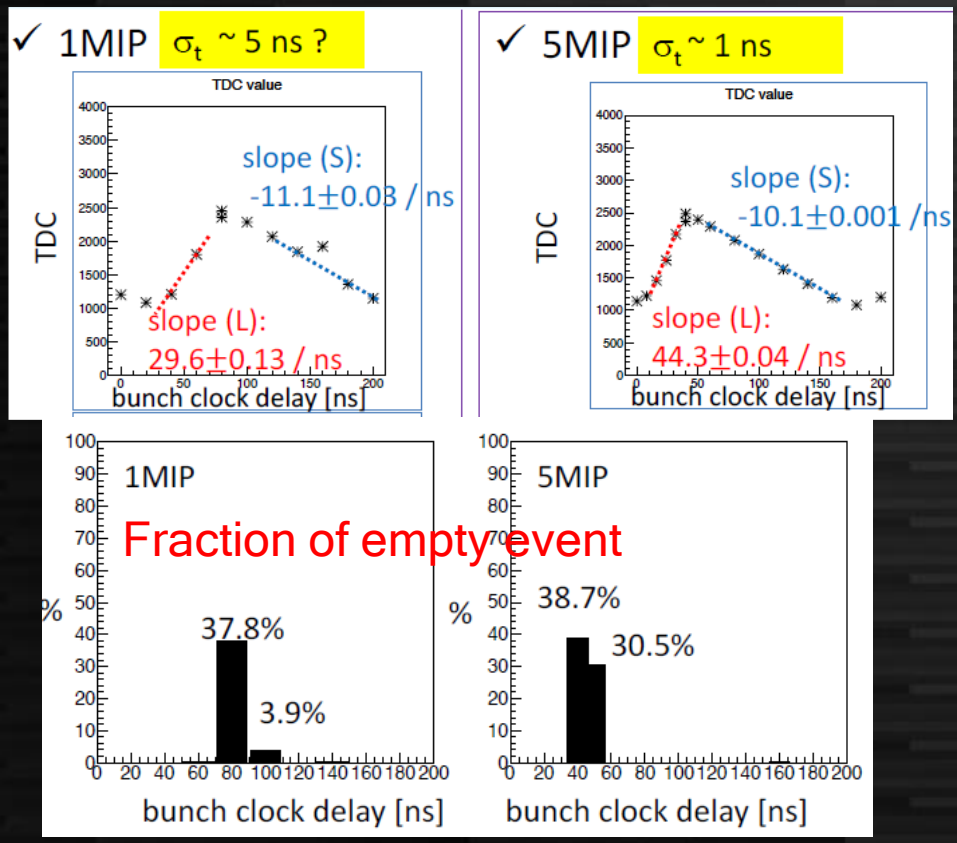
Chip 3/10 are full at around 1 – 1.5 cycle (4000-6000 bx)
Normal : Empty around 8:1 (not dependent on beam)
Retriggering occurs more in no-beam chips
(probably due to longer live time)

Empty event

Empty event occurs at the edge of BX clock

- "Trigger high" remains at the next BX → triggering at BX and BX+1
- Confirmed at testboard by variable delay (~10 ns range with SKIROC2A)

SKIROC2A with testboard



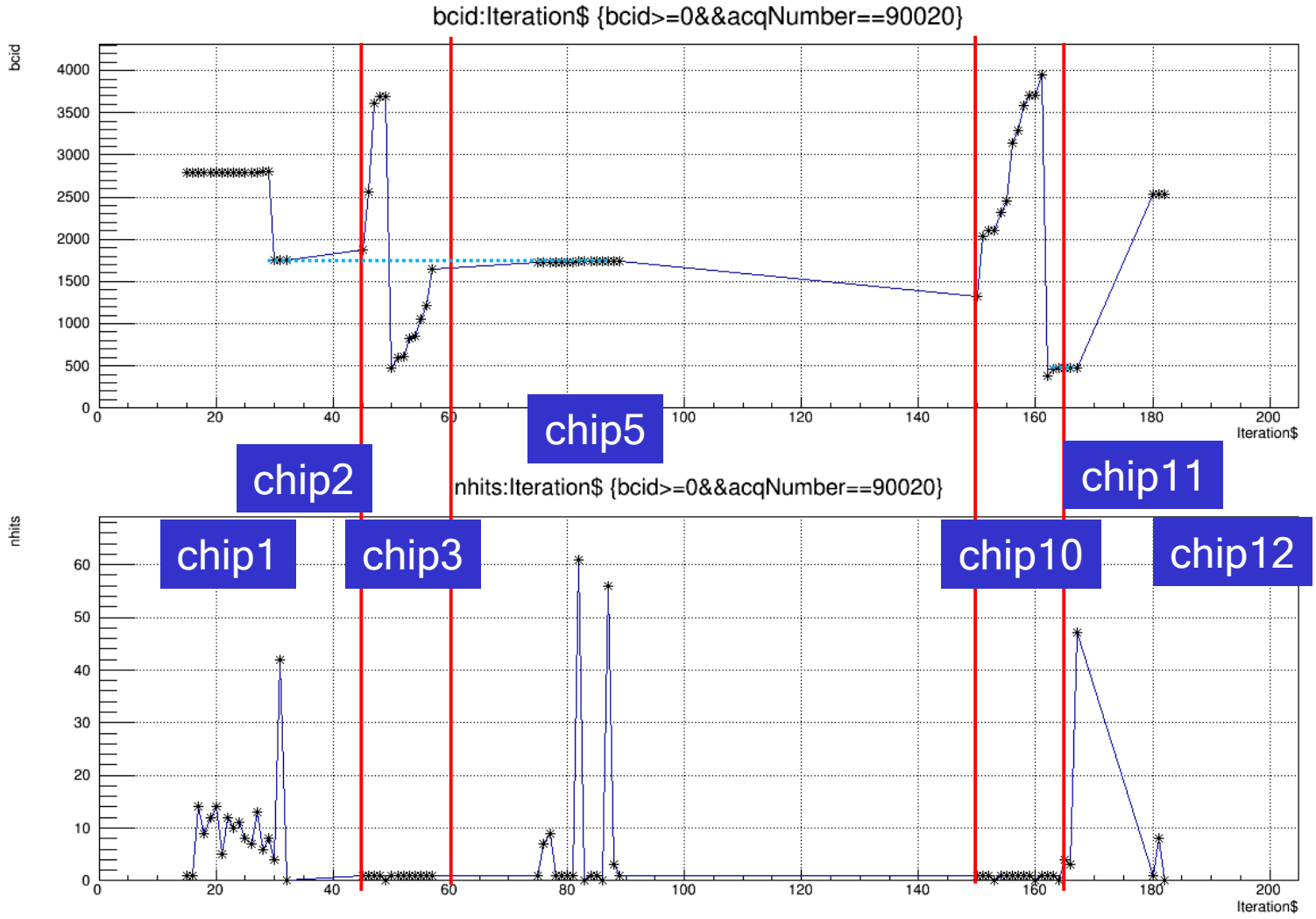
Practically OK for real ILC detector since we do not expect hits just before next BX

Retriggering

- Many hits at BX+2, +3, …
  - With usually no ADC fluctuation (only trigger is affected)
- Sometimes continue 5-10 SCAs
  → consumed up most of SCAs… harmful in real ILC
- Must be an issue to solve in ASIC or PCB
  - Should identify and improve in the next version

- Currently not seen in testboard
  - Still investigating
- Much better than FEV8
  - In FEV8 SCA>0 are hardly usable due to retriggering

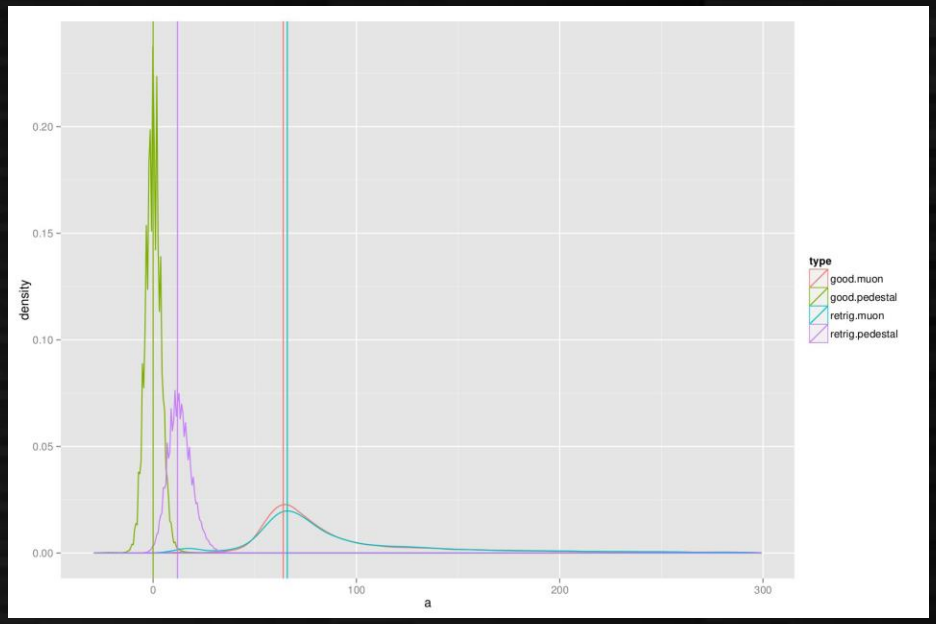
BX distribution on each chip



Relation on chip 2-5, 10-11?

Iteration = chip * 15 + SCA

Retriggering and double pedestal



Well known issues in BT2015
(V. Balagura, 21 Jan. 2016)

What causes “mode change” to right pedestal (then retrig.) is totally unknown

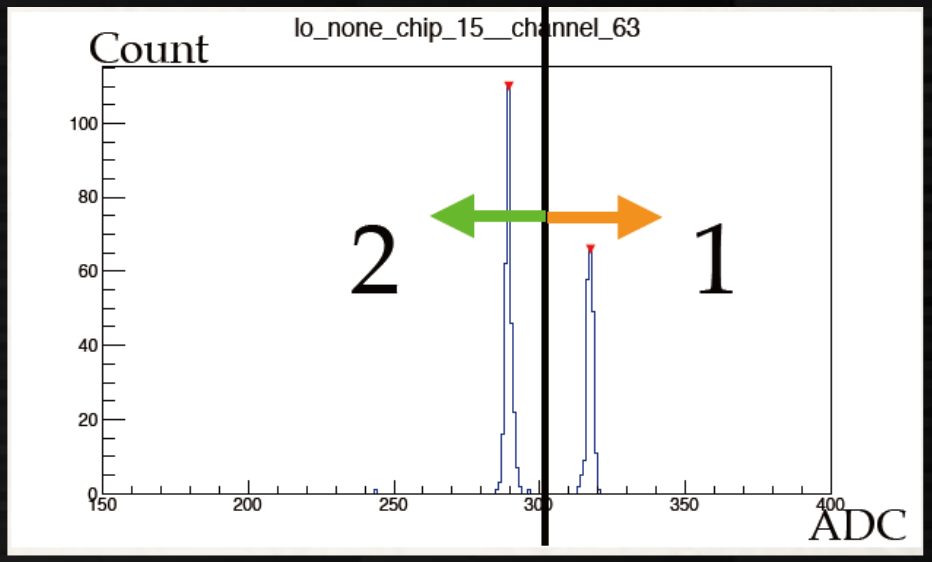
We have “double pedestal” in some of channels

What we found:

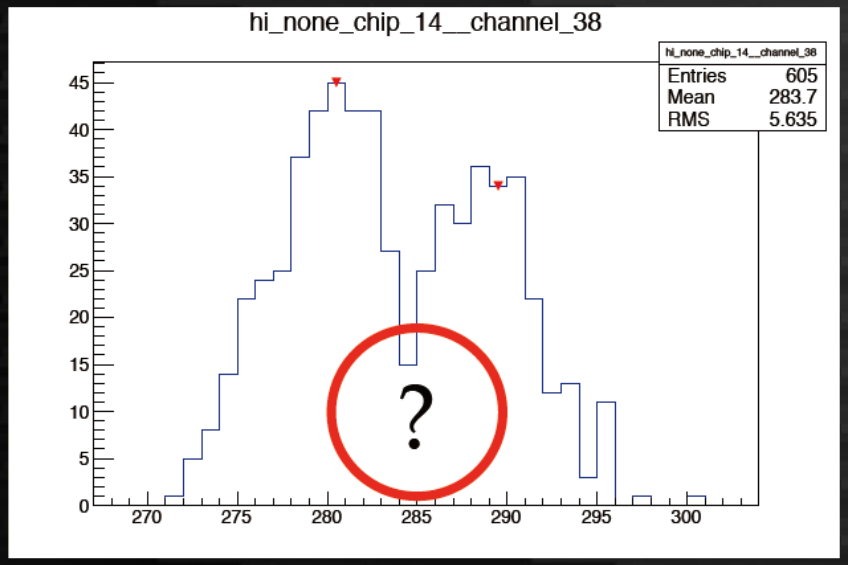
Retriggering occur after the “right pedestal”

Retriggering must not (100%!) occur after the “left pedestal” except “empty event” occurs

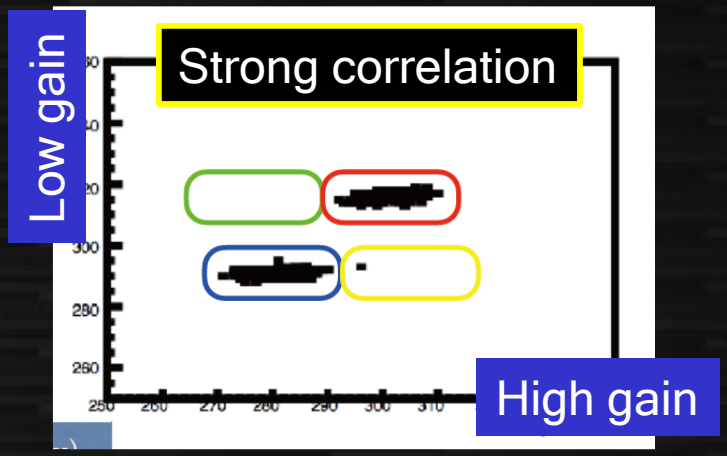
Reminder: double pedestal



Low gain: separation is clear (at least in SCA 0)



High gain: separation is not clear

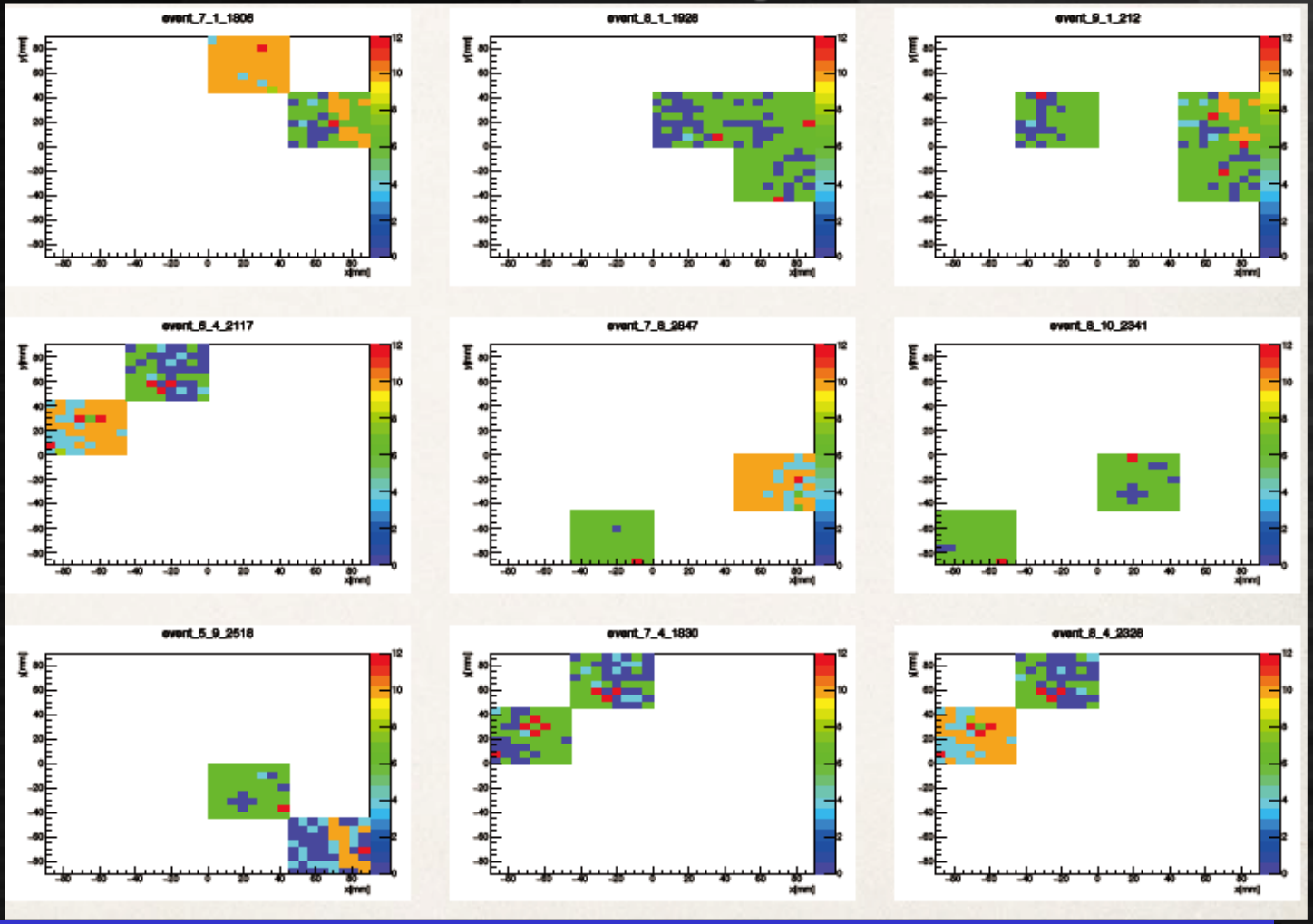


Difference on ADC at two peaks are similar in low and high gain

Difference on ADC by channels varies (0-30 ADC count)

Reminder: double pedestal

Red : hit point
Orange : Double pedestal & Right ADC
Green : Double pedestal & Left ADC
Sian : One pedestal & Right ADC
Blue : One pedestal & Left ADC



Pedestal position (L/R) inside the chip is highly correlated but no strong correlation seen among different chips

Retriggering and empty event

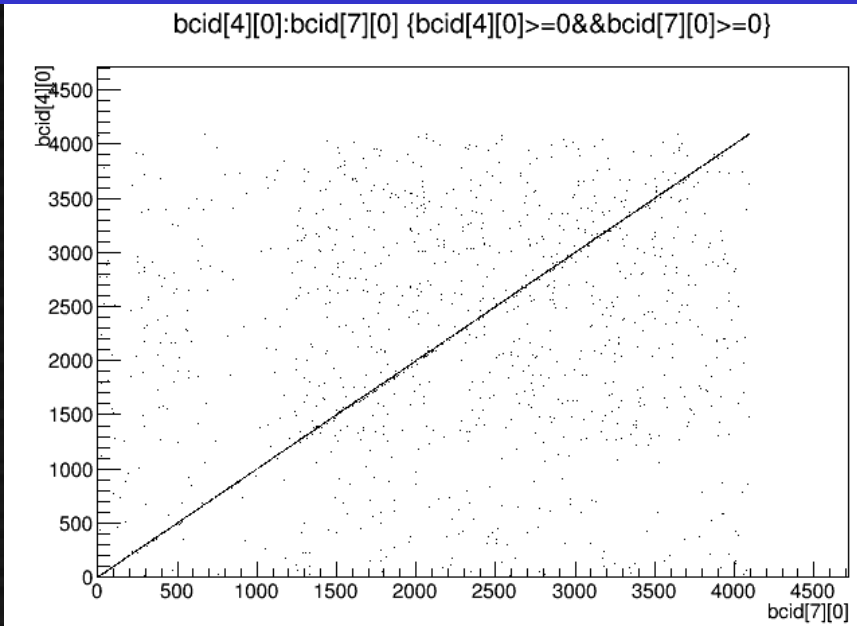
grid41, dif1_1_2, chip0										
Total events	Pedestal at SCA=0		nhits @ SCA=1 (upto BX+5)		BX @ SCA=1		Pedestal at SCA=1		nhits @ SCA=2 (upto BX+5)	
907	left	519	no event	437						
			0	79	BX+1	79	left	56	no event	55
					BX+(2 to 5)	0			0	0
			1 to 4	3					1 to 4	1
			>=5	0					>=5	0
	right	388	no event	14			right	23	no event	0
			0	1					0	0
			1 to 4	94					1 to 4	6
			>=5	279					>=5	17

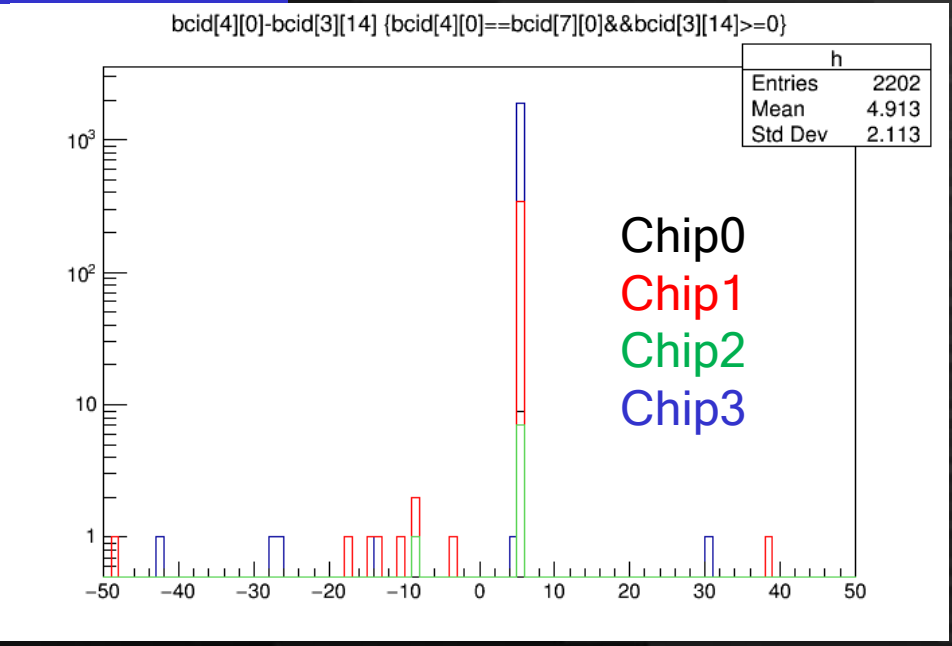
- Chips not on beam (to get more “right” pedestal)
- “Left” pedestal at SCA=0: mostly no event and empty event
- “Right” pedestal at SCA=0: mostly retriggering (have to check the 15 events without retriggering)
- 30% of empty events go to “right” pedestal at SCA=1
- “Left” pedestal at SCA=1: no event (except 1)
- “Right” pedestal at SCA=1: retriggering at SCA=2

Empty event can change the pedestal state

Additional: correlation with others

Grid 41, DIF 1_1_4
Correlation is weaker in other DIFs, but still exists





Bcid[4][0] and [7][0] are highly correlated

Correlation between bcid[][14] and bcid[4][0] (==bcid[7][0])

Chip 4 and 7 are often fired 5 BX after some chip comes to full
→ “busy” may cause some effect

Summary & plan

- Understanding what causes retriggering (and mode change of pedestal) is essential
  - To fully activate DAQ during beam in ILC
  - Empty event can cause mode change (but other reason also exists)
  - If we got some idea on the cause we can try to improve PCB or ASIC on the next version
- Try to reproduce the retriggering in testboard
  - Removing capacitance to be compatible with FEV
- Try to study retriggering with FEV with cosmic/RI
  - Plan to export two slabs to Japan