SiW ECAL
2017 Beam Test Analysis meeting:
DQ & performance

A. Irles, 14th September 2017

Outline

- Masked channels
- Data integrity checks
- Collective/cross talk effects
- Some comments on double pedestals
  - see next talk for more details !!
- Time correlations:
  - Single slab (before even building)
  - Full proto (event building)

Masked channels summary

- Layer 1, Slab 21 → 43.4% (one wafer)
- Layer 2 – 6 , slabs 16,-21 ~6-8%
- Layer 7, slab 22, ~ 16% (one chip)

- 5% are masked manually just before starting the commissioning → same patter in all slabs:
  - Chn 37 in all chips,
  - Chn 41-53, chips 1,9
  - Chn 5, chips 0 and 8
  - Chn 3, 9, 10, chip 7 and 15

- Total # of channels available: 6204 (87%)

Data itnegrity

RAW2ROOT.C : Data Integrity checks

- The root macro checks the data bytes and headers.
  - If additional word is found: warning message and shift of the counter
  - If no additional word is found but spill candidate packet has wrong length (in words) → error message and reject spill candidate (count)
  - Else: if bad number of columns → error message and reject spill candidate (count)
  - Else: if bad chip id → error message and reject spill candidate (count)
  - Else: if error in bits → error message and reject spill candidate (count)

    In this case, we also save (if possible) the bcid andsca were the error happened

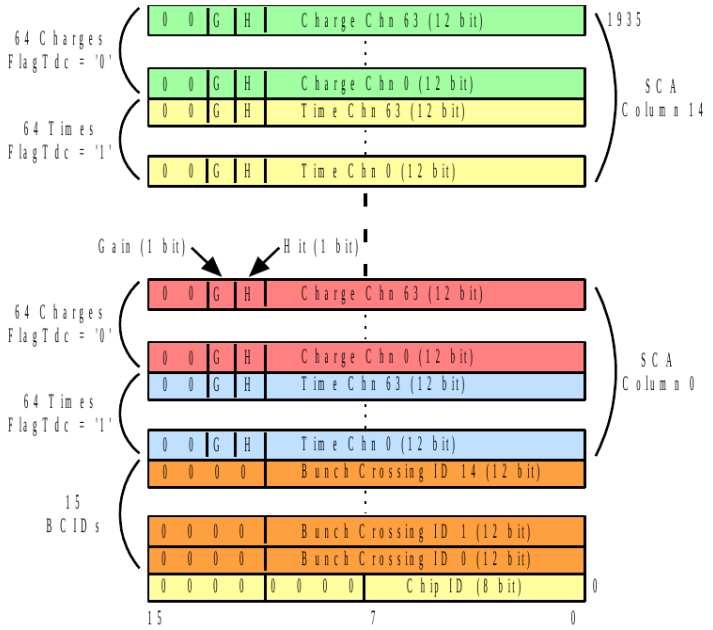
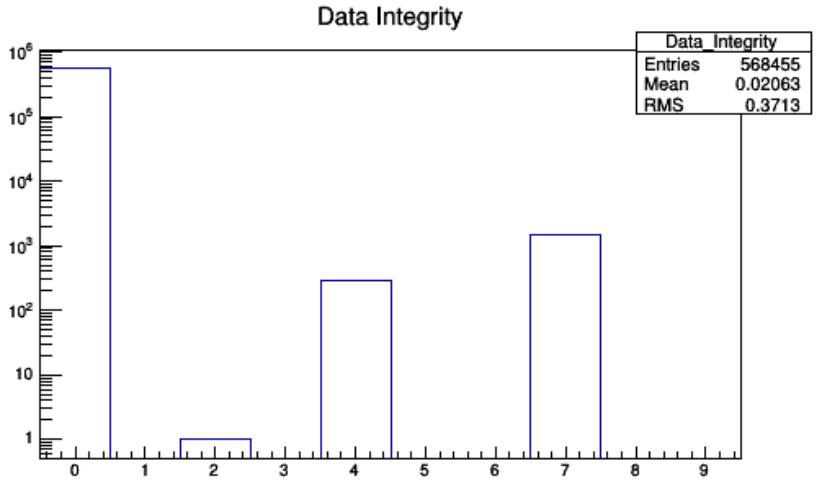


Figure 15: SKIROC2 chip memory mapping

RAW2ROOT.C : Data Integrity checks

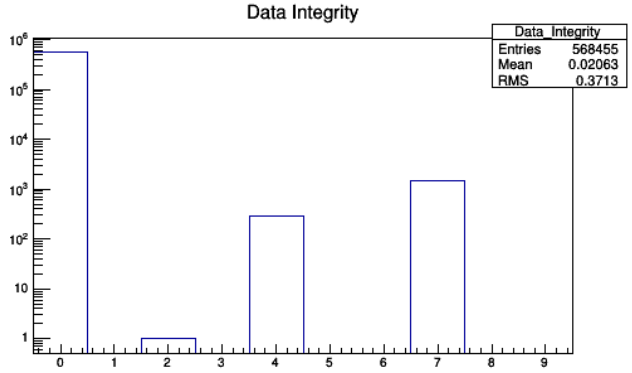
- Data Integrity histogram (spill based):
  - value = 0 --> OK
  - value = 1 --> bad data size
  - value = 2 --> more than 15 memory columns
  - value = 3 --> bad chip number
  - value = 4 --> extra bits in BCID (>12)
  - value = 5 --> extra bits in LOW GAIN charge/hbits --> expected 13 bits, no more. The 14th is for autogain mode --> not used
  - value = 6 --> extra bits in HIGH GAIN charge/hbits --> expected 13 bits, no more. The 14th is for autogain mode --> not used
  - value = 7 --> hit bit from high gain != hit bit from low gain
  - value = 8 --> Bad number of columns or bad number of channels
- Error tagging is not cumulative: if bcid is wrong but hit bit s also wrong, the event is tagged as hit bit wrong.
- Saved in the .raw.root file

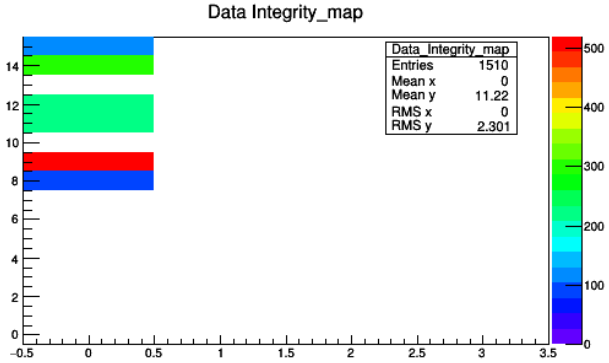


Example for layer 1 (slab 21):

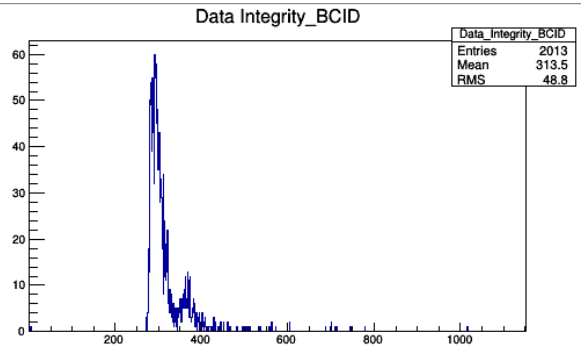
Full mip scan

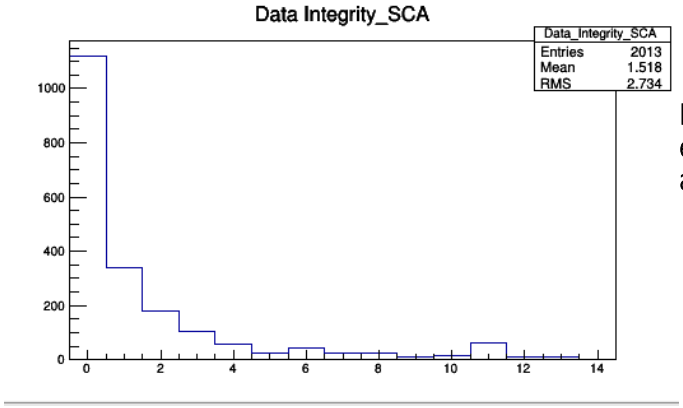
RAW2ROOT.C : Data Integrity checks





Chip channel map (but if error appears in the first channel, then we stop counting)



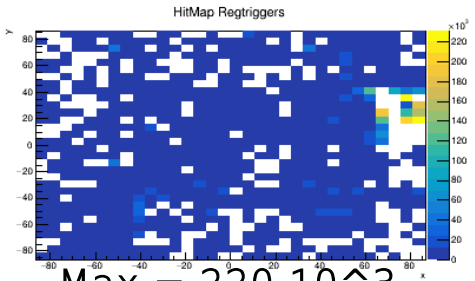


BCID spectra for rejected events looks very similar for all slabs → shifting bit ?

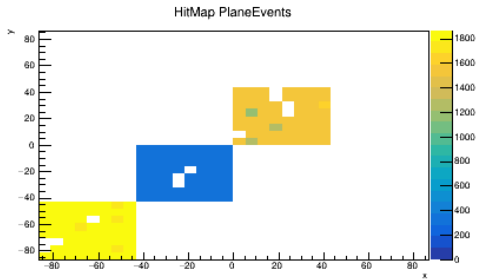
Example for layer 1 (slab 21):Full mip scan

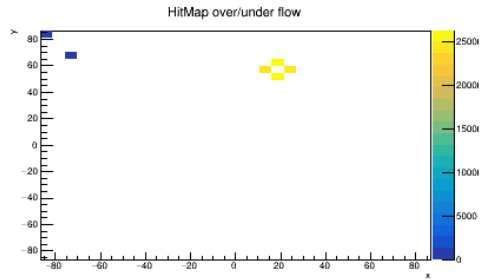
Cross talk issues

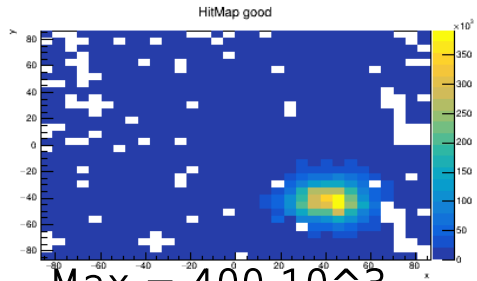
Issues observed: adc4/retriggers/plane events



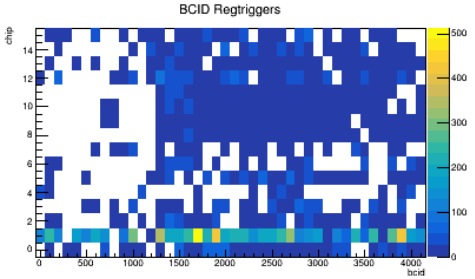
Max = 220 10^3

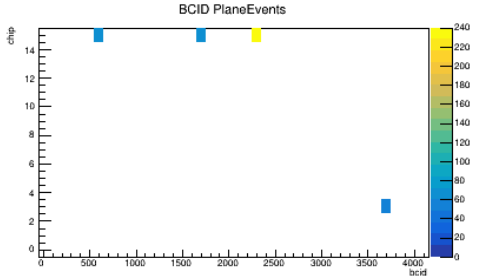


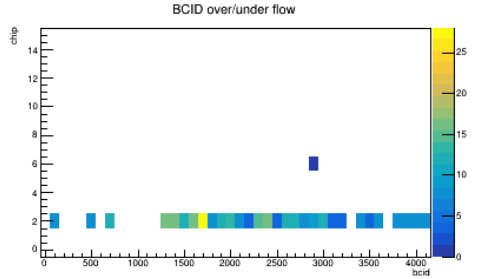


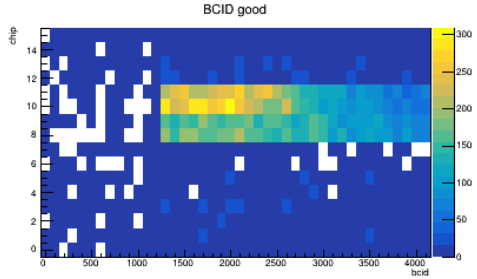


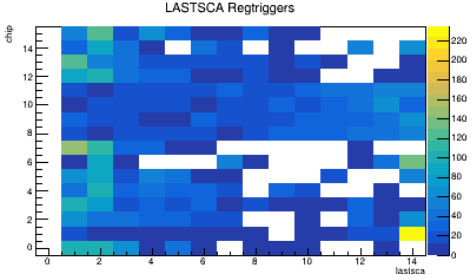
Max = 400 10^3

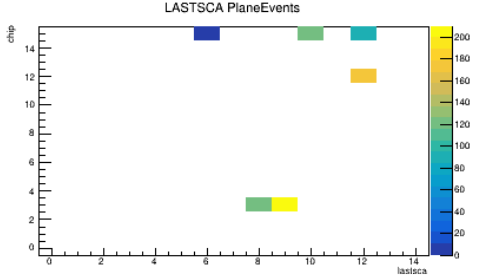


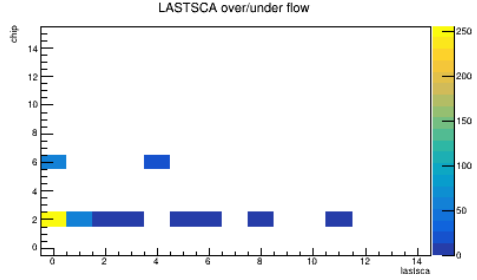


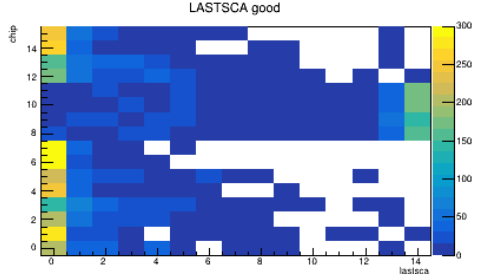












Issues observed: adc4/retriggers/plane events

- Retrigger rates in the beam spot are consistent with the BCID+1 issue:
  - ~ 15% rate (not easy to see in the plot, I agree)
  - Last sca filled for retriggers is randomly distributed for chips in the beam spot (10,11,12,13) Similar situation with pedestal (double peaks associated to retrigger, see backup)
  - Last sca filled for retriggers far from the beam spot = 15. Not BCID issue.
- From other monitoring plots, I see that Plane Event and Retriggers have very similar signatures (high threshold for these plots= 32 channels)
- Crosses are always ADC=4 related.

Issues observed: adc4/retriggers/plane events

- Collective/cross talk effects ? Skiroc2 is too sensitive to noise in the preamp/analogue part of the chip (baseline shifts) → retriggers ? Adc =4 entries ?
  - During important phase of the precommissioning: the BCID2050 and noise/adc4 issues were convoluted and not properly understood → need new studies.

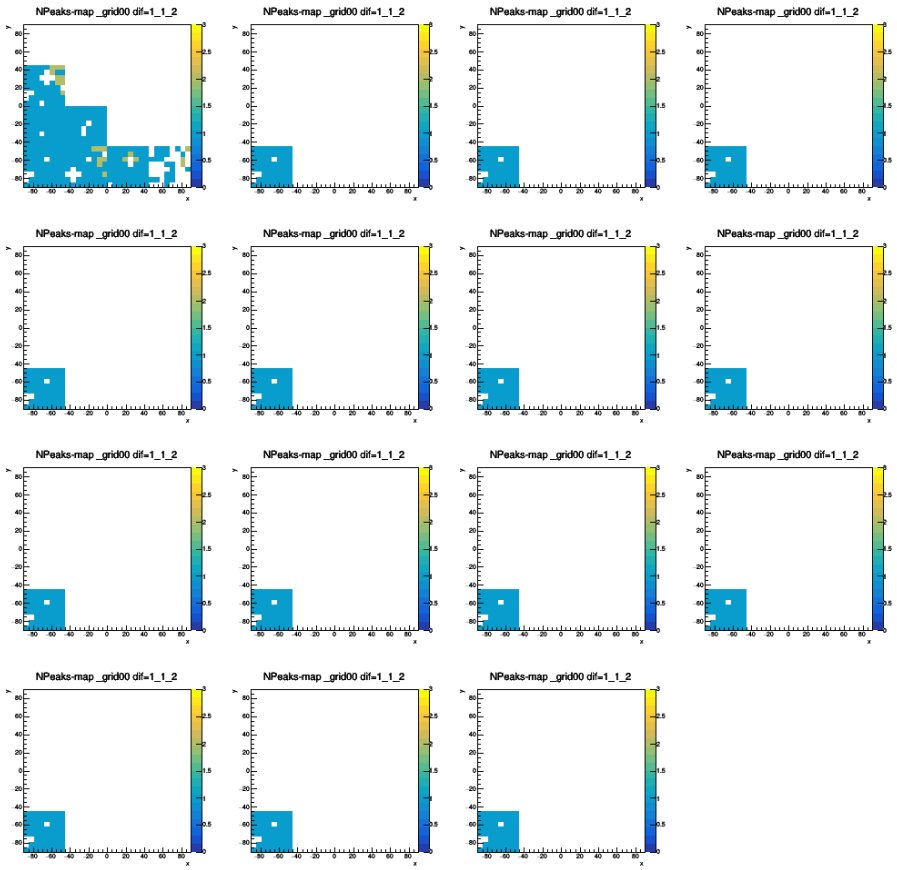
- FEV11 shows some shortcomings but not showstoppers.
  - Nothing prevent us to make physics, as seen during the beam test.
- See last talk of this session (beam test results)

Double pedestals

- Only some preliminary results, see next talk for more details.

Pedestal npeaks maps (filtered events)

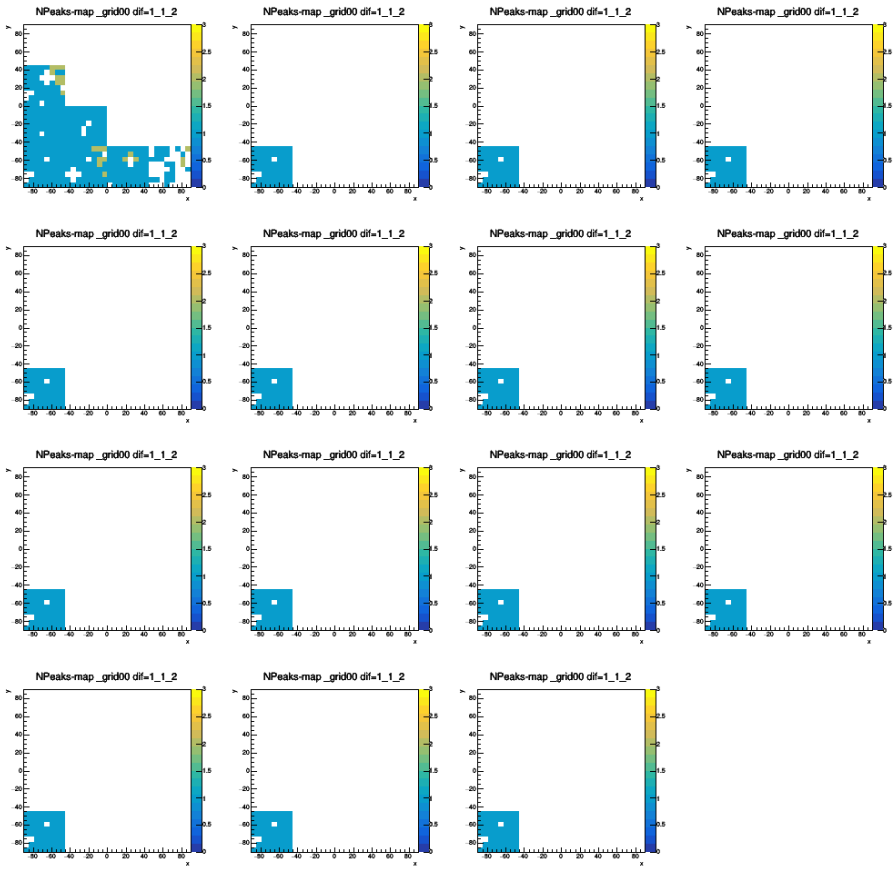
Grid 0, dif_1_1_2



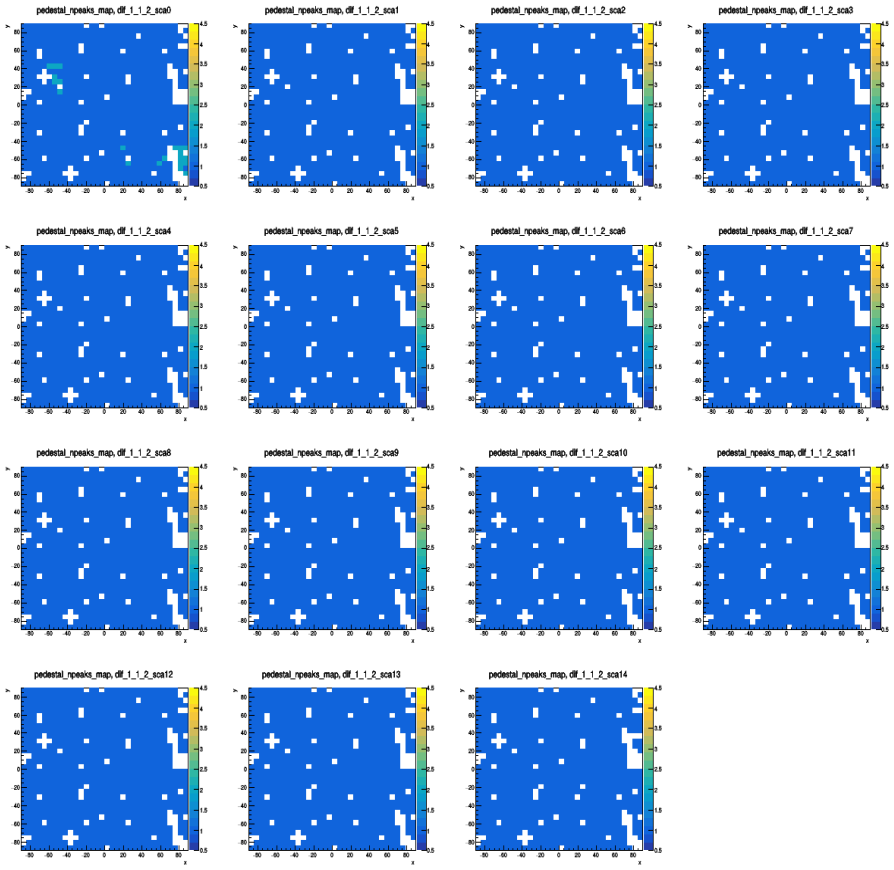
- 15 x-y maps (one map per SCA)
- Only one MIP scan run (grid 0), Layer 2 (dif_1_1_2)
  - Similar for all layers
- Masked channels are removed from the analysis
  - Mask means: disabled trigger and disabled preamps.
- For the calculation of the pedestals:
  - We only save the pedestal information if we have enough statistics in ~ all SCAs
  - i.e. in this example, we will only save the pedestal information for chip 15 (left bottom corner)

Pedestal npeaks maps (filtered events)

Grid 0, dif_1_1_2

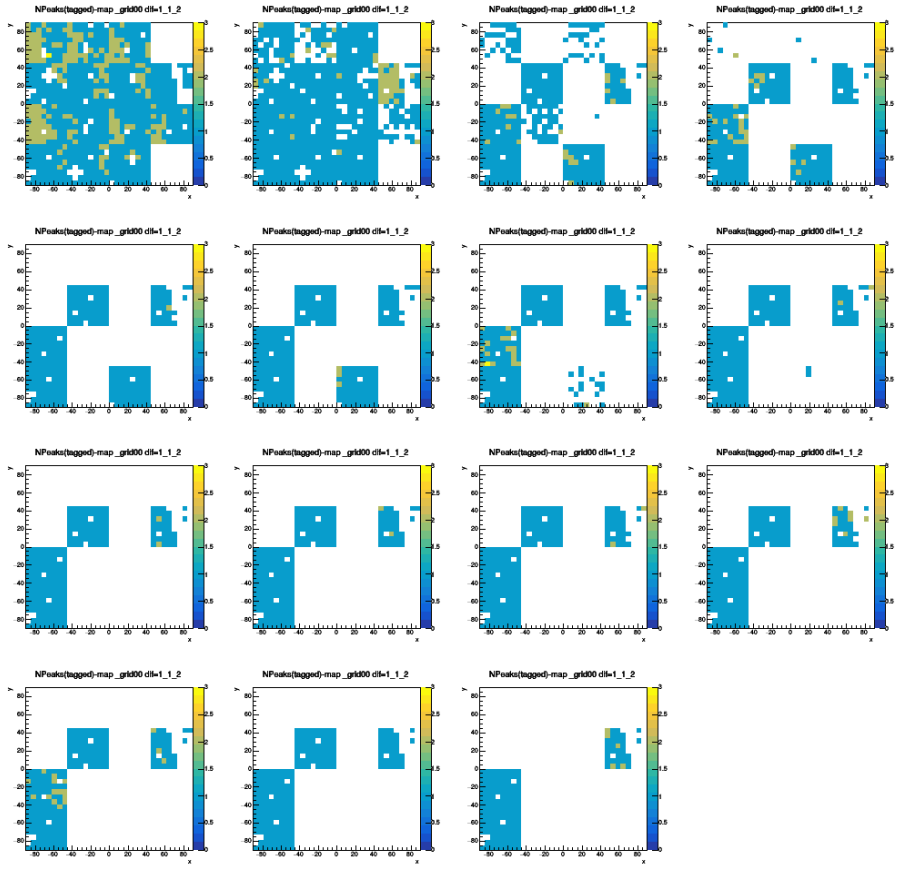


All grid points, dif_1_1_2

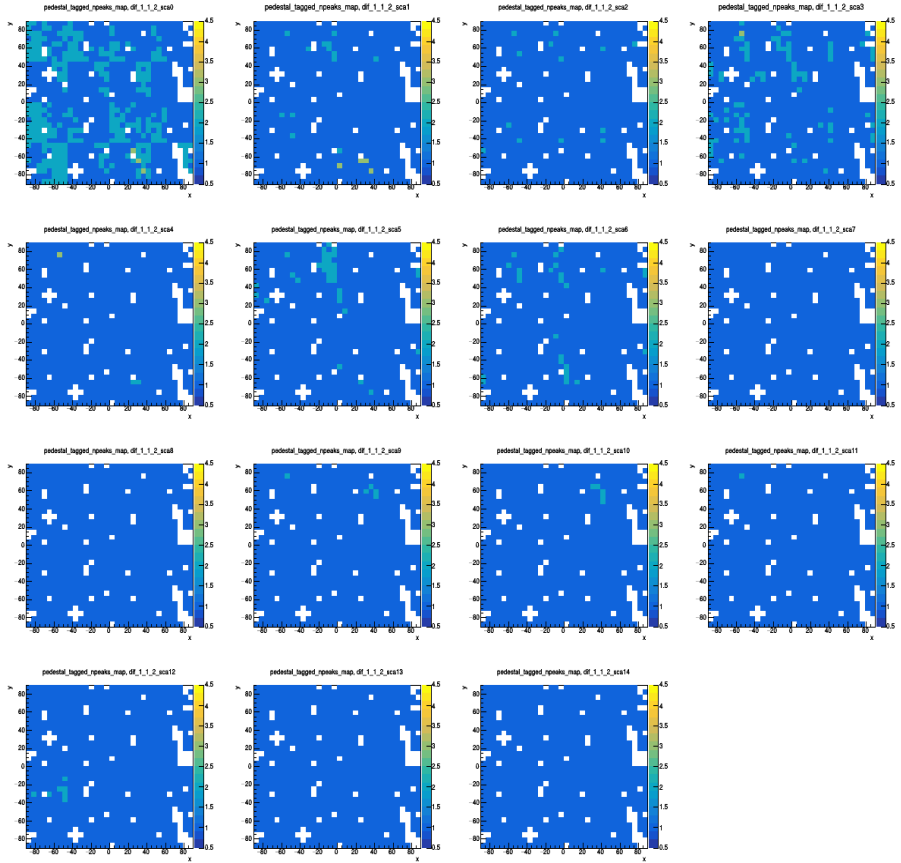


Pedestal npeaks (bad events) maps

Grid 0, dif_1_1_2

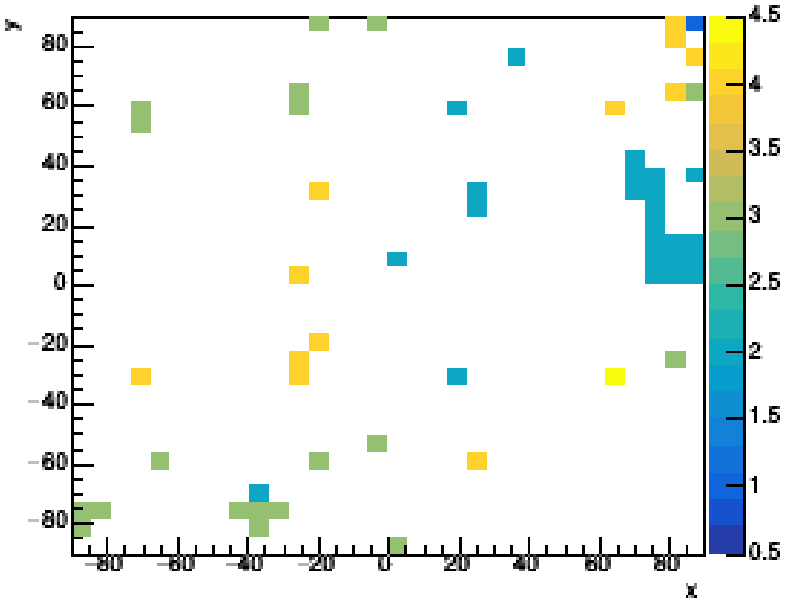


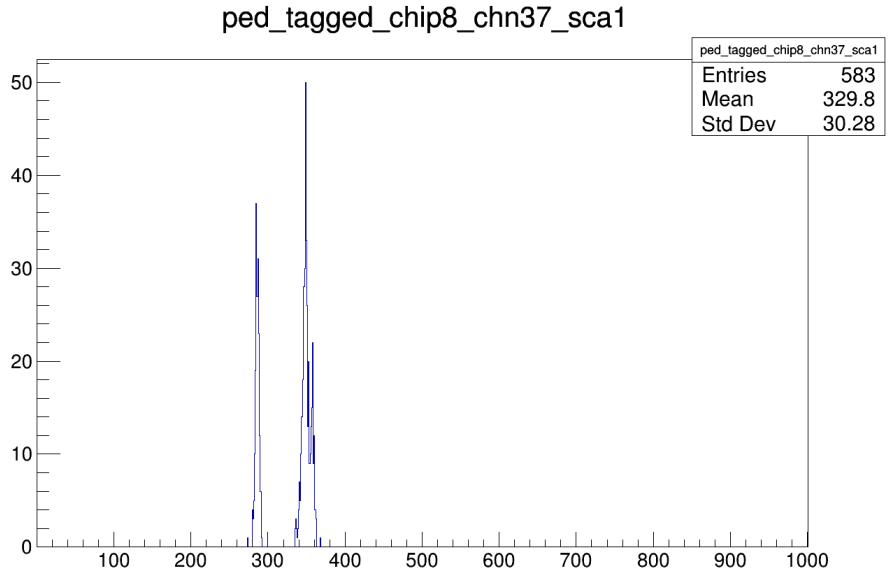
All grid points, dif_1_1_2



Pedestal npeaks maps

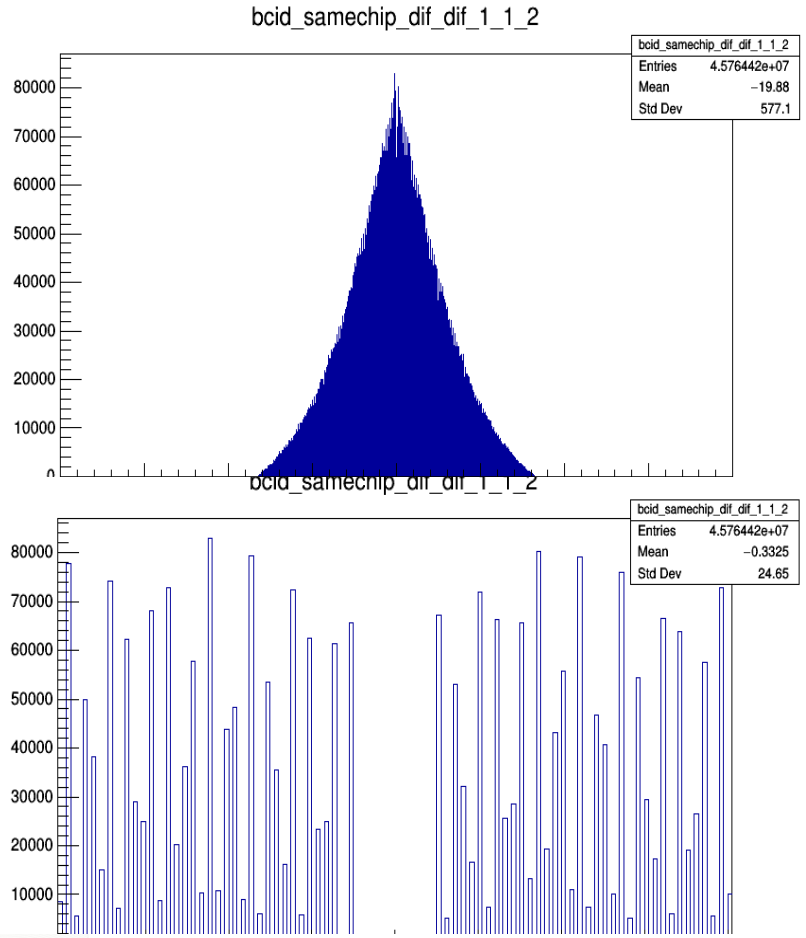
- Expanding the analysis to the masked channels (disabled preamps):
- Double pedestal happens also with disabled preamps





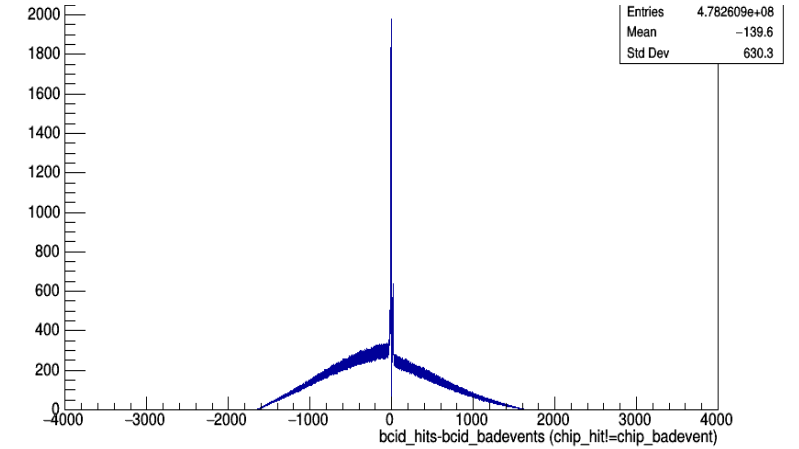
Good event/bad events time correlations

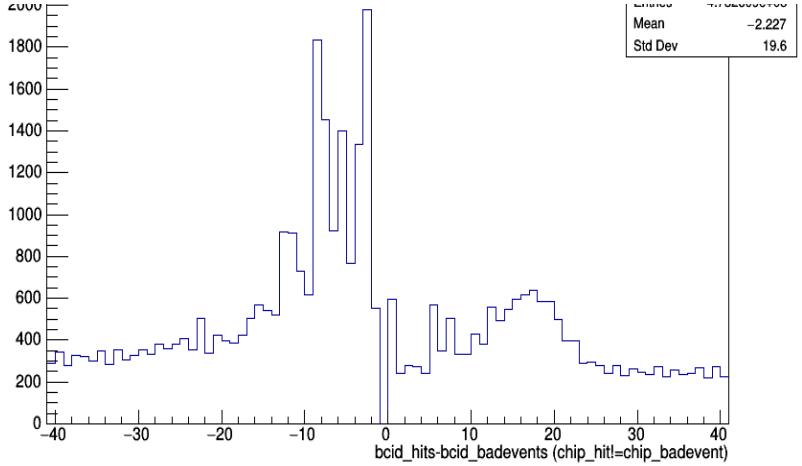
Retriggers & plane events: time correlations for single slabs



- Dif_1_1_2, grid41
- Selection:
  - Good hits are selected firstly.
  - Then, bad hits are search in **THE SAME chip, different channel** were the good hit was generated
  - bcid are compared (within a spill)
- Bad hit == retrigger and/or plane event or origin of retrigger
- In the same chip, there is no correlation between triggers and following retriggers
- Gap of +- 15 bcid due to offline definition of retrigger.

Retriggers & plane events: time correlations for single slabs

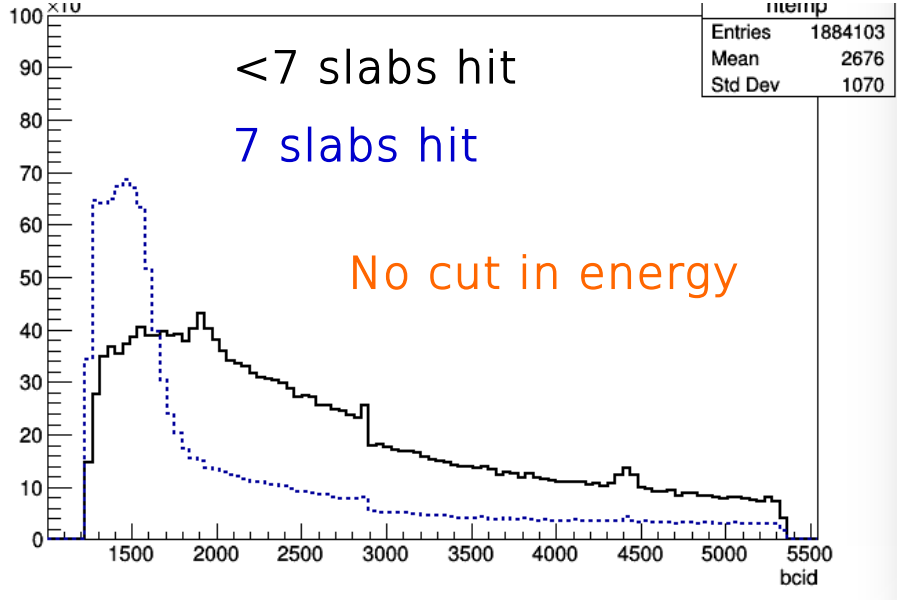


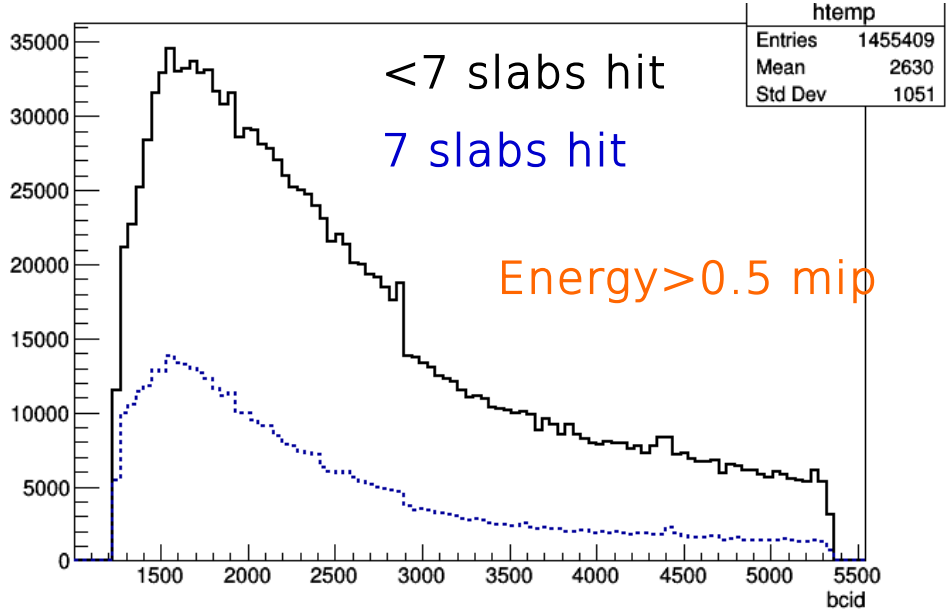


- Dif_1_1_2, grid41
- Selection:
  - Good hits are selected firstly.
  - Then, bad hits are search in **A DIFFERENT chip** were the good hit was generated
  - bcid are compared (within a spill)
- Bad hits == retrigger and/or plane event or origin of retrigger
- Pattern: ~3,6,9,12,15 bcids after a hit, we see retriggers in other chips
- Also a bump of bad events happening before the good hits ?
  - To be understood.

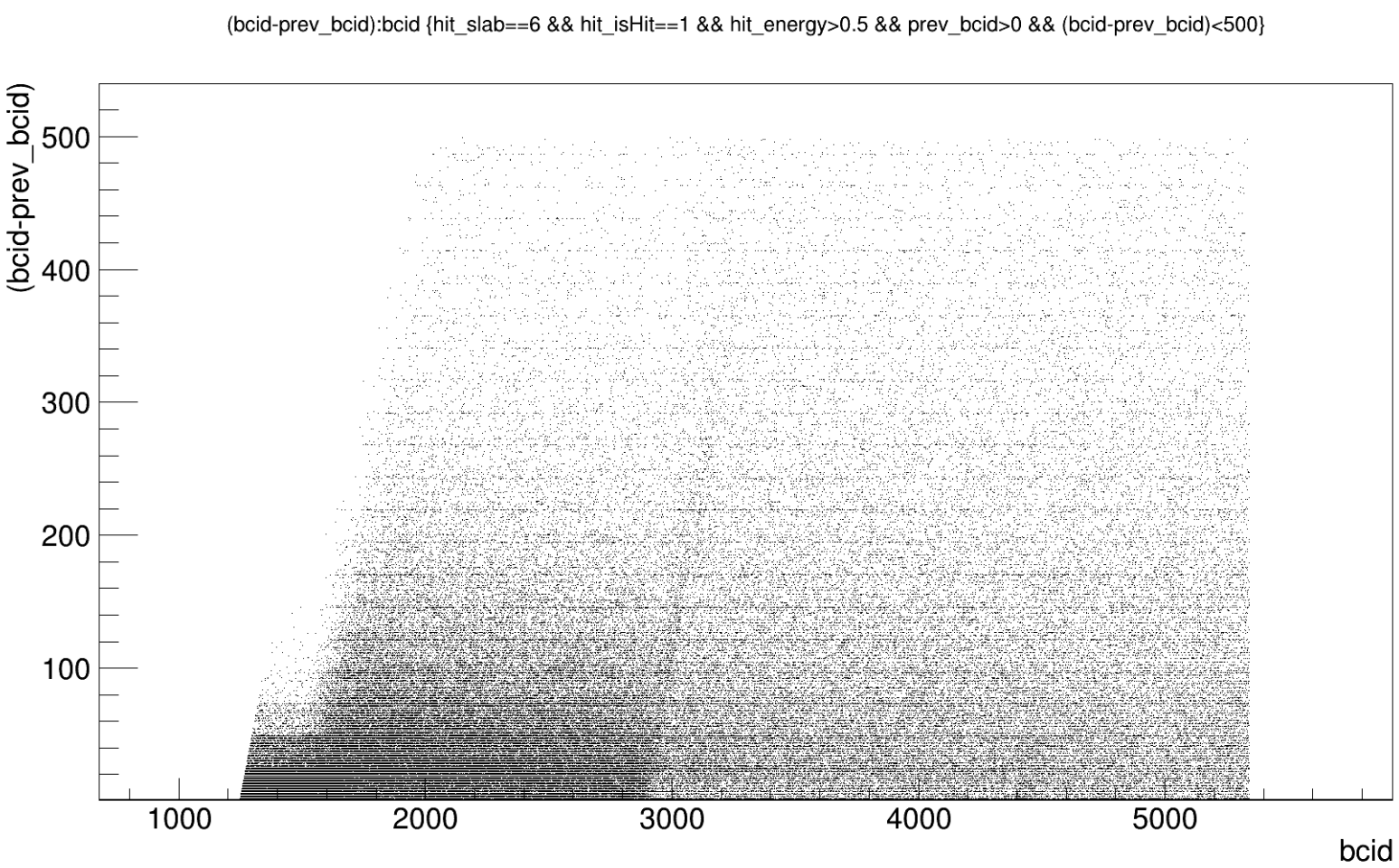
Time correlations after even building and filtering

- Filtering is done (retriggers/plane events)
- Basic event building within a spill (bcid merging for all chips in all slabs).
- Results for 4GeV showers
- Very simple analysis using root ntuples

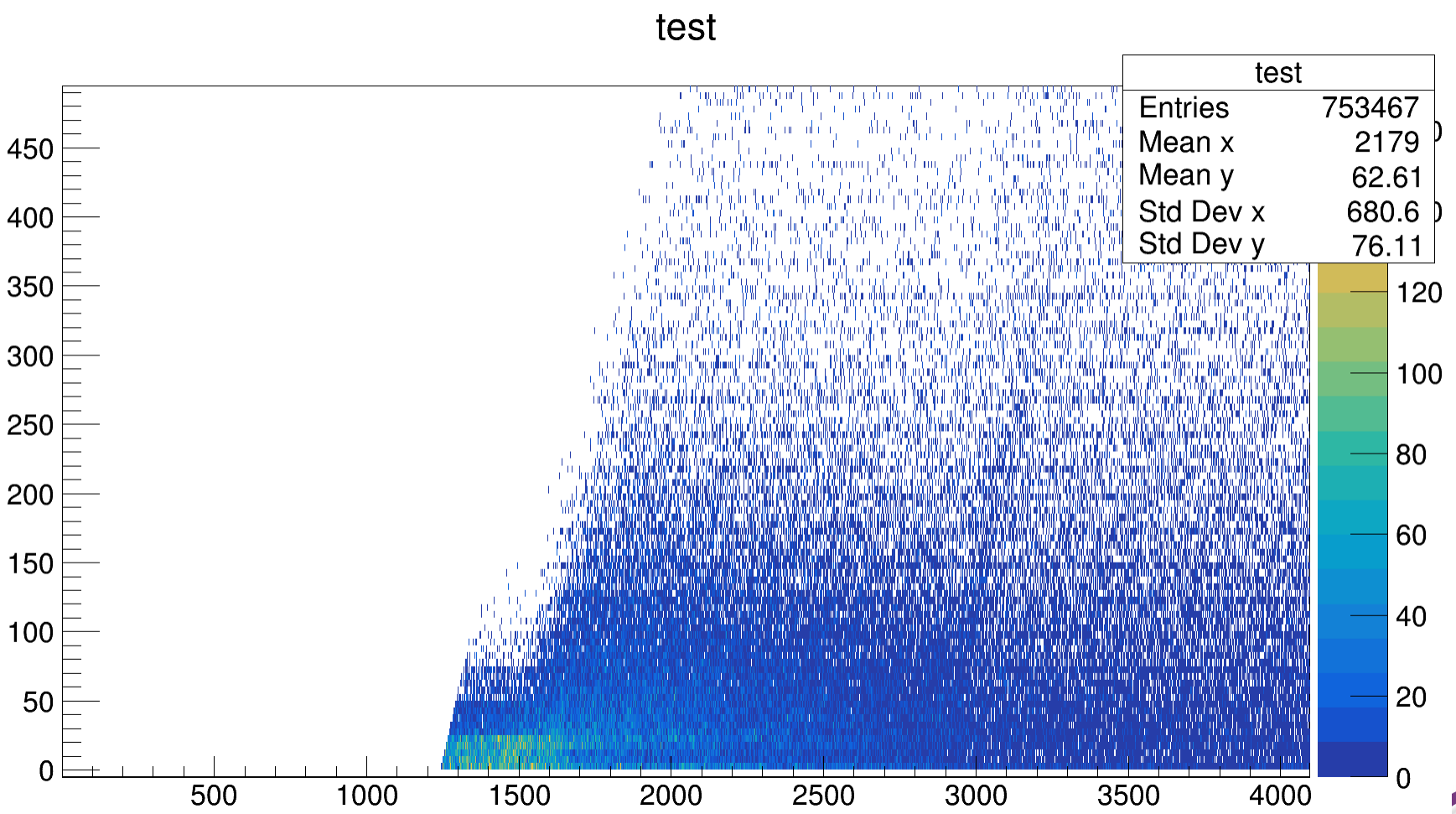




Time correlations after even building and filtering



Time correlations after even building and filtering

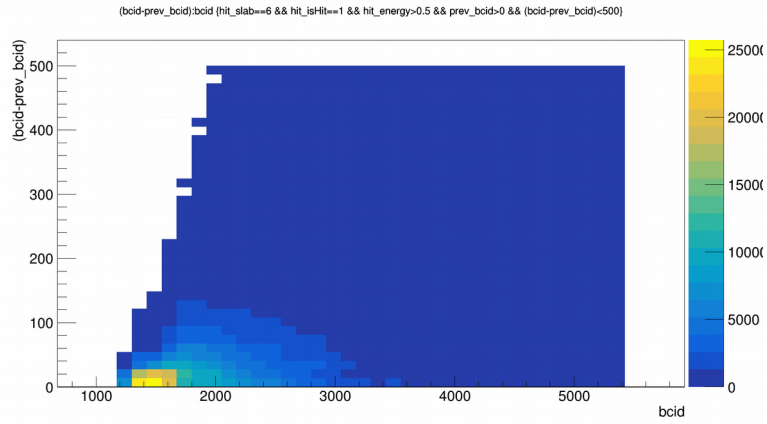


Time correlations after even building and filtering

- Diagonal line starting on bcid ~ 3000
  - This is when the noise burst happen.
  - Cut during analysis.

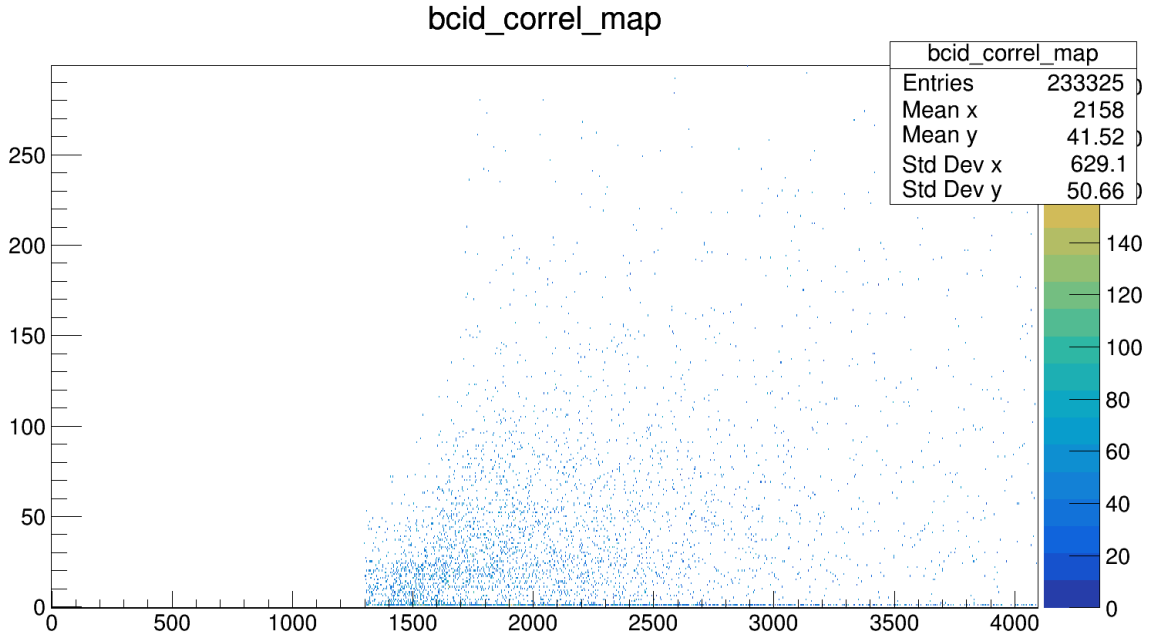
- Is there a pattern every 25 bcids = 10 us ?(bcid-prev_bcid = ~25,50,75,100…) ?

- Most of hits are separated by 1500 bcid = 600 us → 1.7 kHz (~beam rate)



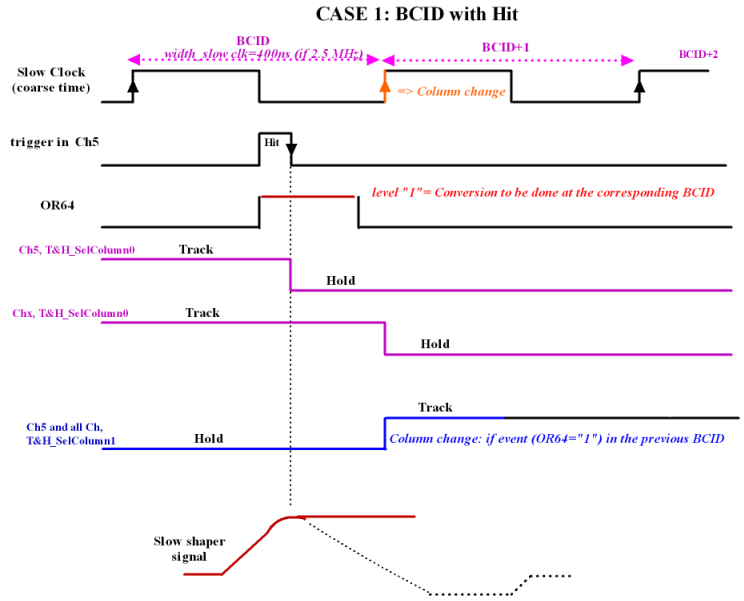
Time correlations after even building and filtering

- Same but doing a proper analysis requiring all 7 slabs with good hits
  - Good hits are defined as non-isolated hits with energy > 0.5 MIP in events where all slabs have these good hits
- Hint that the pattern is associated to some “internal” source

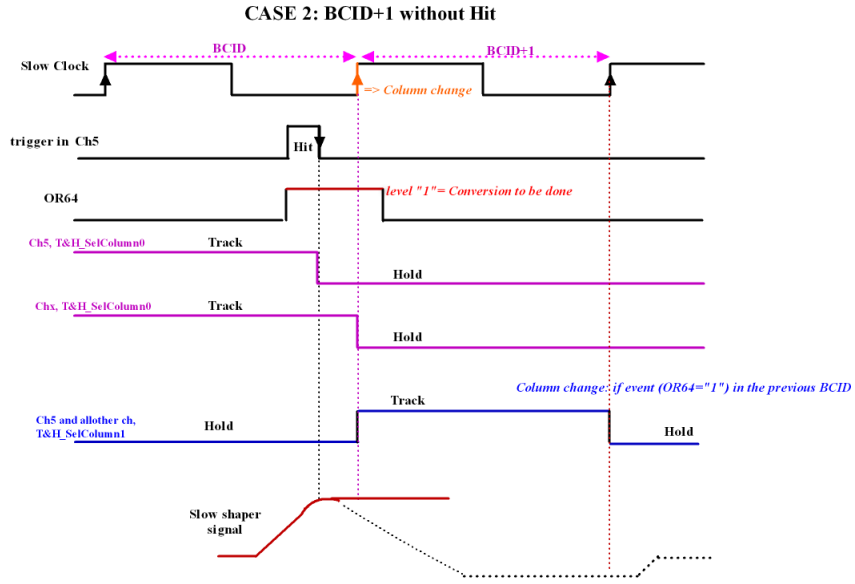


Back up slides

BCID+1 events



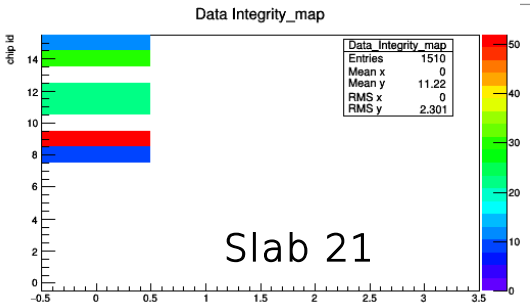
Conversion: BCID with one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal, other SCAi= ped
BCID+1: No conversion because OR64 level=0 during this BCID+1

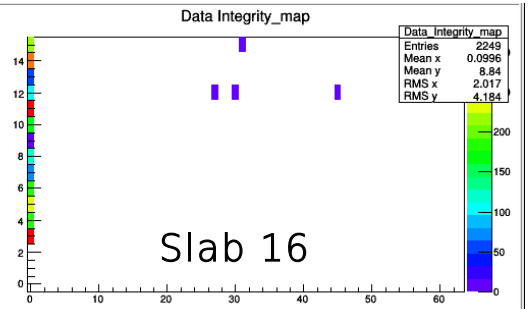


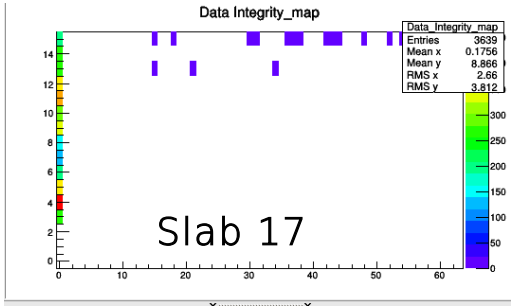
Conversion: BCID, one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal
BCID+1, no hit, SCA1 ch5 holded value=value < pedestal or pedestal, other SCA1 holded value=ped.

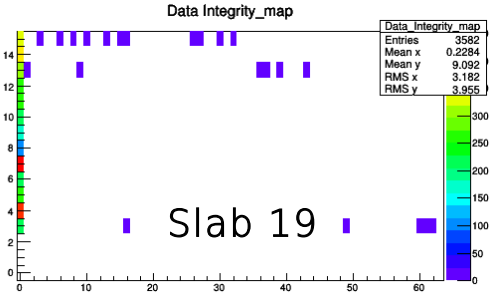
- This are not bad events !!
- Next SCA (NSCA+1) is filled with a zero, but SCA=NSCA is usable → not remove from analysis !
- ~ 15% of chances of happening (reduced to ~0 in skiroc2a)

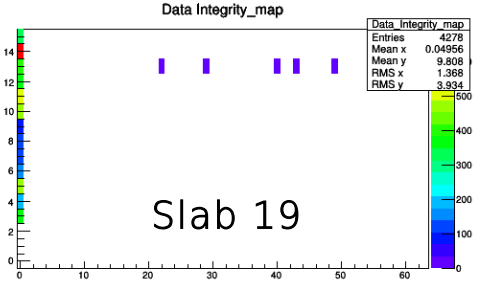
RAW2ROOT.C : Data Integrity checks

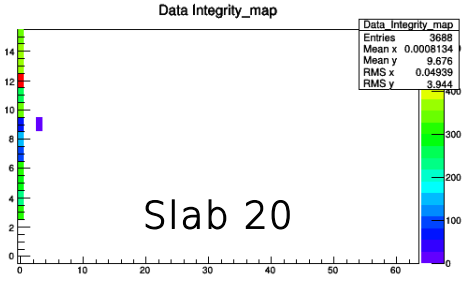


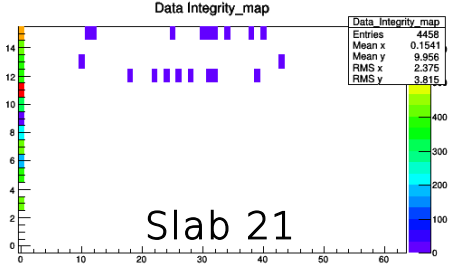












Why there are no errors in chips 0,1,2 ?

Are these chips superseeded by other sources that are not chip-taggable (i.e. bad number of columns, bad chip id, bad number of words) ??