SiW ECAL Technical report from 2017 Beam Test

- Outline/purpose of the meeting
- New actors:
  - Slab/prototype commissioning for physics
  - New DAQ → super nice scripting capabilities and DQM !!
- TB report
- Issues: BCID 2050, ADC=4, retriggers (collective effects?)
  - In fact very similar situation to 2015 and easily avoidable issues.
- To do / next steps ?

https://twiki.cern.ch/twiki/bin/view/CALICE/SiWDESY201706

A. Irles

LLR, Palaiseau 11th July 2017

Outline / purpose of the meeting

- **We should congratulate ourselves for the very successful beam test**
  - Nice team work: Kyusu/LAL/LLR/LPNHE/OmegaLLR/SKKU
  - Hard work before and during beam test

- **Signal came “before” noise** (MIP spectrum, MIP homogenety, pedestal stability, shower profile studies on site)

Outline / purpose of the meeting

- We will conclude (next slides) that we **had a succesful testbeam** with nice data to analyse and make physics (linearity, response homogenity, etc) but
- the technical purpose of this previous beam test was to serve as **commissioning beam test**:
- to **gain experience running the detector** (from the expert to the shifter level)
- to **prepare ourselves for more exciting beam tests:**
  - Cern beam test with combined with a hadron calorimeter
  - Combined beam test with a telescope
  - Even a standalone beam test with ~20 layers and hadron beam sounds exciting from the physics and engineering points of view.: test sk2a in a system level experiment, real case online monitor, full e-calorimeter detector running…
- …
- This meeting purpose is to collect all acquired knowledge to discuss the next steps

New Actors

- Commissioning: preparation and exhaustive test of the slabs for physics
  - Conservative approach (for the masking, thresholds) for the single slab commissioning.
  - More realistic for the full prototype commissioning,
  - Clearly improvable (scripting, documentation, integration with in pyrame etc) but efficient.
  - Wafer information is still missing
- Once that we set the beam on, the configuration from the passport were almost unchanged during the 2 weeks. Only some remasking done during the MIP scan (~10-50 channels in total)
- New DAQ pyrame/calicoes3 and Frederic in the beam hut with **time** to debug it.
  - Very nice performance of the scripting capabilities.
  - DQM development and nice performance !

    Including data integrity, retriggers, underflow events plane events mappings
- We even had some time for analysis during the shifts (Artur, Bokyeom, Izumi, Kostia, Younes, Yu and myself) and to have a BBQ :)
- And to solve the 1T configuration unplanned issues

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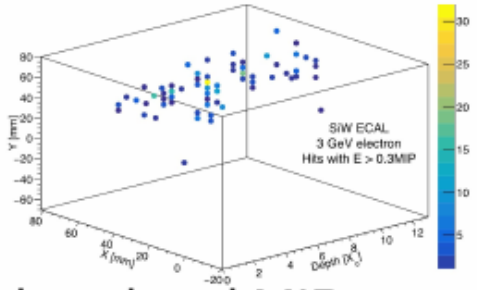
Results of the beam-test



- Very good results…
- Perfect calibration pre-test
- Full position scan → good pedestal and MIP uniformity
- Shower tests with different W configurations
- A lot of coherent events
- Real-time monitoring
- 1T magnet experiment with remote harware

Frederic slides (production of short slabs meeting)

...but a lot of noise problems

- A lot of channels had to be masked
- Noise conduction problem
  - BCID 2500
  - All connection pieces had to be remade in plastic
  - The back plate had to be protected with kapton scotch
  - When the scotch had been scratched by W plates → BCID 2500 appeared again

- Layer 1, Slab 21 → **24% (one wafer)**
- Layer 2 – 6 , slabs 16,-21 **~6-7%**
- Layer 7, slab 22, **~ 8%**

- 3% are masked manually just before starting the commissioning (the adc=4 channels)

Frederic slides (production of short slabs meeting)

- Noise burst observed coherently in all (many) slabs when grounding loops are present
  - Not always in 2050 but, fortunately, always in high values → no problem when running in beam test (high rates)
  - Makes difficult cosmic runs if this problem is not solved.
  - Appeared back in the beam test, but not problematic thanks to the high rates.
  - Completed solved by proper isolation of the ground of the slabs →
  - Any intrinsic underlying reason for this? Would need deep studies. For the moment, check the response with new patch pannel (D. Jehano & R. Cornat).
- **Once that we know the issue: it is easy to bypass it. It does not prevent us to make physics.**

3 slabs are broken

- Slabs 13, 14 and 15 are unusable for data taking
- Too much noise prevent signal acquisition
- This problem appears suddenly during a manipulation phase (pre-beamtest calibration)
- Quick observation of the slabs dont reveal an obvious problem
- Conclusion
  - → Complete analysis has to be performed
  - → no new slabs until the cause has not been found and solved
  - → These slabs need to be repaired

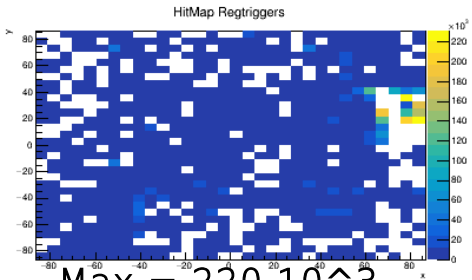
- Slab 13 was dead from the beginning. Even had some problems related with the colling procedure.
- Slab 14 had wafer problems since the beginning of precomissioning. Resoldering was done and it suffer a lot of handling and 3 trips by car (LLR-LAL).
- Slab 15 was working and suddenly not → first one into "suffer" the commissioning procedure, which required open them and manipulate them quite a bit.

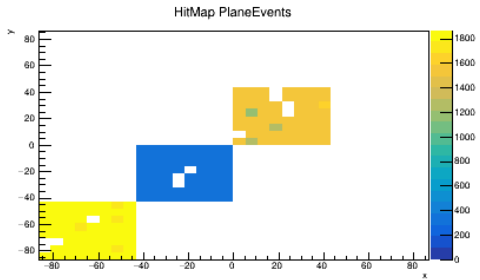
Frederic slides (production of short slabs meeting)

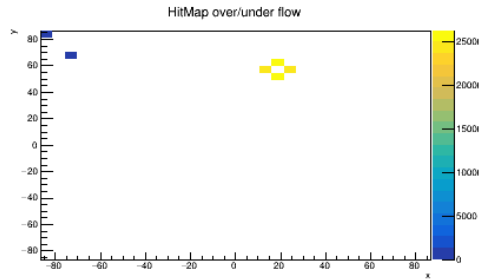
Issues observed: adc4/retriggers/plane events

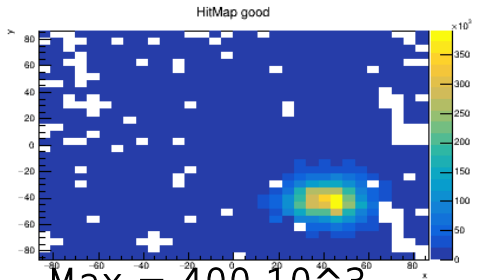
- ADC = 4 channels, retriggers, plane events. Seems that we are in the **same situation than in 2015 ?**
- **Once that we know the issue: it is easy to bypass them:** masking adc=4 channels (conservative approach ?) and filter events offline.
- These events have been monitorized

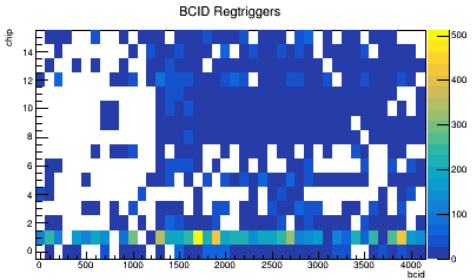
Issues observed: adc4/retriggers/plane events

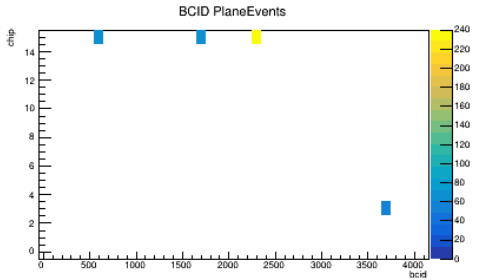


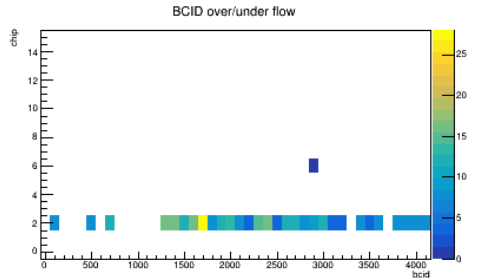


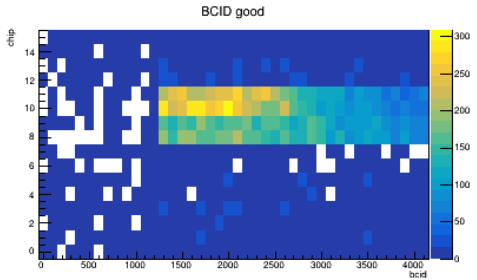


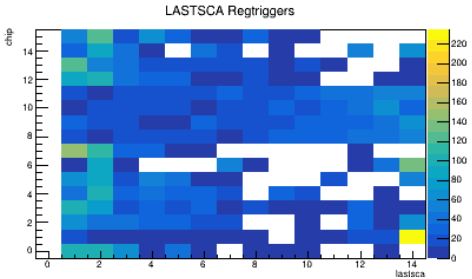


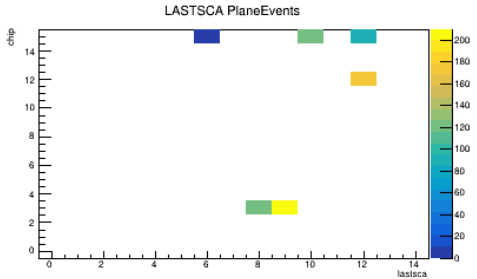


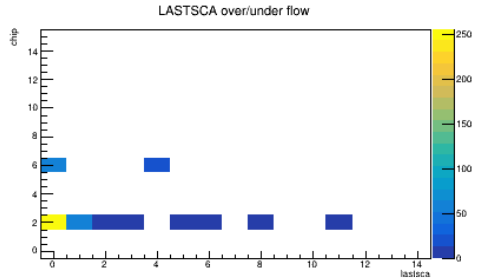


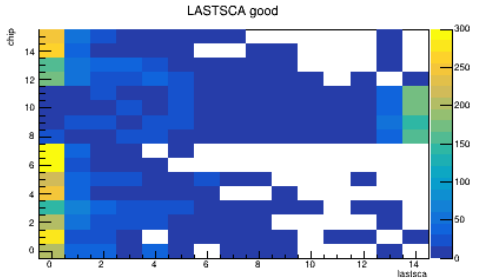












Issues observed: adc4/retriggers/plane events

- Retrigger rates in the beam spot are consistent with the BCID+1 issue:
  - ~ 15% rate (not easy to see in the plot, I agree)
  - Last sca filled for retriggers is randomly distributed for chips in the beam spot (10,11,12,13) Similar situation with pedestal (double peaks associated to retrigger, see backup)
  - Last sca filled for retriggers far from the beam spot = 15. Not BCID issue.
- From other monitoring plots, I see that Plane Event and Retriggers have very similar signatures (high threshold for these plots= 32 channels)
- Crosses are always ADC=4 related.

Issues observed: adc4/retriggers/plane events

- Collective/cross talk effects ? Skiroc2 is too sensitive to noise in the preamp/analogue part of the chip (baseline shifts) → retriggers ? Adc =4 entries ?
  - During important phase of the precommissioning: the BCID2050 and noise/adc4 issues were convoluted and not properly understood → need new studies.

- FEV11 shows some shortcomings but not showstoppers.
  - Nothing prevent us to make physics, as seen during the beam test.

To do / next steps

- We are ready, with some small improvements, to run another useful testbeam “tomorrow”. Issues observed so far are not critical
- We are in a better situation than ever for a consistent continuation of the detector development.

To do / next steps

Short /medium term (i.e. CALICE meeting)

- Establish latest DAQ/DQM/Commissioning developments (repository/ document/fill holes)
- Repair/understand slabs 13, 14, 15 → how much effort should we put in this ? 15 seems recoverable.
- DIF firmware update (disable skiroc clock while acquisition my help with the noise issues)
- Bring into operation LAL rack (borrow the LLR rack and a GDCC)
- Study again the adc=4 problem under controlled conditions (no bcid=2050)
- BCID2050 behaviour with a new rack.
- …

Medium term (2017)

- Test of skiroc2a at system level
- DQM4HEP ?
- EUDAQ 2 ?

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Back up material

Test Beam Summary

- Beam spot seen minutes after the beam was switched on.
- Smooth run for the 2 weeks with stable configuration
  - Dedicated commissioning of the slabs with Passport production at LAL

    https://twiki.cern.ch/twiki/bin/view/CALICE/SiWDESY201706Commissioning
  - This lead to a minimal remasking of few channels during the MIP runs → needs automatization.
  - Spill settings: 5 Hz, 3.7 ms width (0.9 start acq + 0.5 val evt + 2.3 ms)

    Overrunning BCID (bcid step = 0.4 us) → but with desy high rates, it overruns only (if it does) in chips far from the beam spot
  - Gain: PA = 1.2pF, CC=6pF (cc does not afect to the gain)
  - Threshold >= 225/230 DAC (chip based)

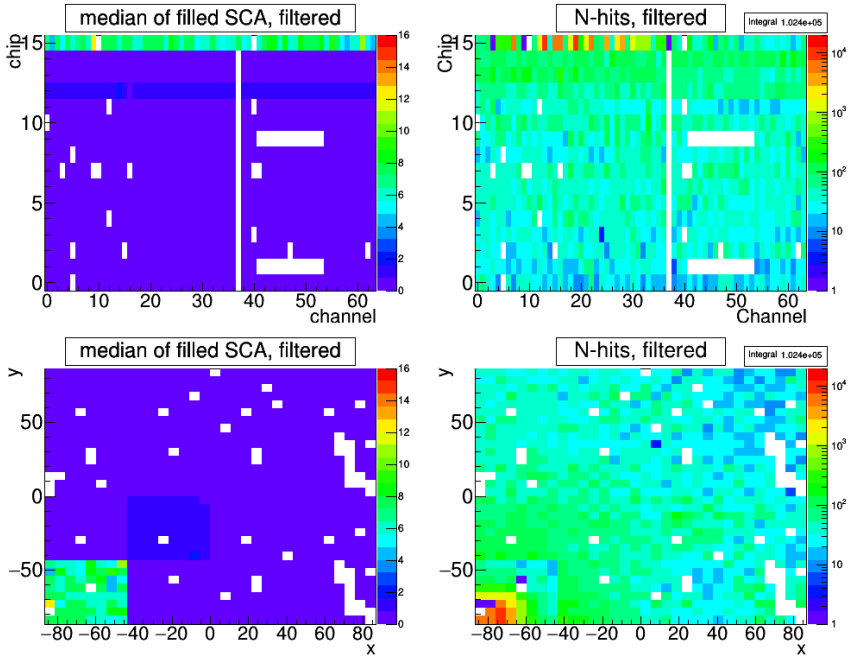
    Extracted from the scurves as the maximum between 225 and 5 times the deviation from the error function mean value. During the commisioning, we started with 230 as minimum but we end with 225.

Data taking program

Layer	SLAB	LV cables/connectors	LV PS	HV cables/connectors	GDCC_port	Name	Position
1	21	1	1	5	1_1	dif_1_1_1	1
2	16	2	1	5	1_2	dif_1_1_2	2
3	17	3	1	6	1_3	dif_1_1_3	3
4	18	4	1	6	1_4	dif_1_1_4	4
5	19	5	1	6	1_5	dif_1_1_5	5
6	20	6	2	7	2_1	dif_1_2_1	6
7	22	7	2	7	2_2	dif_1_2_2	10

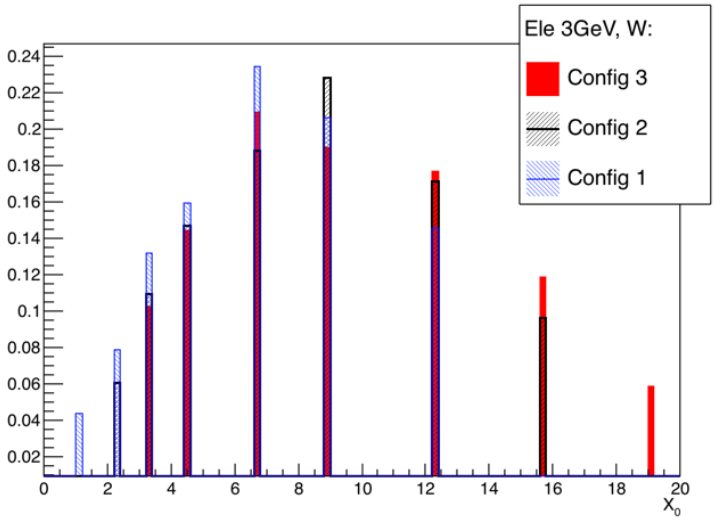
- MIP scan
  - Positrons of 3 GeV (~2 kHz rate, beam spot with slightly irregular shape and size <2cm diameter)
  - Grid of 9x9 points separated by 2 cm → using the CALICE table and the scripts made by Frédéric !!
  - Single acquisitions of 30 minutes
  - Enough statistics (~1000 entries) in the corners f the beam spot (to be increased merging several grid points)

- https://cernbox.cern.ch/index.php/s/v16dXBpIPeTGyVc?path=%2FMIPscan



Data taking program

- Tungsten program
  - Scans of various positron energies (from 1-5.8 GeV).
  - Rates at 5-5.8 GeV were very low: overnight runs
  - Higher rate at 2-3 GeVs → runs of 1h.
  - Three different configurations (see figure)

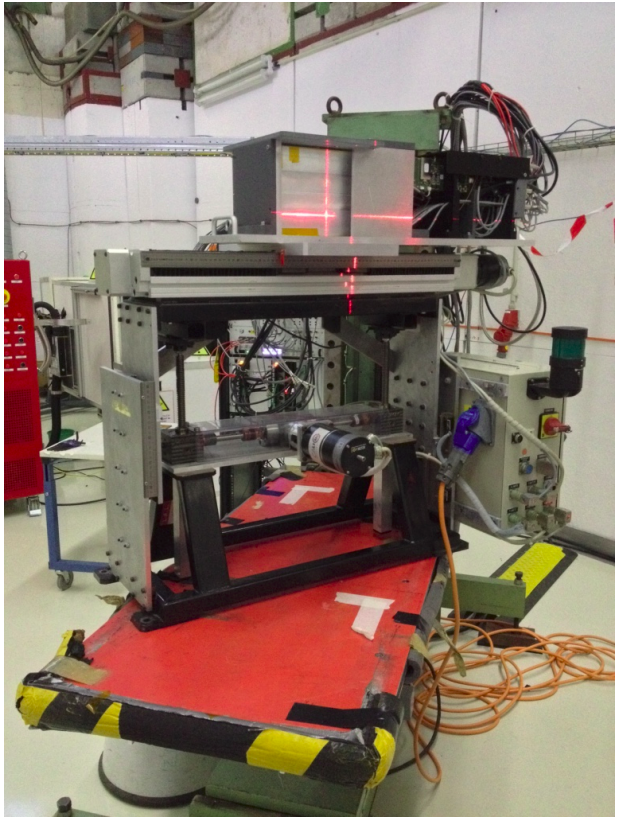


- https://cernbox.cern.ch/index.php/s/v16dXBpIPeTGyVc?path=%2F
  - see W_XgeV folders, where X =1, 2, 3, 4, 5, 5.8

Data taking program

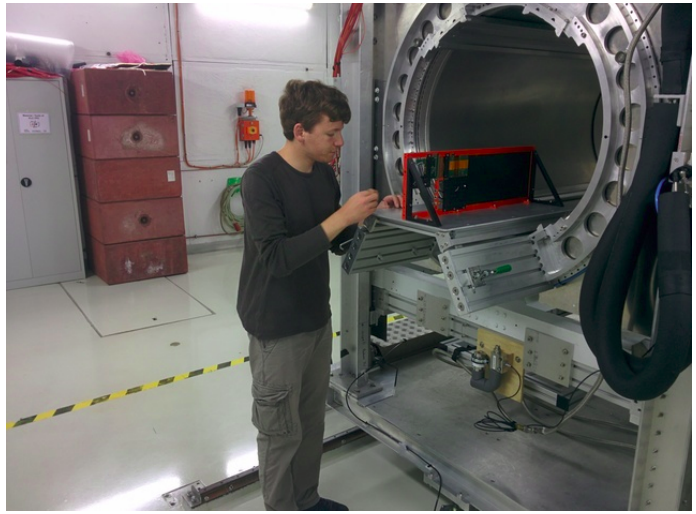
- MIPs at ~43.6 degrees
  - 1s layer removed from the run (for magnetic tests preparations)
  - Tungsten plates removed.
  - 3GeV positrons.

- https://cernbox.cern.ch/index.php/s/v16dXBpIPeTGyVc?path=%2F
  - See 3GeV_3GeV folder
  - Mistake in the folder naming !!



Data taking program

- Magnetic field tests
  - Slab 21
  - Magnetic field from 0 to 1 T.
  - With and without beam.
  - Almost same configuration than in the other beam area.
  - https://llrelog.in2p3.fr/calice/1611



- https://cernbox.cern.ch/index.php/s/v16dXBpIPeTGyVc?path=%2F
  - See XT_YGeV folders

RAW2ROOT.C : Data Integrity Checks

- The root macro checks the data bytes and headers.
  - If additional word is found: warning message and shift of the counter
  - If no additional word is found but spill candidate packet has wrong length (in words) → error message and reject spill candidate (count)
  - Else: if bad number of columns → error message and reject spill candidate (count)
  - Else: if bad chip id → error message and reject spill candidate (count)
  - Else: if error in bits → error message and reject spill candidate (count)

    In this case, we also save (if possible) the bcid andsca were the error happened

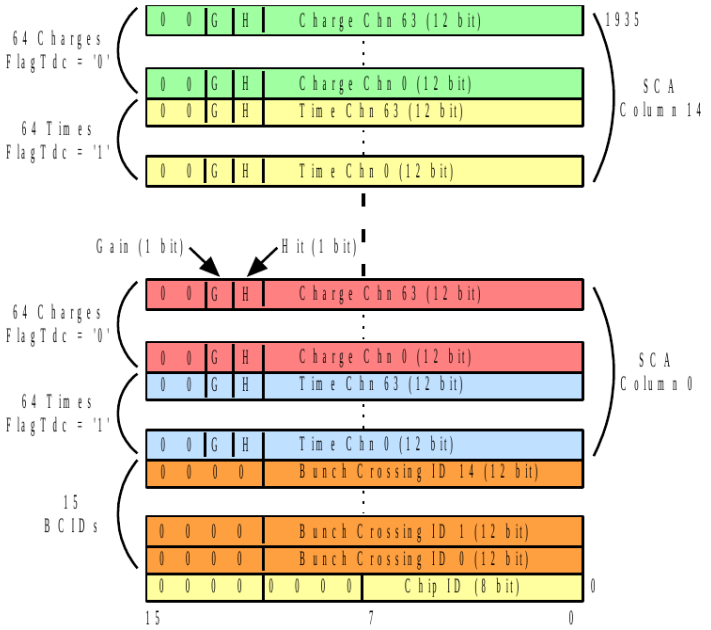
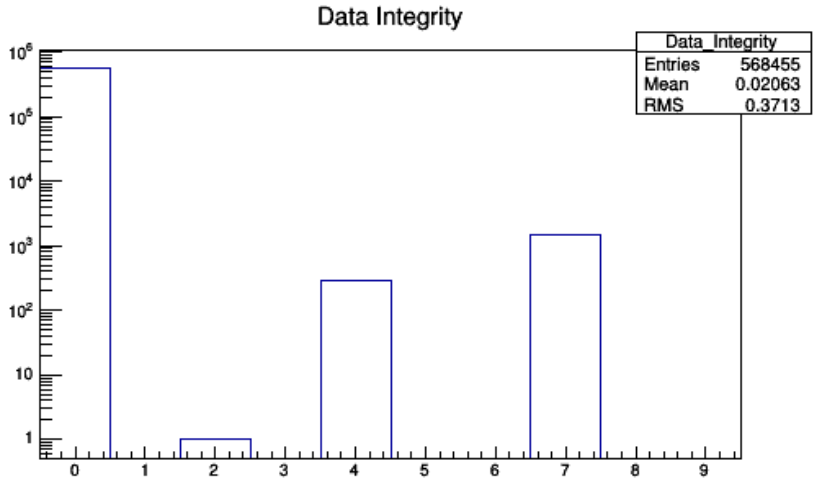


Figure 15: SKIROC2 chip memory mapping

RAW2ROOT.C : Data Integrity Checks

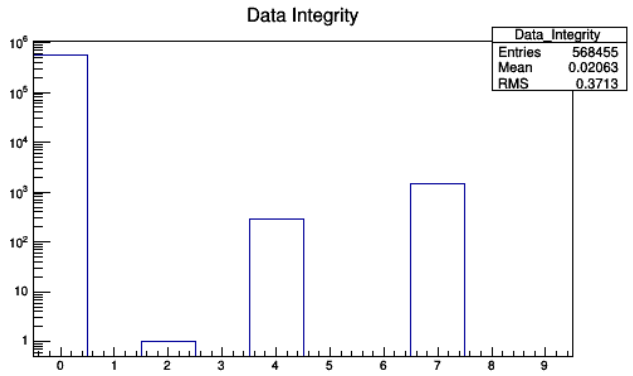
- Data Integrity histogram (spill based):
  - value = 0 --> OK
  - value = 1 --> bad data size
  - value = 2 --> more than 15 memory columns
  - value = 3 --> bad chip number
  - value = 4 --> extra bits in BCID (>12)
  - value = 5 --> extra bits in LOW GAIN charge/hbits --> expected 13 bits, no more. The 14th is for autogain mode --> not used
  - value = 6 --> extra bits in HIGH GAIN charge/hbits --> expected 13 bits, no more. The 14th is for autogain mode --> not used
  - value = 7 --> hit bit from high gain != hit bit from low gain
  - value = 8 --> Bad number of columns or bad number of channels
- Error tagging is not cumulative: if bcid is wrong but hit bit s also wrong, the event is tagged as hit bit wrong.
- Saved in the .raw.root file

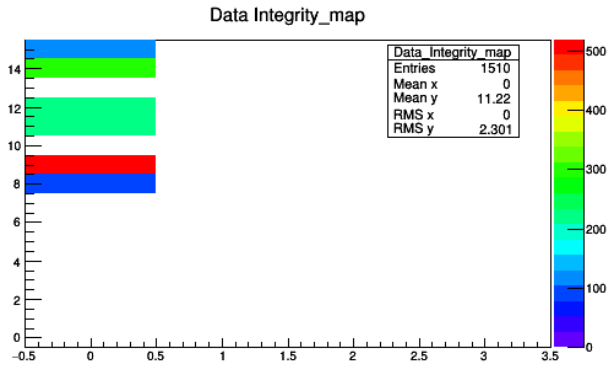


Example for layer 1 (slab 21):

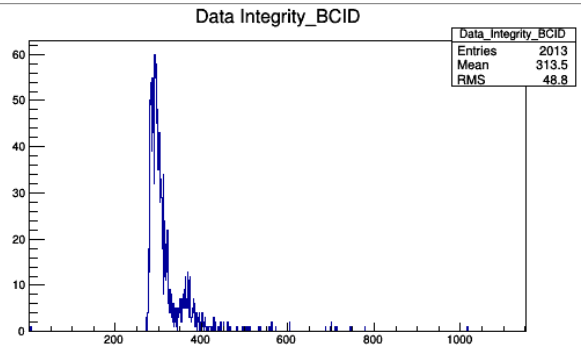
Full mip scan

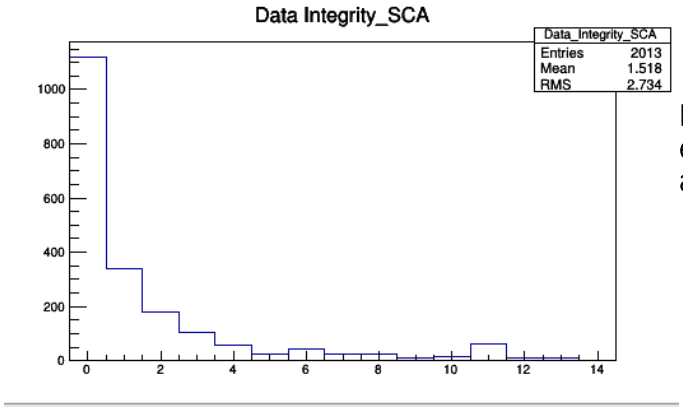
RAW2ROOT.C : Data Integrity Checks





Chip channel map (but if error appears in the first channel, then we stop counting)

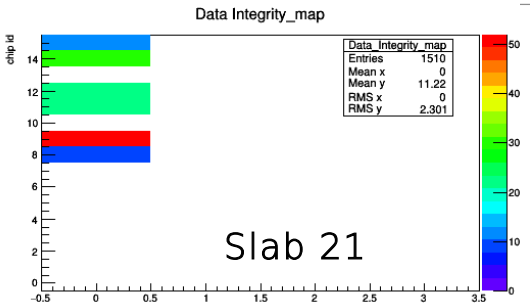


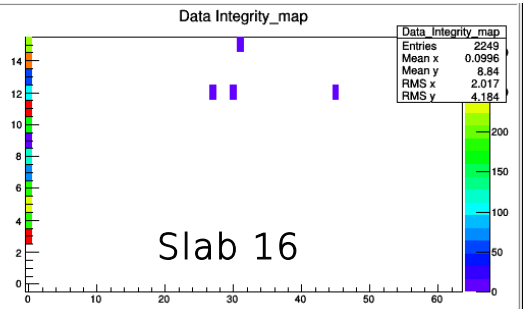


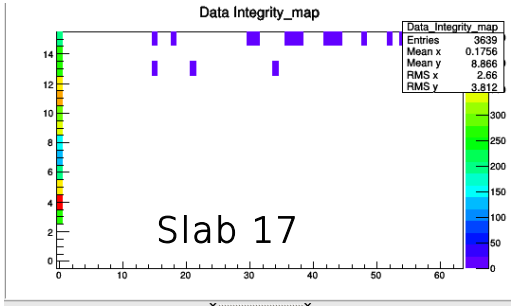
BCID spectra for rejected events looks very similar for all slabs → shifting bit ?

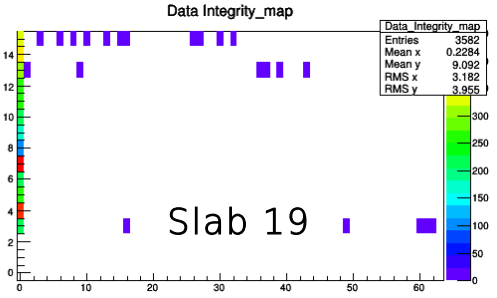
Example for layer 1 (slab 21):Full mip scan

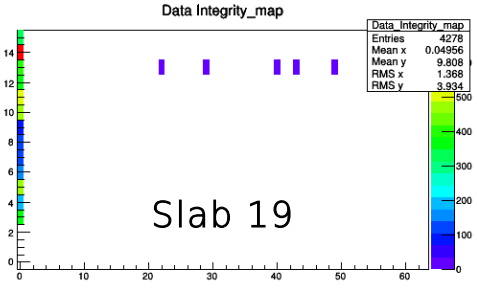
RAW2ROOT.C : Data Integrity Checks

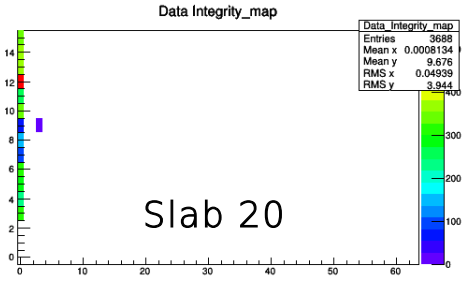


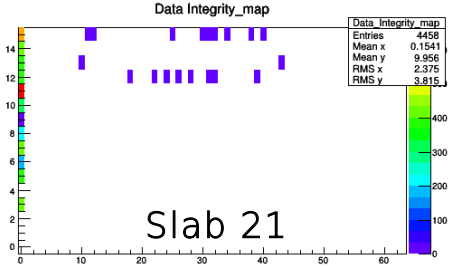








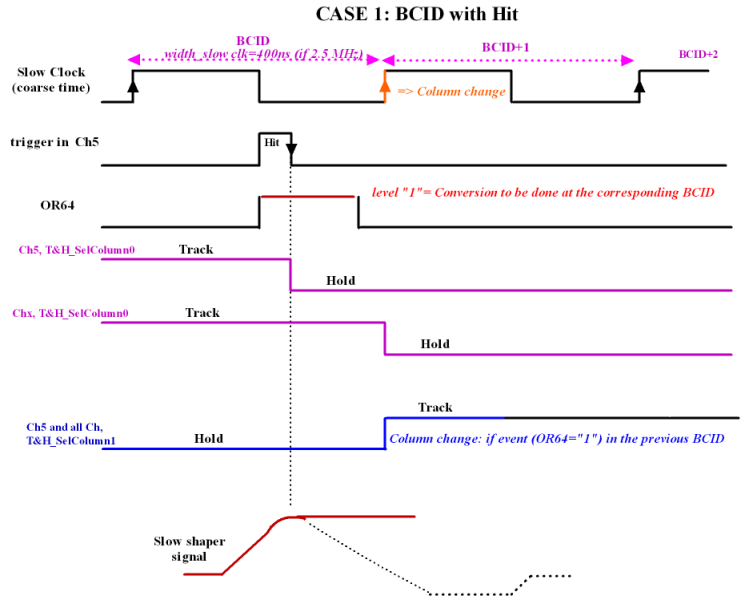




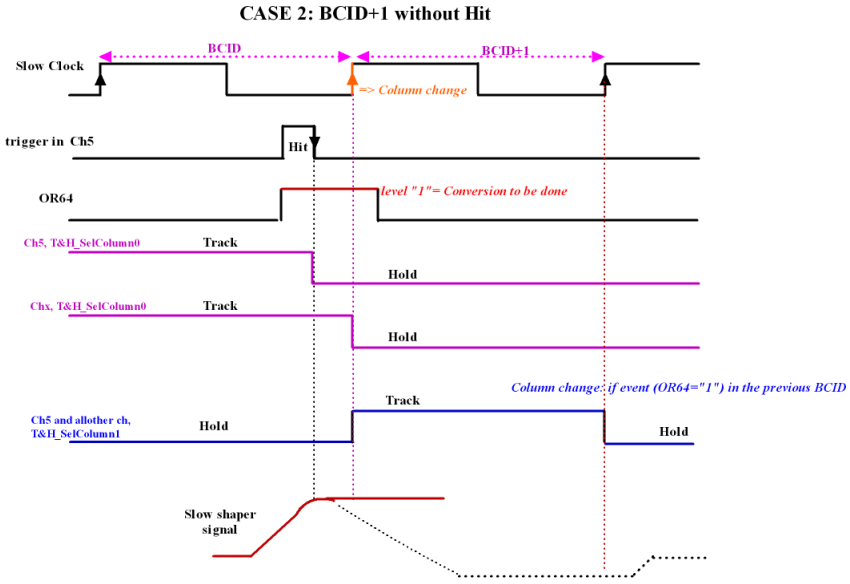
Why there are no errors in chips 0,1,2 ?

Are these chips superseeded by other sources that are not chip-taggable (i.e. bad number of columns, bad chip id, bad number of words)

BCID+1 events



Conversion: BCID with one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal, other SCAi= ped
BCID+1: No conversion because OR64 level=0 during this BCID+1



Conversion: BCID, one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal
BCID+1, no hit, SCA1 ch5 holded value=value < pedestal or pedestal, other SCA1 holded value=ped.

- This are not bad events !!
- Next SCA (NSCA+1) is filled with a zero, but SCA=NSCA is usable → not remove from analysis !
- ~ 15% of chances of happening (reduced to ~0 in skiroc2a)

Retriggers, plane events and underflow data

- Retrigger: different issue than BCID+1 but similar “signature”
  - Retrigger creates lots of entries in consecutive bcids.
  - Are usually associated to a pedestal shift – double pedestal distributions

    a change in the reference analog power supply level ? → fake signals
  - Identified by checking the previous bcid, if small difference → tagged.
- Plane event: similar cause ? Identified easily by selecting events with less than X channels triggered (X depends on the beam composition, usually 32 is a right number)
- Underflow data (ADC=4):
  - a) by sampling in the undershot (in principle solved/reduced in sk2a)
  - b) only at SCA, due to some noise (and timing) extra sensitivity on analog part intrinsic to skiroc2 (in principle solved in 2a) → very located channels, probably near some power/other lines that introduce some noise in the analog part of the chip.

Tagging these events: badbcid

- How are all these events identified ?
- Using the nhits[16][15] variable (counts all hits in one SCA with ADC>10)
- Using the badbcid[16][15] variable. It is filled doing the following checks sequentially:
  - ==0 if SCA=0
  - ==1-16 if bcid[chip][sca]-bcid[chip][sca-1]=1-16
  - ==+32 if a negative entry (ADC<10) is found in the chip for this sca
  - ==0 if none of the previous.

Tagging these events: badbcid

- Issues observed:
  - We tag the bcid+1 events as bad events
  - SCA 0 is always tagged as good but we see some double pedestals (see Yu's slides)
- Solution ?
  - ==1-16 if bcid[chip][sca+1]-bcid[chip][sca]=1-16
  - ==+32 if a negative entry (ADC<10) is found in the chip for this sca
  - ==0 if none of the previous.
- New RAW2ROOT version to be updated (and checked) in the repository

PRESTIGE
POSTDOCTORAL RESEARCH FELLOWSHIPS IN FRANCE
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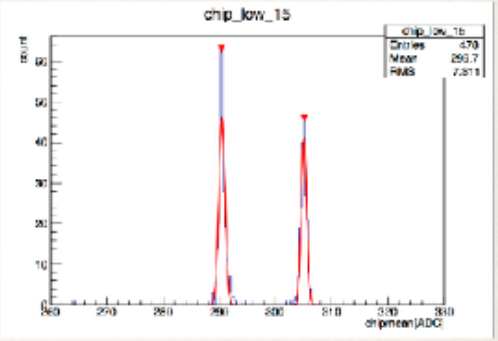
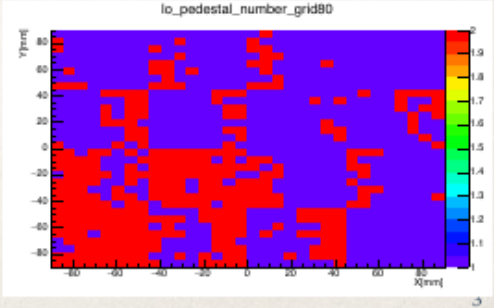
Issues observed: BCID2050/adc4/retriggers

- Similar situation with pedestal (double peaks associated to retrigger)

Double pedestal

- When we produced histogram, double pedestal was seen !
- Double pedestal was seen at **RED region**
- Data
  run number : 20170616_175712
  MIP scan : 1800 seconds
  Beam shout point : grid 80
  Beam energy : 3 GeV
  DIF : 1_1_4
  Memory cell : 0 only
  Charge : low gain
  Tungsten (W) : none





Yu slides (first tb2017 analysis meeting)