#5 Beam Test Preparation Meeting (June 2017, DESY)

- Status Bench
- Status Slabs
- Status Monitoring
- Summary of HV + other features found so far.
- Tentative calendar

A. Irles, LAL, 16th Mai 2017

Non exhaustive list of features found (and solved) so far

- Slow control: cc<4pF makes one of the slabs too noisy, with very bad data integrity (slab XX)
  - Use c=6pF, PA=1.2pF:
    0xFE000031FE2F8A8082800000000000000044444444444444444444444444444444444444444444444444444444444444442842AA0000000000000000000000000000000000000000019D
  - Hold value ?
- ADC=4 channels → these channels create noise in other channels &/or pedestal shifts (?)
  - BT2015 analysis meeting https://indico.in2p3.fr/event/13006/contribution/2/material/slides/0.pdf
  - BT2017 Readiness meeting https://indico.in2p3.fr/event/14535/contribution/1/material/slides/
  - (conservative) solution: mask and disable their preamps. List: https://llrelog.in2p3.fr/calice/1183 → 3% of channels
  - After the masking only 1-10 channels per slab are masked (0.1-1%)
  - After mask noisy → monitor cosmic and beam runs to make sure that no new channels appear.
- HV + grounding issues that create burst of noise at a given BCID (3 consequitive BCIDs)
  - Improving the grounding-cabling (slabs, patch pannel, prototype connectors) and use mini-patch pannel for HV
  - Continuous monitoring BCID on not beam runs to optimize the spill length in case the noise appears back.

Status Bench

- Jerome is revisiting the LV cablage:
  - One power supply still not plugged (only 5 slabs at once)
  - Some LEDs are broken
  - DIF power connectors are loose (more than 10 uses)
- Revisiting HV cablage + grounding
  - HV/LV/Patch pannels/cabling/stack …. something creates a burst of noise at a given BCID (first was 4096+2050, now is 4096+850)
  - Possible contingency plans (so far) if BCID issue is not solved

    → use the 2012-13 mini patch pannel to avoid the connectors in the prototype
    → old pvc stack
    → just monitor and trust the the BCID issue appears late enough...
    → ??
- Evelyn will do some updgrades in the prototype:
  - Modify white supports for the slabs → i.e. make a bit more of space for slab 13 (thick HV filtering) –> before the 29th May
  - Add capotage aluminum structure (before beam test ?)

BCID-issue HV tests

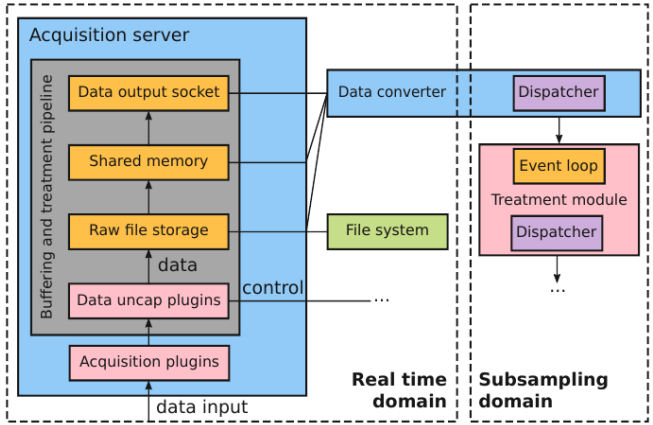
- DIF firmware totally discarded as cause.
- Since last week, we tested several configurations (Remi, Jerome, Adrian)
  - in/out prototype,
  - different DIFs,
  - different cables,
  - Using patch pannel in the prototype or not
  - Scaling number of slabs.
- We were quite sure that we hunted up the problem $\rightarrow$ inside the stack (not DIF, not patch pannels, not cablings...) but now it is not that clear.

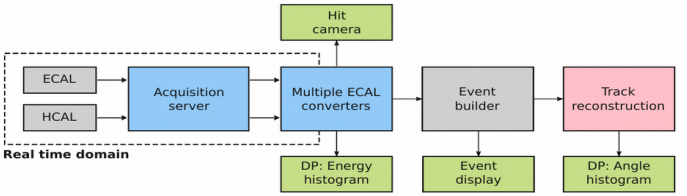
Status Slabs

- https://forge.in2p3.fr/projects/calice/wiki/Si-WEcalSlabs
- Uniform the light shielding (and grounding?)
  - Slab 15 is the best so far, has different grounding and maybe different wafers. The same grounding was tested in slab 16 without clear improvement $\rightarrow$ to be assured.
  - Old shielding still on slabs 13, 18, 22
  - All but 15 have the old grounding (to the charge injection input lemo connector)

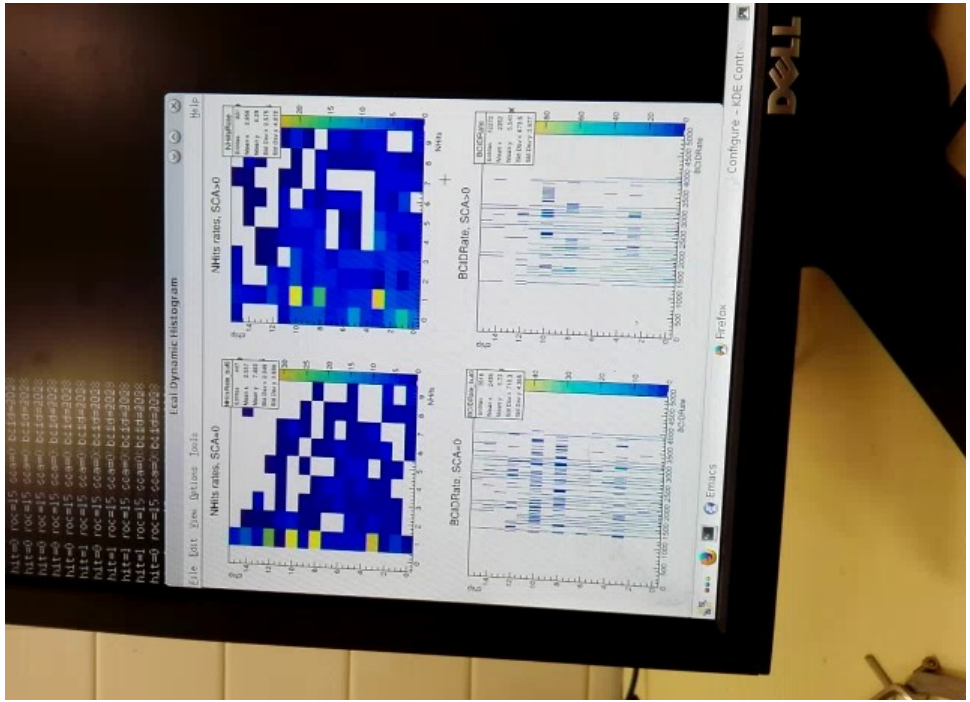
Monitoring

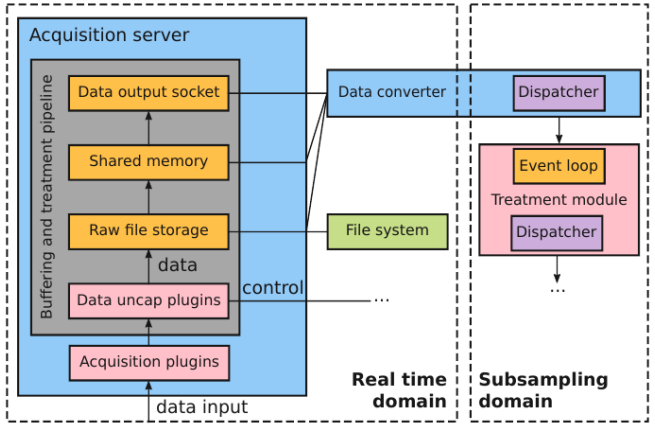
- Real online monitoring in calicoes → converted/dispatcher launched automatically
- Monitoring “modules” launched manually (once) and reinitialized with:
  - Start-acq, i.e. hit maps, slab based monitoring, etc
  - Never, i.e. simple modules for full statistics counting, etc
- Only single DIF modules (for the moment)
  - Event Builder works but Frederic and myself will need one/two days to work on this…
  - calendar is getting tight: realistic planning is that we weill not have “calorimetry” plots until end of first week of BT
- Some “root” issues found so far
  - some crashes when manually update histograms, etc.
  - Creation of tabs

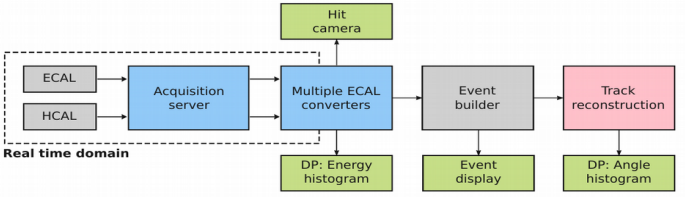




Monitoring


ECal Dynamic Histogram
File Edit View Options Tools
NHits rates, SCA=0
BCIDRate, SCA=0
Configure - KDE Contr...
Firefox
Emacs


Acquisition server
Buffering and treatment pipeline
Data output socket
Shared memory
Raw file storage
data
Data uncap plugins
Acquisition plugins
data input
Data converter
File system
control
...
Real time domain
Dispatcher
Event loop
Treatment module
Dispatcher
...
Subsampling domain


Hit camera
ECAL
HCAL
Acquisition server
Multiple ECAL converters
Event builder
Track reconstruction
Real time domain
DP: Energy histogram
Event display
DP: Angle histogram

Temptative calendar for final commissionig

- 17th-19th Preparation for commisioning
  - Cabling (DIF, grounding, mini patch), shielding slabs.
  - Test of mini patch pannel→ BCID issue ?
  - Finish commissioning software (scurves, find noisy, mip runs…)
  - Monitoring (in parallel)

Monday	Tuesday	Wednesday	Thursday	Friday	Saturday	Sunday
15	16	17	18	19	20	21
22	23	24	*25-28* *Long Weekend (friday?)*			
29	30	31	1	2 -5 Long weekend → cosmics in the stack		
2-5 Long weekend → cosmics in the stack	6	7	8	9		

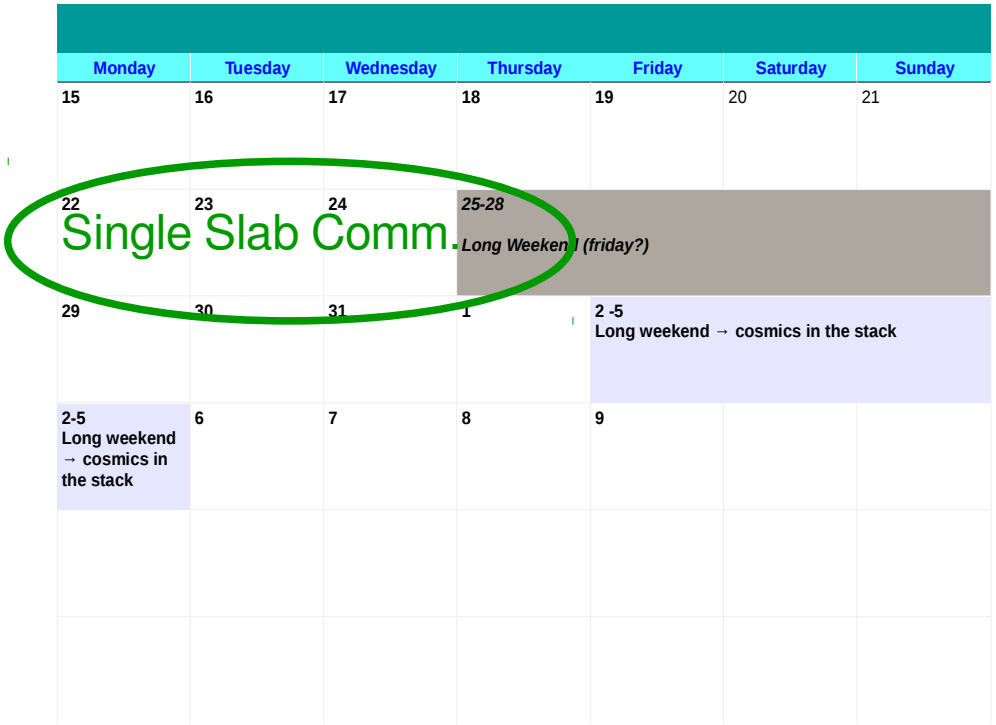
Preparation for commissioning

Temptative calendar for final commissionig

- 22, 23, 24, (29?)Single Slab commisioning
  - At LLR (independent of rack power supplies).
  - ~2-3h per slab:

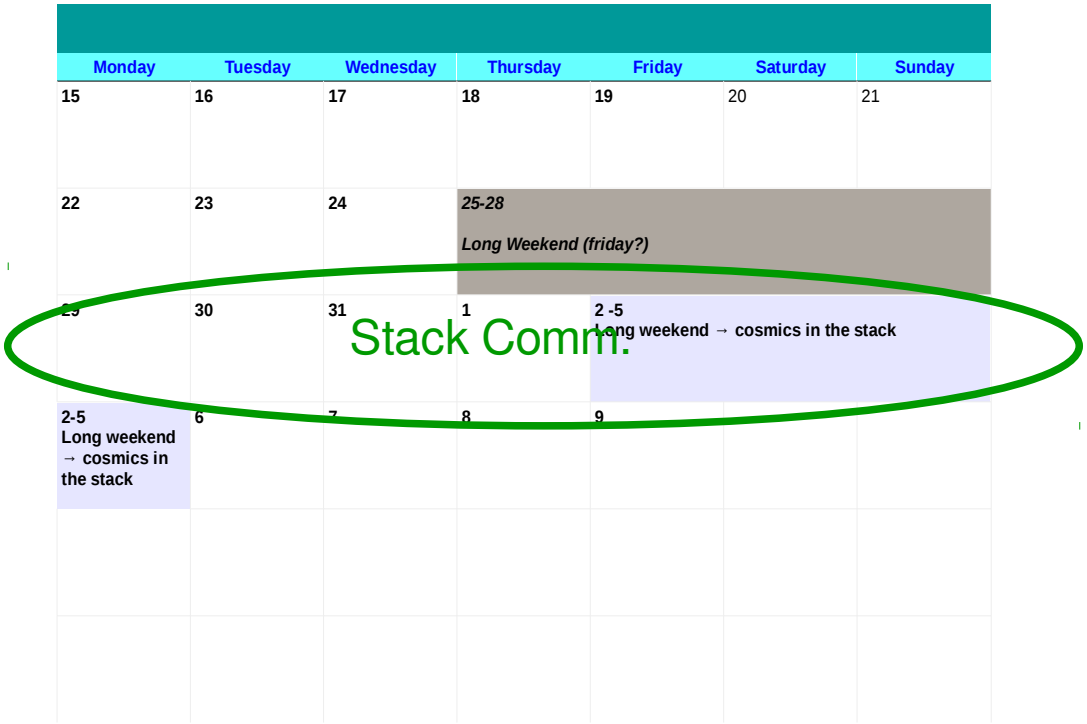
1) HV Ramp up (30 min)
2) FindNoisy + scurves (30min)
3) Cosmic run 1-2 h.

  - Define and document, for every slab, chip-channel threshold, masked channels, HV currents, MIP+pedestal positions.
- Optimal setup:
  - find noisy + scurves with slab in vertical
  - cosmic run with slab laying on the table.



Temptative calendar for final commissionig

- 29-30th Stack commissioning I
  - Integrate all slabs in the stack with HV tests (one by one)
  - BCID issue?
  - Solve unexpected issues
- 30th-31th Stack commissioning II
  - Findnoisy, scurves and compare with single slabs
  - Prepare a long cosmic run… short spill if BCID issue is not solved.
- 31st – 1st - long weekend : Cosmic runs
  - I won't be able to connect remotely so we need to start the 1st in the morning as latest.



Temptative calendar for final commissionig

- 6th - 9th Packing + monitoring + analysis ? + etc

Monday	Tuesday	Wednesday	Thursday	Friday	Saturday	Sunday
15	16	17	18	19	20	21
22	23	24	*25-28* *Long Weekend (friday?)*			
29	30	31	1	2 -5 Long weekend → cosmics in the stack		
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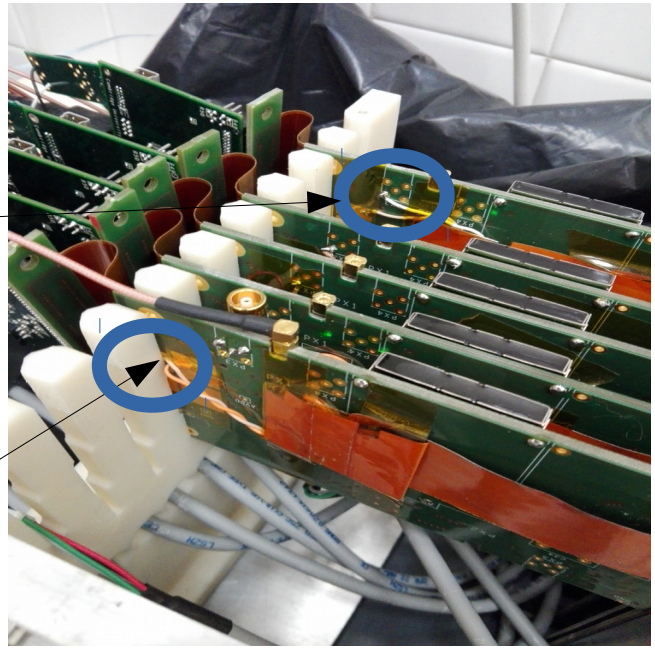
Packing

Backup

Differences between slabs 15 and 16 (and the others):

Both have the aluminum shielding.
According to the log, the 16 had some issue with interconnects, FIXED.
https://forge.in2p3.fr/projects/calice/wiki/Si-WEcalSlabs

Grounding of **16**
(in fact, most of them are like this, ground to the injection pin connector)



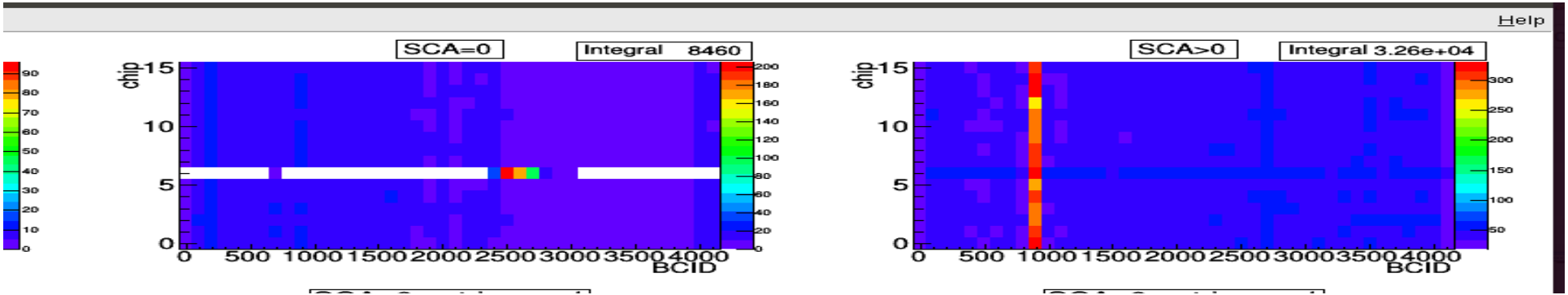
Grounding of **15**

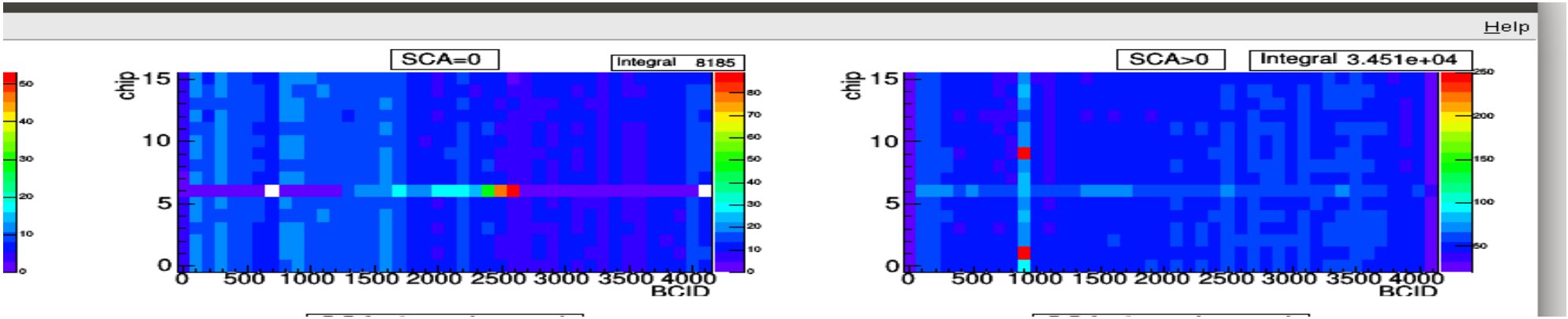
Slab 16.

BCID-issue HV tests

Top → HV delivered through the patch pannel in the rack and connected to the prototype
Bottom → HV directly plugged to the slab.

Currents of ~5-5.2uA in both cases





Slab 15.

Top → HV delivered through the patch panel in the rack and connected to the prototype
Bottom → HV directly plugged to the slab. Currents of ~1.8-1.9uA in both cases