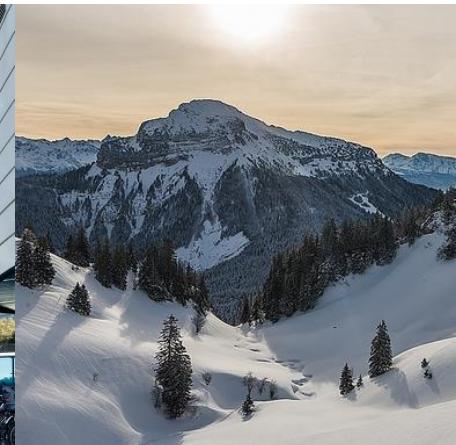


FROM RESEARCH TO INDUSTRY



LES TECHNIQUES D'ASSEMBLAGE 3D, APPLICATION AUX DÉTECTEURS SEMICONDUCTEURS

Séminaire imageur - Paris - Juin 2017



leti

G. Parès / CEA-Leti

- **CEA-Leti brief overview**
- **Introduction to 3D and advanced packaging**
- **3D technology modules state of the art & development at Leti**
 - Chip's Interconnections : micro-bumps/pillars
 - Chip intra-connections: TSV
- **3D application examples: imaging sensor**
 - Image sensor for visible
 - Image sensor for high energy particles
- **Conclusion**



Bio medical
plateform



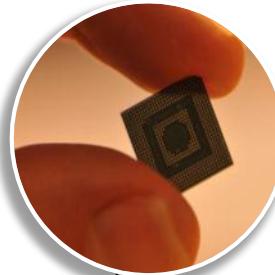
Chemical &
material
platform



Photonic
plateform



Embedded
systems



Micro &
Nanoelectronic
platform

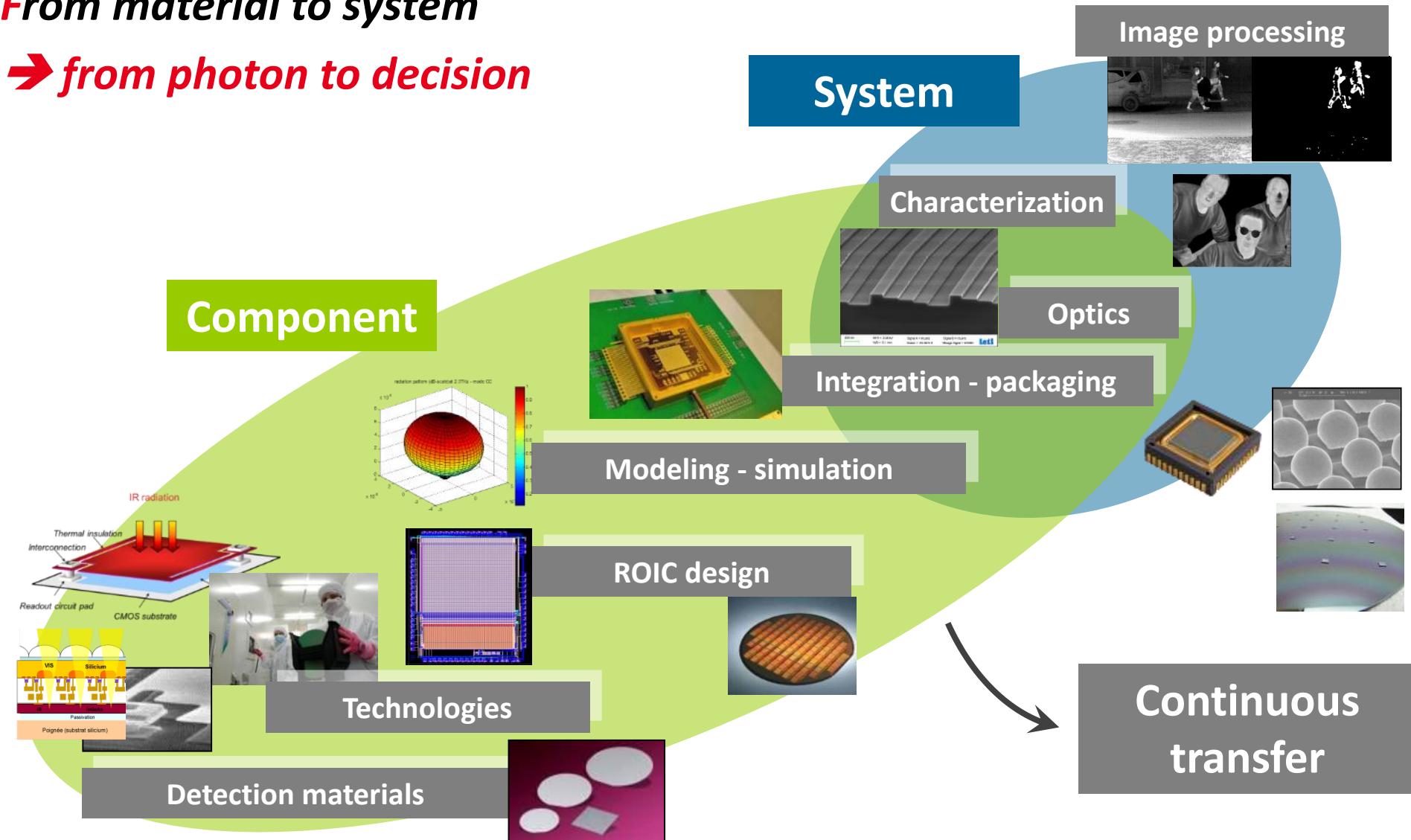


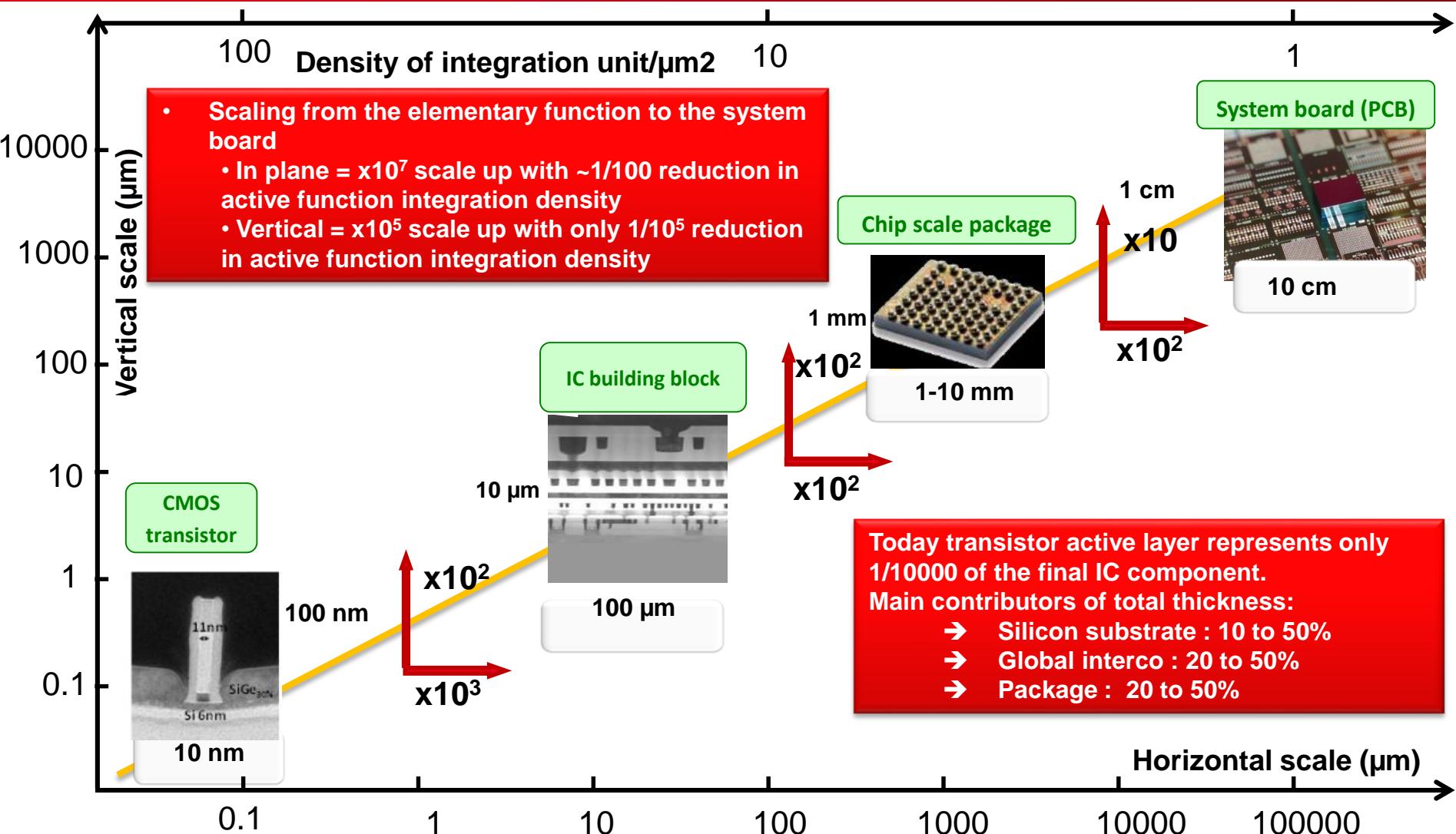
Nanocharacterisation
platform



From material to system

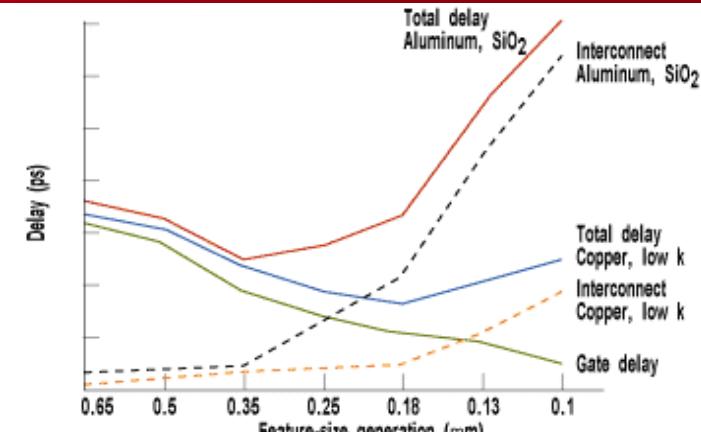
→ **from photon to decision**



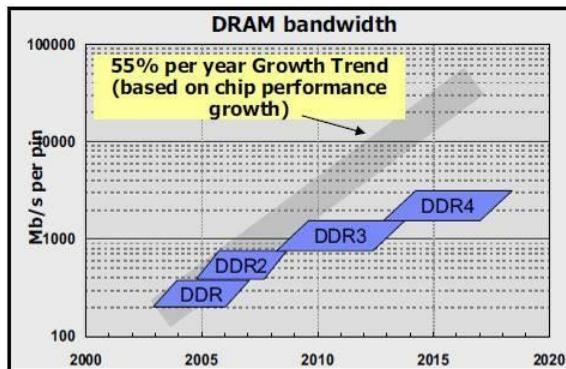


Packaging and 3D technologies are the new frontier for more integration in electronics with:
→ More functions integrated with less substrate and less package

- Increase performances & decrease power consumption**
 - With technology scaling, delay is migrating into the wires
 - 3D is a powerful mean of reducing interconnect length

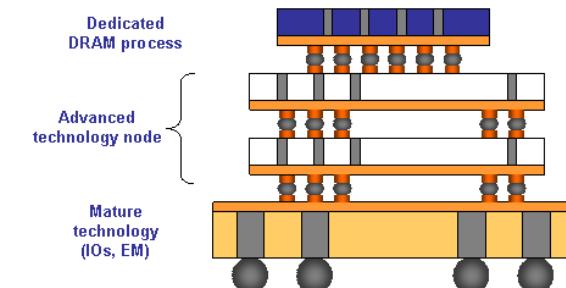


Source: Cadence

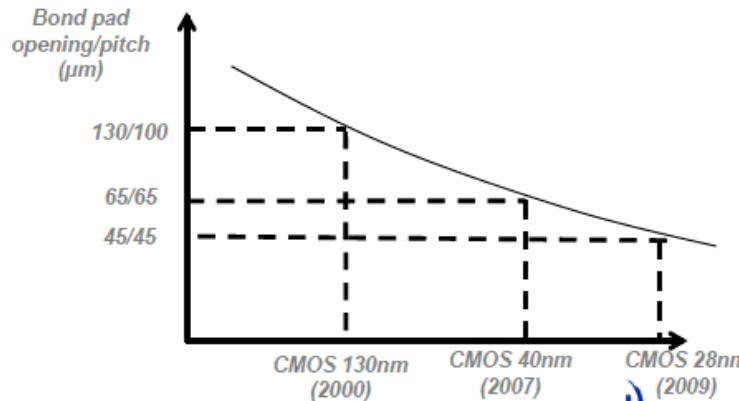


Source: Mike Ignatowski, GLSVLSI'08

- Increase bandwidth to fight the “memory wall”**
 - The clock speed of microprocessors has leveled out to 3-4 GHz
 - 3D technology is the ultimate solution for implementing high bandwidth memories with parallel access.

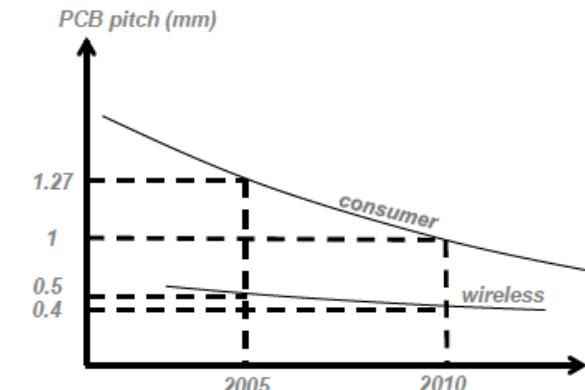


Source: A. Valentian / CEA-LETI

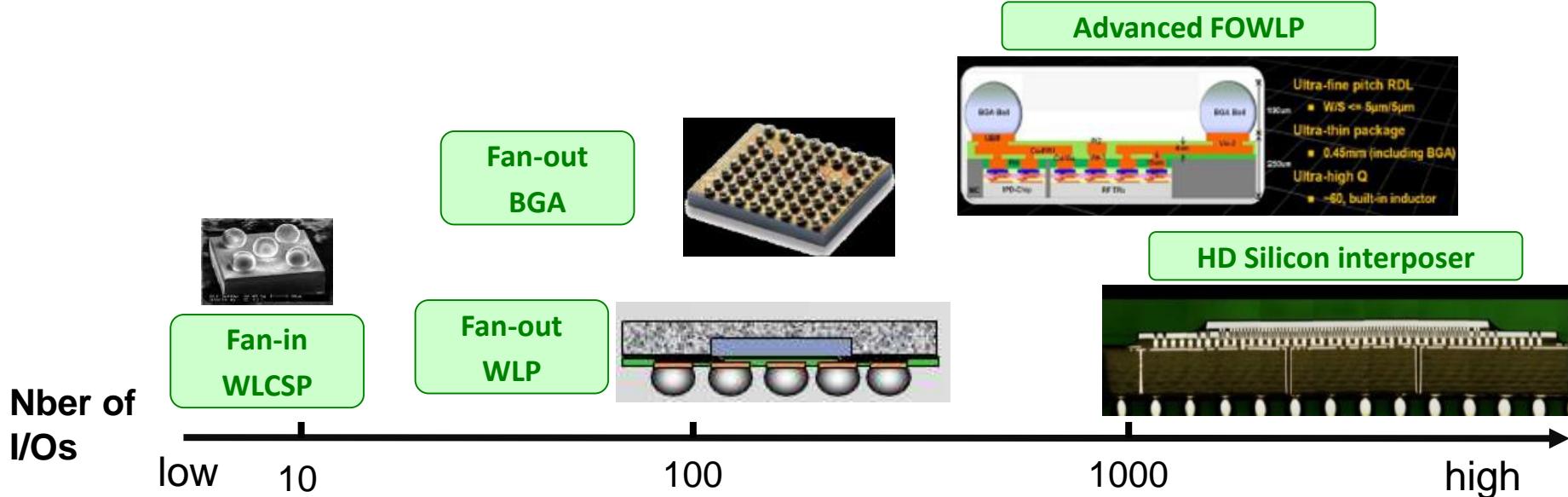


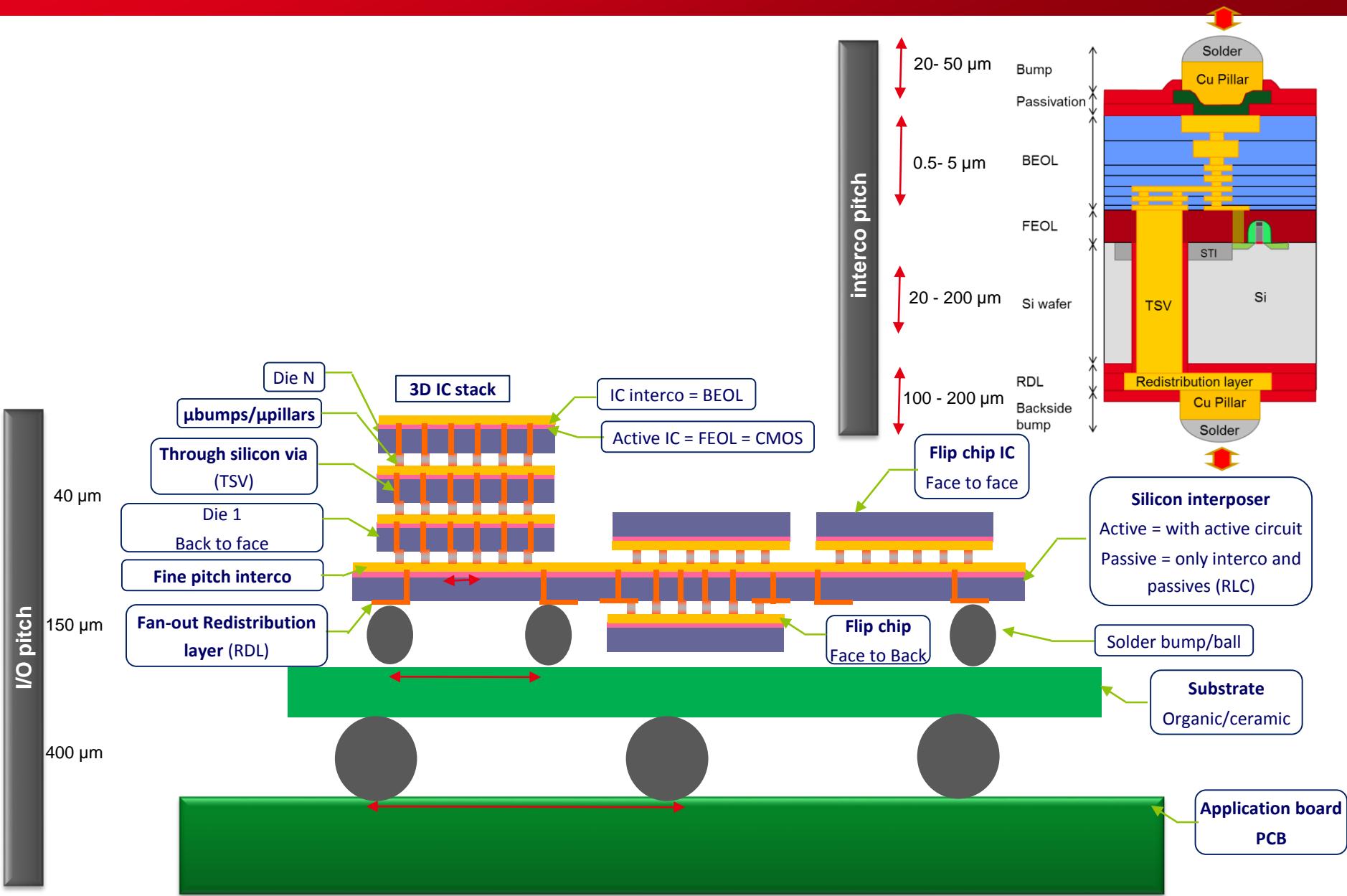
X10 gap to cover

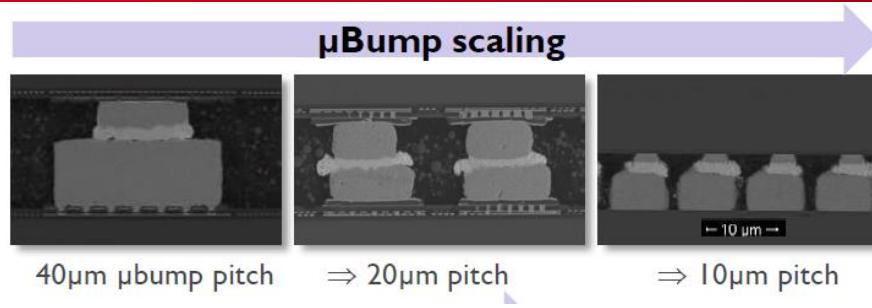
- Wide I/O
- Signal integrity
- Power consumption



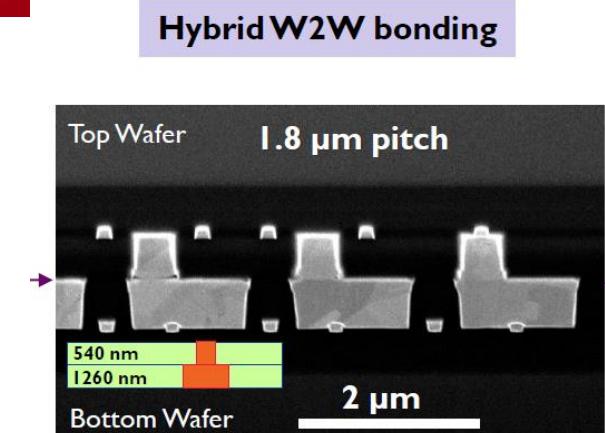
3D and packaging technologies are aiming to bridge the gap between the ICs I/Os and the system board



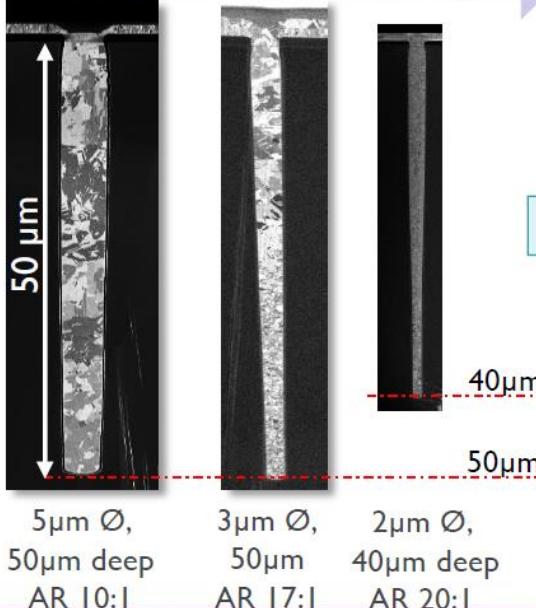




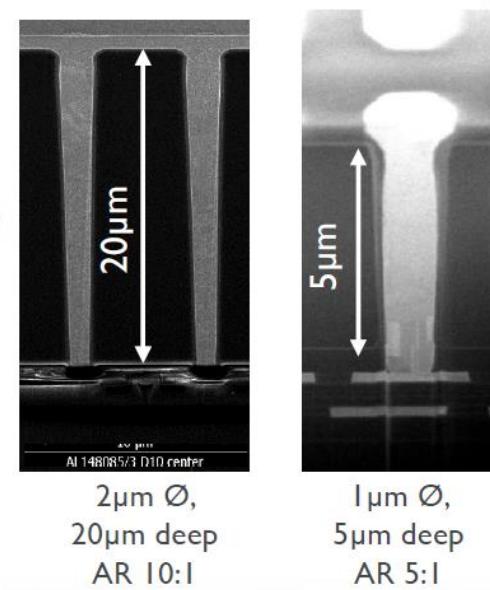
Interconnections between IC chips



TSV Via Middle Scaling

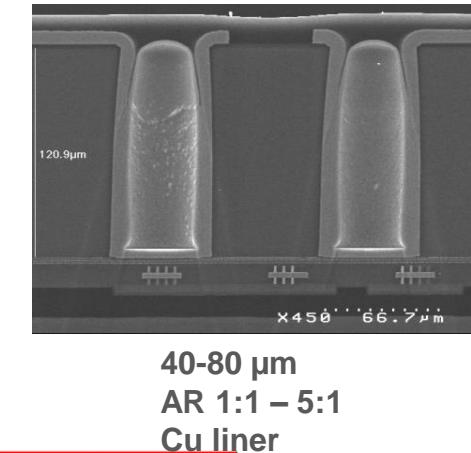


Via Last after W2W bonding



Copper/SiO₂ hybrid bonding

Via Last back side



Interconnections through IC chips (TSV)

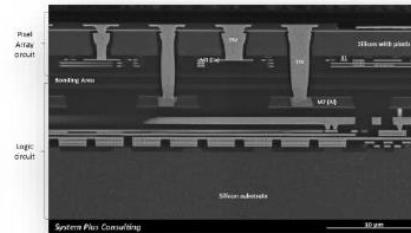
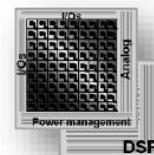
3D Application

Image sensors

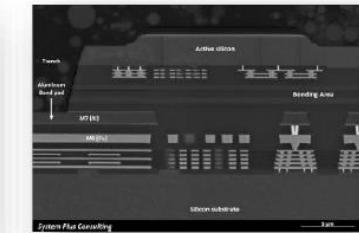
Active WtW bonding
TSV-last

Example Industry Implementation

Sony 8MP, 1.5µm-pixel stacked BSI CIS
Apple iPhone 5S
(2013)



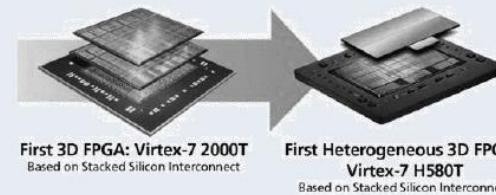
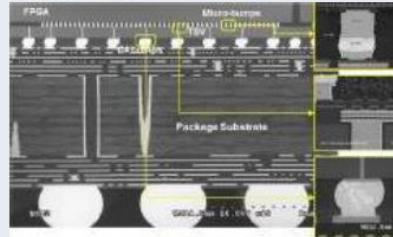
Source : E. Beyne IMEC, 2016



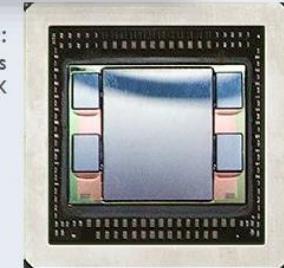
Interposer stacking (“2.5D”)

2.5D interposer
HD connections

Xilinx: FPGA



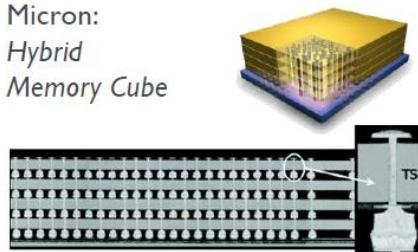
AMD:
Graphics
Radeon R9 FURY X



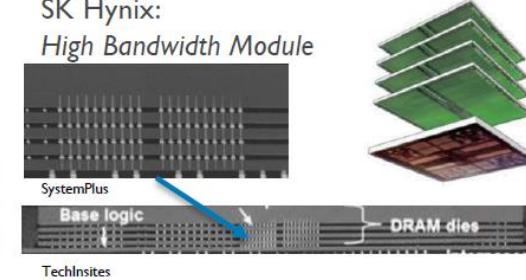
Memory stacking Advanced DRAM

3D IC stack
MD connections

Micron:
Hybrid
Memory Cube



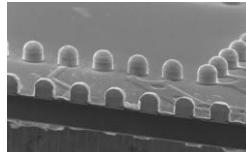
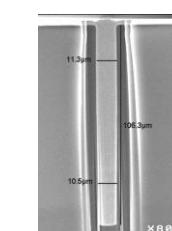
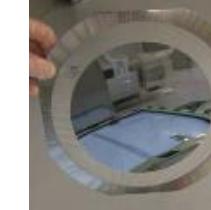
SK Hynix:
High Bandwidth Module



Samsung:
128GB 3D DDR4 RDIMM



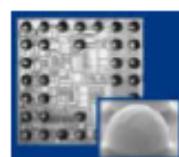
Challenge : standardization of 3D architectures //
→ Use of 3D technologies tool box concept

Connecting	Die to Substrate	TSV	Handling thinning	Die Placement	WL Molding
Solder balls	Wire Bonding	TSV First	handling	High throughput P&P	Thick Polymer molding
Copper Pillars	Solder balls	TSV Middle AR10	Temp Bonding (Zonebond)	High precision P&P	Thin Polymer molding
Via belt	Copper pillar	TSV Last AR2.5	High temp. bonding	Self Assembly	Thin Oxide planarization
μ tubes		TSV Last AR5	Permanent bonding	Wafer To Wafer	WLUF
Cu-Cu		TSV Last High temp	Thinning		Capillary Underfill
Rdl Thick Cu		TSV Last High density	Super thinning		
					

**THE DIE-TO-DIE VERTICAL
INTER-CONNECTIONS:
SOLDER BALLS/BUMPS
MICRO-BUMP/MICRO PILLARS
UBM**

Usual Bumping Technologies and Pitches

Placement of pre-formed solder balls



SAC (tin, silver, copper), tin, polymer,...

WLP (need for 'high' 'elastic' balls)

Electro-less chemical growth



Nickel, Au

Used for finishings or UBMs (Under Bump Metallurgy): "low profile growth"

stencil printing



solder

Is usually applied before ball formation or placement

Stud bumping



Cu, Au

Balling done by wire bonding not a wafer level technology

Electroplating (incl. Cu pillars)



Cu, Au, Sn

For fine pitches or high aspect ratios

Log(Distance between 2 adjacent bumps)

10µm

100µm

500µm

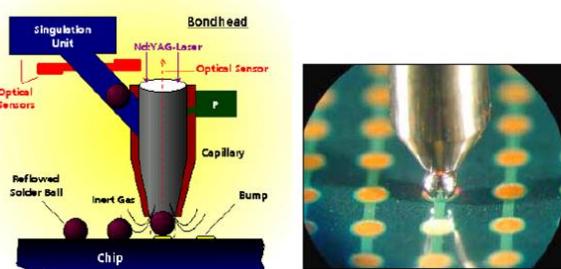
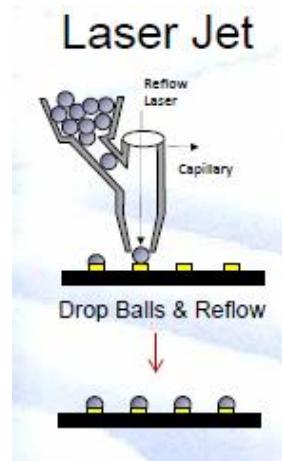
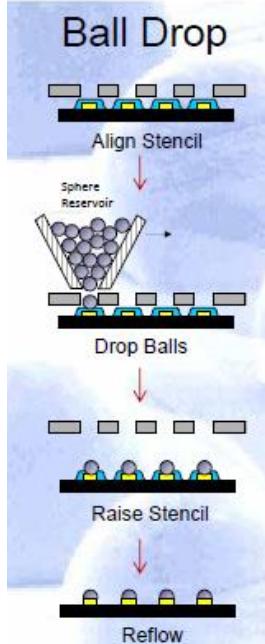
1000µm



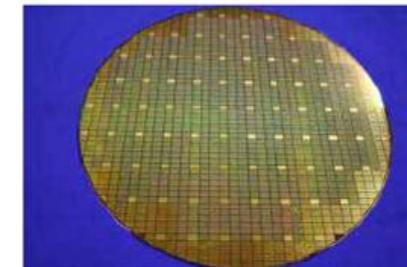
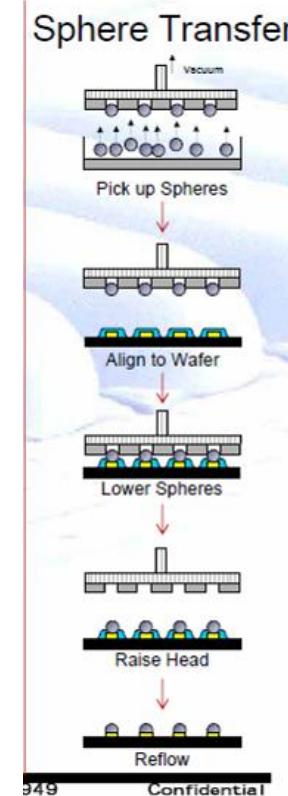
- Galvanic growth (electroplating) is the most suited technology to make fine-pitch bumps at the wafer level with a high aspect ratio. High aspect ratio bumps are useful to get more "elasticity" for reliability. Copper pillars (made by electroplating) are increasingly being used for flip chip BGA as the first level interconnect technology of choice.

Courtesy of Nexx

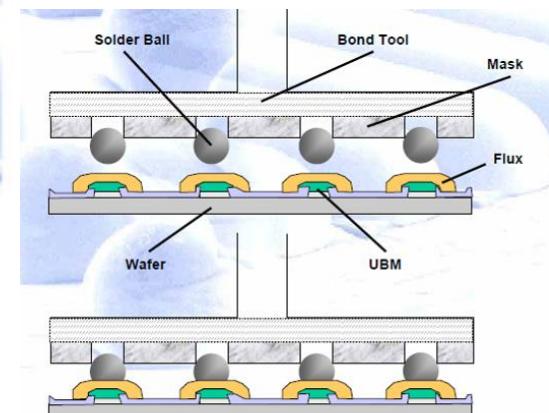
- Direct ball droping
- Laser jet
- Sphere transfer



Source : Pac Tech

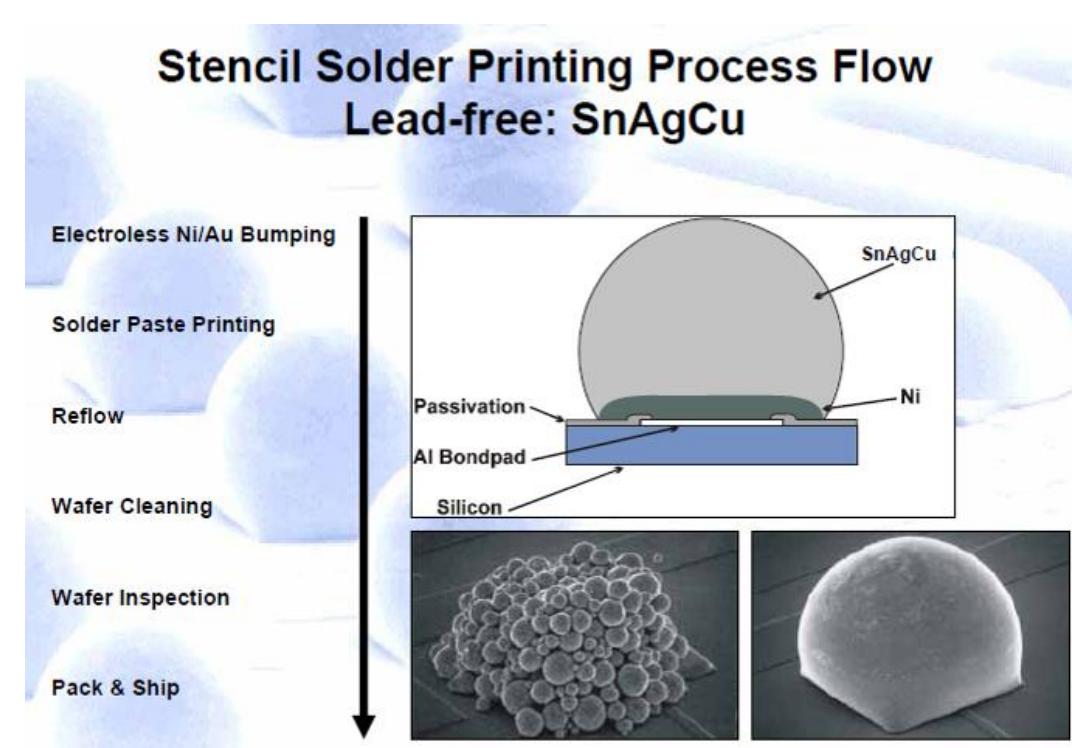
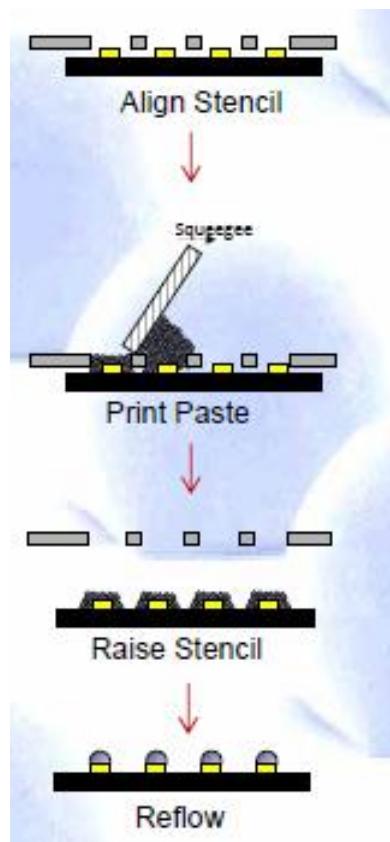


Bumped wafer



■ Standard Printing

- Standard stencil technique
- SnAgCu – SnAg - ...

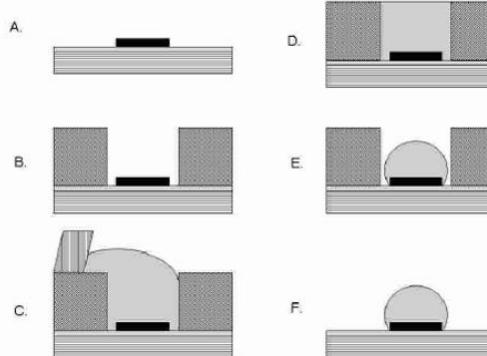


Source : Pac Tech

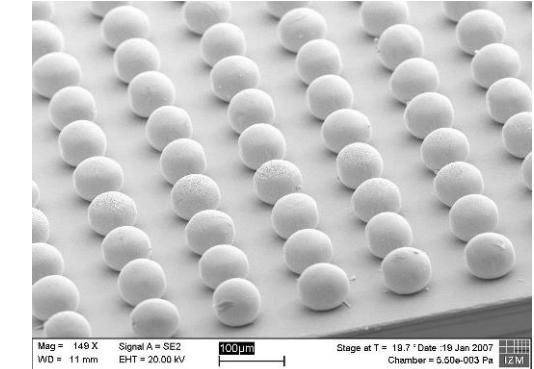
SOLDER BUMPS BY PRINTING (C4)

■ Alternative techniques for Printing

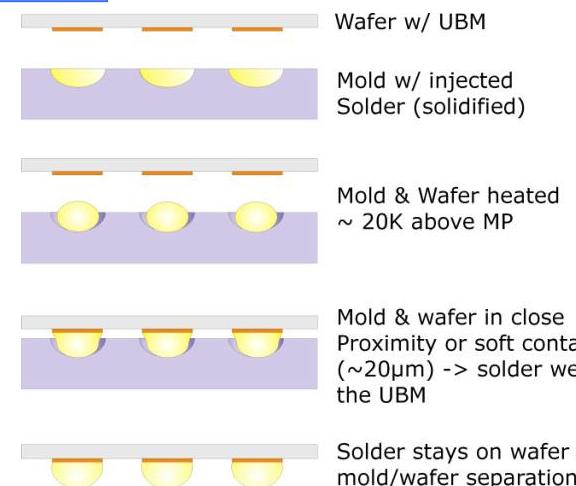
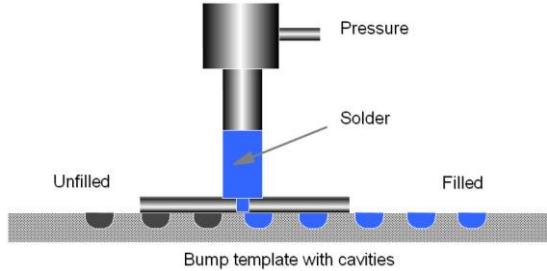
■ Direct printing on a film



Source : T. Baumgartner /
Fraunhofer IZM / EPTC 2007



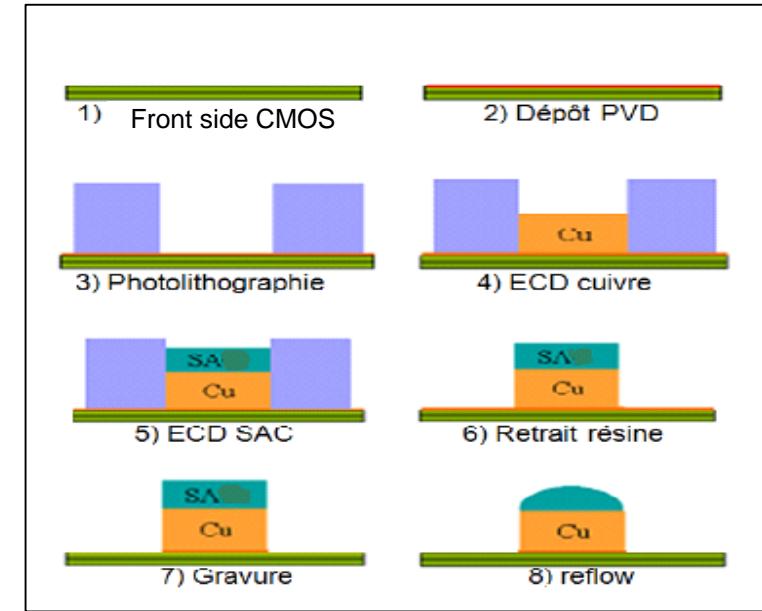
■ C4NP technique



Source : D. Tonnes / Suss Microtech

Semi-additive electroplating growth:

- Full sheet seed PVD deposition Ti-Cu
- Photolithography with thick resist (>0 or <0)
- Electroplating of the metals:
Cu-(Ni)-SnAg- (Au)
- Resist stripping
- Seed wet/dry etching
- Reflow



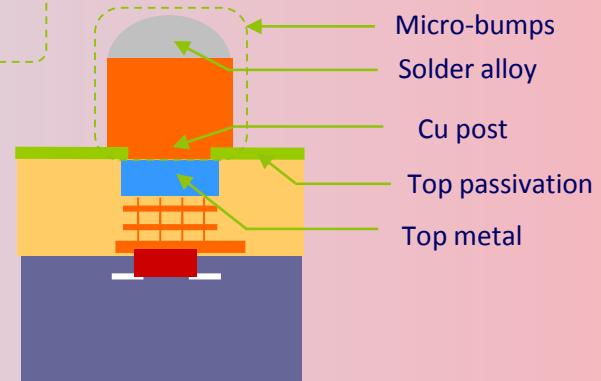
From C. Ribi  re CEA-Leti 2015

Challenges for fabrication of microbumps $\ll \text{Ø}20\mu\text{m}$:

- New thick resist with better definition
- Limitation of the seed layer under-etching
- Control of the IMC Cu/SnAg for reliability (mechanical and EMG)

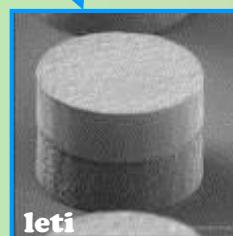
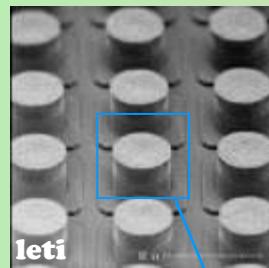
- Wafer size : **300 - 200 mm**
- Micro-bumps material : **Cu post / SnAg 305 solder**
- Minimum pitch : **40 µm**
- Minimum micro-bumps diameter : **20 µm**
- Micro-bumps thickness (typical): **Cu 10µm / SnAg 10µm**

Micro-bumps DRM & schematic

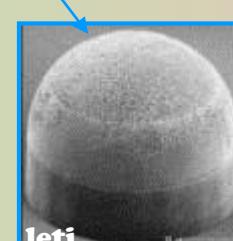
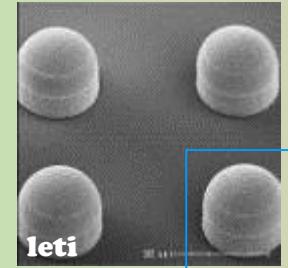
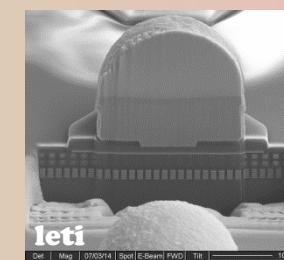
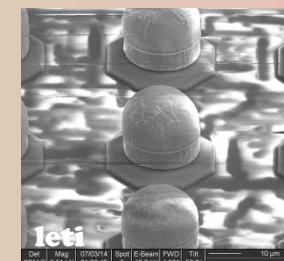
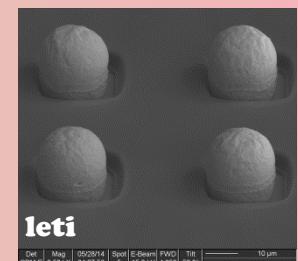


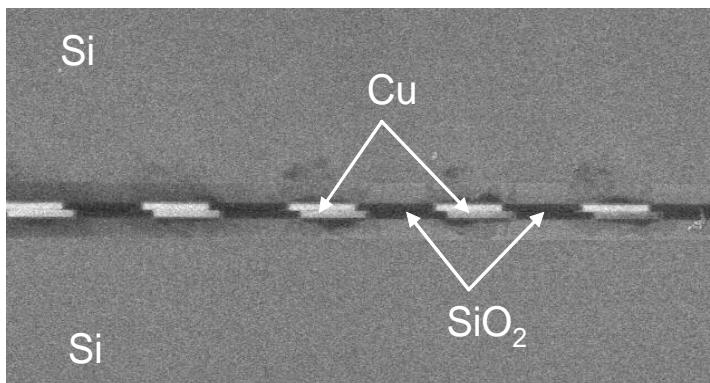
Micro-bumps Morphological illustrations

Micro-bumps before reflow

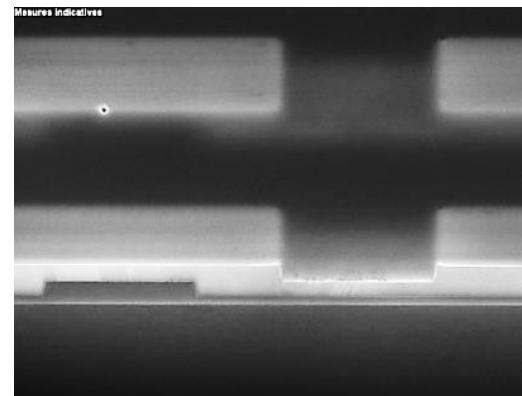


Micro-bumps after reflow

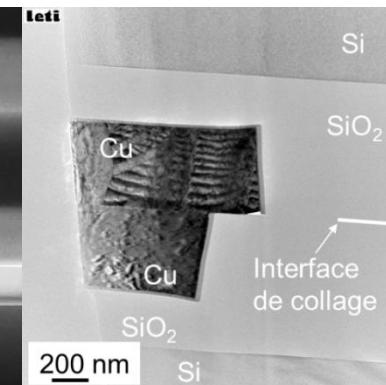
Micro-bumps on C65
D= 25 µmMicro-bumps on FDSOI28
D= 18 µm



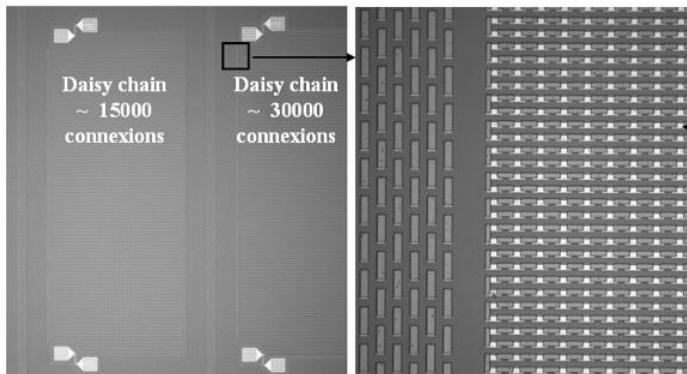
Direct bonding
WtW or DtW
Composite Cu/SiO₂ interface



SEM of bonded patterned structure (hybrid oxide-metal) at 400°C



transmission electron imaging of the copper pad bonding



14 μm pitch along x
7 μm along y

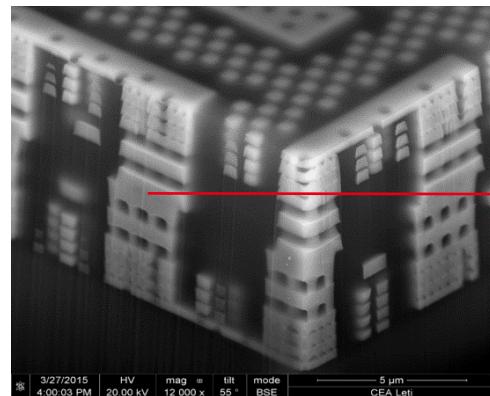
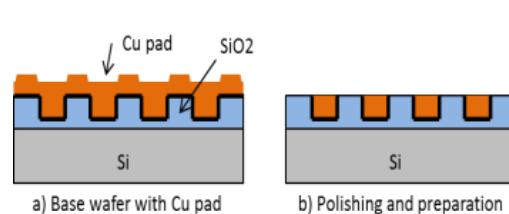
Perfect ohmic contact: $22.5 \text{ m}\Omega \cdot \mu\text{m}^2$
(Equivalent to bulk copper)
Measured resistance of 29422 interconnect daisy chain:

→ **88.5% yield, 1,2% standard deviation**

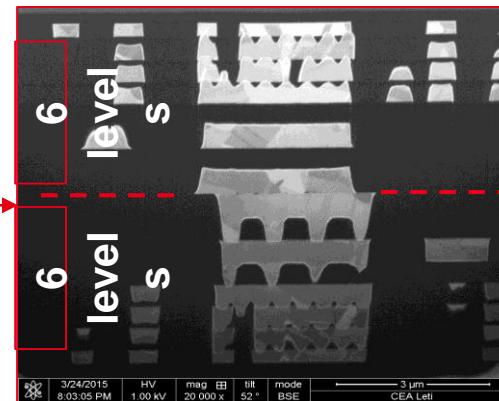
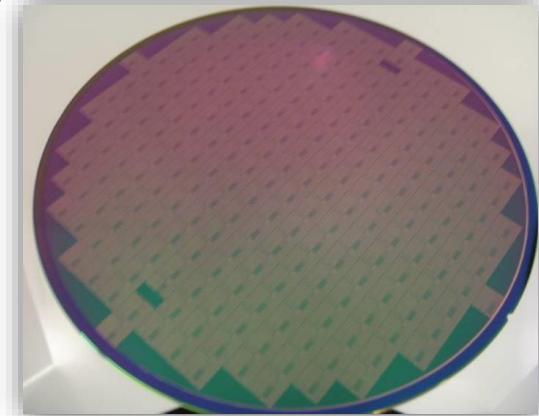
→ **Roadmap to Pitch lower than 2 μm, In Progress**

Post bonding annealing	Min (Ω)	Max (Ω)	Average resistance (Ω) DC5	Standard deviation (%)
400°C for 2h	2162	2291	2202	1.18

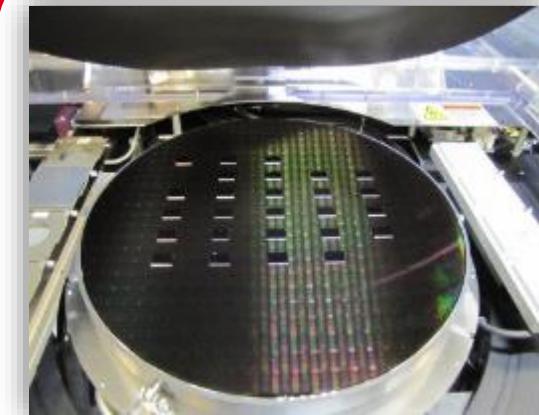
Source: "200°C direct bonding copper interconnects : Electrical results and reliability", L. Di Cioccio et al, IEDM 2011



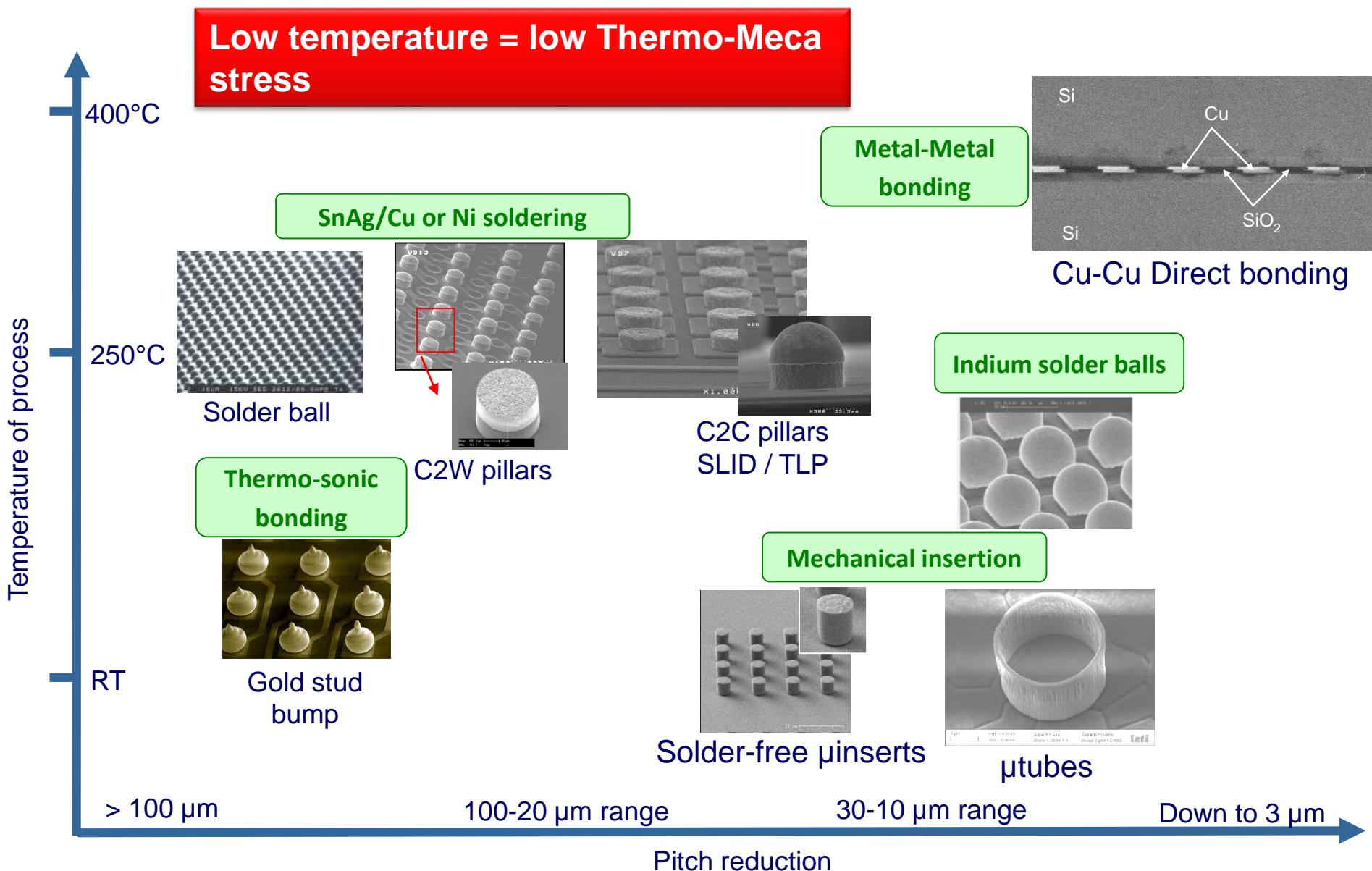
6M+ 6M BEOL

**Wafer-to-wafer**

Ultra fine pitch (<<10µm)
Throughput

Chip-to-wafer

Heterogeneity
Multi dies Stacking



3D IC stacks: (Memories)

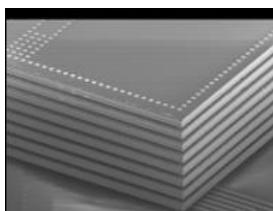
- Chip to chip
 - + Flexible : size / technologies / sources
 - Many dies stack
 - + Yield : known good dies
 - - no WL process (mass reflow, WLUF)
 - - - Throughput
 - - Alignment

2.5D/Interposer: (HPC)

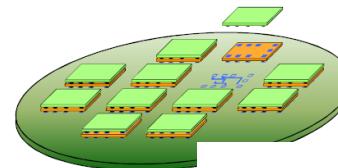
- Chip to wafer
 - + Flexible : size / technologies / sources
 - + Yield : known good dies
 - - Throughput
 - - Alignment

Direct/Hybrid bonding (Imager)

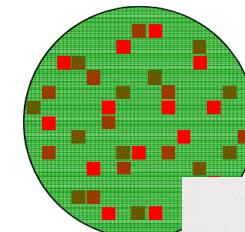
- Wafer to wafer
 - + Cost
 - + Throughput
 - - Wafer yield
 - - 2 levels
 - - TSV needed
 - - Chips size must match
 - - Interco techno limitation



SET FC 300



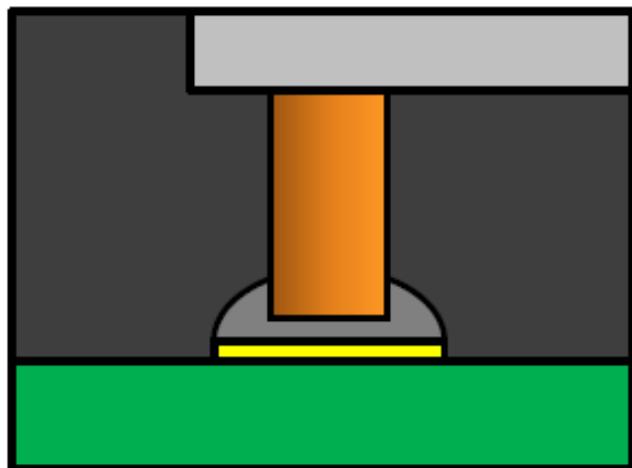
Source : G. Lecarpentier / SET / DPC
P&P Besi, Toray,
Panasonic
Séminaire imageur - Paris - Juin 2017



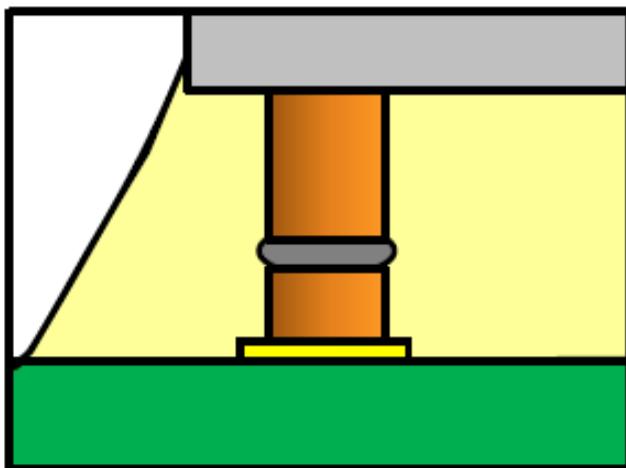
Bonder EVG 520i

2 die bonding techniques with copper pillars

Thermal Bonding



Thermo Compression Bonding



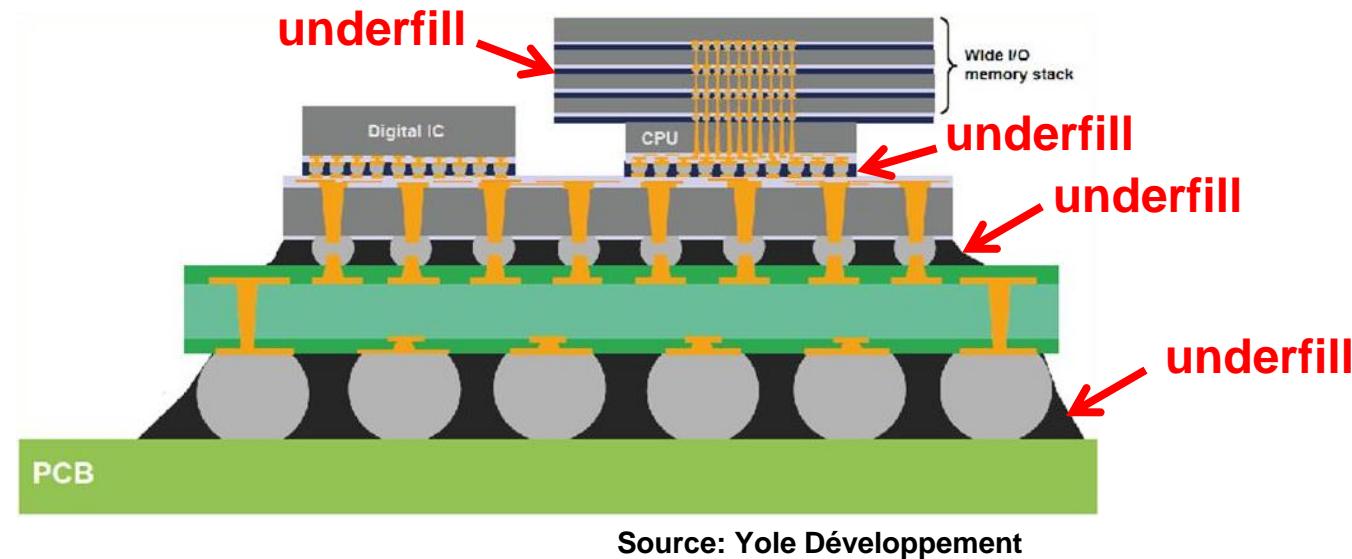
- Fluxing followed by device level reflow soldering.
- Post bond underfill (capillary or MUF)
- High bonding accuracy (pitch > 70 μm for capillary and 120 μm for MUF)
- uph = 2000-3000
- Applications:
 - Low cost flip chip (especially in mobile applications)
 - Flip chip on leadframes (PMUs, power devices)

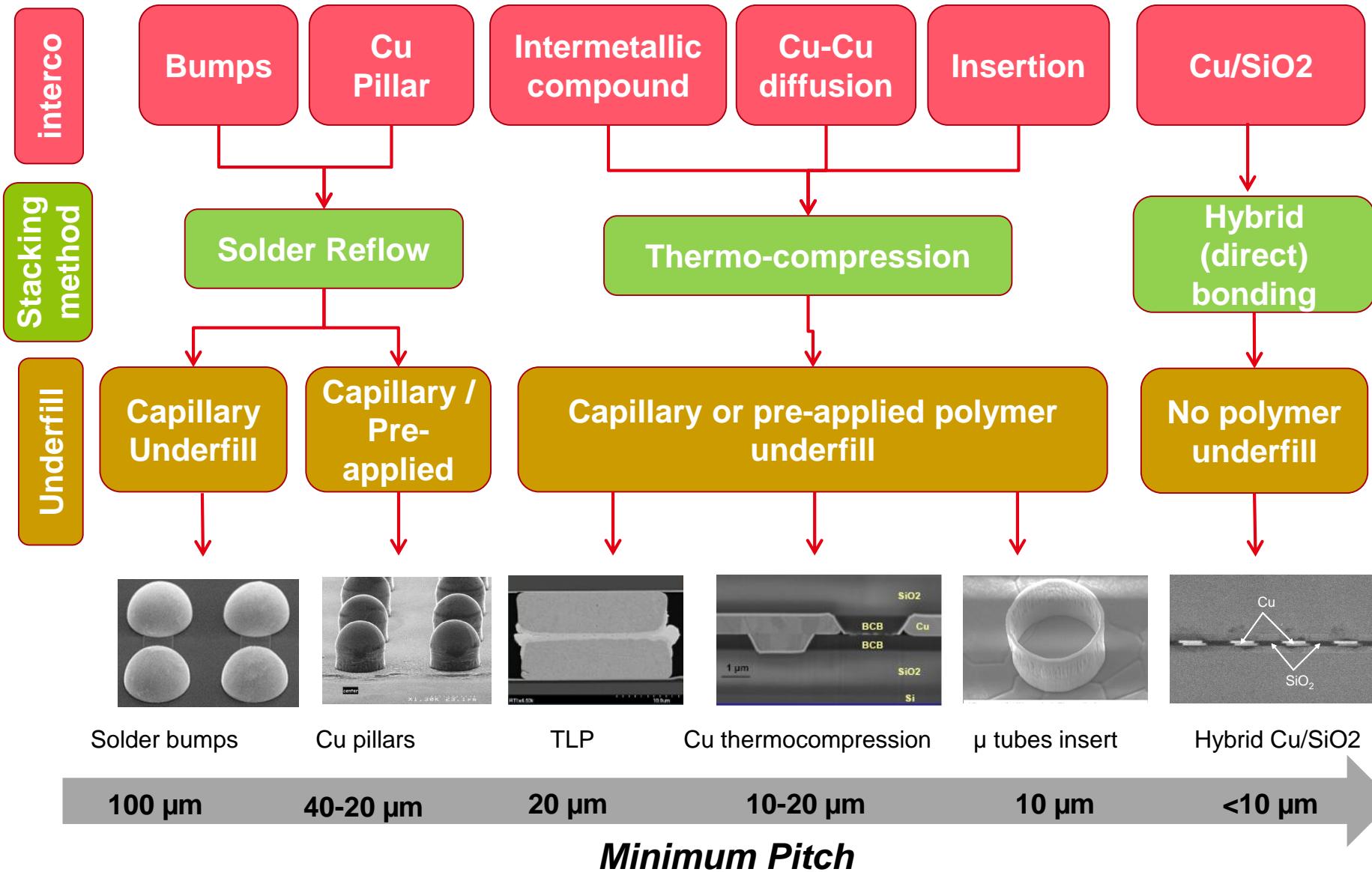
- No fluxing, thermo compression with local reflow
- NUF (pre-bond underfill)
- Very high bonding accuracy. Pitch down to 20 μm in the coming years
- uph=500
- Applications:
 - Low cost flip chip with high IO density
 - On current CSP and BGA substrates
 - On coreless substrates
 - Silicon to silicon microbumping

Underfill = material filling the gap created by interconnections between two parts (chip or substrate)

Used for different purposes:

- physical barrier to moisture to avoid corrosion
- filling the air gap around the interconnections before overmolding
- lowering strains and stresses in the interconnections when subjected to thermo-mechanical fatigue





THE INTRA CHIP CONNECTIONS: THROUGH SILICON VIA (TSV)

Post process vias or via last

CMOS FE

CMOS BE

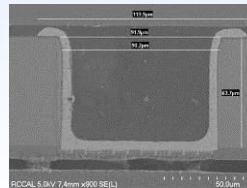
Vias

Packaging



Low temp. process
Technology flexibility
Very Low resistance

Copper liner



Mid process vias

CMOS FE

Vias formation

CMOS BE

Vias exposure

Packaging

BEOL comp.
Technology cost
Low resistance



Holes filled with W/Cu

Pre process vias
Or Via first

Vias formation

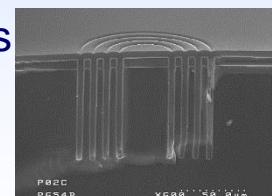
CMOS FE

CMOS BE

Vias exposure

Packaging

FEOL/BEOL comp.
Technology cost
medium resistance



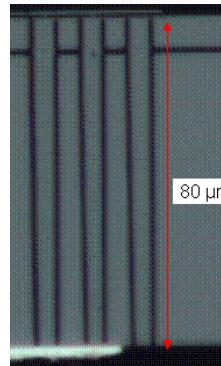
Annular rings

filled with
polysilicon

**no dedicated design
Density limitation**

**Dedicated design
High density capability**

**Application specific
Density limitation**

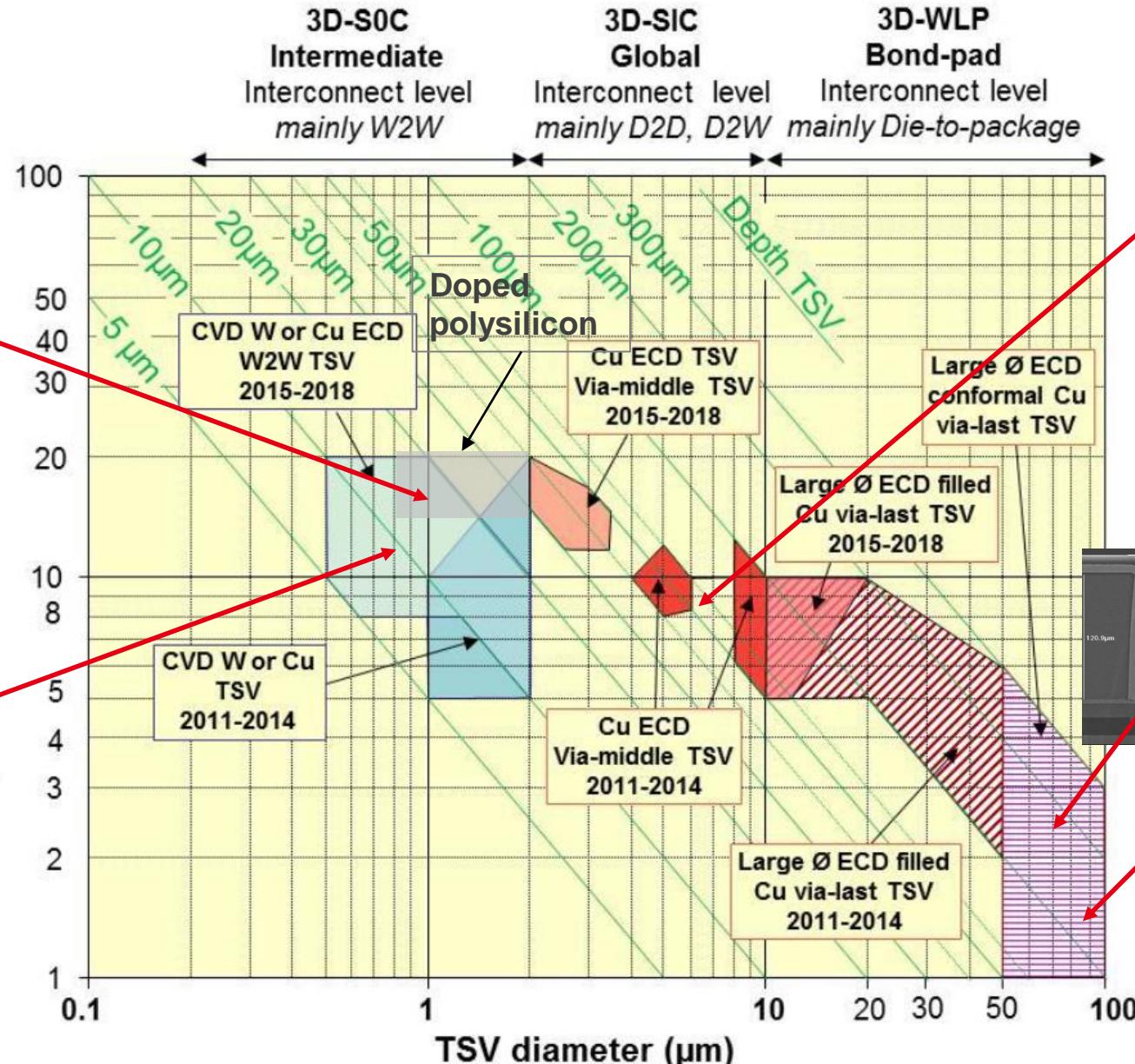


Poly Si

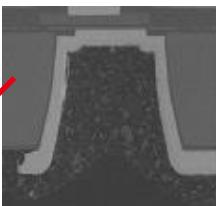
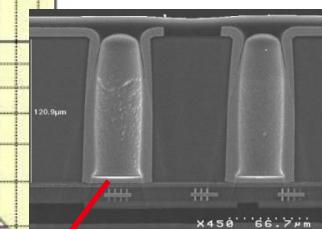


Tungsten

TSV Aspect Ratio:
Depth : minimum width or diameter



Copper liner

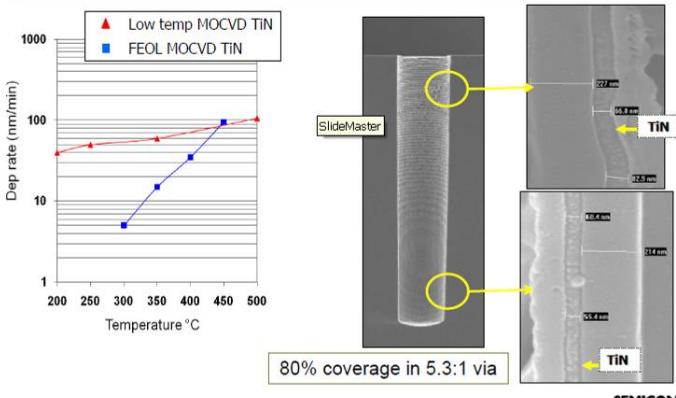


Copper filled

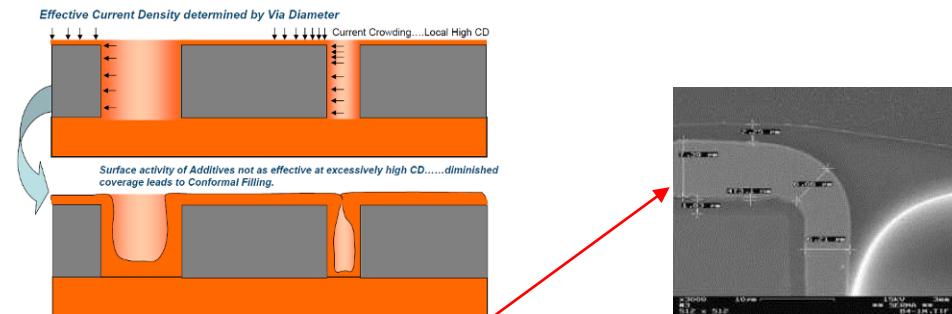
Isolation and Metallization : due to temporary bonding technique use of low temperature processes ($< 250^{\circ}\text{C}$ / $< 200^{\circ}\text{C}$) is required

- Isolation dielectric : Low temperature CVD SiON with high conformity deposition (~50%)

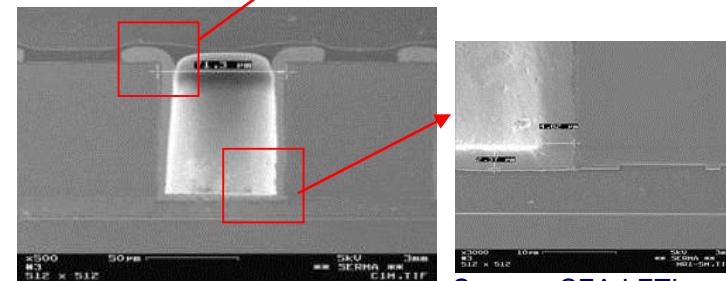
<200°C MOCVD TiN Barrier

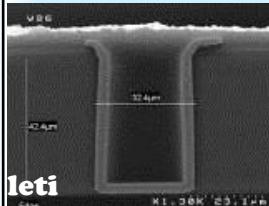
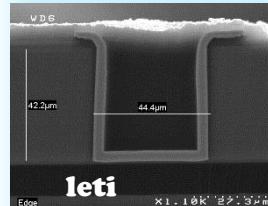
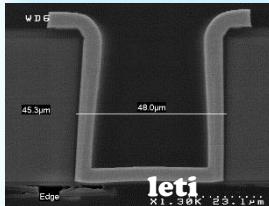
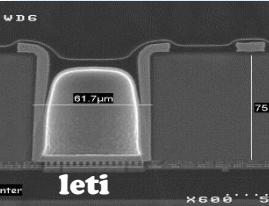
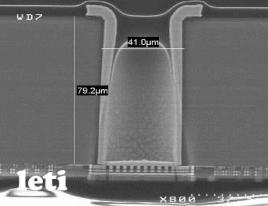
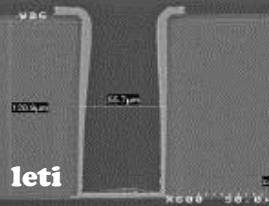
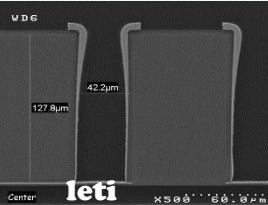
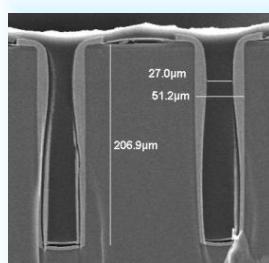
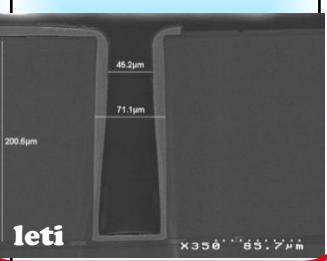


- Barrier / seed layer deposition :
 - PVD \rightarrow AR $\leq 2:1$
 - MOCVD Ti/Cu deposition \rightarrow AR $> 2:1$



- Electroplating
 - Cu liner or Cu filling
 - Choice of electrolyte : 2 or 3 additives
 - DC or pulse current
 - Hydrodynamic conditions



TSV diameter	30 µm	40 µm	50 µm	60 µm	80 µm	
AR 1:1 & 1.5:1						
AR 2:1	Not yet demonstrated :(	Available Not yet required :-)			
AR 3:1	Not yet demonstrated :(	Available Not yet required :-)			
AR 5:1	Available Not yet required :-)		Not yet demonstrated :(

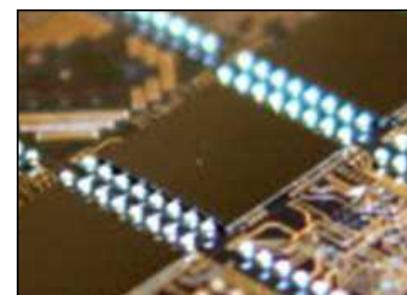
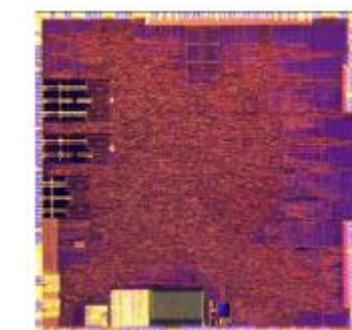
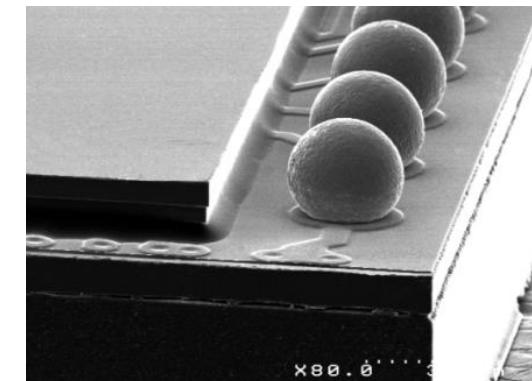
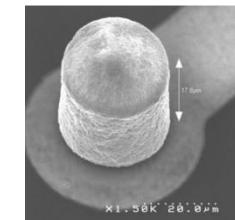
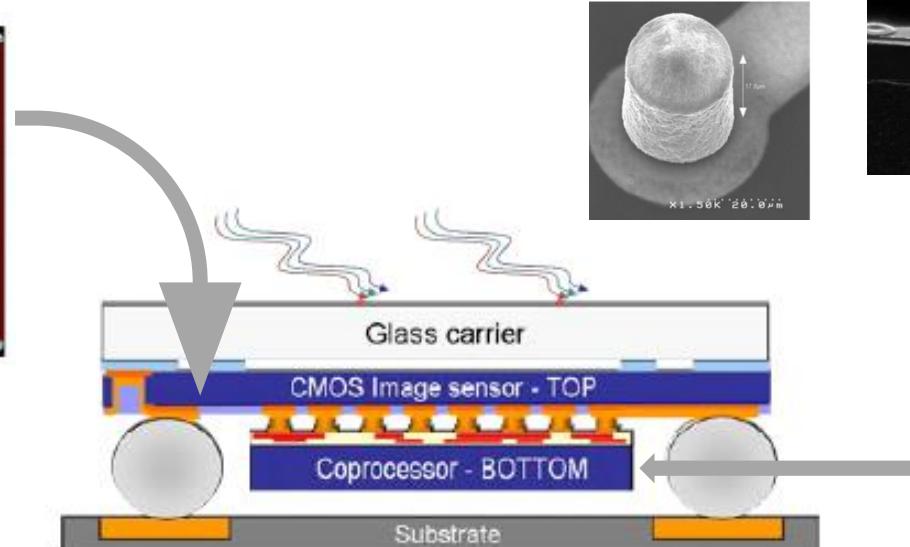
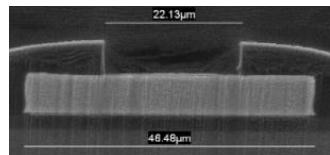
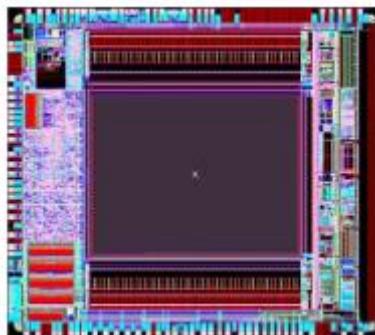
APPLICATION EXAMPLES

IMAGE SENSORS

- **Visible light**
 - Cmos Image Sensors for consumers (mobile): CIS
- **X-rays / Elementary particles**
 - CERN: Medipix experiment
 - CERN: ATLAS experiment

CMOS images sensor 3D demonstration (2012)

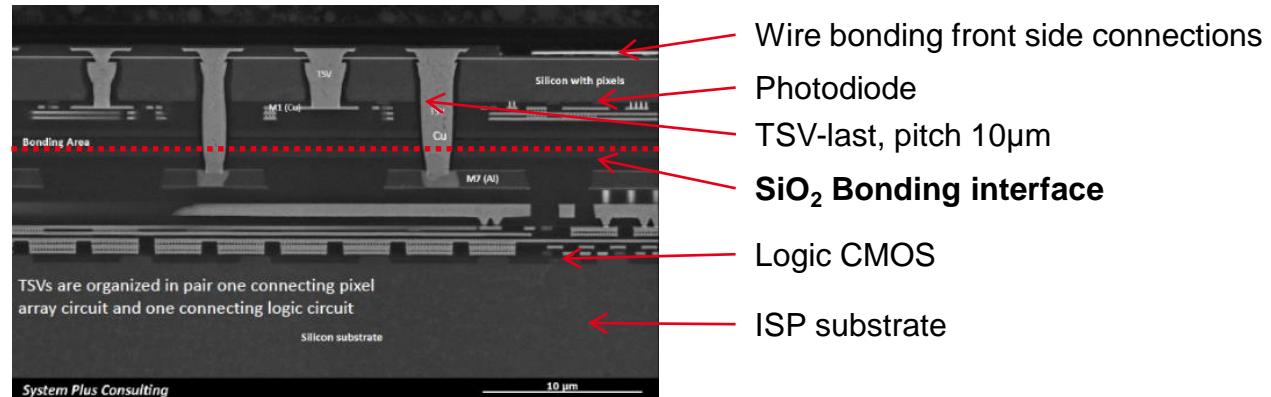
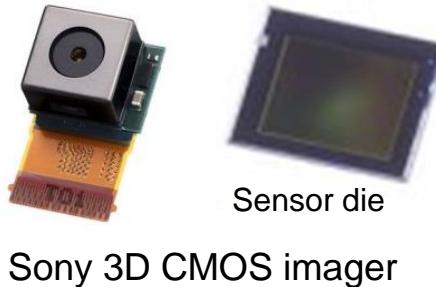
- 3D stack of 2 partitionned dies
- 65nm processor reported below a 130nm image sensor



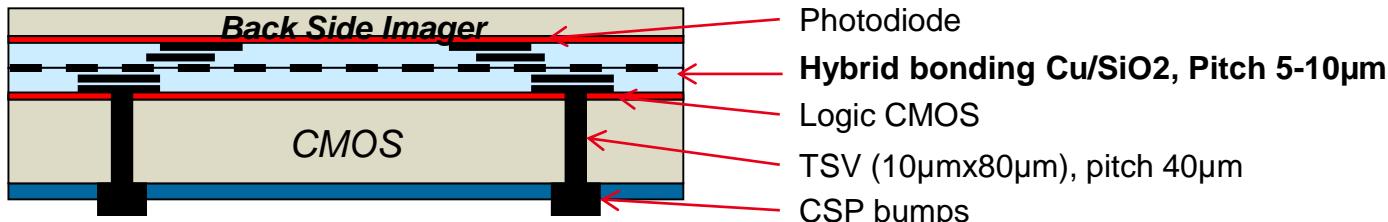
ANR 3D-IDEAS project -
2012

	CMOS	BEOL	I/O count	Dimensions
Image sensor	130 nm	3ML + AP	80	5.0x4.4 mm ²
Coprocessor	65 nm	7ML + AP	164	3.4x3.5 mm ²

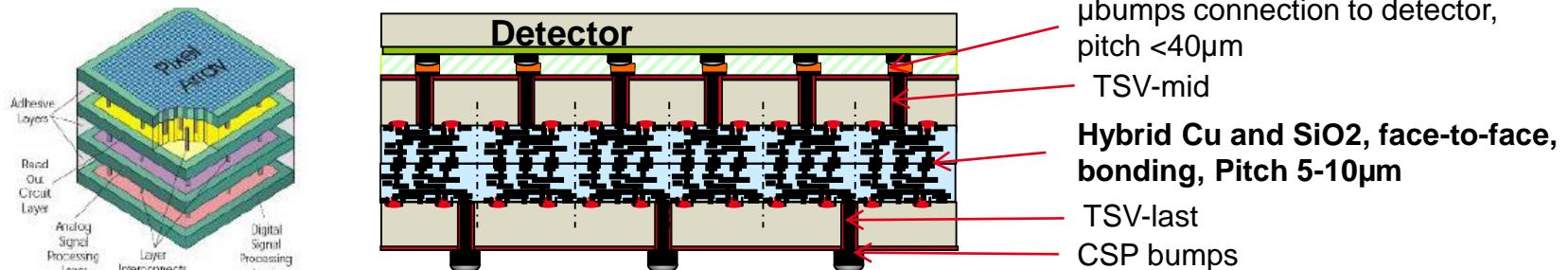
- Step 1 : current solution (Back Side Imager stacked on Image signal processor)



- Step 2 : 2-layer 3D imager (BSI stacked on CMOS with hybrid Cu/SiO₂ bonding)



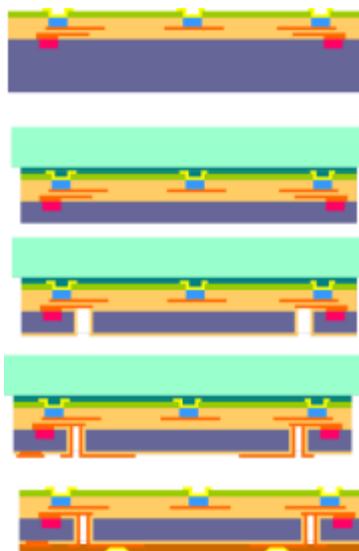
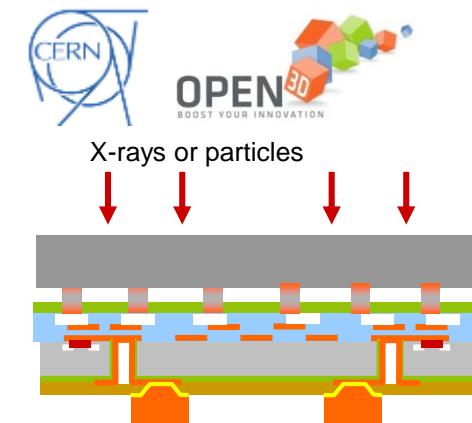
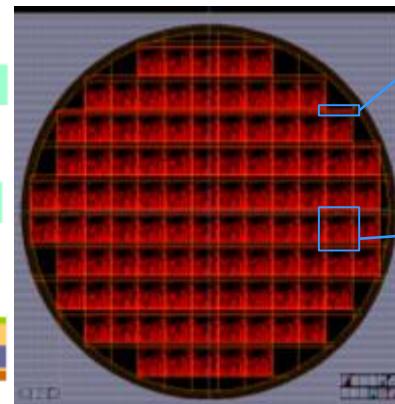
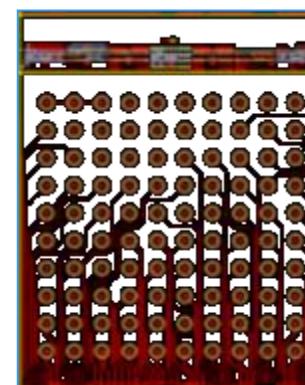
- Step 3 : 3-layer 3D imager (detector on 2 CMOS layers)



- **Visible light**
 - Cmos Image Sensors for consumers (mobile): CIS
- **X-rays / High energy**
 - CERN: Medipix experiment
 - CERN: ATLAS experiment

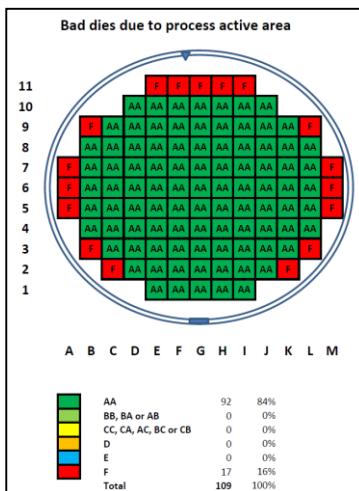
CERN – LETI project summary 2011 -2015

- Product : hybrid pixel detector for medical applications
- TSV-last made in Medipix3 - Medipix RX – timepix3 wafers (130nm)
- Suppression of lateral wire bonding
- Buttable sensors assembly: no dead zone between sensor

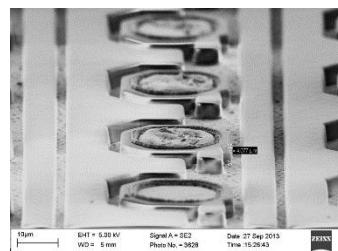
**Medipix specifications****Design****Process Flow****Wafer view****Test structures****Single chip**

- Wafer diameter: 200mm
- Wafer thickness: ~725um
- IC Technology: 130 nm / IBM
- Top Surface: Al + Nitride
- Chip size : 14100 x 17300 μm
- TSV per chip: ~100
- TSV aspect ratio :
120:60 μm (MEDIPIX RX)
50: 40 μm (timepix3)

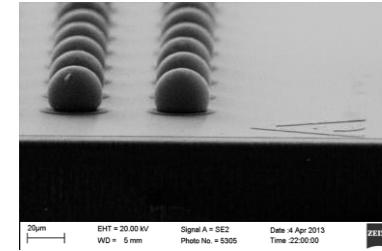
MEDIPIX3 FUNCTIONAL RESULTS (2013-2014)



→ No yield loss due to TSV technology except on wafer edge due to process edge exclusion

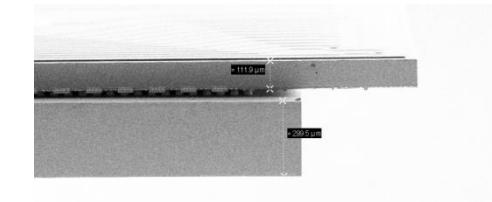


Pixel pad on ROC

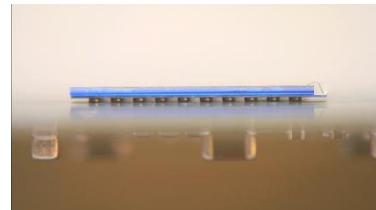
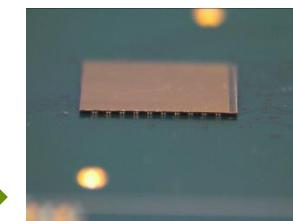
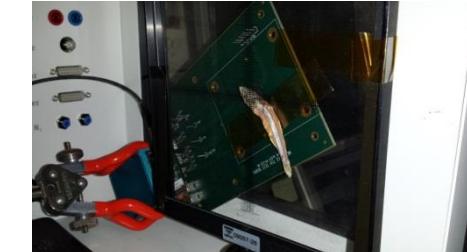


Sensor with Sn-Pb solder bumps
After reflow process

SEM images courtesy of Advacam



First Edgeless-TSV assembly
5 were provided to CERN in October 2013



BGA pads on the back side redistribution layer have been prepared with low temperature solder spheres

Assembly has been done manually for several chip and the obtained "BGA" components could be mounted using standard equipment



First image obtained with a TSV processed hybrid pixel detector (flat field corrected)



Particle detectors for ATLAS experiment (CERN)

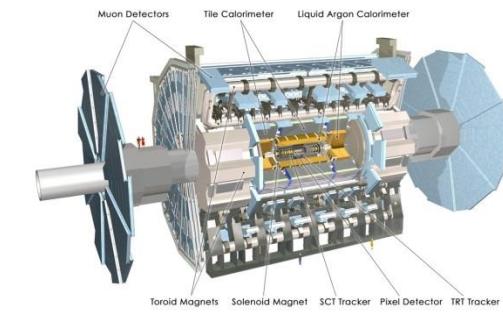
Atlas detector



Particle detectors for ATLAS experiment (CERN)

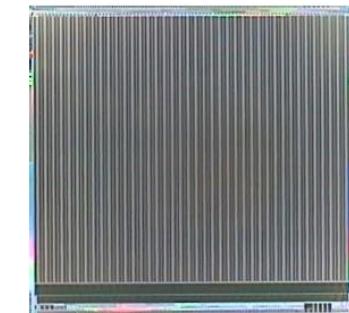
- Realization of 60 μm fine pitch Cu pillars
- Stress management of ultra large & thin ASIC Read-out circuits (20x20 mm²)

Develop an alternative wafer level back-side process, called Stress Layer Compensation (SLC), that compensates for the CTE mismatch of the ROIC CMOS front-side stack



Glasgow university

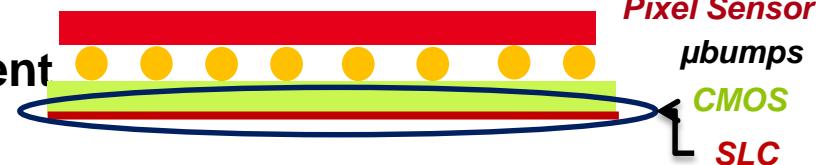
Atlas FE-I4



FEI4 size: 20 x 18.9 mm²

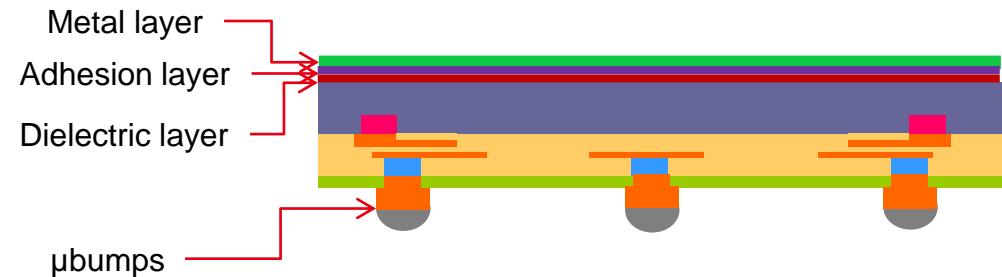
Stress compensation layer applied on thinned wafer backside

Compensation effect needs to be dynamically effective with temperature ranging from ambient to solder reflow (260° C)



Wafer level technology modules processed on FEI4 ROIC wafers

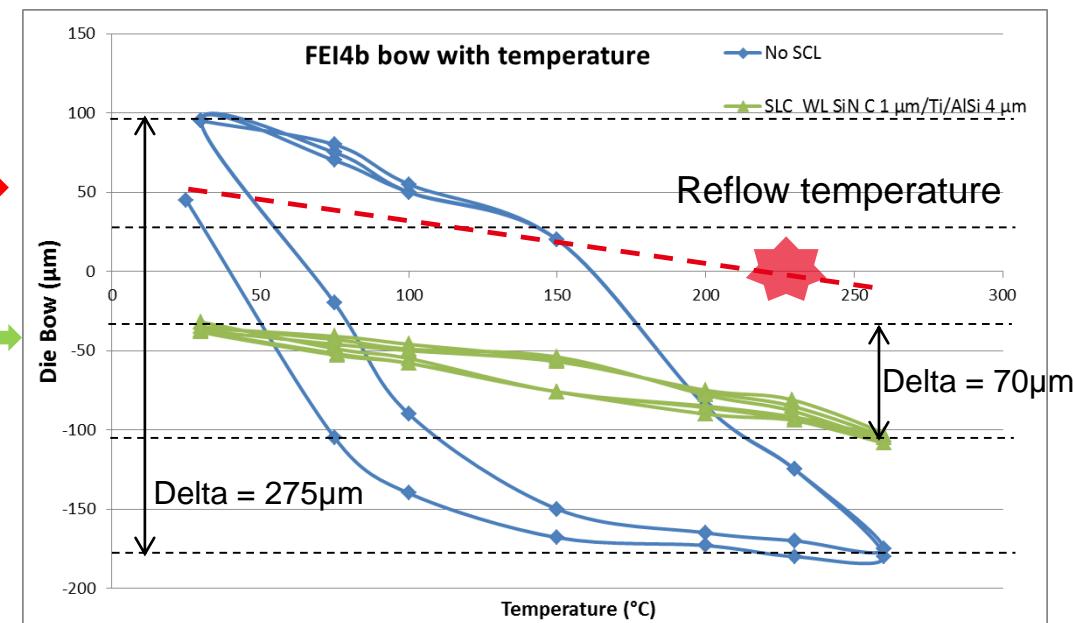
- Thermo-meca. modeling of the technology stack
- Engineering on material and processes
- Addition of dedicated layers for stress compensation



FEI4b deformation during temperature excursion corresponding to solder reflow

Simulation with 4 μm of SiN = →
Ideal results

Last and best results obtained →
SiN C 1 μm /AlSi 4 μm

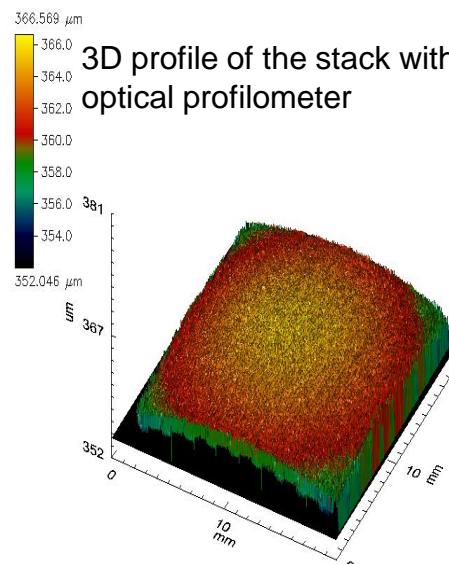


→ Already 4X reduction of bow amplitude with SCL

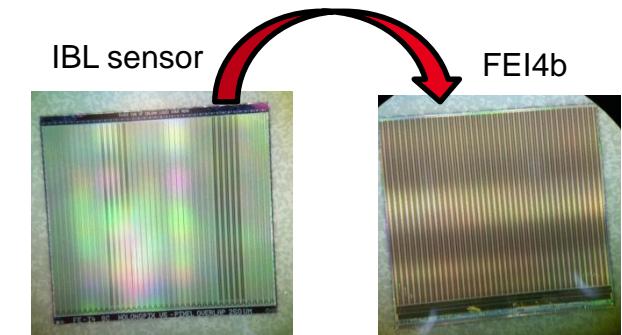
- Work done in collaboration with **LAL-Orsay**
- FEI4 functional chips with micro-bumps, thickness = 280 µm
- IBL functional chips with UBM Ti/Ni/Ag pads, thickness = 280 µm

Flip chip technology:

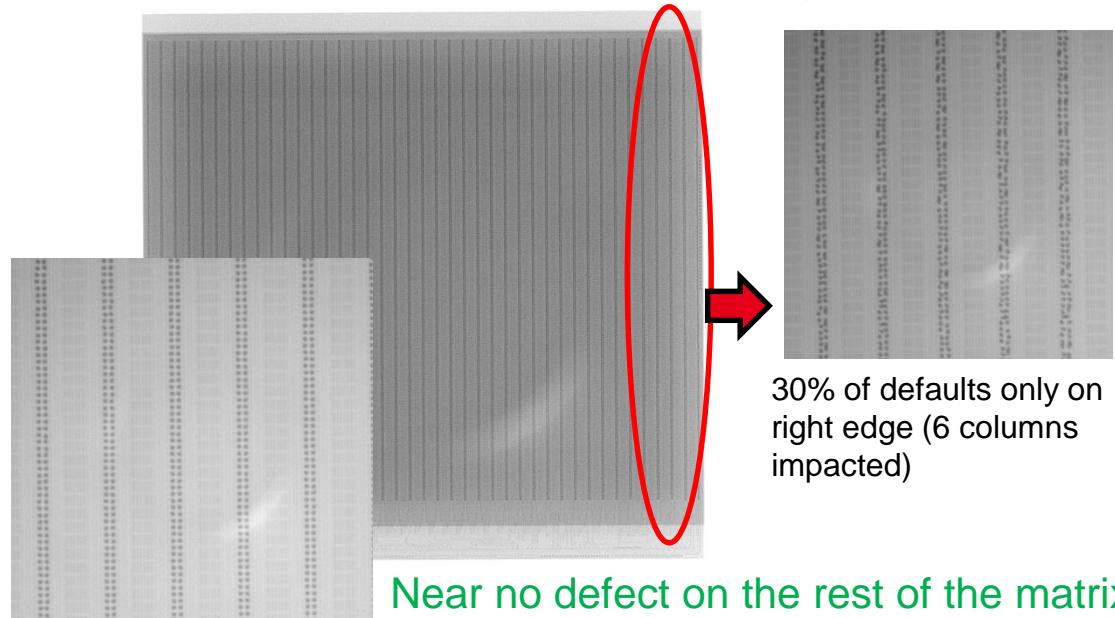
- Flux dipping of bottom die (FEI4)
- Pick and Place with high precision automated equipment (SET150)
- In Situ soldering by thermo-compression



co-planarity after die stacking ~ 6 µm



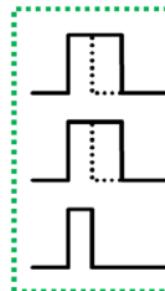
RX picture of the full die after flip chip soldering



→ New developments are discussed with CERN for RD53 ROIC

The passage of the ionizing particle translates into two coincident avalanche current pulses

SPAD "top"



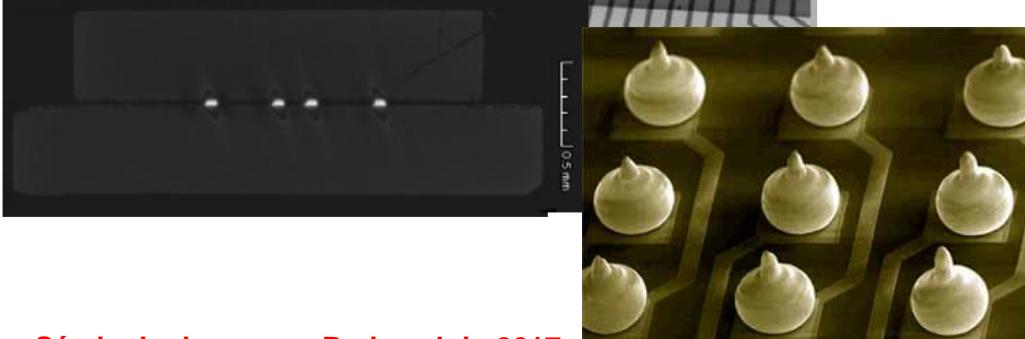
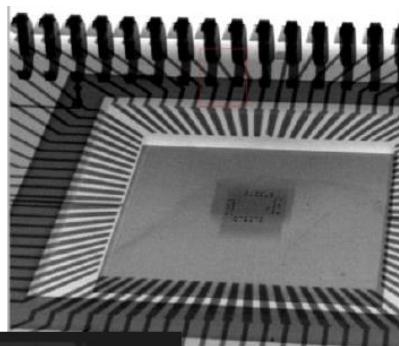
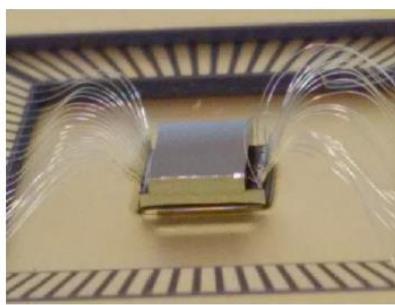
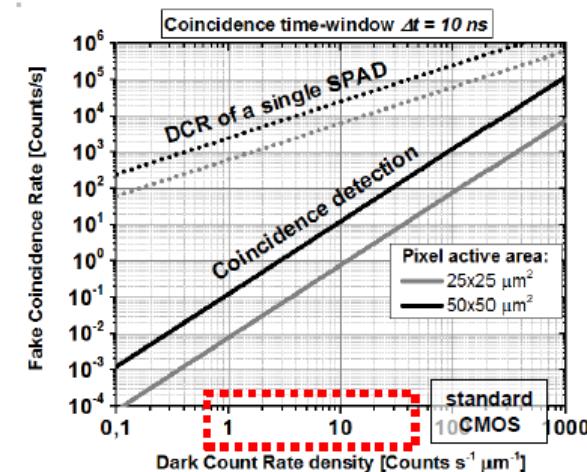
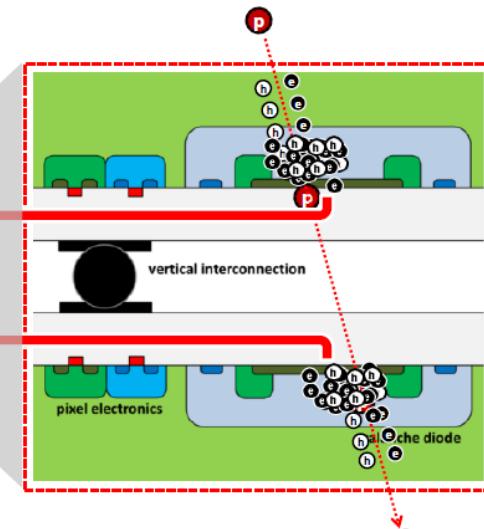
SPAD "bottom"



coincidence



The coincidence is verified thanks to dedicated electronics

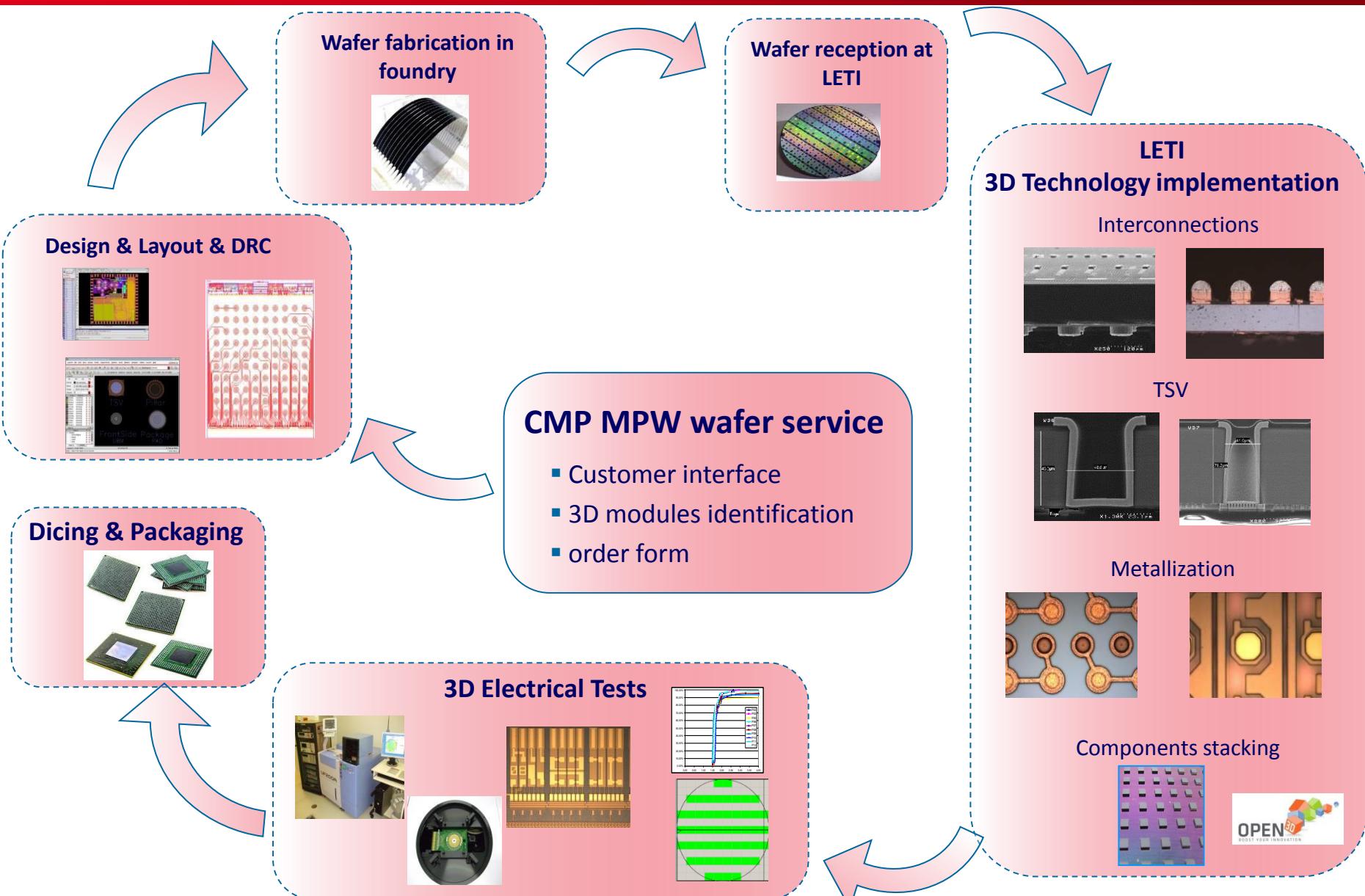


Gold stud bumping :

- Ball bonding (Thermo-sonic)
- Tail cutting
- (Coining for equalization)

Flip chip assy

- Thermo-compression (can be with NCP)
- Thermo-compression ($T > 350^\circ\text{C}$) or Thermo-sonic (+ UF)



- **Continuous developments in 3D technology field involve:**
 - High density and fine pitch interconnections
 - Low temperature interco
 - High reliability for critical applications (automotive, aerospace, medical)
 - Thermo-mechanical constraints and stress management
- **Image sensor has long been a key driver for 3D and will continue to be, we see a lot of demands in this domain from consumer, industrial to specific applications**
- **CEA-Leti can provide a broad and mature 3D technology portfolio:**
 - μ bumping and solder interface CMOS post-processing
 - Flip chip stacking D2D and D2W
 - TSV first, mid and last with different AR
 - MPW is open for 3D technologies provided by Leti