

Small pitch, thin 3D pixel sensors for phase 2 upgrades at LHC

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Journée thématique:
Fabrication de détecteurs semiconducteurs



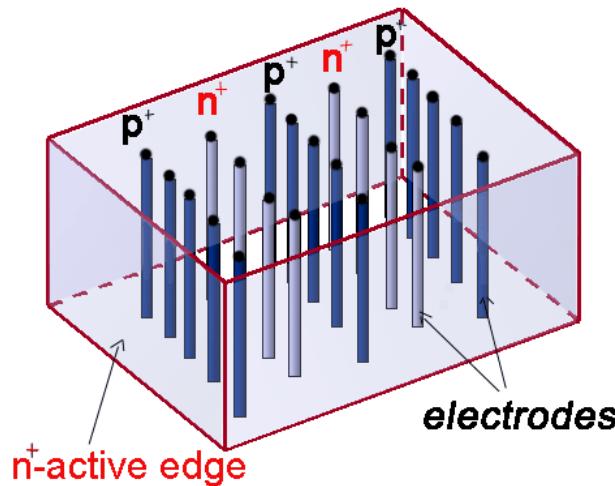
14 juin 2017

Outline

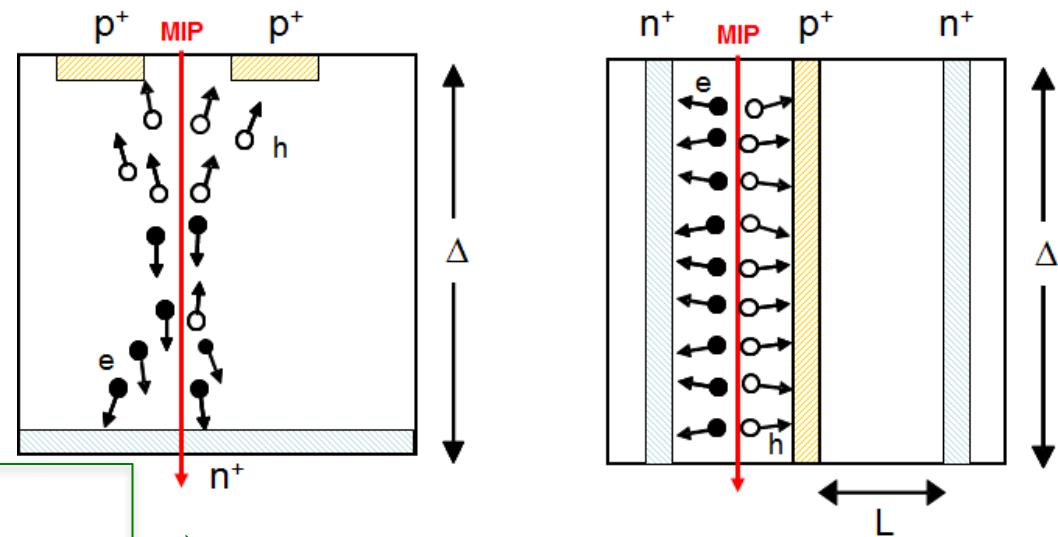
- Introduction:
 - 3D sensors
 - The HL-LHC challenge
- New small-pitch, thin 3D sensors
 - Main design and technological issues
 - Results from 1st batch
 - Design of 2nd batch
- Conclusions

3D sensors

S. Parker et. al. NIMA 395 (1997) 328



Electrode distance (L) and active substrate thickness (Δ) are decoupled $\rightarrow L \ll \Delta$ by layout



ADVANTAGES:

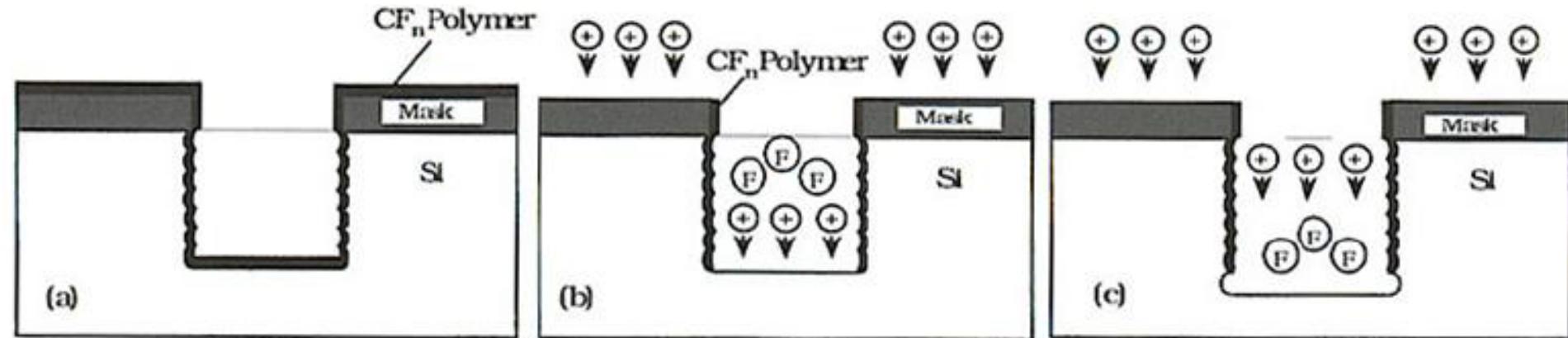
- Low depletion voltage (low power diss.)
- Short charge collection distance:
 - Fast response rise
 - Less trapping probability after irr.
- Lateral drift \rightarrow cell “shielding” effect:
 - Lower charge sharing
 - Low sensitivity to magnetic field
- Active edges

HIGH RADIATION HARDNESS

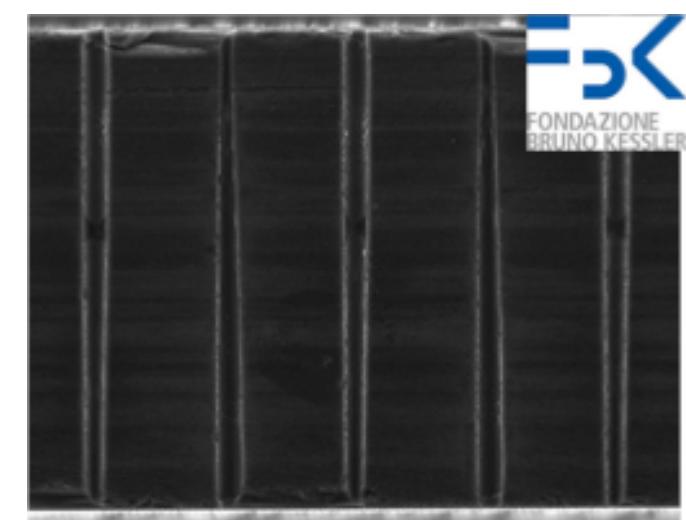
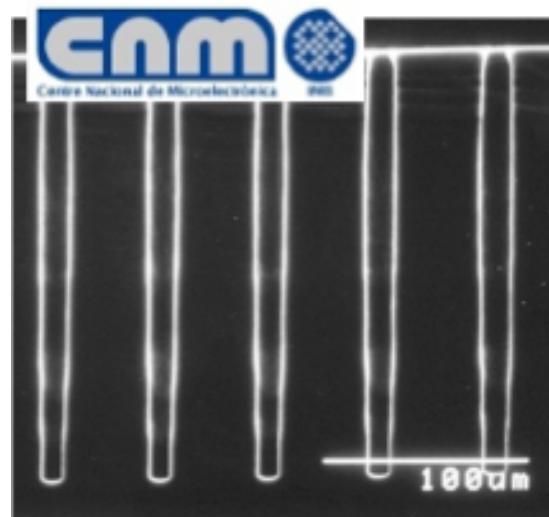
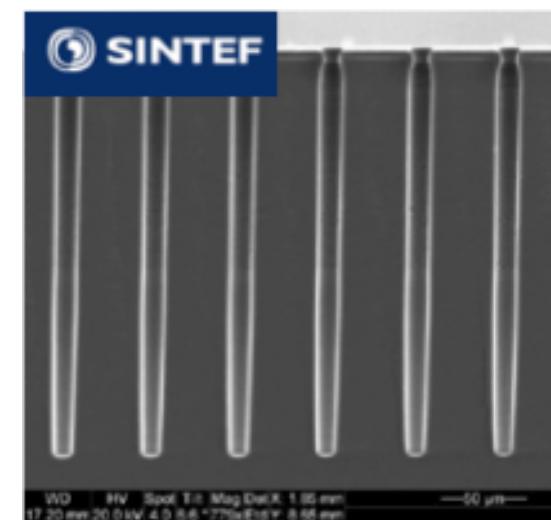
DISADVANTAGES:

- Non uniform spatial response (electrodes and low field regions)
- Higher capacitance with respect to planar ($\sim 3\text{-}5x$ for $\sim 200\ \mu\text{m}$ thickness)
- Complicated technology (cost, yield)

Key technology: DRIE by the Bosch process

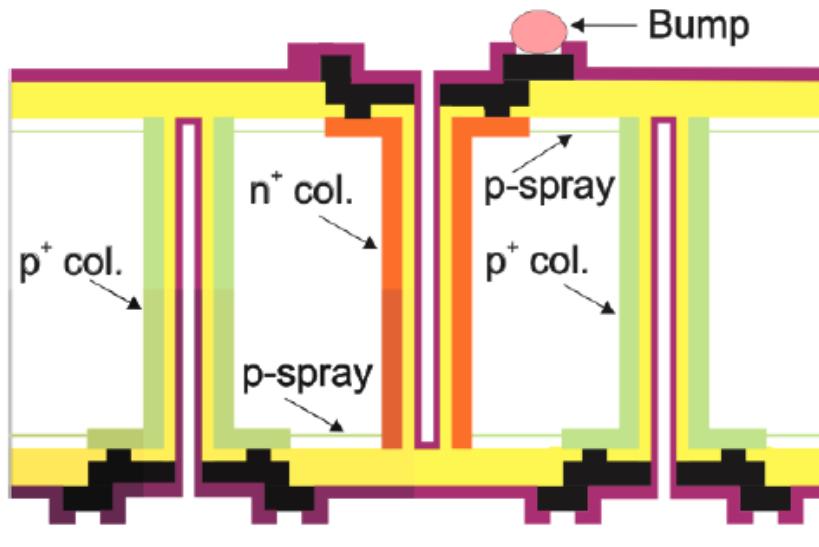


- Alternating etch cycles (SF_6) and passivation cycles (C_4F_8)
- High aspect ratio (~20:1 or better for trenches) and good uniformity



Double-sided 3D sensors of ATLAS IBL

FBK (Trento, Italy)

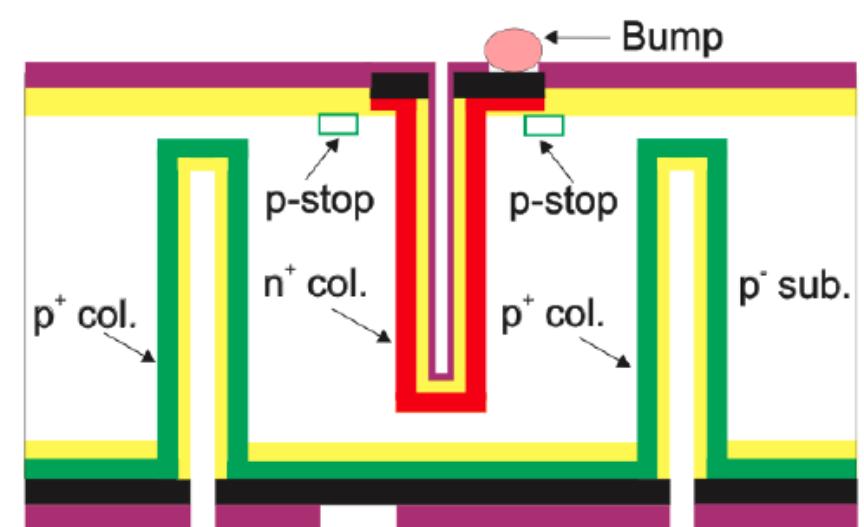


oxide	metal	passivation
p- Si	p+ Si	n+ Si

A. Zoboli et. al., IEEE TNS 55(5) (2008), 2775

G. Giacomini, et al., IEEE TNS 60(3) (2013) 2357

CNM (Barcelona, Spain)



oxide	metal	passivation	
p- Si	p+ poly-Si	n+ poly-Si	p+ Si

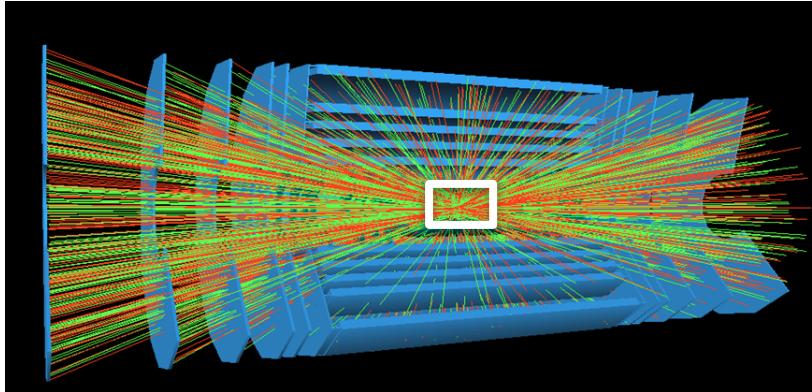
G. Pellegrini et. al. NIMA 592(2008), 38

G. Pellegrini et. al. NIMA 699(2013), 27

- Do not use a support wafer
 - Reduced process complexity, but mechanically more fragile
 - Back-side accessible for bias, easier assembly within systems
 - Active edge not feasible, but allows for slim edge

Pixel Roadmap: LHC → HL-LHC

N. Wermes, 9th TN Workshop (Genova, 2014)



Next ROC generation (RD53 65 nm)

$50 \times 50 \mu\text{m}^2$ and $25 \times 100 \mu\text{m}^2$ pixels

$C_{\text{DET}} \leq 100 \text{ fF}$

$I_{\text{leak}} \leq 10 \text{ nA/pixel}$ (no amp. comp.)

Threshold: ~1000 electrons

M. Garcia-Sciveres, J. Christiansen,
<http://rd53.web.cern.ch/RD53>

Increased luminosity requires

- higher hit-rate capability
- increased granularity
- higher radiation tolerance ($2 \times 10^{16} n_{\text{eq}}/\text{cm}^2$)
- lighter detectors

Implications for 3D sensors

Modified technology/design for:

- thinner sensors (~100 um)
- narrower electrodes (~5 um)
- reduced electrode spacing (~30 um)
- very slim (or active) edges (< 100 um)

A ~ 2x device scaling

Viable technological approaches

1) Enhanced double-sided process

- Requires minimum wafer thickness of $\sim 200 \mu\text{m}$, and improved column aspect ratio to reduce dead volumes
- Can work for 4" wafers, not suitable for 6" (too fragile)

Pros: established process, easier front side layout, back-side bias for free, higher Q for low tilt particles owing to thickness

Cons: mechanical fragility, front/back alignment critical for small pitch, larger capacitance, larger clusters at high eta due to thickness.

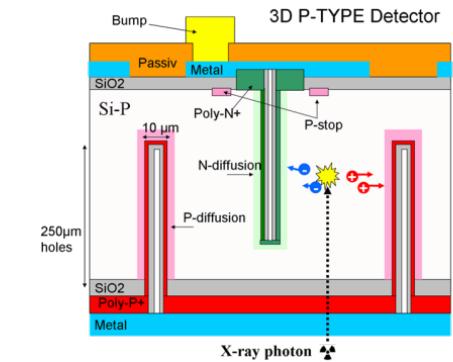
2) Single-sided process with back-side bias

- Original Full-3D Stanford process with support wafer with variations allowing for back-side bias

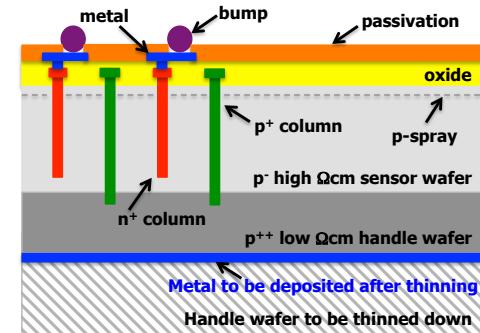
Pros: mechanical robustness, active layer thickness easily reduced to desired value, compatible with active edges

Cons: requires post processing for support wafer removal and metal deposition, front side layout can be complicated

DS-3D
on 4" wafers
at CNM



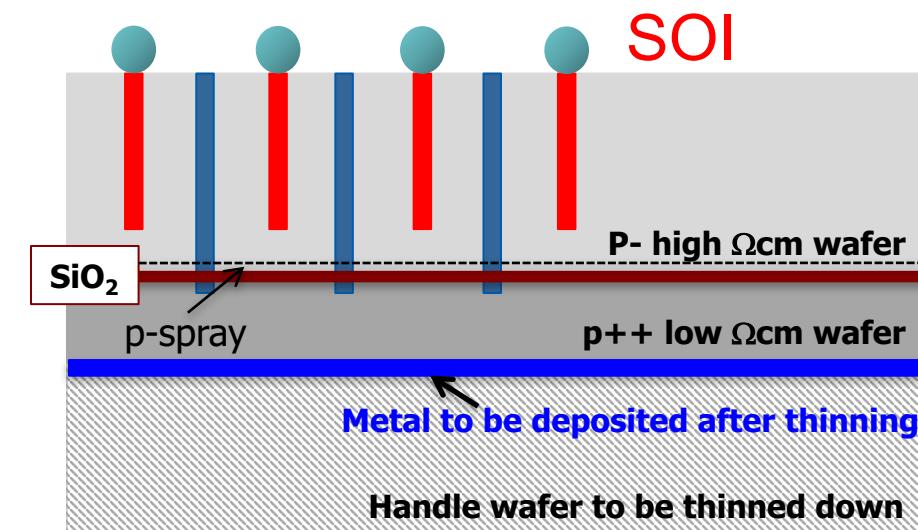
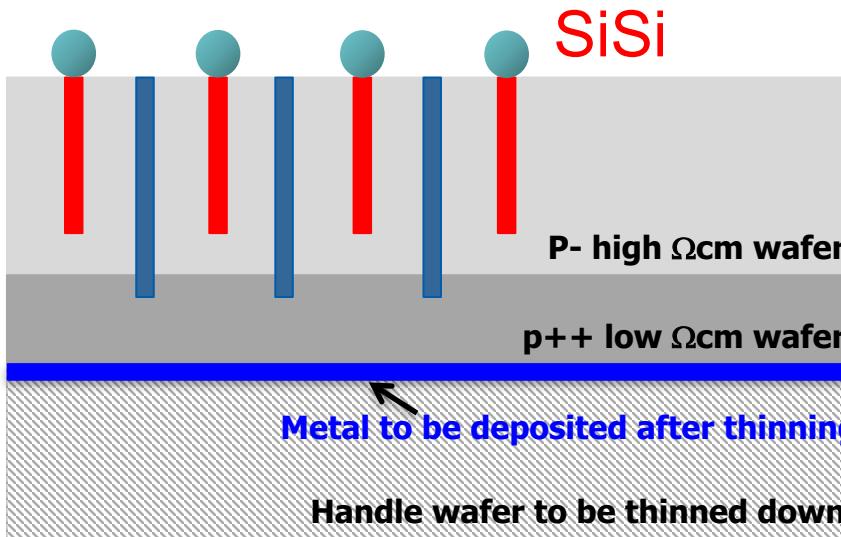
SS-3D
On 6" wafers
at FBK



New SS-3D approach at FBK

- Proposed by INFN-FBK, also used at SINTEF and SNF

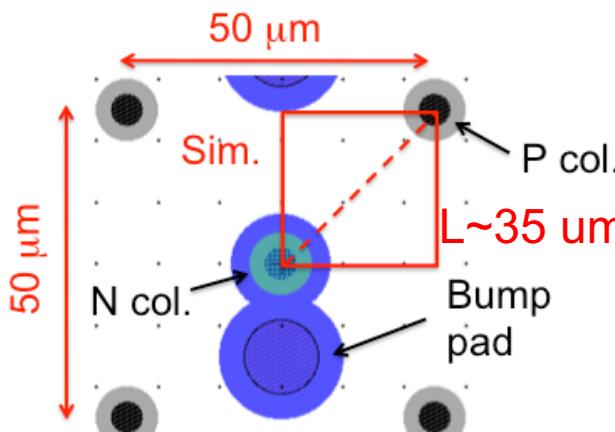
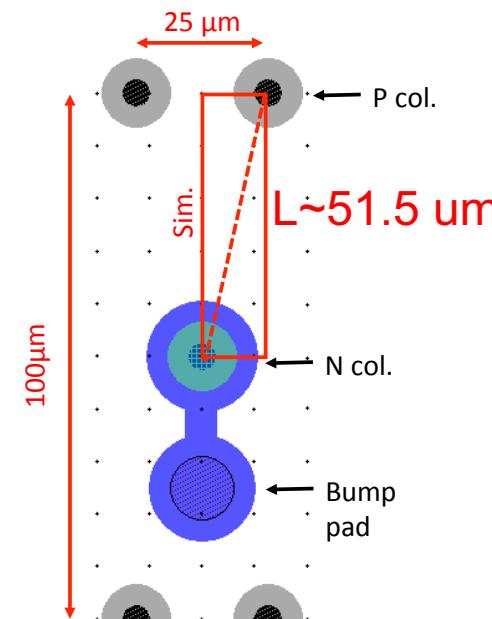
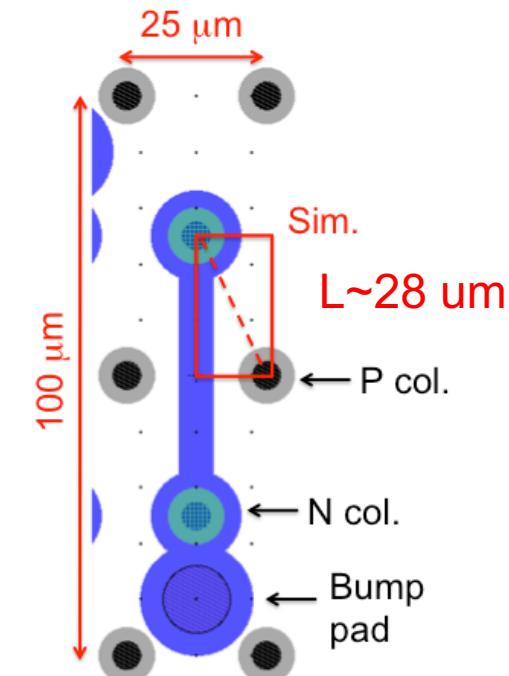
G.-F. Dalla Betta et al.,
NIMA 824 (2016) 388



- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~5 um
- Holes (at least partially) filled with poly-Si

Process
Tests

Small-pitch 3D pixel layouts: geometrical constraints

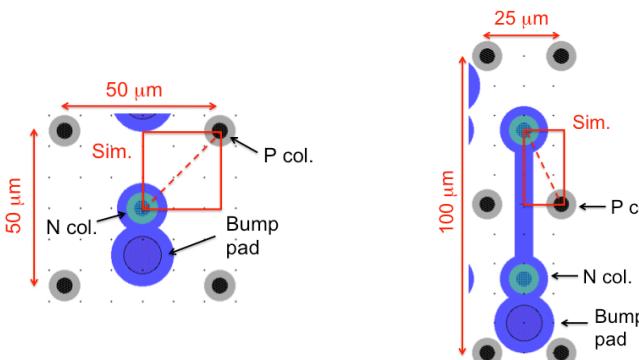
50 x 50 (1E)**25 x 100 (1E)****25 x 100 (2E)**

All designs refer to FBK SS-3D process, assuming $d=5 \mu\text{m}$

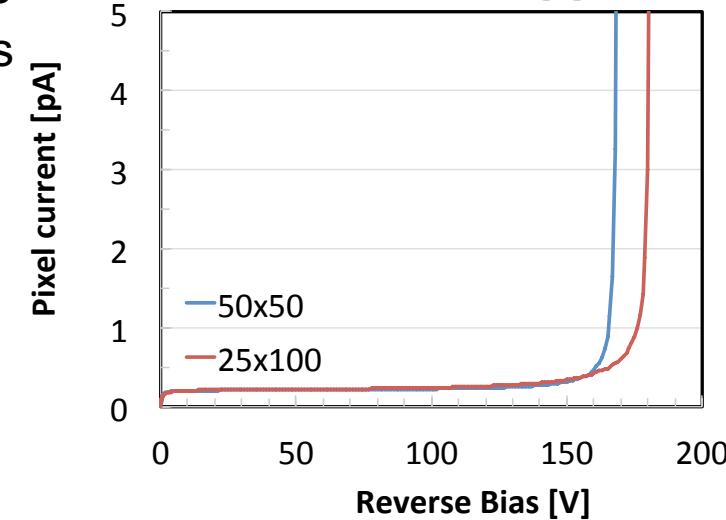
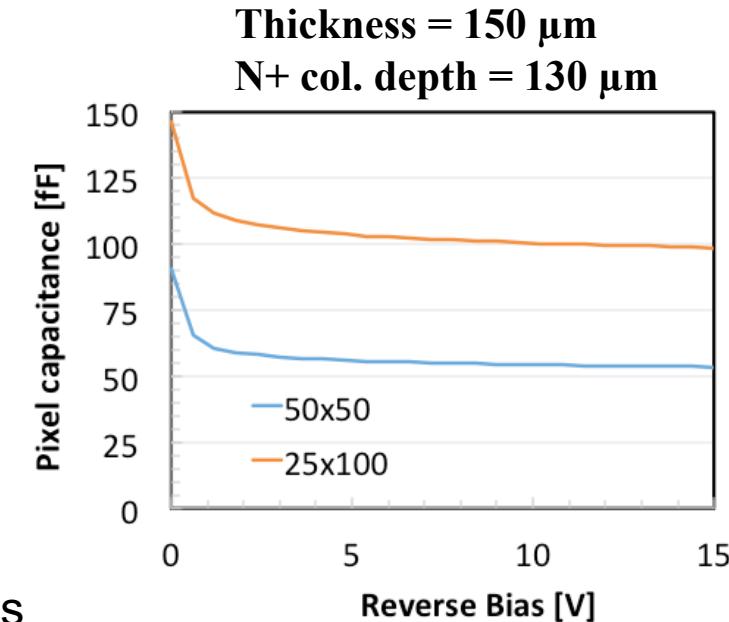
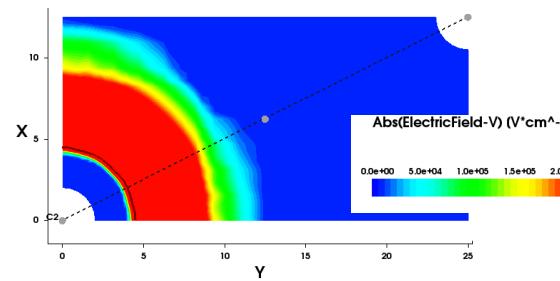
- No problems with 50x50 -1E (and 25x100 -1E) designs
- 25x100 -2E is difficult with SS-3D, because of the bump pad (not scaling ...)
- New ideas to be tested in SS-3D (e.g., bumps on columns)

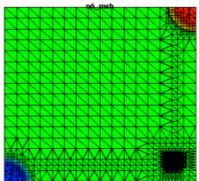
New SS-3D pixel simulations

- Full 3D simulation with parameters representative of FBK technology
- All simulations assuming $d=5 \mu\text{m}$



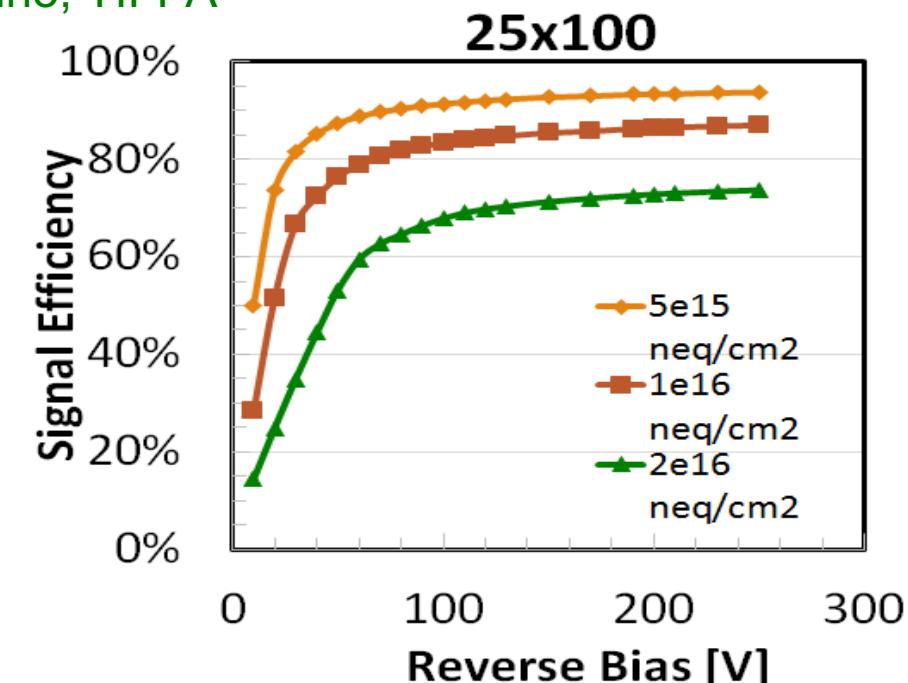
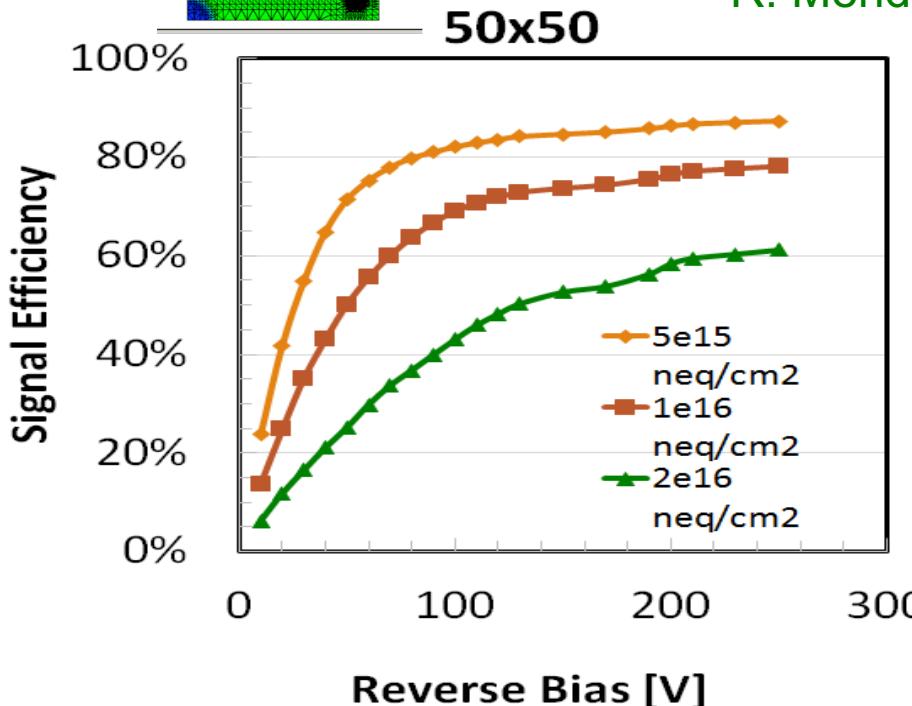
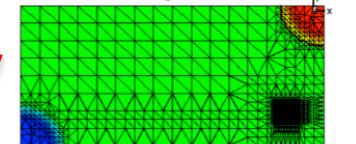
- 50x50-1E and 25x100-2E structures
- Capacitance compatible with RD53s specifications ($\sim 50 \text{ fF}$ per column)
- Initial breakdown voltage very high





Simulated Signal Efficiency

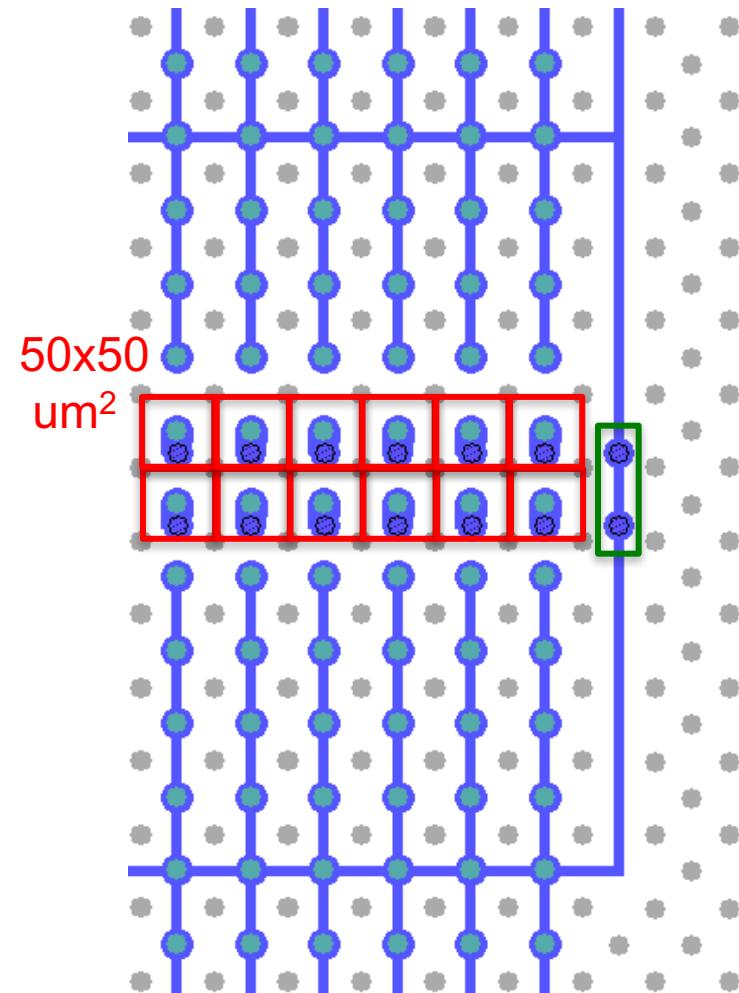
R. Mendicino, TIFPA



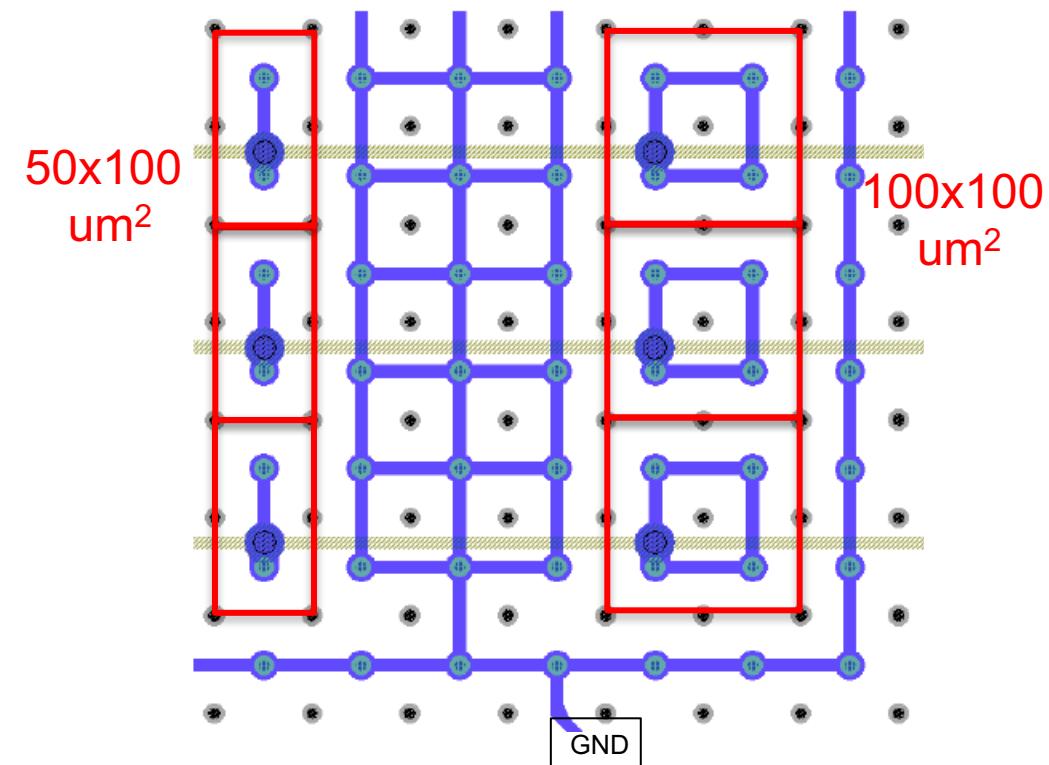
- Simplified simulation domain (2d slice), no pixel edge effects
- Bulk damage: new Perugia radiation damage model
- Very high average signal efficiency
- Significant variations of signal efficiency with hit position
- Possible impact ionization effects at high field

New pixels with existing ROCs ?

ATLAS FE-I4 50x50 (1E) + grid



CMS PSI46: 50x50 (2E+4E) + grid

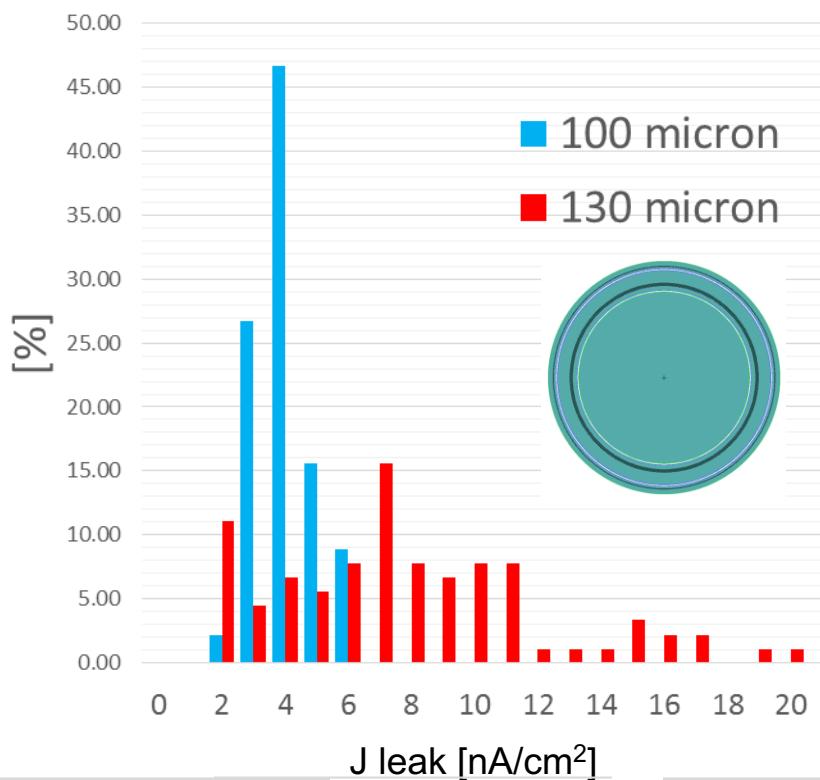


- Small-pitch pixels take all bonding pads
- + rest of pixels at GND using a **metal grid** and **extra-pads** at the periphery
- Small “RD53” prototypes (FE65-p2, CHIPIX65)

SiSi DWB substrate qualification

Planar sensor test batch, 2014

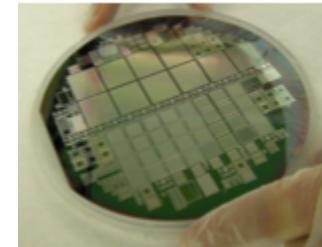
Circular diode, 4 mm², two GRs



J_{leak} distribution on 135 diodes

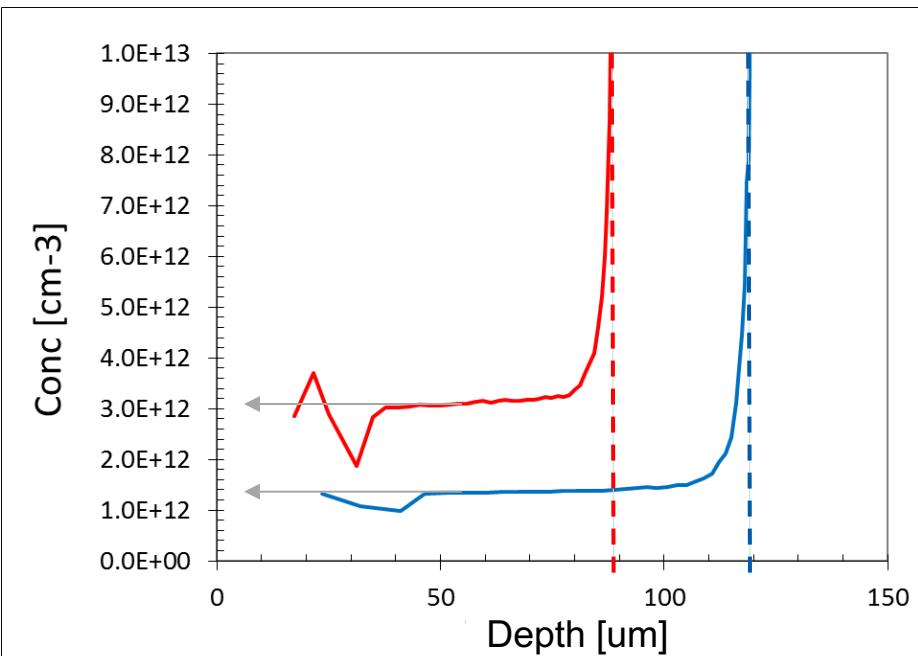
→ Different material quality ?

G.-F. Dalla Betta,
NIMA 824 (2016) 388

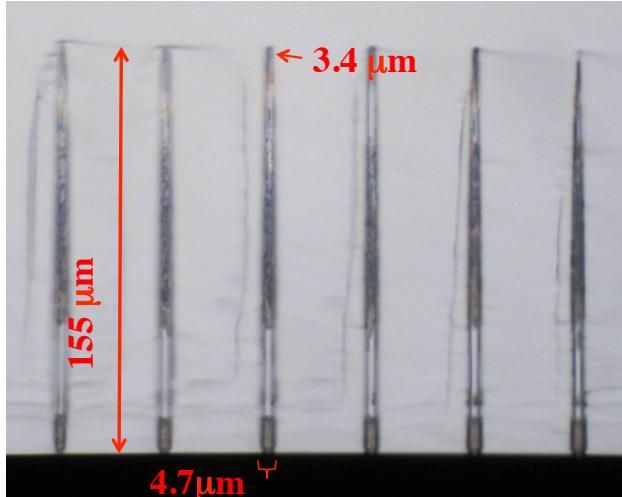


Doping concentration profiles:

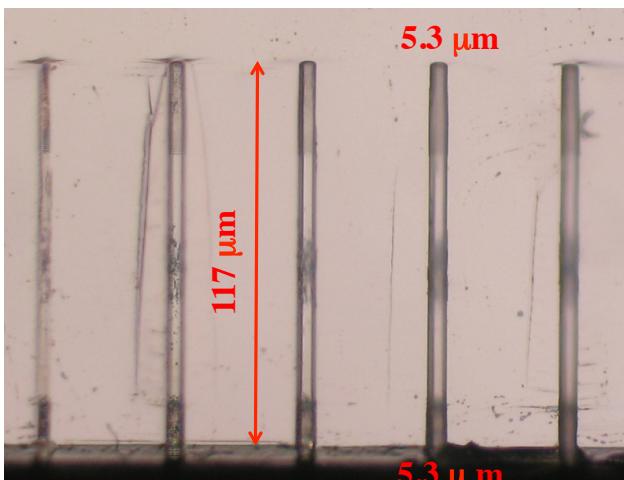
- Active layer doping $1 - 3 \times 10^{12} \text{ cm}^{-3}$
- Thicknesses about 10 μm lower than the nominal values, due to Boron diffusion from support wafer



Etching narrow columns by DRIE

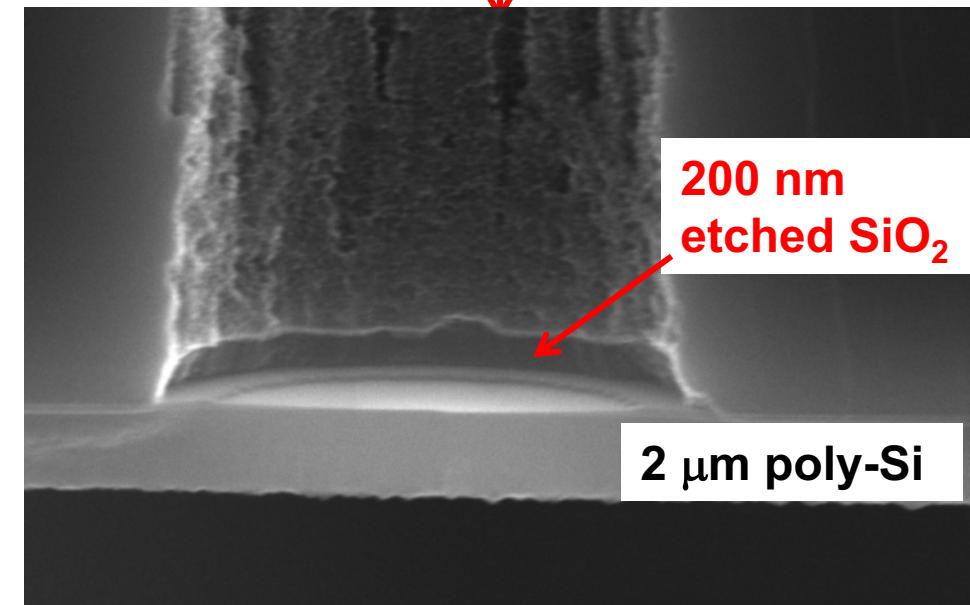
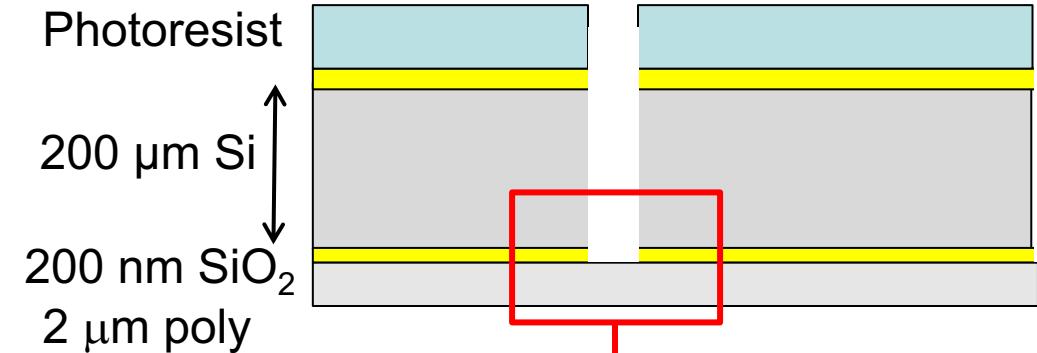


Ohmic columns optimized for depth

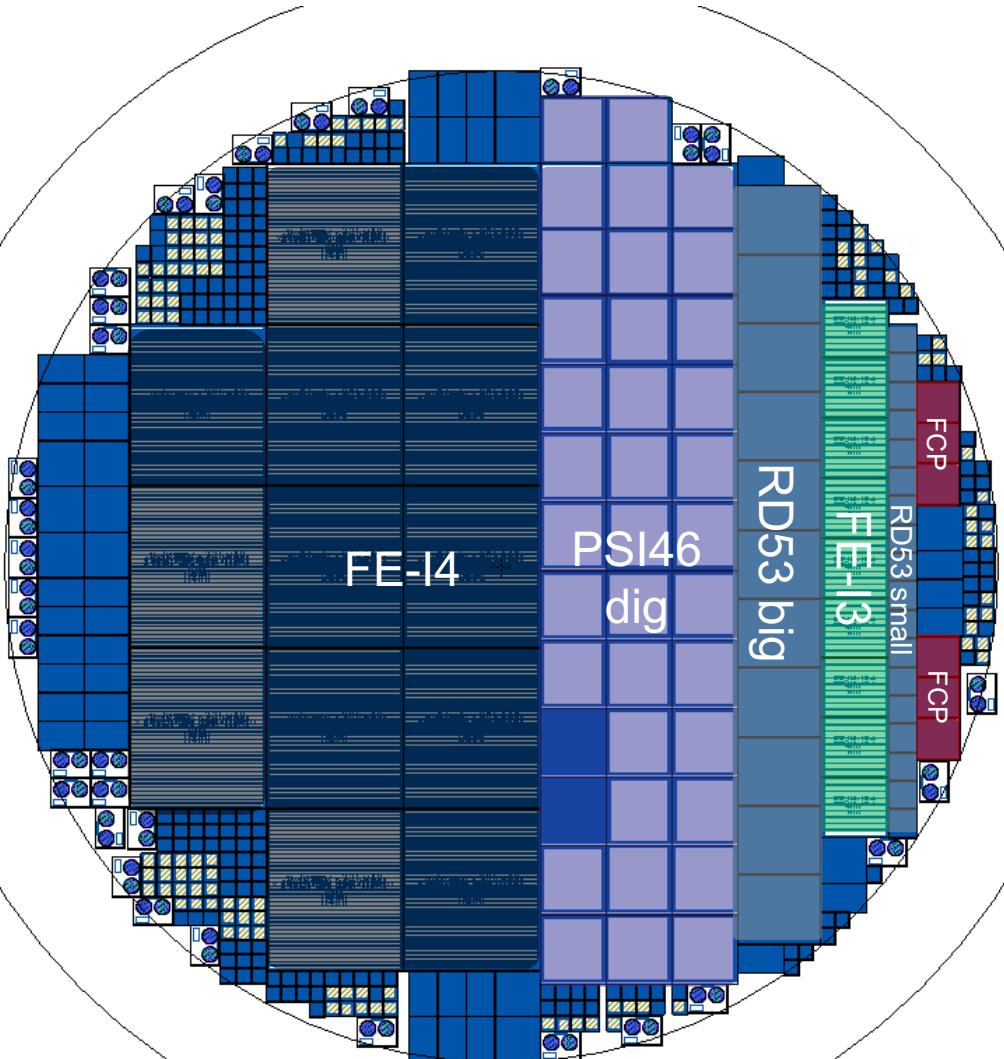


Junction columns optimized for uniformity

Testing different etching depth and etching through oxide layer for SOI approach



1st SS-3D Pixel Wafer Layout



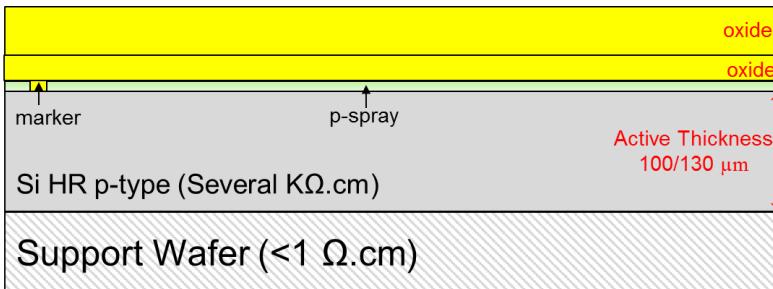
Many different pixel geometries and pitch variations:

- **FE-I4**
 - 50 x 250 (2E) std
 - 50 x 50 (1E)
 - 25 x 100 (1E and 2E)
 - 25 x 500 (1E)
- **FE-I3**
 - 50 x 50 (1E)
 - 25 x 100 (1E and 2E)
- **PSI46dig**
 - 100 x 150 (2E and 3E) std
 - 50 x 50 (1E and 2E)
 - 50 x 100, 100 x 100 (2E + 4E)
 - 50 x 100, 100 X 150 (2E + 6E)
 - 25 x 100 (1E and 2E)
- **FCP**
 - 30 x 100 (1E)
- **RD53/CHIPIX65**
 - 50 x 50 (1E)
 - 25 x 100 (1E)
 - 25 x 100 (2E)

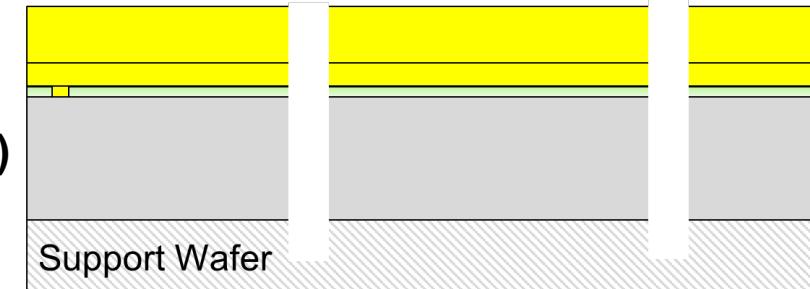
+ Test structures (strip, diodes, etc)

Fabrication process (1)

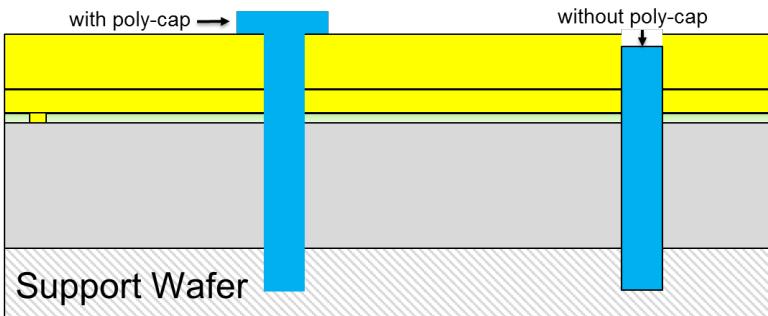
(a)



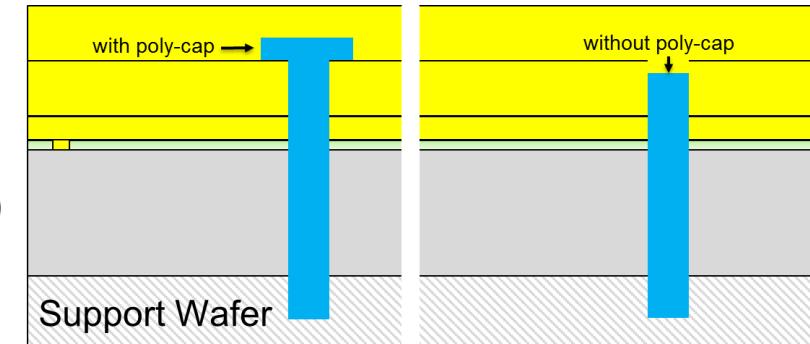
(b)



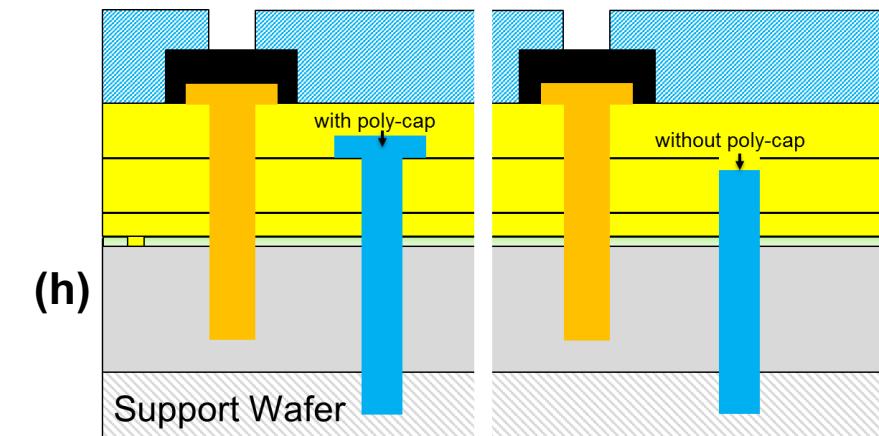
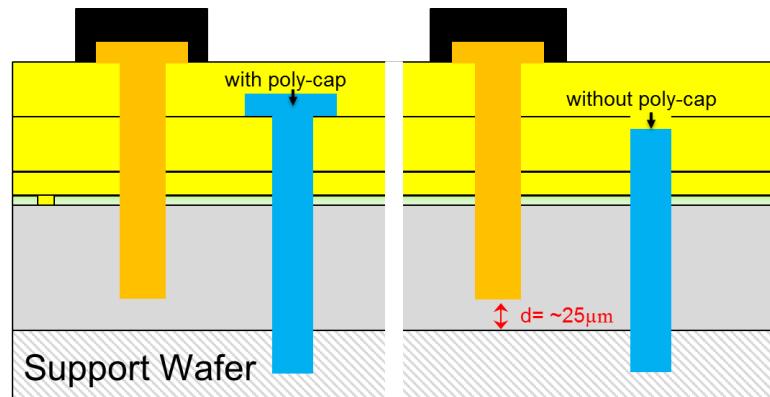
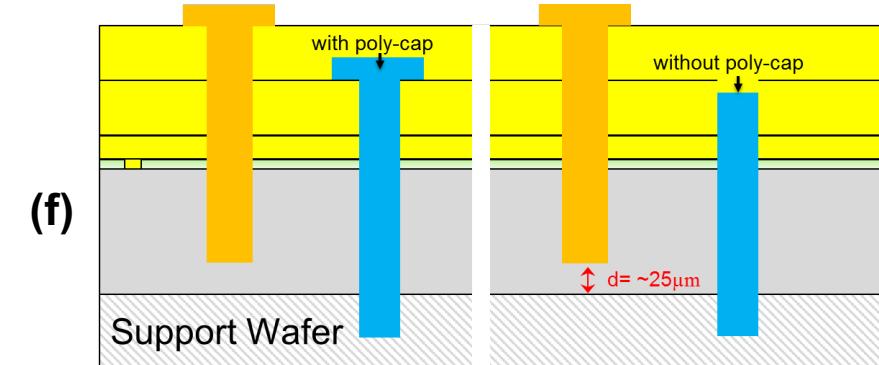
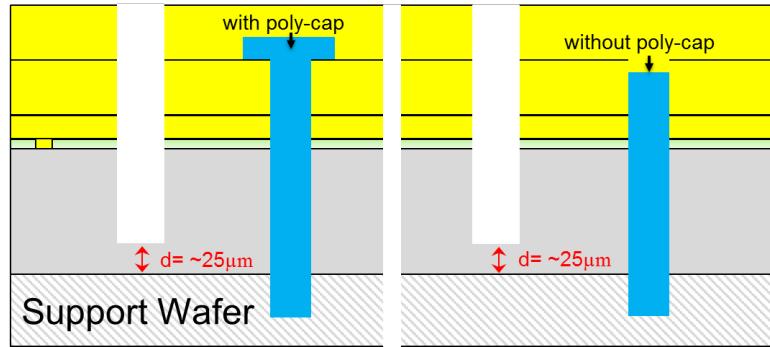
(c)



(d)

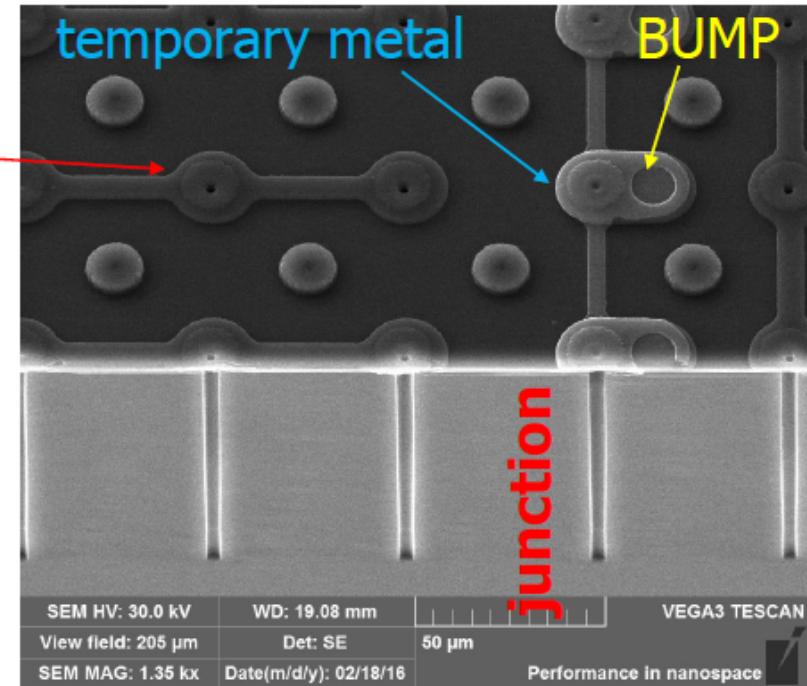
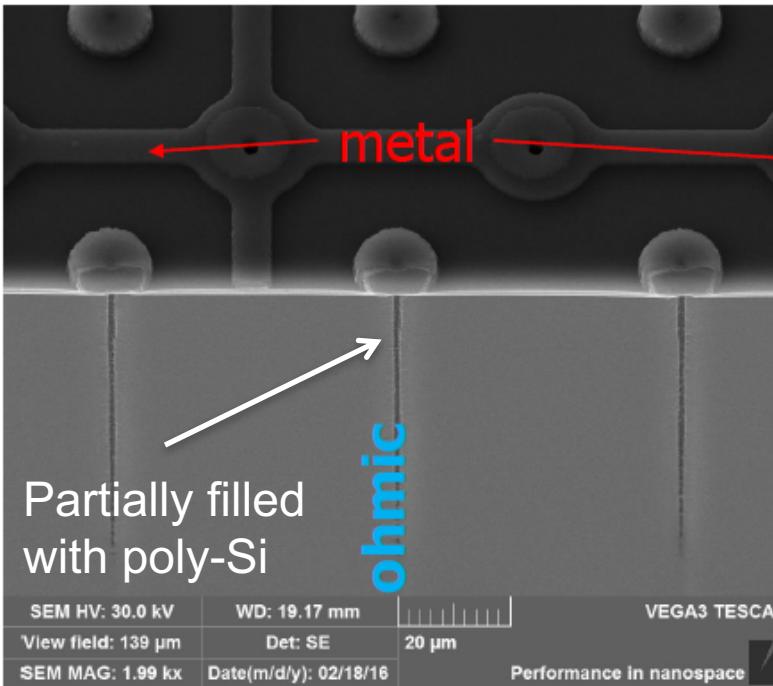
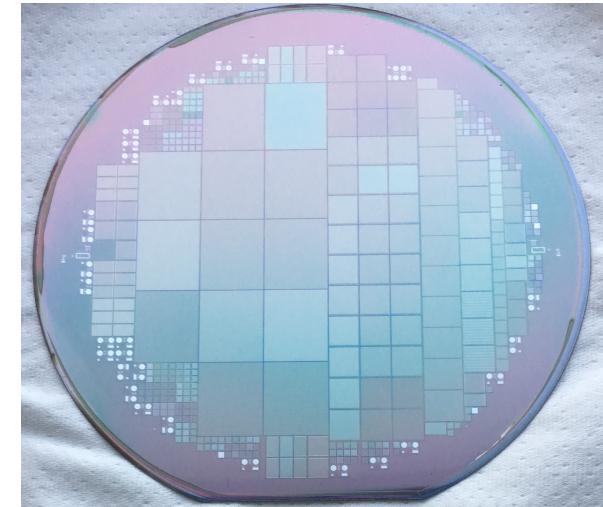


Fabrication process (2)



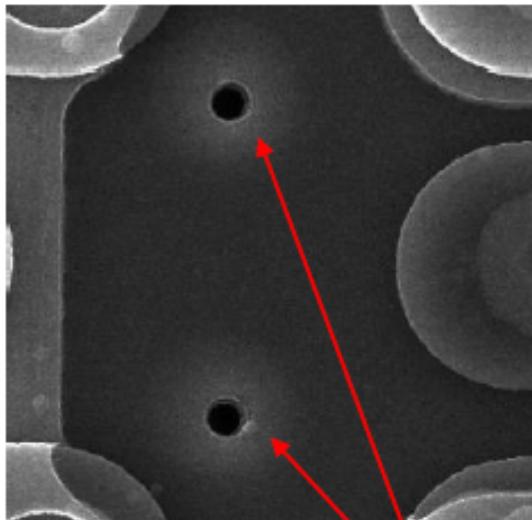
1st batch fabrication

- Ten wafers processed
- Two different active thicknesses: 100 vs 130 μm
- Two process splits:
 - sintering temperature (350 vs 420° C)
 - p-Poly-Si etching (with and w/o mask)

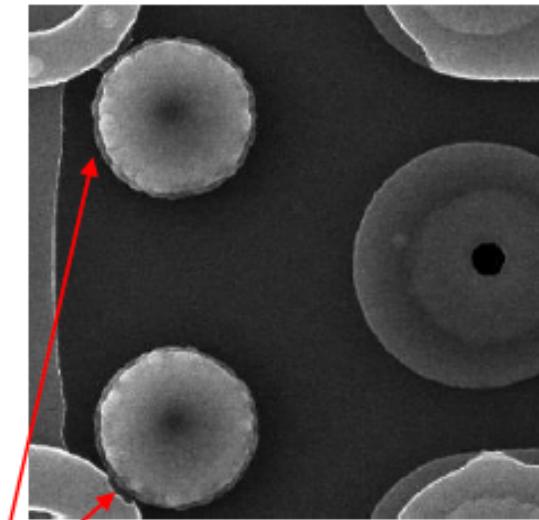


p-Poly-Si etching split

without poly cap



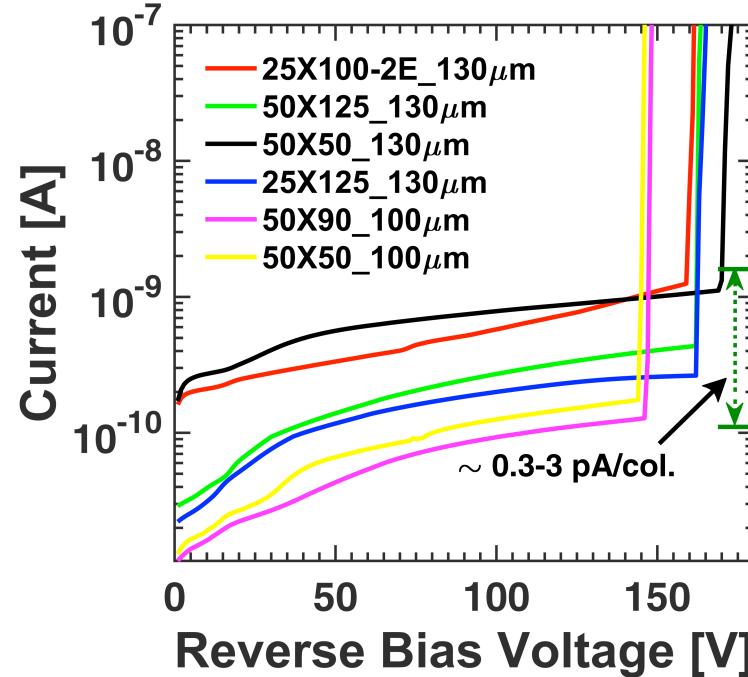
with poly cap



Ohmic columns



Test results: 3D diodes



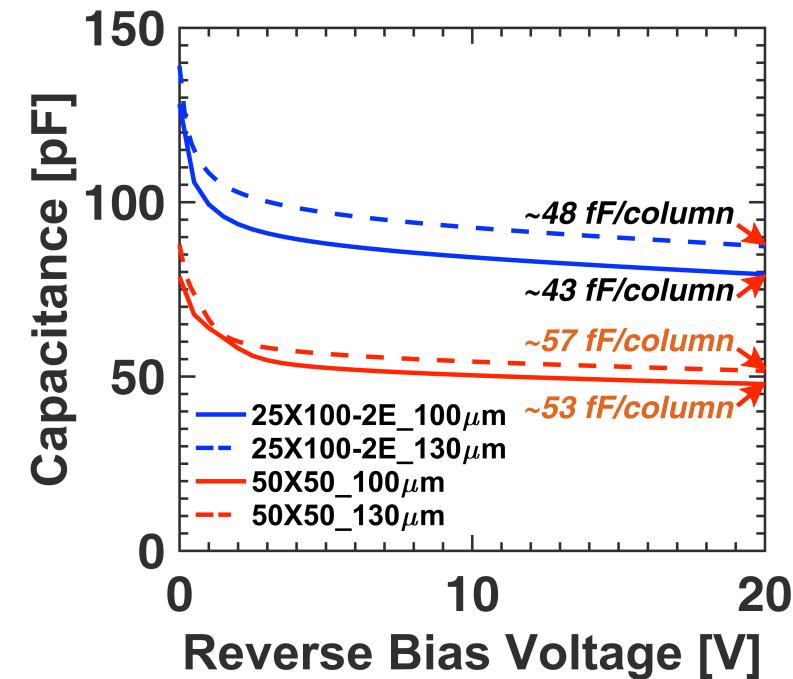
3D diodes also used for irradiation tests:

- Gamma rays (Sandia)
- Neutrons (JSI and Sandia)
- Protons (LANSCE)

They are being tested in collaboration with Univ. New Mexico

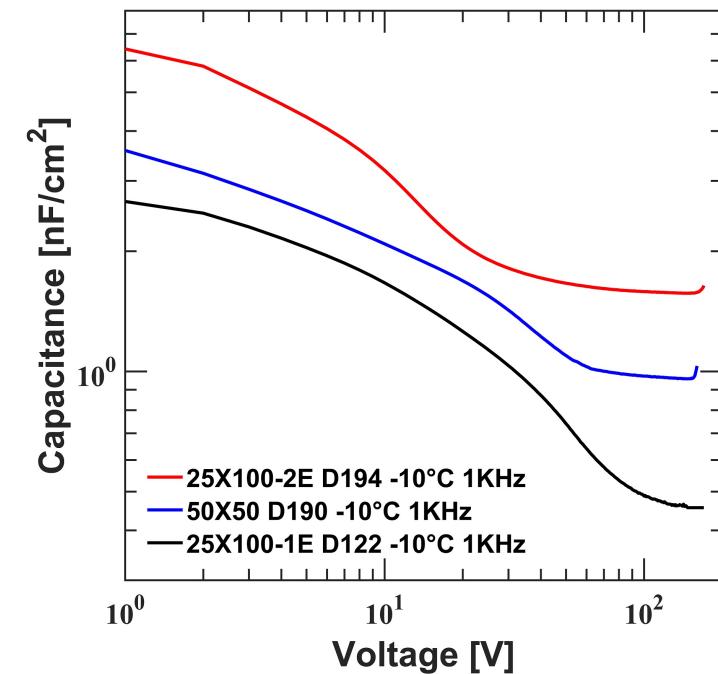
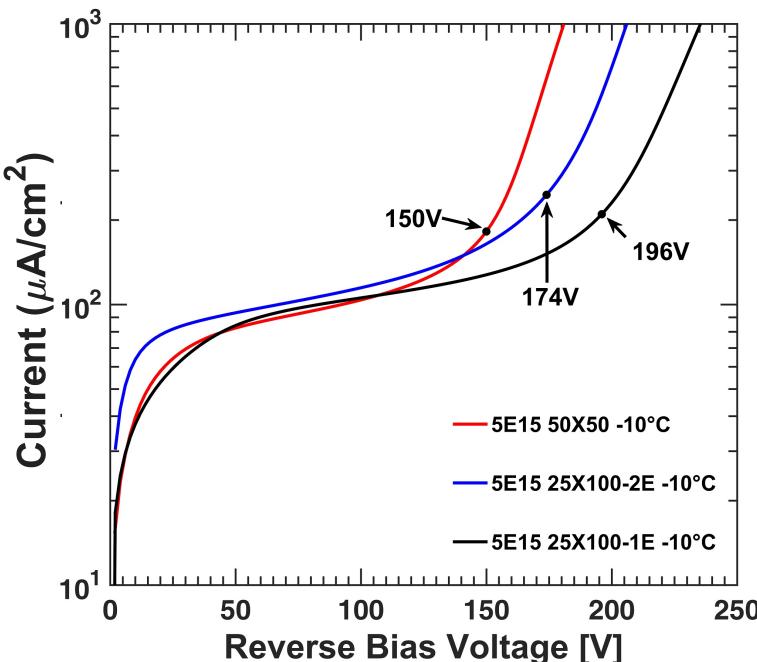
Good electrical figures:

- low depletion voltage
- capacitance as expected
- low leakage current
- high breakdown voltage
- good agreement with simulations

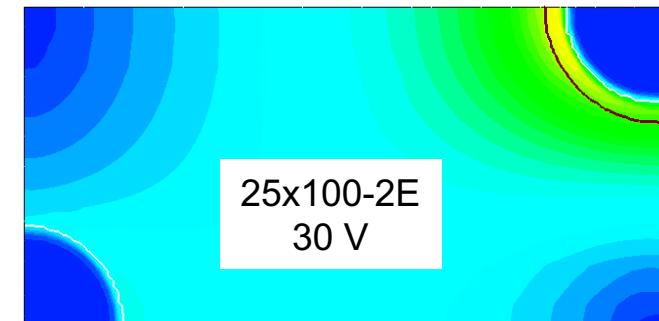


3D diode neutron irradiation

Neutron irradiation at $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ (JSI Lubiana, thanks to V. Cindro)



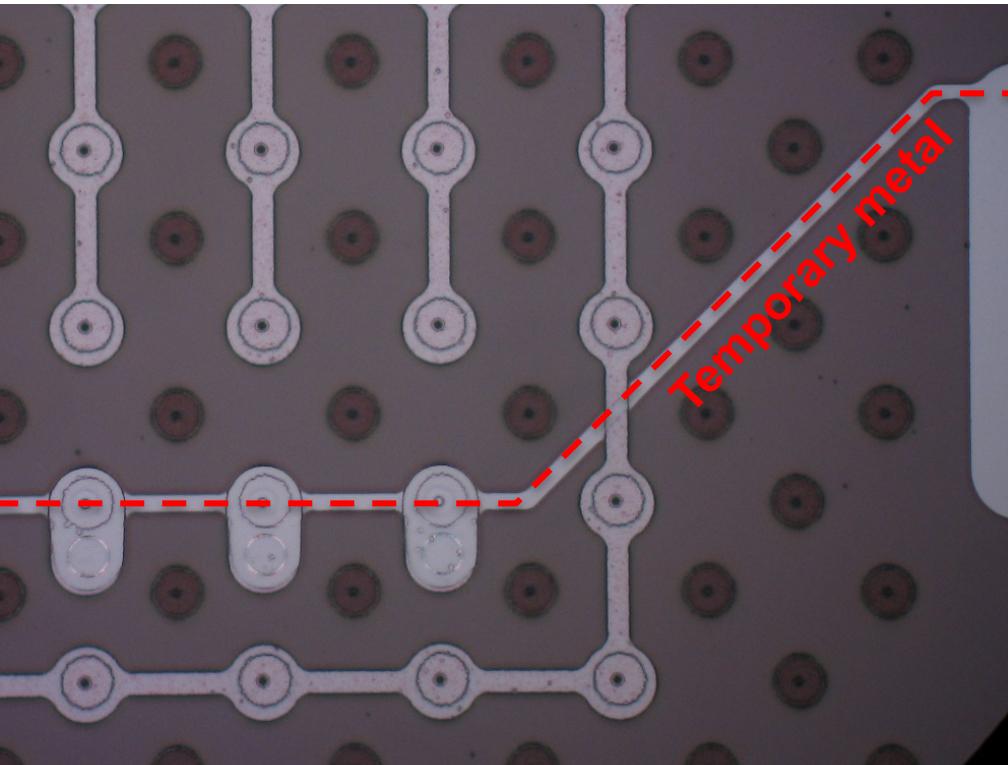
- Leakage current increases as expected:
 - Damage constant $\alpha \sim 4 \times 10^{-17} \text{ A/cm}$
- Breakdown voltage also increases and is large enough wrt depletion voltage



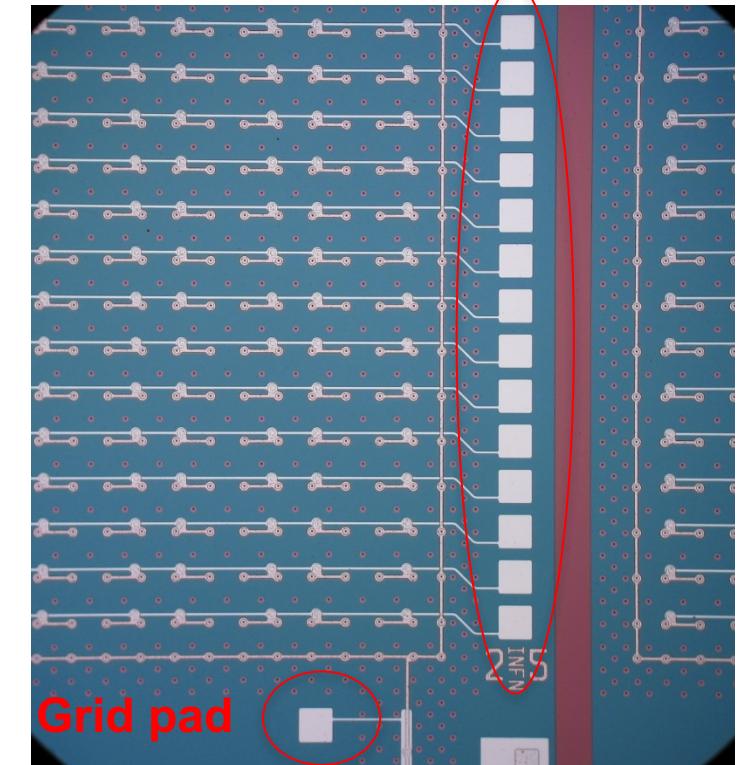
Temporary metal tests on pixels

- Rows of pixels are shorted by temporary metal for electrical tests on wafer (more effective monitoring of process defects)
- Total currents are obtained by the sum of all single-row and grid currents

Permanent metal

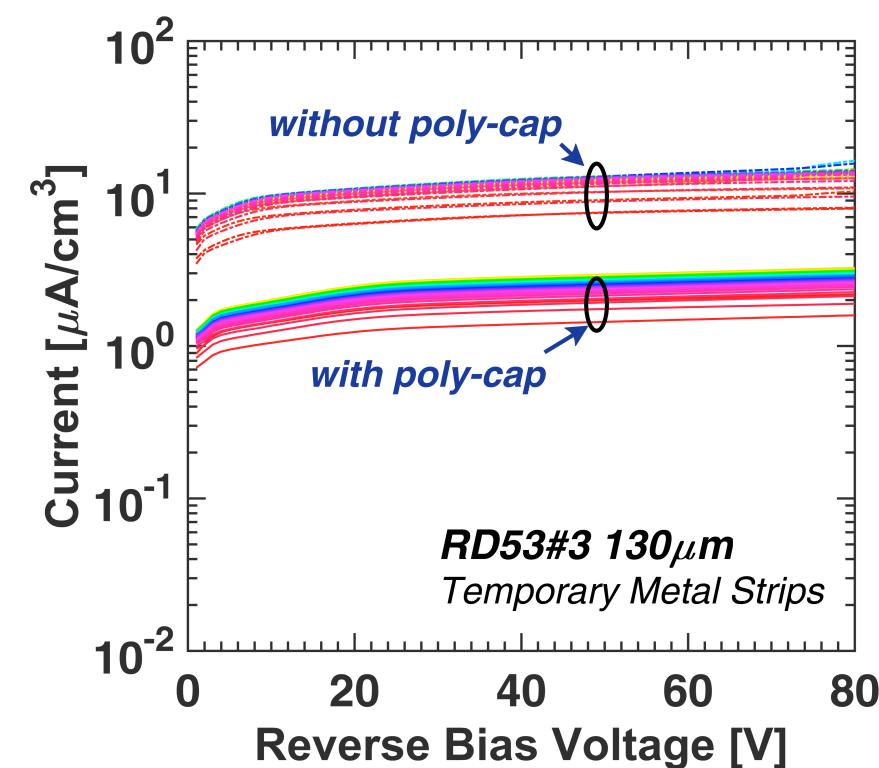
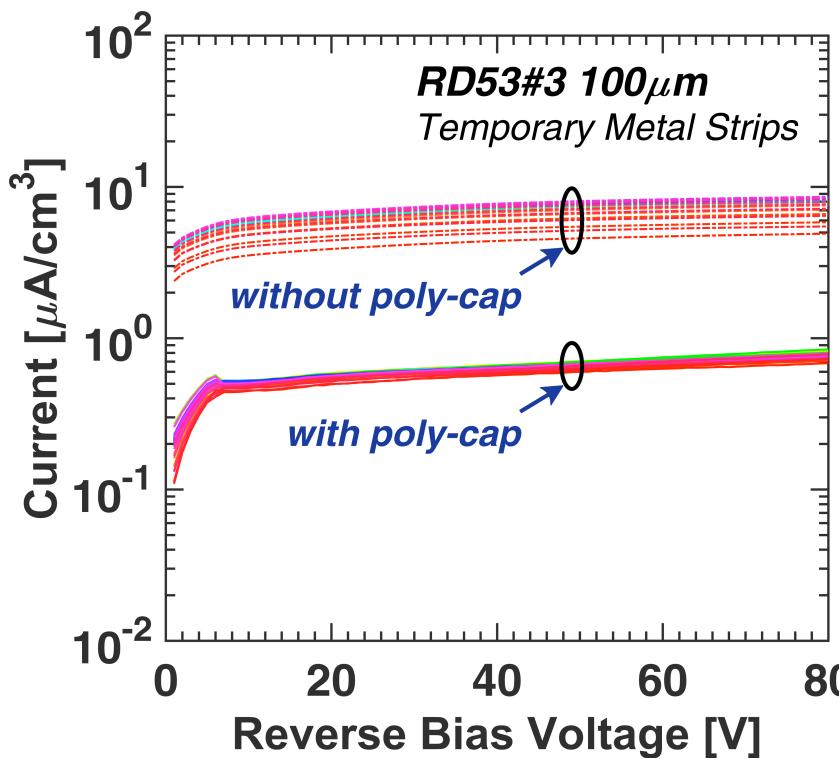


Temporary metal pads



Impact of p-poly-cap on leakage current

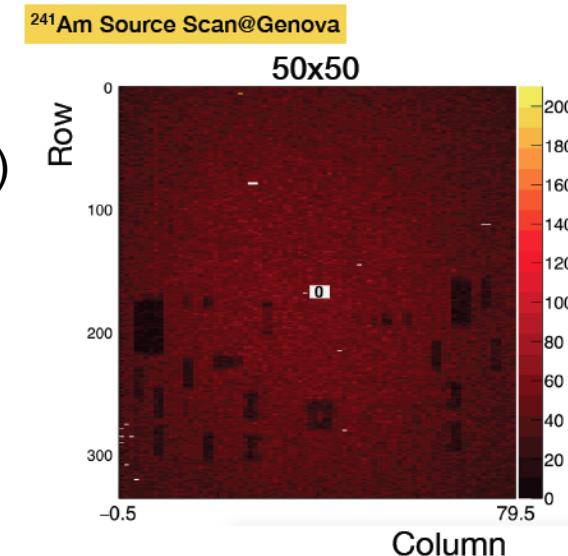
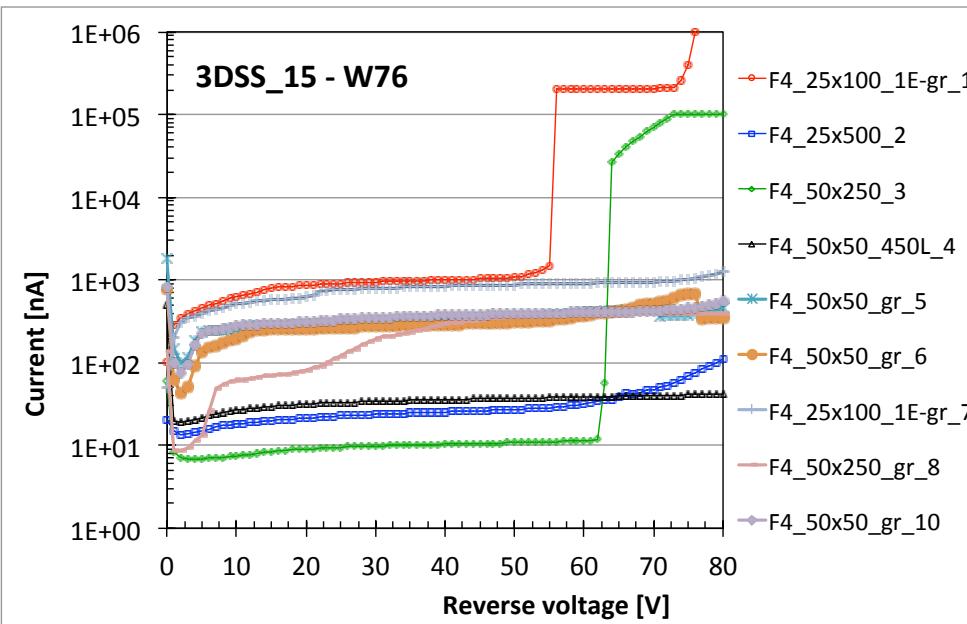
- From temporary metal “RD53” measurements (raws of pixels)
- Leakage currents are all low (~ 1 pA per column),
- But a significant difference can be observed w and w/o poly-cap (probably due to residual damage at column opening)



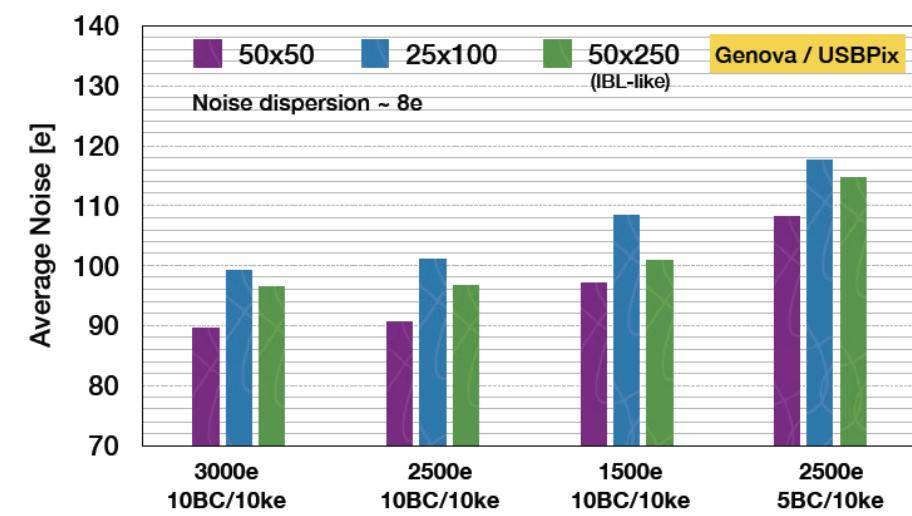
First 3D pixel assemblies

- Wafers ranked according to overall yield from I-V curves (sorting by leakage current, breakdown voltage and slope)
- Two wafers (76, 78) sent to Leonardo (former Selex) for bump bonding (other wafers to be sent to IZM)
- Sensors from W76 assembled and tested in 2016
- Sensors from W78 assembled and being tested in 2017

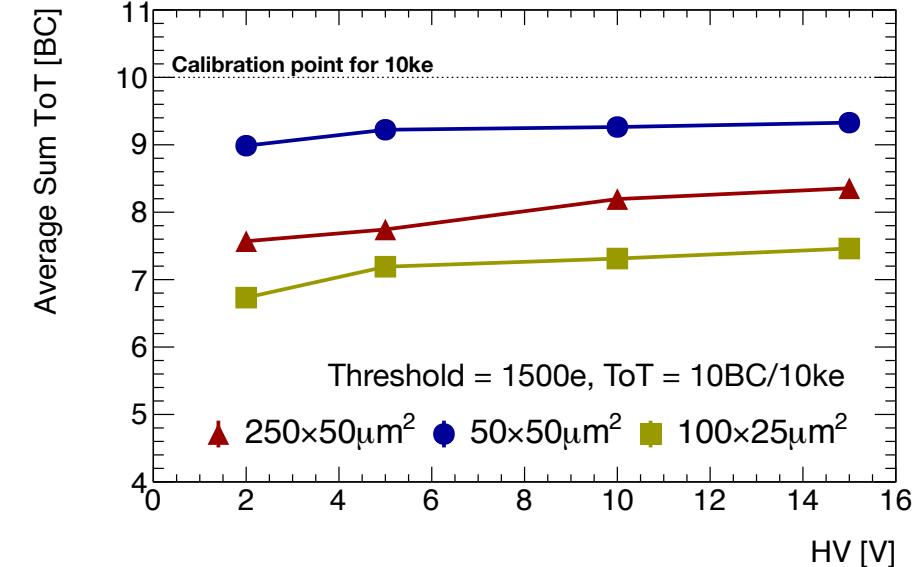
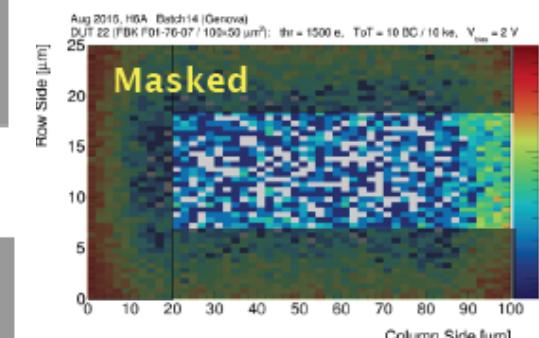
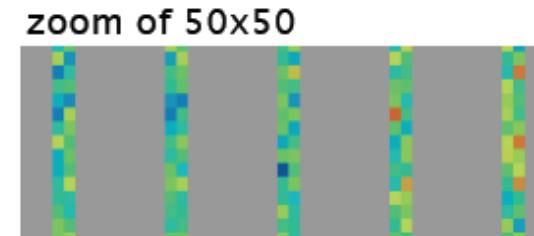
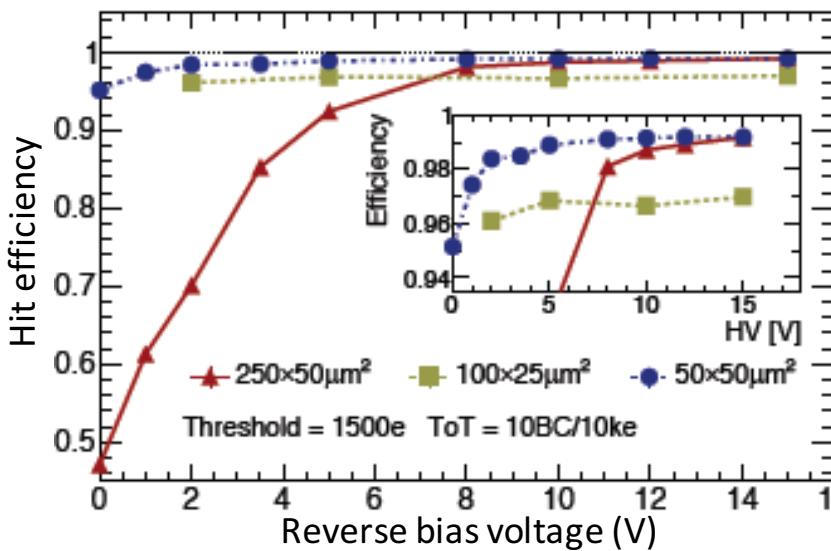
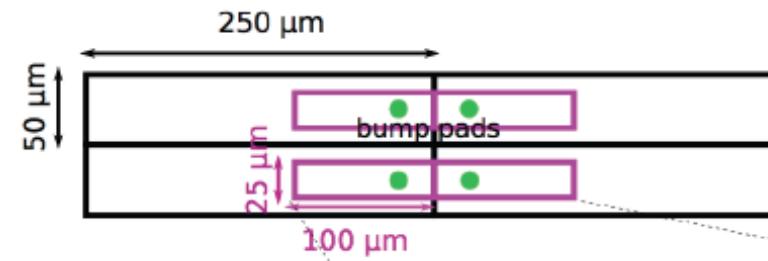
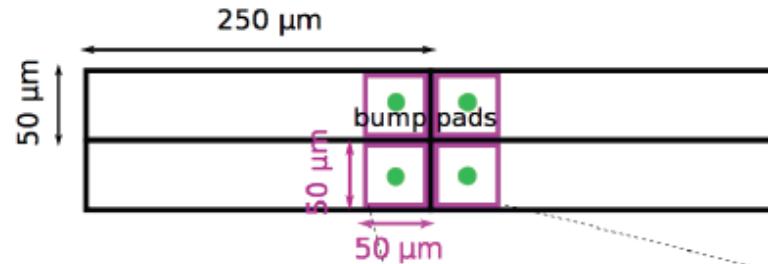
Total I-V curves of 9 FEI4 sensors in W76



Module tuning with USBPix

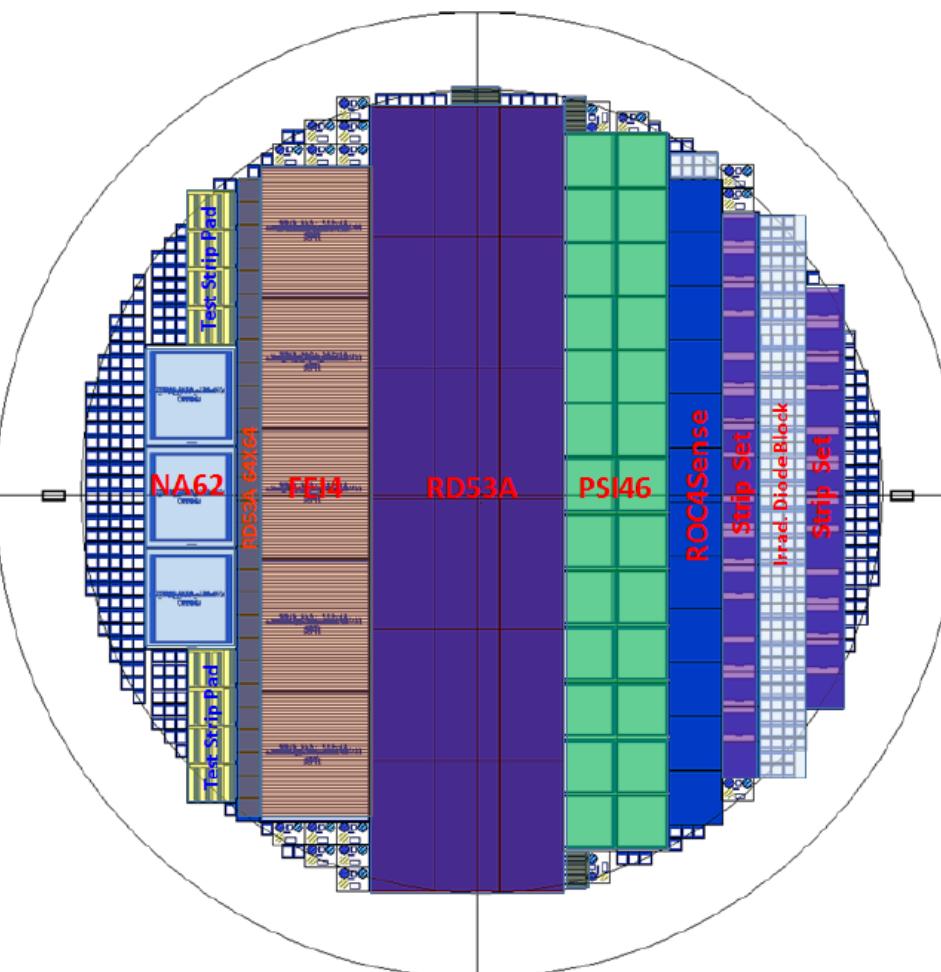


Test beam at CERN, Aug. 2016



2nd SS-3D Pixel Wafer Layout

- Batch funded by AIDA2020 and INFN
- Fabrication on going, to be completed by July



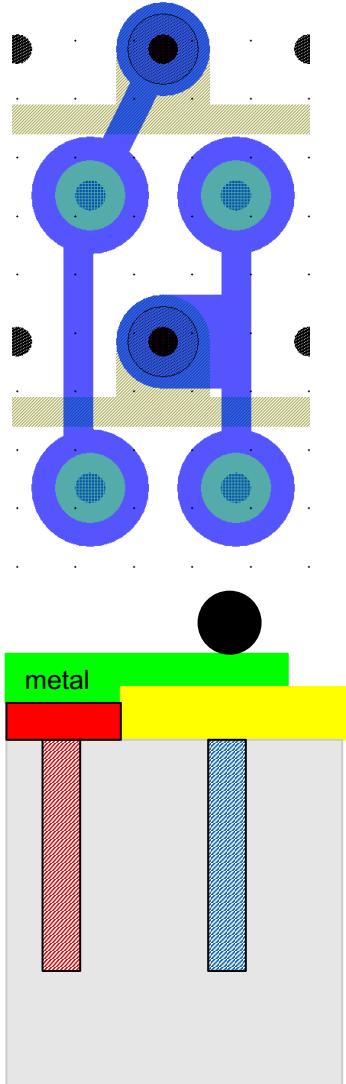
DMS Sultan, UniTN

- **FE-I4**
 - 50 x 250 (2E) std
 - 50 x 100 (1E+9E)
 - 50 x 50 (5E)
- **PSI46dig** (also with BOC option)
 - 100 x 150 (2E and 3E) std
 - 50 x 50 (1E)
 - 25 x 100 (1E and 2E)
- **R4S**
 - 50 x 50 (1E)
 - 25 x 100 (1E and 2E)
- **RD53A** (also with BOC option)
 - 50 x 50 (1E)
 - 25 x 100 (1E and 2E)
- **CHIPIX65**
 - 50 x 50 (1E and 2E)
 - 25 x 100 (1E and 2E)
- **NA62**
 - For timing studies

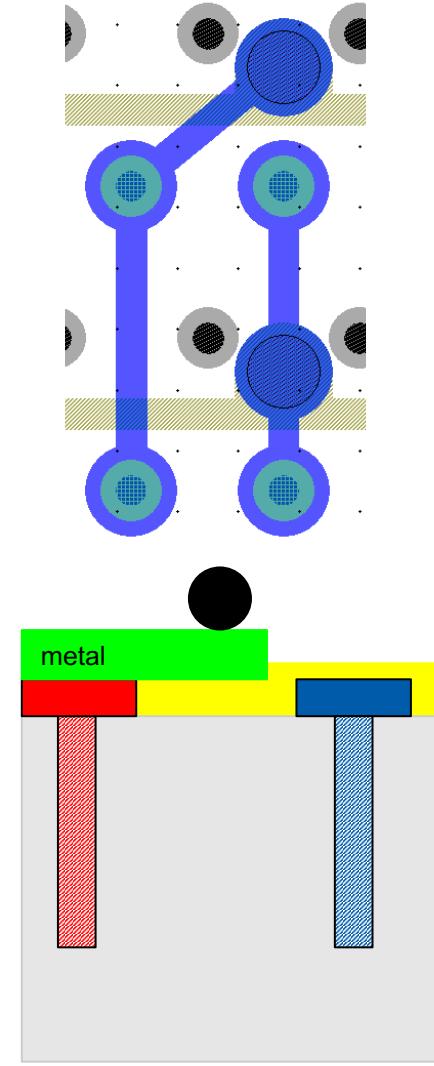
+ Test structures (strip, diodes, etc)

RD53A Pixel Sensors (25x100-2E)

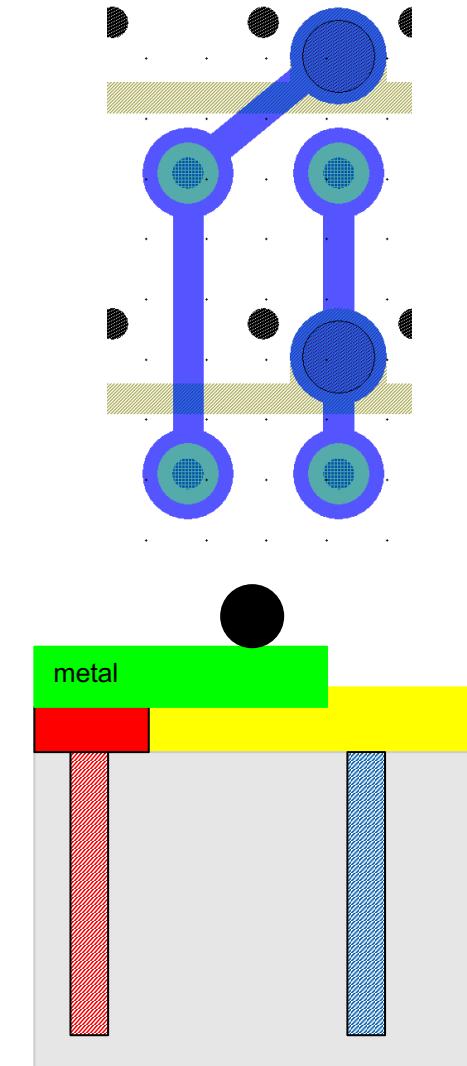
Bump over column



Bump over pad & poly cap



Bump over pad & without poly cap



Conclusions

- 3D sensor technology has made impressive progress in the past few years
- Learning from the ATLAS IBL experience, a new generation of 3D pixel sensors is being developed for HL-LHC upgrades
- In spite of the significant dimensional scaling (2x), fabrication of small-pitch 3D sensors is feasible
- Initial results from sensors of the first batch are encouraging:
 - Good electrical characteristics (close to TCAD simulations)
 - High hit reconstruction efficiency at low voltage before irradiation
 - Wide bias voltage operational margin after irradiation
- Functional tests on irradiated pixel assemblies are under way
- A second batch (mainly oriented to the RD53 chip) has been designed and is now in fabrication at FBK, due by July 2017

Acknowledgements

- This work has been partially funded by:
 - the Italian National Institute for Nuclear Physics (INFN) through the Projects ATLAS, CMS and RD_FASE2 (CSN1);
 - the Autonomous Province of Trento through the Project MEMS3;
 - the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168 (AIDA-2020).
- Special thanks to all colleagues from the INFN-FBK "Phase 2" Collaboration
- Fruitful discussions with Cinzia Da Via (Manchester University), Sebastian Grinstein and Joern Lange (IFAE), Giulio Pellegrini (CNM), Marco Povoli and Ozhan Koybasi (SINTEF), Chris Kenney and Jasmine Hasi (SNF), are also acknowledged.

Thank You

Back-Up Slides

The INFN-FBK “Phase-2” R&D program

- Initially proposed in 2013 as INFN CSN5 Call project “ACTIVE” (ATLAS and CMS Towards InnovatiVe pixEls), but not approved
- Funded from 2014 by INFN CSN1 “RD_FASE2” and INFN-FBK-PAT “MEMS3” agreement

12 INFN GROUPS INVOLVED, ~20 FTE

ATLAS (BO, CS, GE, MI, TN, UD), **CMS** (BA, FI, MIB, PG, PI, TO)

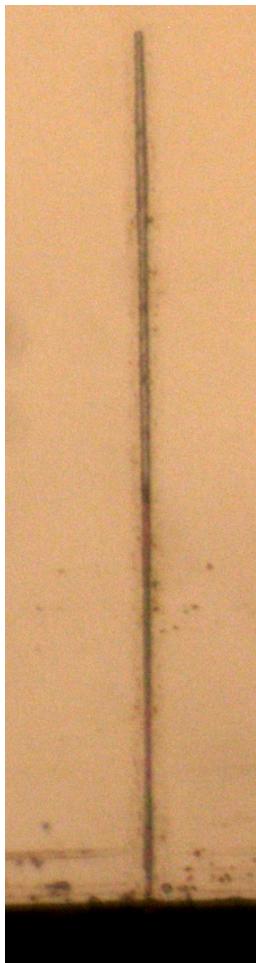
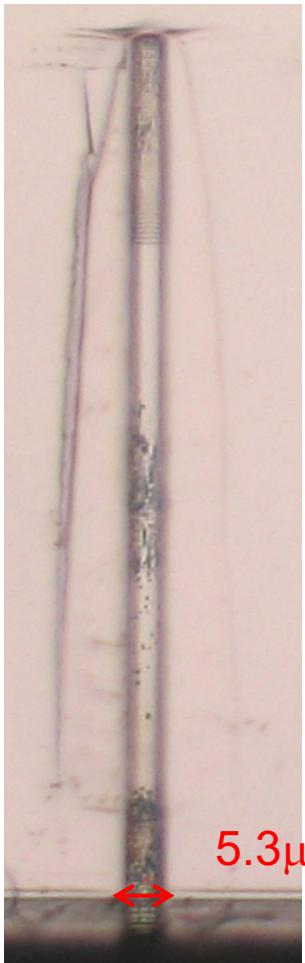
GOAL: development of new thin 3D and Planar Active Edge (PAE) pixel sensors on 6" p-type wafers at FBK:

- Technology and design to be optimized and qualified for extreme radiation hardness ($2 \times 10^{16} n_{eq} \text{ cm}^{-2}$)
- Pixel layouts compatible with present (for testing) and future (RD53 65nm) FE chips of ATLAS and CMS

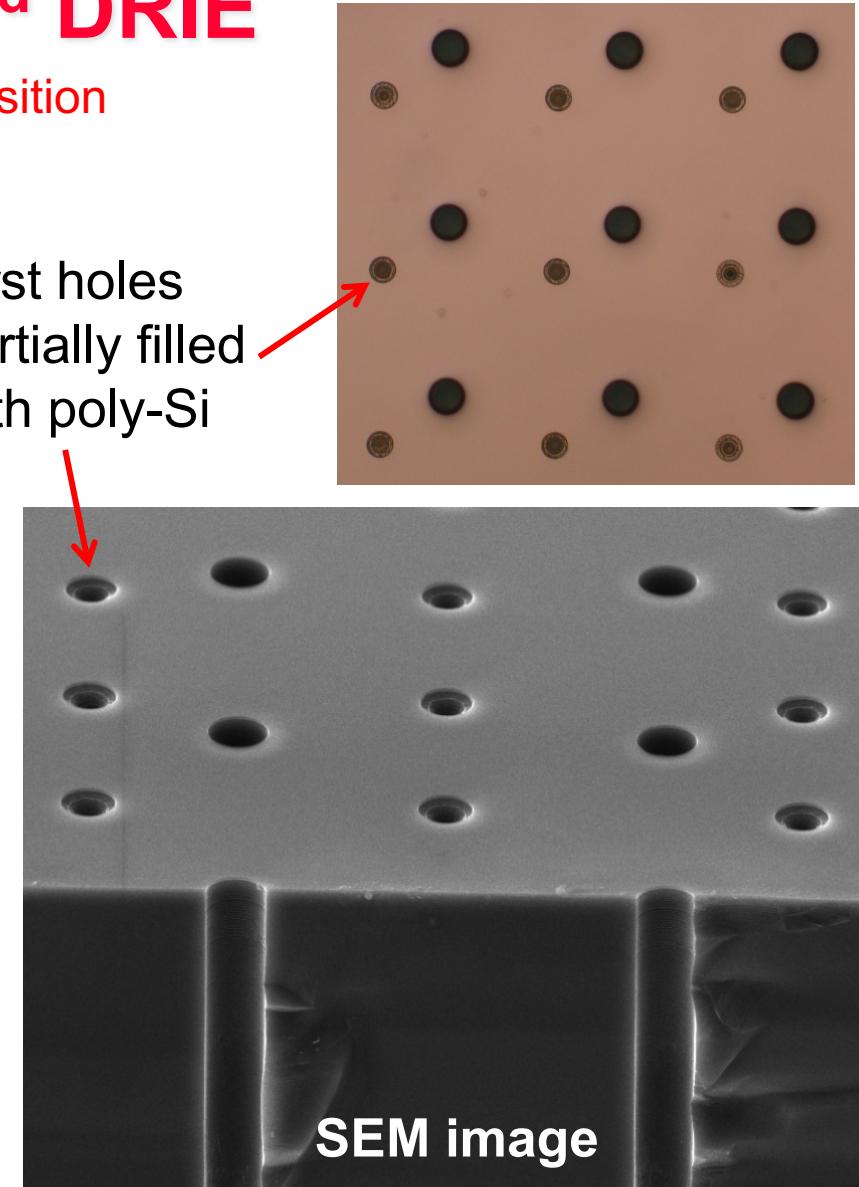
Strong sinergy with WP7 of AIDA2020

Poly-Si filling and 2nd DRIE

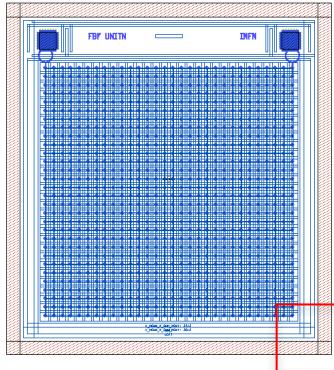
Reducing the hole diameter with poly-Si deposition
to ease the 2nd DRIE on the same wafer side



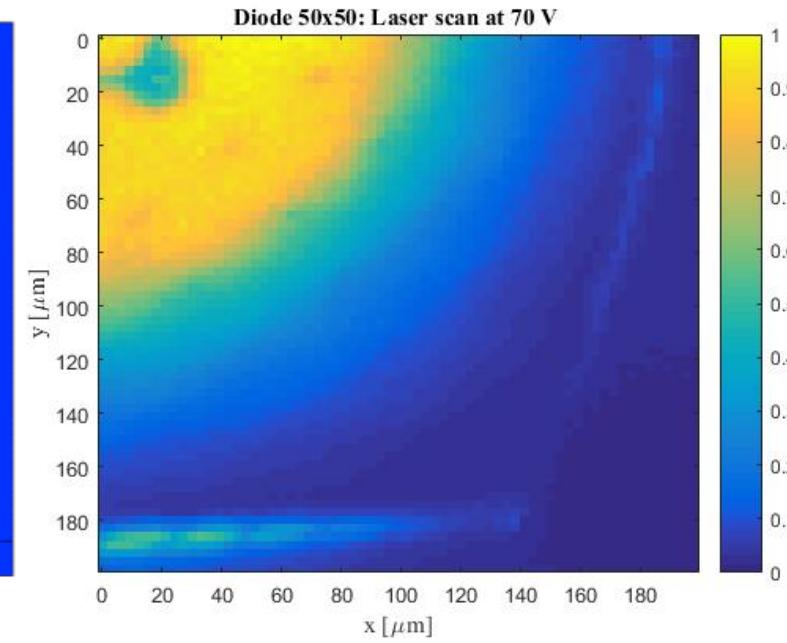
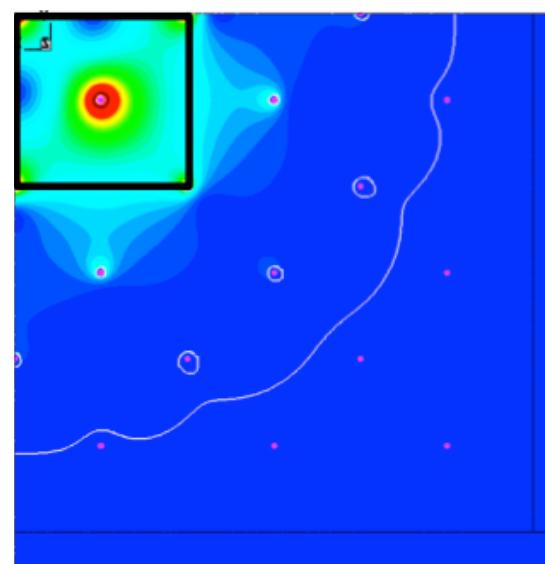
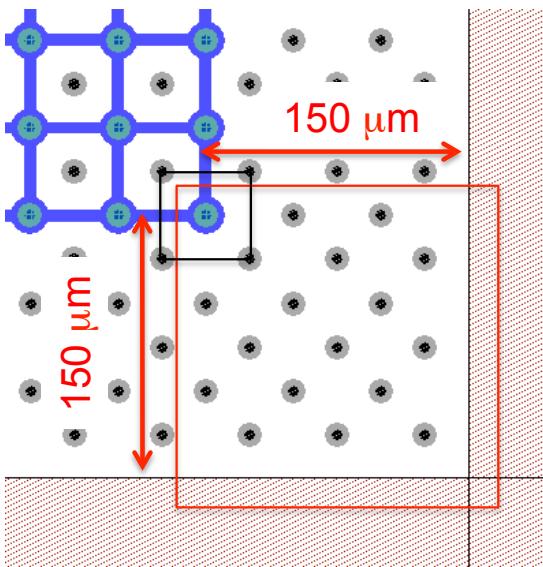
First holes
partially filled
with poly-Si



Slim edge laser test



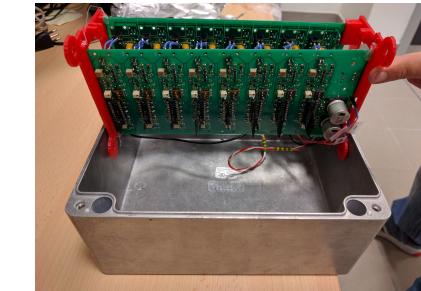
- Slim edge based on multiple ohmic columns developed for IBL (~200 μm) M. Povoli et al., JINST 7 (2012) C01015, here made slimmer (~100 μm) with reduced inter-electrode spacing
- Safe operation of 3D diode (50 μm x 50 μm design) tested with position resolved laser system
- High signal indicates extension of the depleted volume at the corner (~80 μm at 70 V), in good agreement with simulations



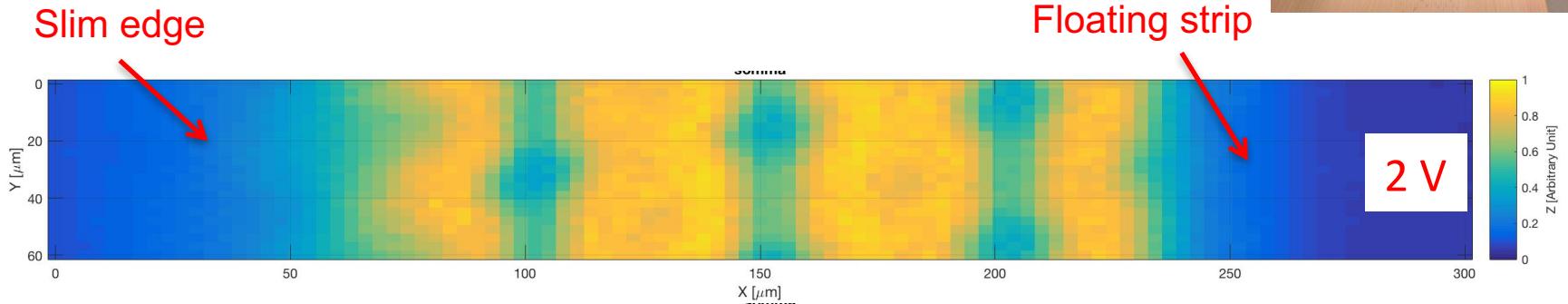
Preliminary results with 3D strips

R. Mendicino, TIFPA

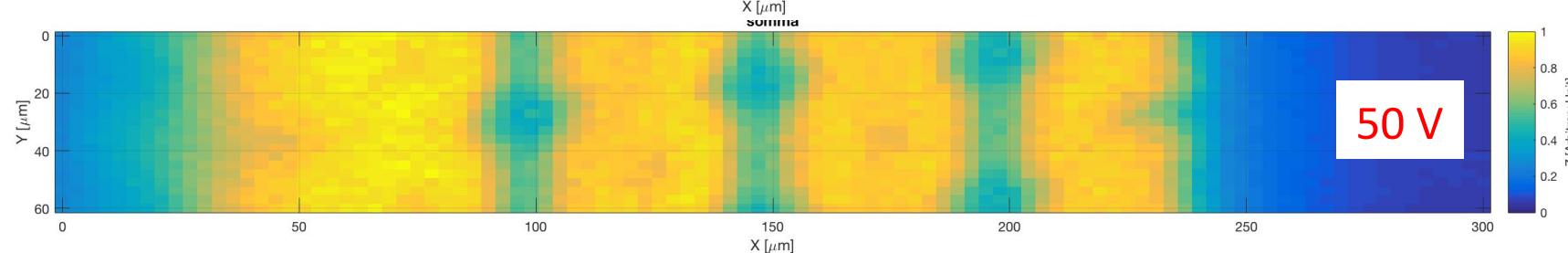
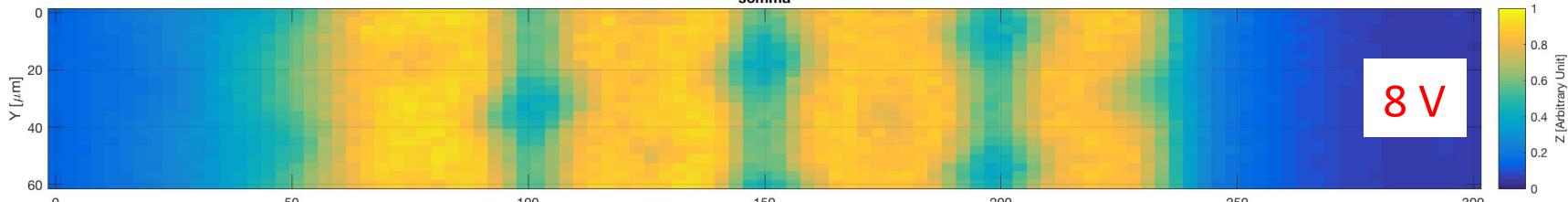
- Position sensitive laser setup ($\lambda=1064$ nm)
- House made (discrete) read-out electronics
- High efficiency already at low voltage



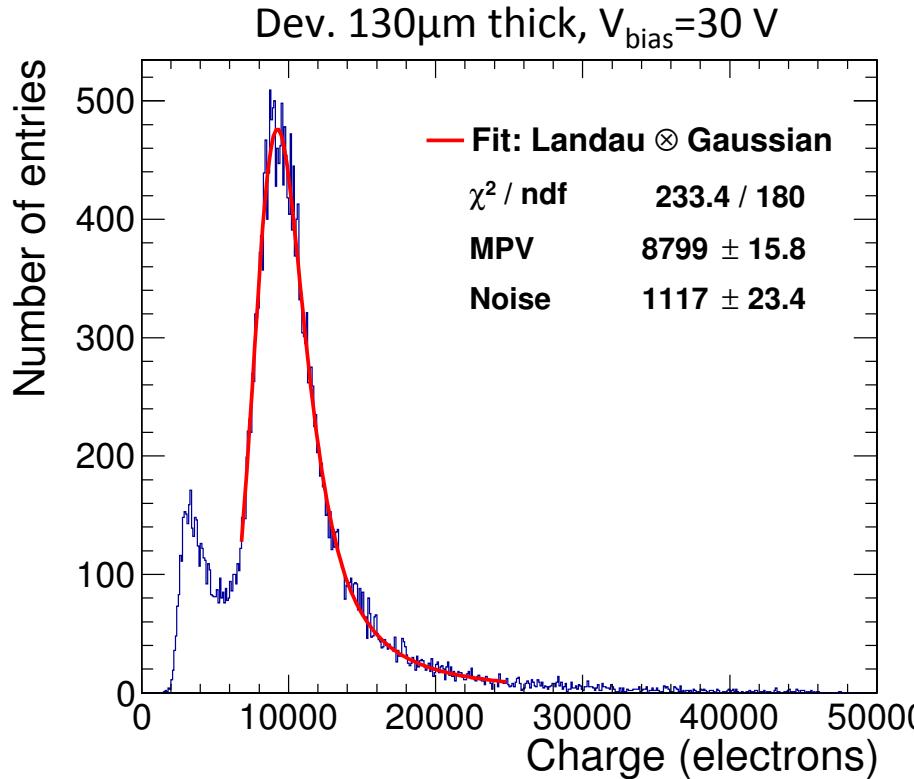
Slim edge



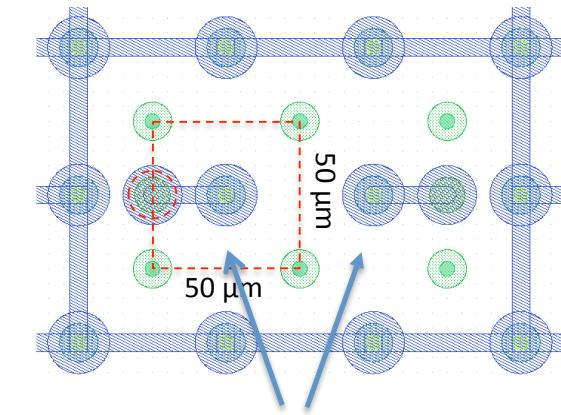
Floating strip



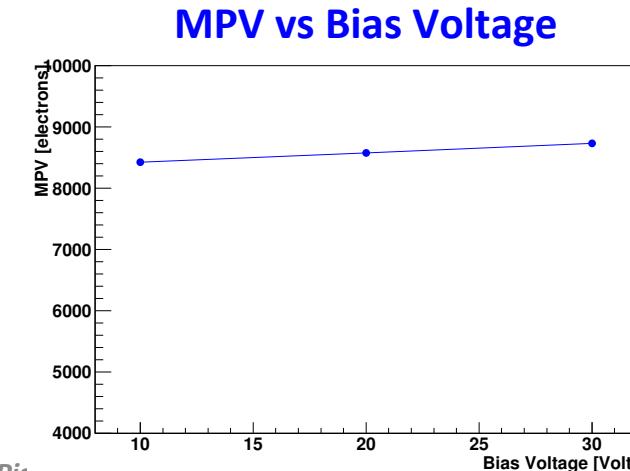
CMS test beam at Fermilab, Dec. 2016



Charge shared with not readout adjacent pixels. Effect over 3/4 cell sides

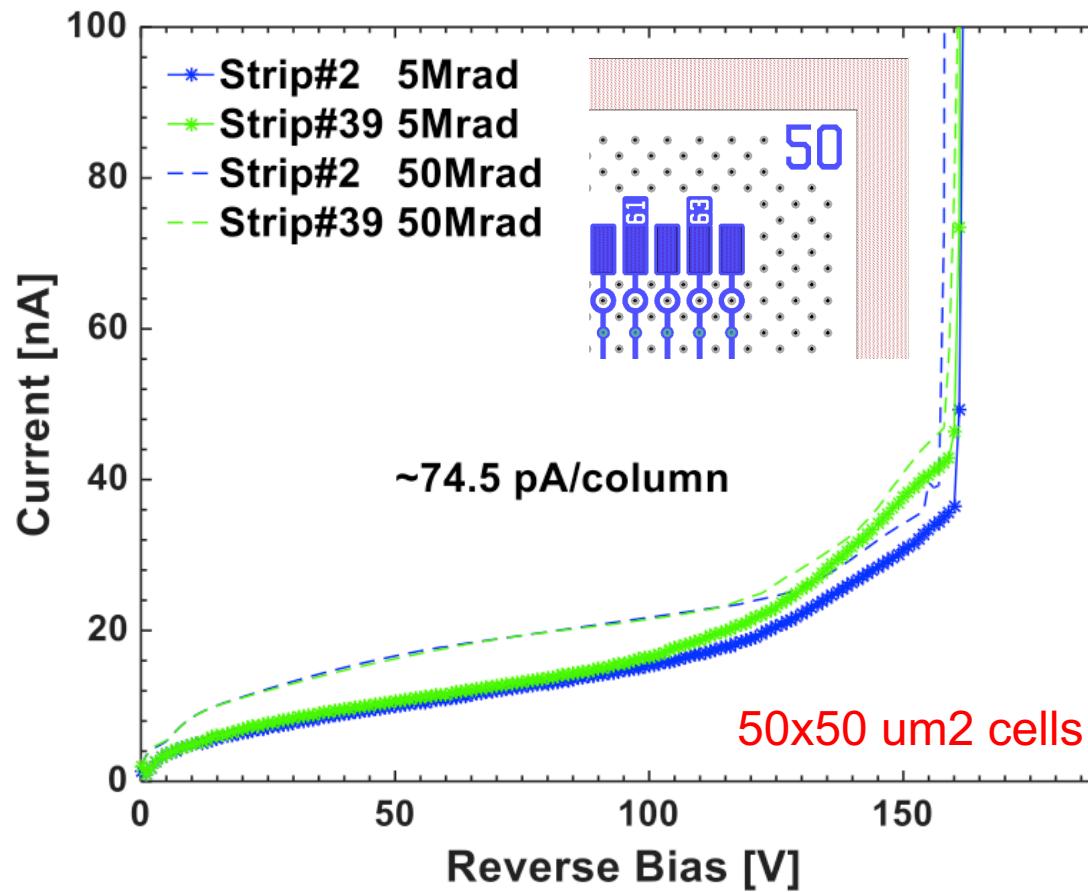


Two adjacent double columns pixel readout
 ROC (PSI46dig) fully connected
 Sensitive area readout: 1/6

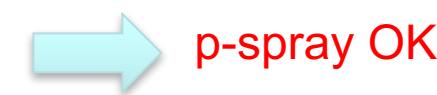


3D strip irradiations

- Eight 3D strip sensors (four pairs of different layouts) irradiated at RAL with X-rays (thanks to John Matheson) to two doses: 5 and 50 Mrad(Si)
- Minor effects of X-ray dose on breakdown voltage: breakdown on column tips ?



- Interstrip resistance measured to check surface isolation:
~several G Ω even after the highest dose.

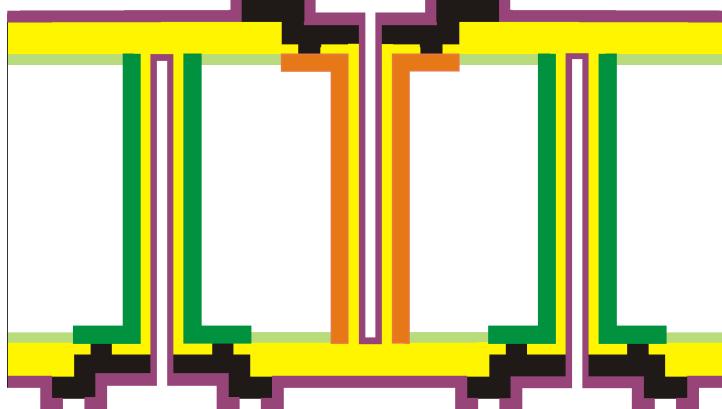


- Other 3D strip sensors irradiated with protons at CERN and neutrons at JSI Lubiana up to $2 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
They will be tested in collaboration with Univ. Freiburg with ALIBAVA

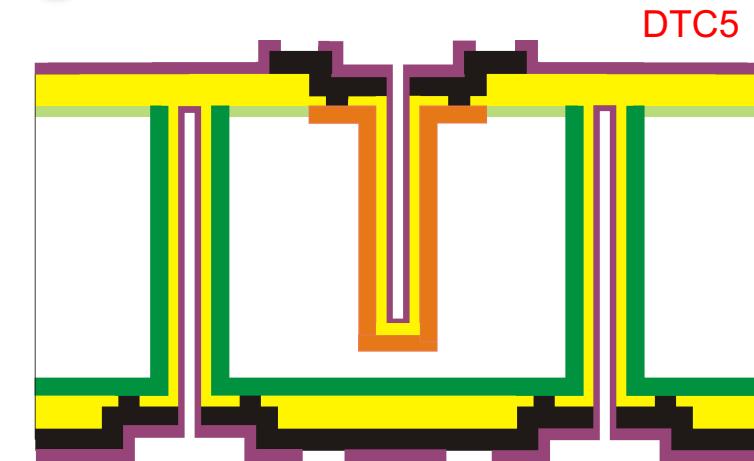
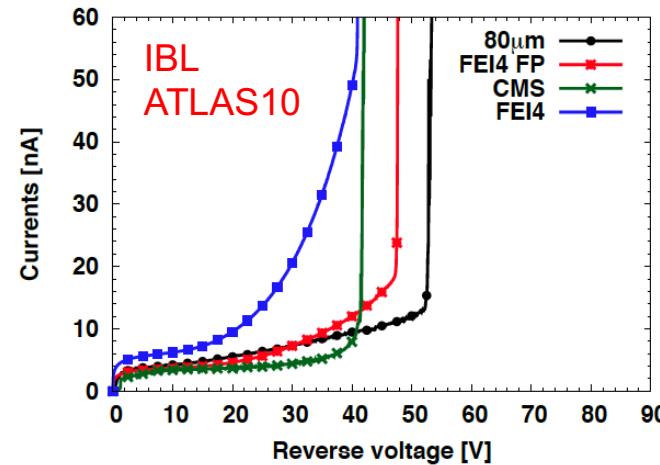
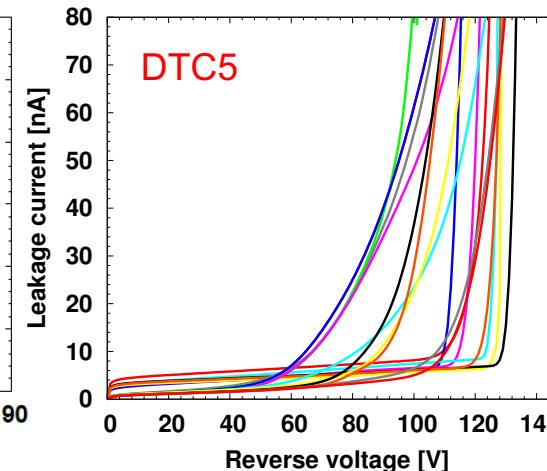
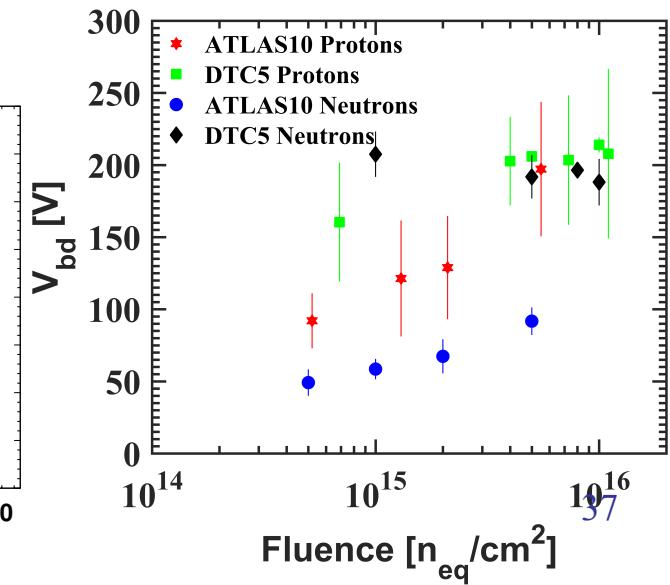
G.-F. Dalla Betta

Paris, June 14, 2017

Breakdown voltage control

 IBL
 ATLAS10


- passivation
- metal
- oxide
- p-spray
- p⁺ Si
- n⁺ Si


 M. Povoli et al.,
 NIMA 699 (2013) 22

 G.F. Dalla Betta et al.,
 IEEE NSS 2013, N41-1

 G.F. Dalla Betta et al.,
 JINST 11 (2016) P09006


Improved radiation damage model

Goal: extend the predictive capabilities of a past radiation damage modeling

to HL-LHC radiation damage levels

F. Moscatelli et al., IEEE TNS, 2016, in press

Defect	E (eV)	σ_e (cm 2)	σ_h (cm 2)	η (cm $^{-1}$)
Acceptor	$E_c - 0.42$	1.0×10^{-15}	1.0×10^{-14}	1.6
Acceptor ($\phi \leq 7 \times 10^{15} \text{ cm}^{-2}$)	$E_c - 0.46$	7.0×10^{-15}	7.0×10^{-14}	0.9
Acceptor ($7 \times 10^{15} \text{ cm}^{-2} \leq \phi \leq 1.5 \times 10^{16} \text{ cm}^{-2}$)	$E_c - 0.46$	3.0×10^{-15}	3.0×10^{-14}	0.9
Acceptor ($1.6 \times 10^{16} \text{ cm}^{-2} \leq \phi \leq 2.2 \times 10^{16} \text{ cm}^{-2}$)	$E_c - 0.46$	1.5×10^{-15}	1.5×10^{-14}	0.9
Donor	$E_v + 0.36$	3.23×10^{-13}	3.23×10^{-14}	0.9

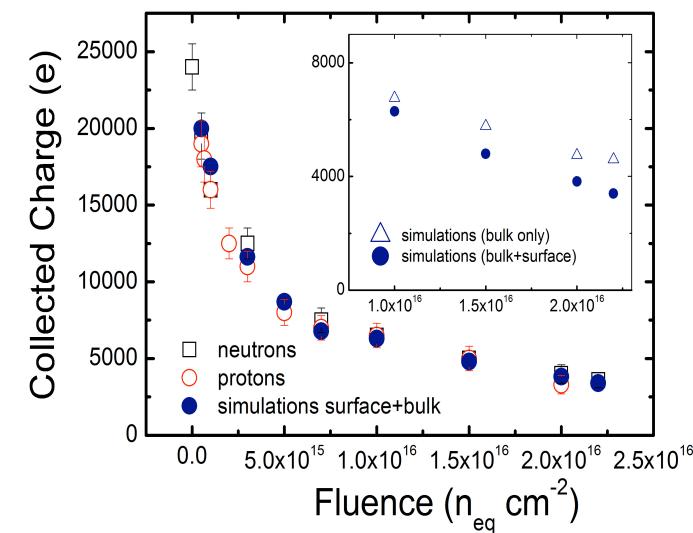


New “Perugia” Bulk + Surface Damage Model



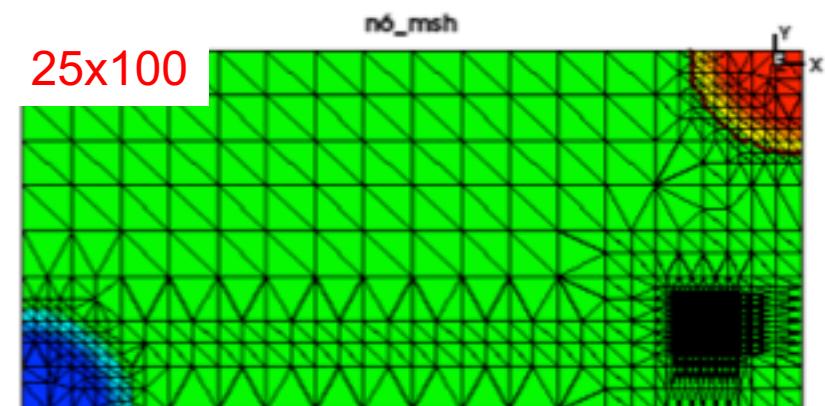
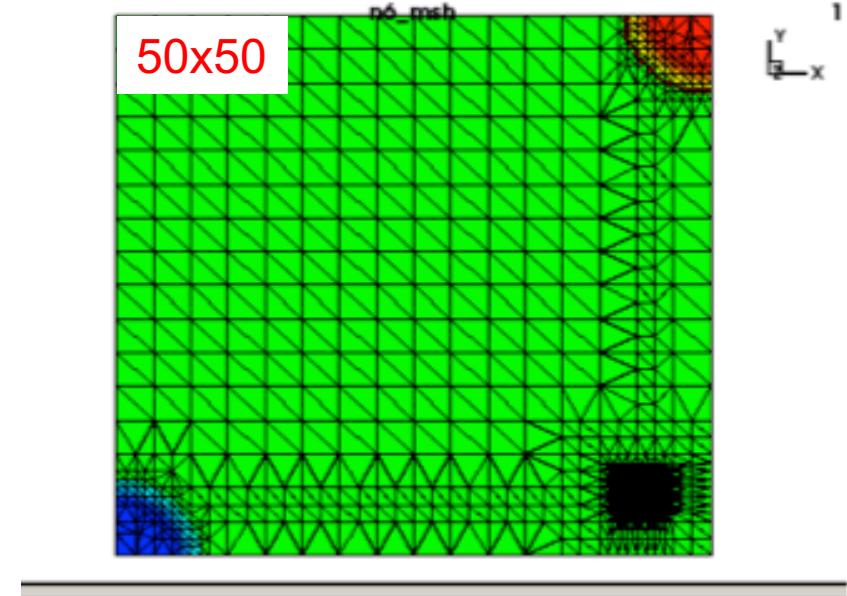
Defect	E (eV)	Concentration
Acceptor	$E_c - 0.4$	40% of acceptor N_{IT}
Acceptor	$E_c - 0.6$	60% of acceptor N_{IT}
Donor	$E_v + 0.6$	100% of donor N_{IT}

$N_{IT} = 8 \cdot N_{eq}$



CCE simulation approach

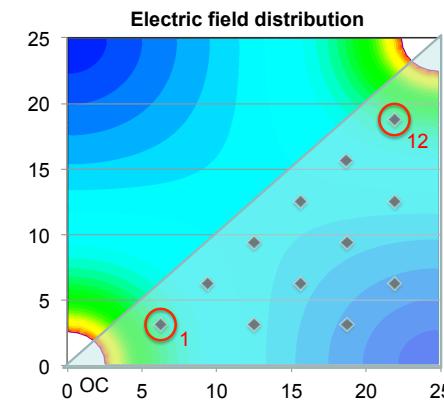
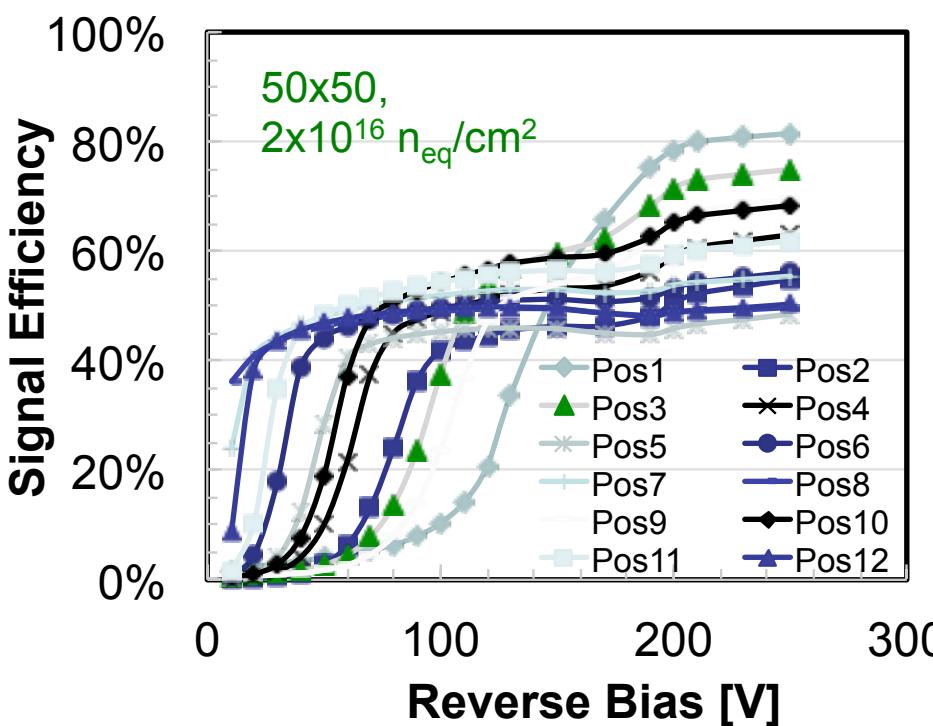
- Simplified simulation domain (~2d):
 - 1 μm thick slice (1/4 or 1/8 of pixel)
- MIP (heavy ion model): vertical hits at several different positions representing different electric field values
- New Perugia radiation damage model
- Avoiding boundaries: no charge sharing
- Subtract leakage current
- 20-ns integration of current signals
- Average charge over all hit positions
- Normalization to injected charge
- Repeat at different bias voltage



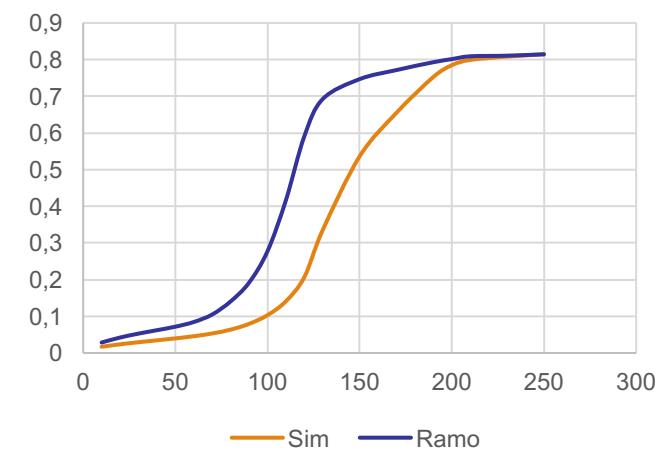
Position dependent Signal Efficiency

R. Mendicino, TIFPA

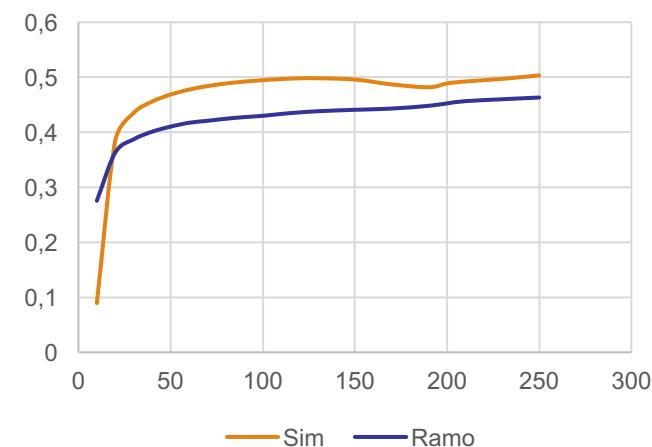
- SE vs bias trend
depends on hit point
- Explained by Ramo's theorem



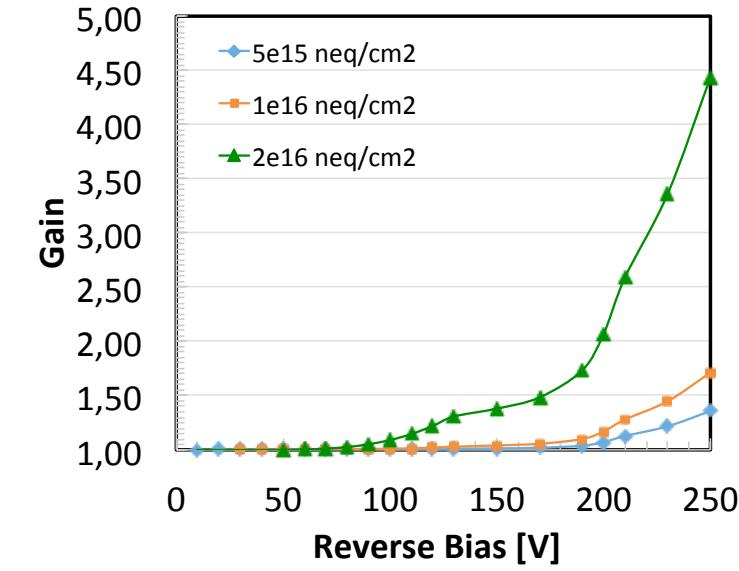
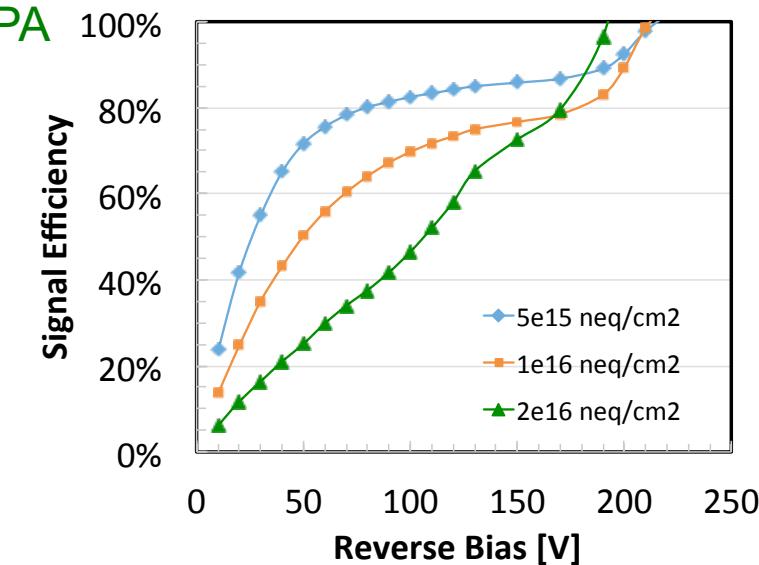
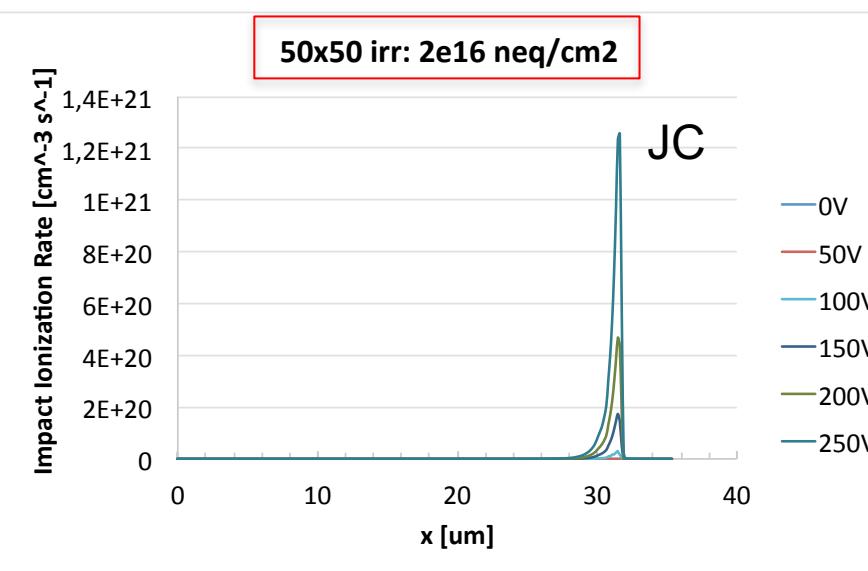
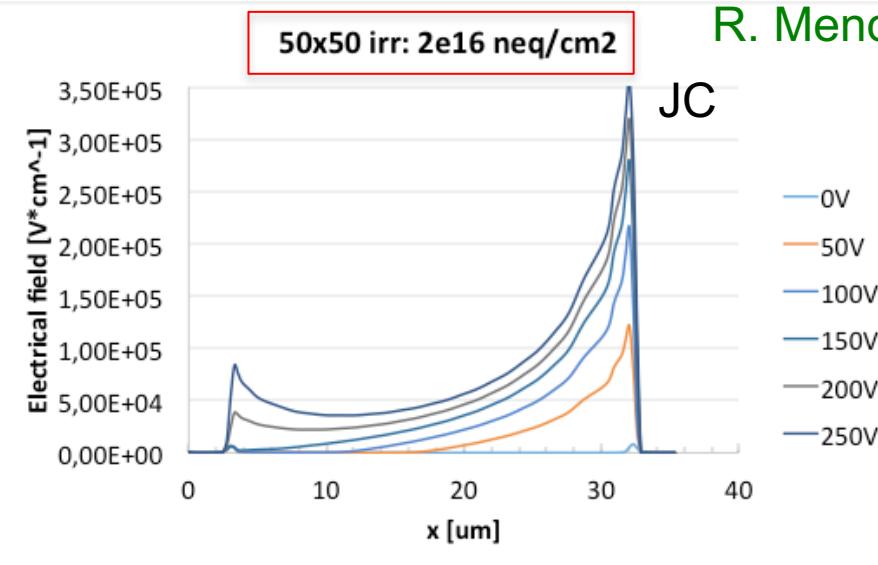
Pos 1: close to ohmic col.



Pos 12: close to junction col.

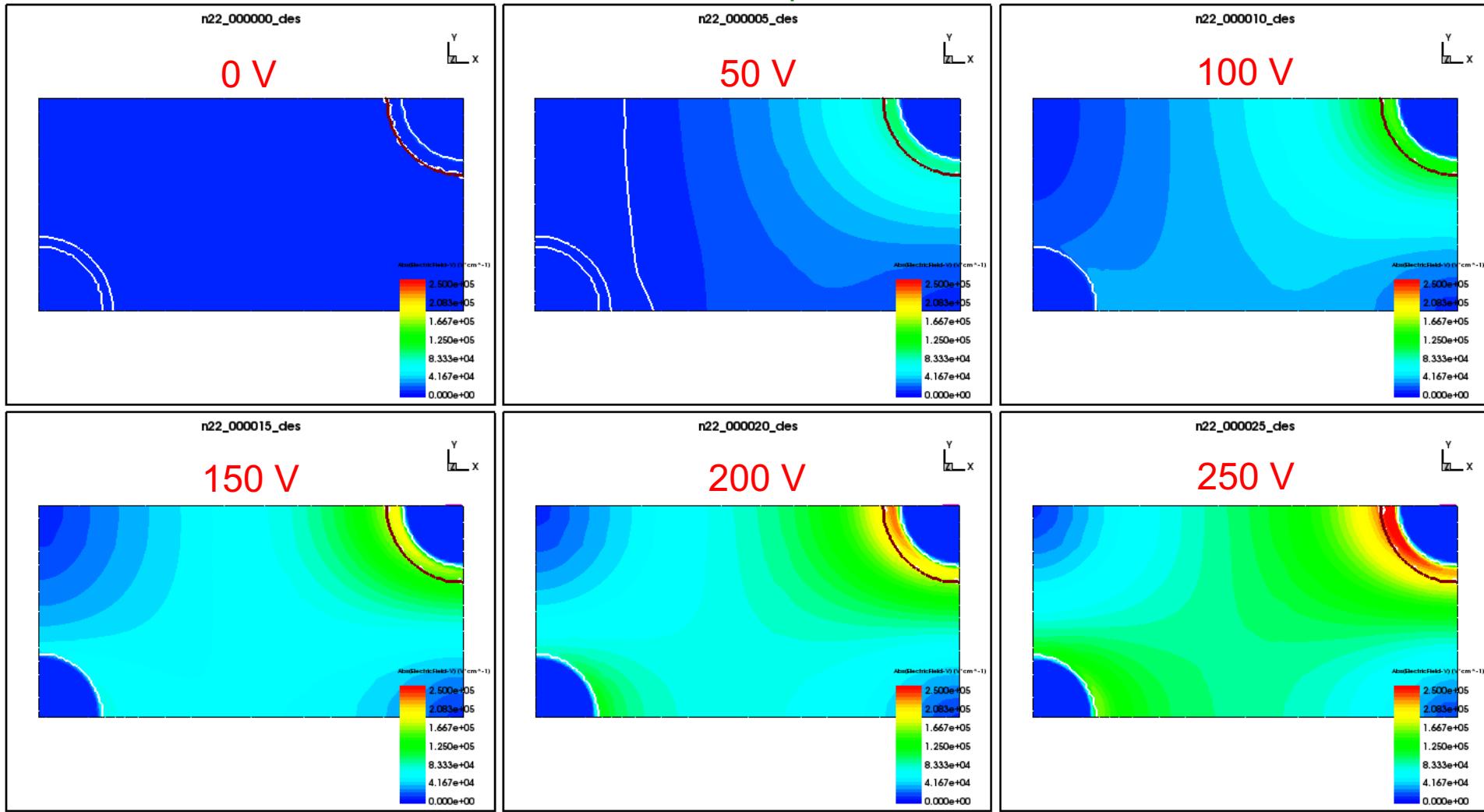


High field effects (50x50)



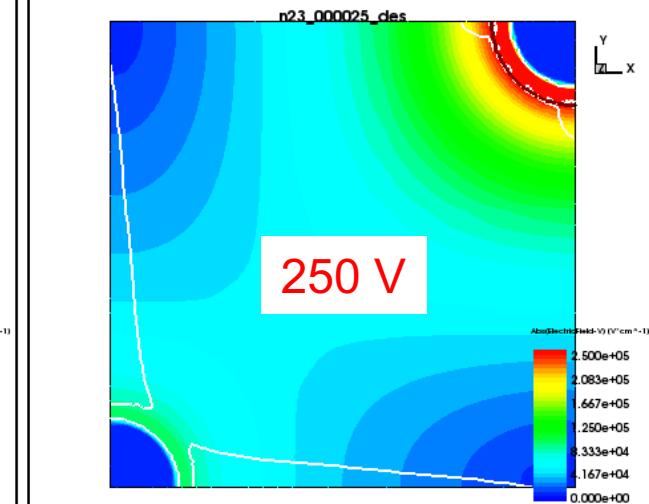
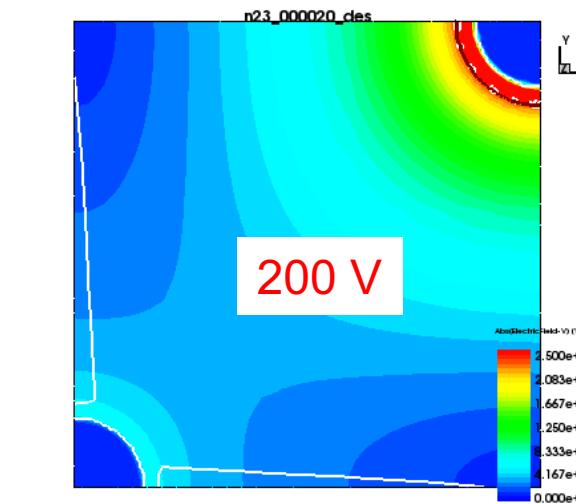
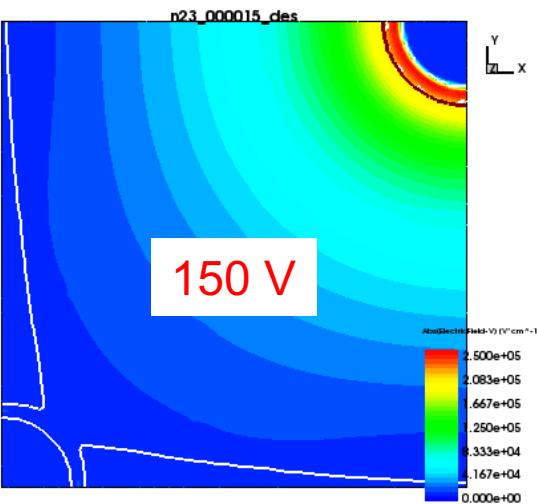
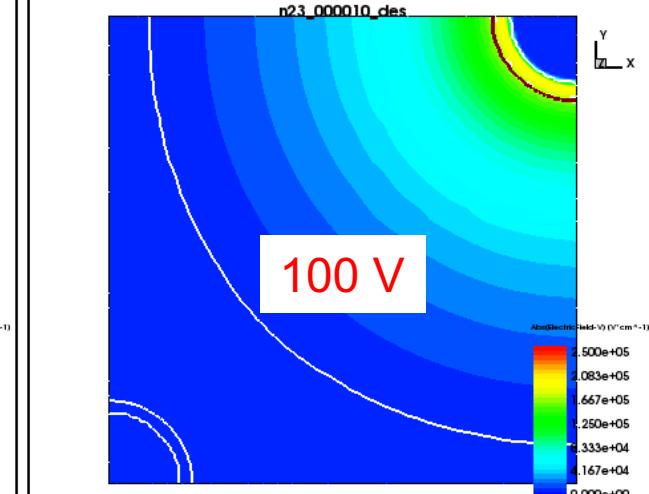
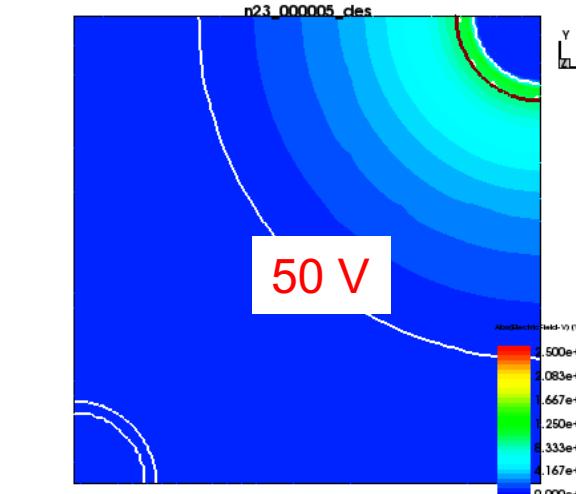
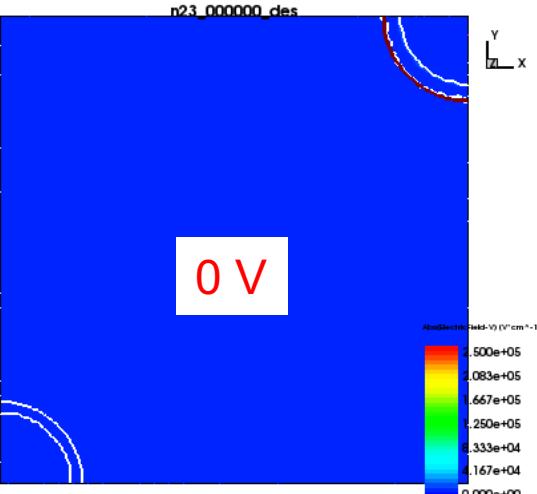
25x100: electric field 2d (preliminary)

$2 \times 10^{16} n_{eq}/cm^2$



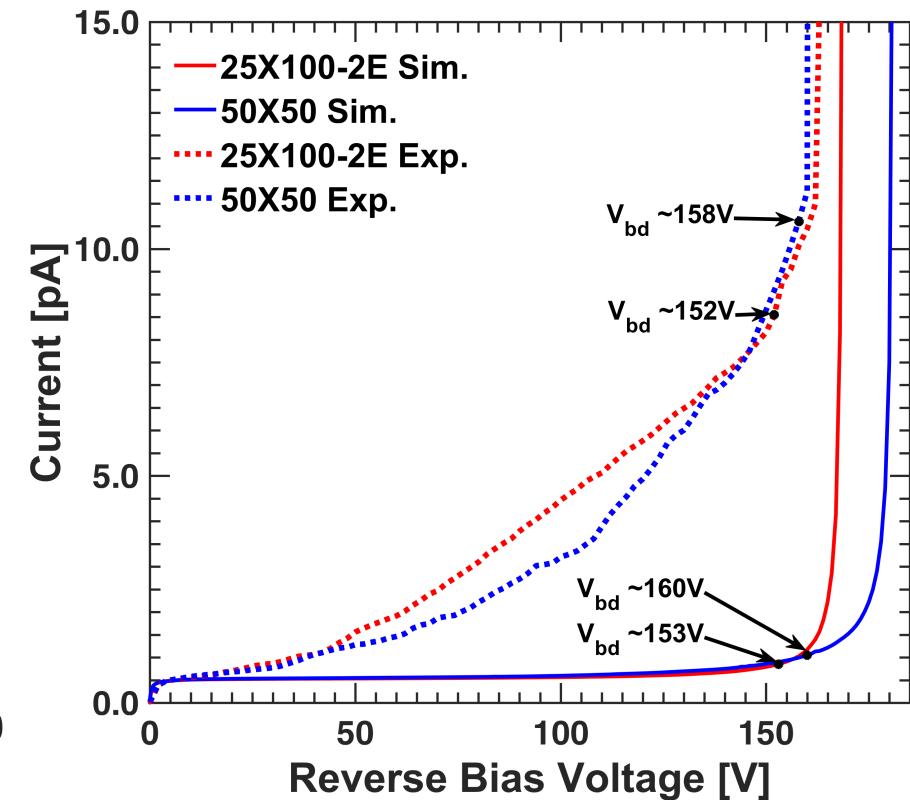
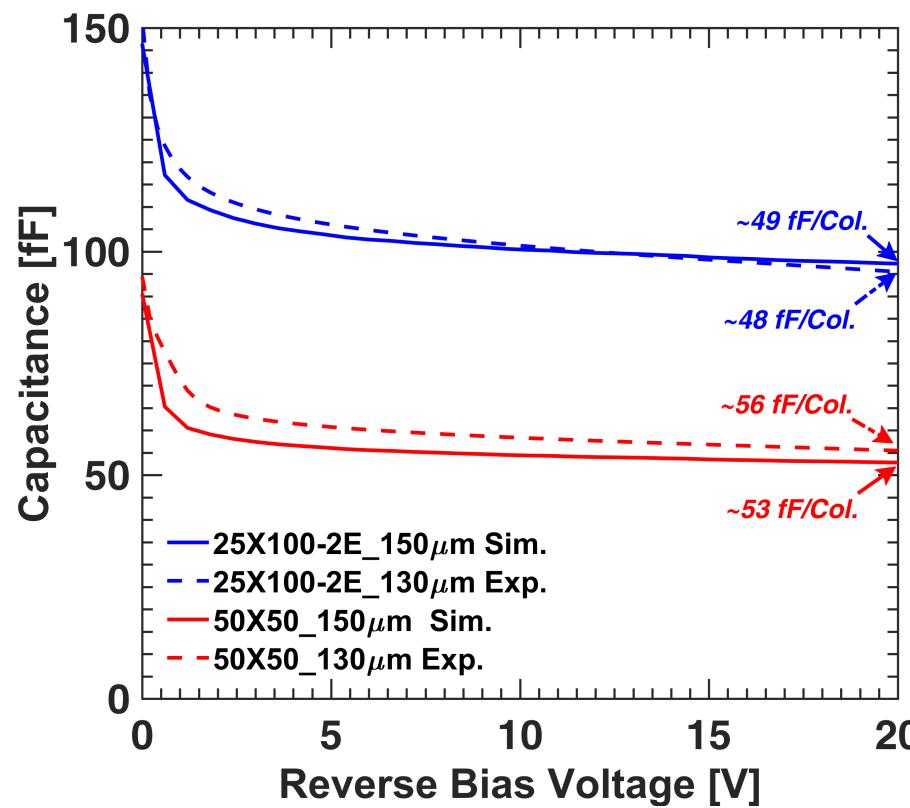
50x50: electric field 2d (preliminary)

$2 \times 10^{16} n_{eq}/cm^2$



Measurements vs TCAD simulations

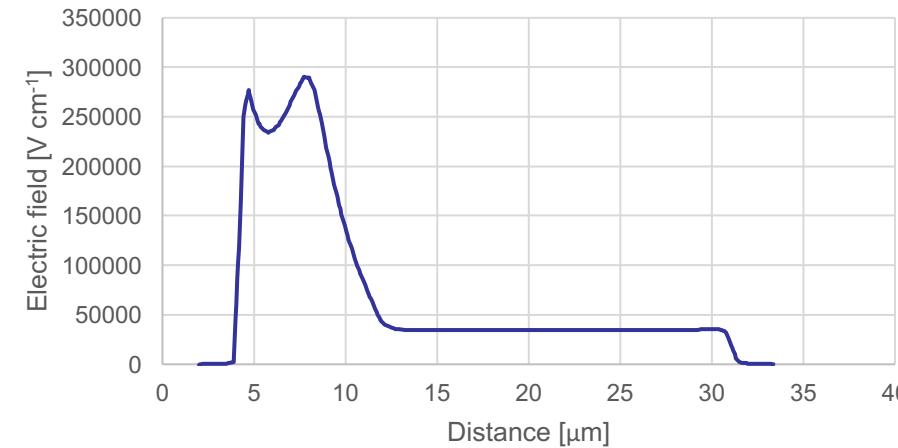
- From 3D diode measurements
 - Very good agreement in C-V curves
 - Good agreement in I-V curves but for the slope
(that depends on interface states, so far not included in the model)
- G.-F. Dalla Betta et al.,
Vertex 2016



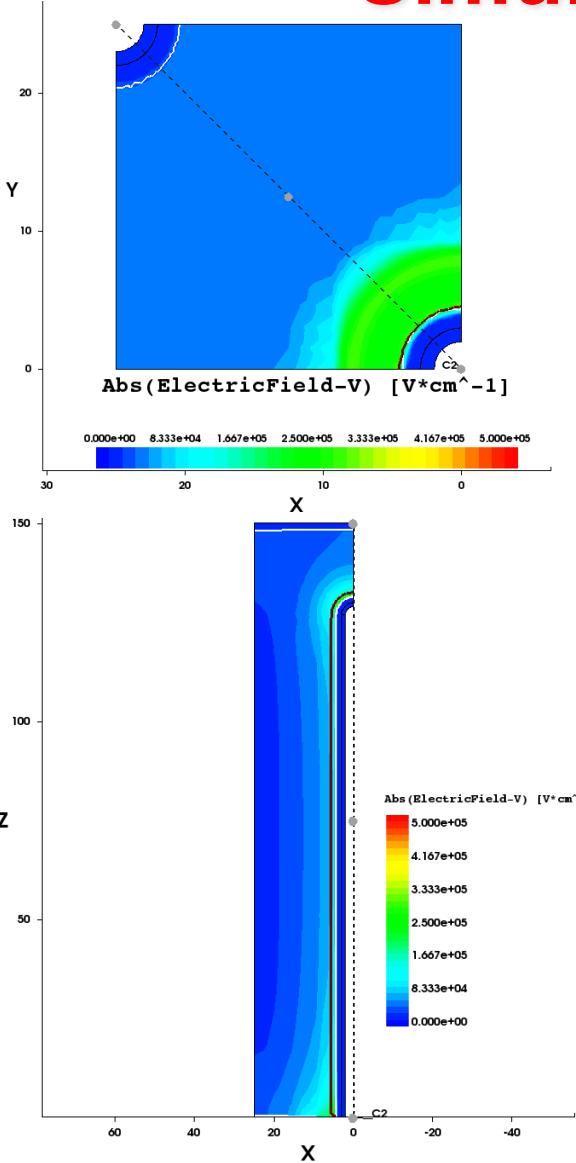
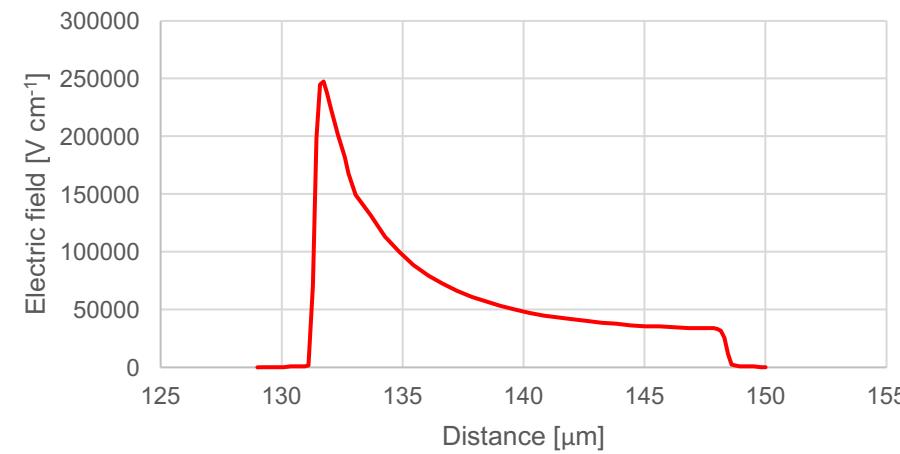
Simulated breakdown voltage

Electric field, 50x50, 160V

Cut surface

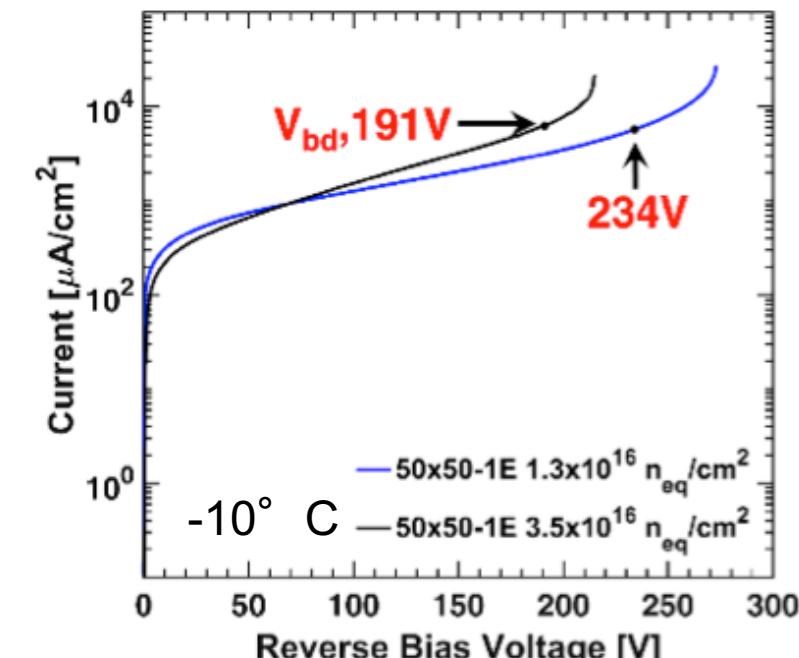
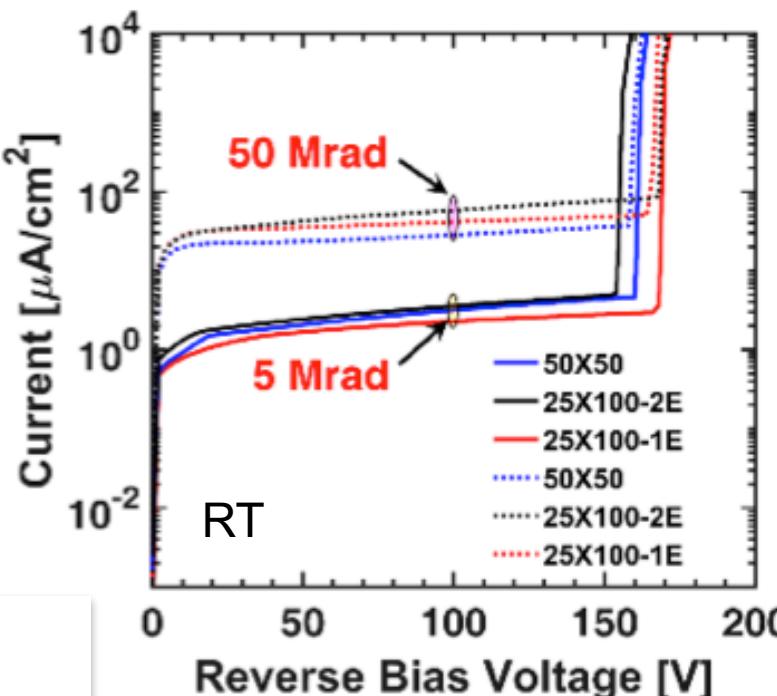


Cut Column



3D diode: γ -ray and proton irradiation

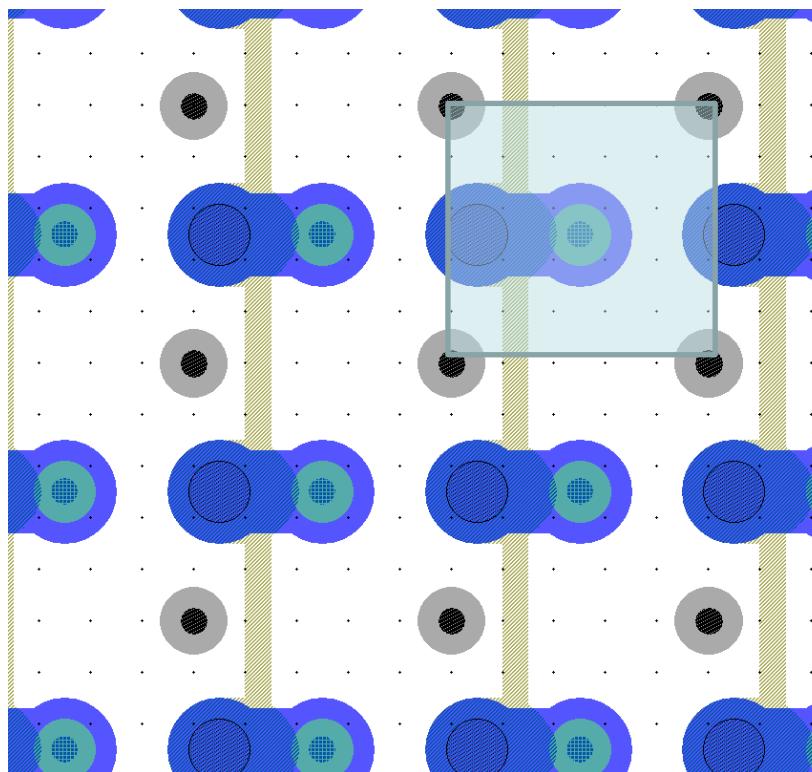
Gamma irradiation at SANDIA, protons irradiation at LANSCE
 (thanks to M. Hoeferkamp and S. Seidel)



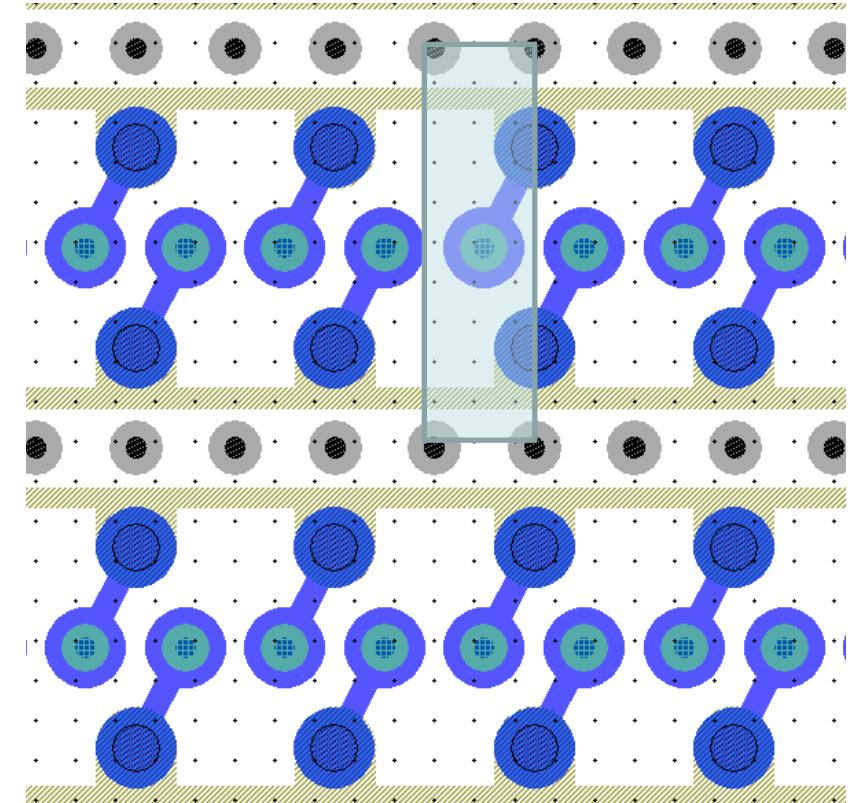
- Minor change of breakdown after gamma irradiation
- For proton irradiation, breakdown voltage increase comparable to neutron irradiation (but larger V_{bd} observed with protons on strips at lower fluences)
 \rightarrow breakdown likely occurs at junction column tips

RD53A Pixel Sensors

RD53A (50X50)



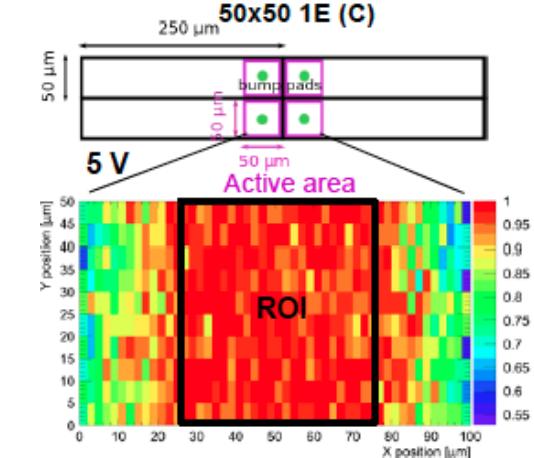
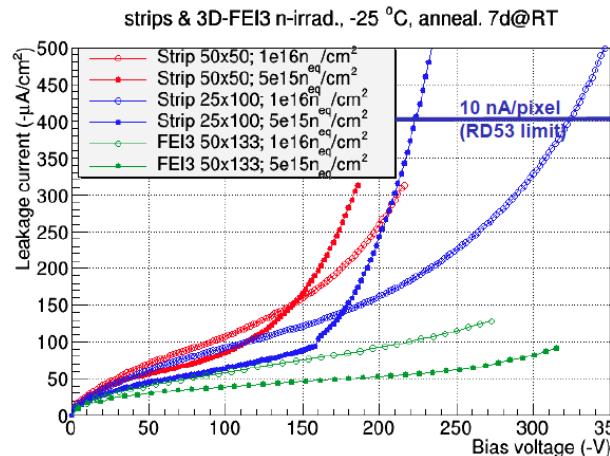
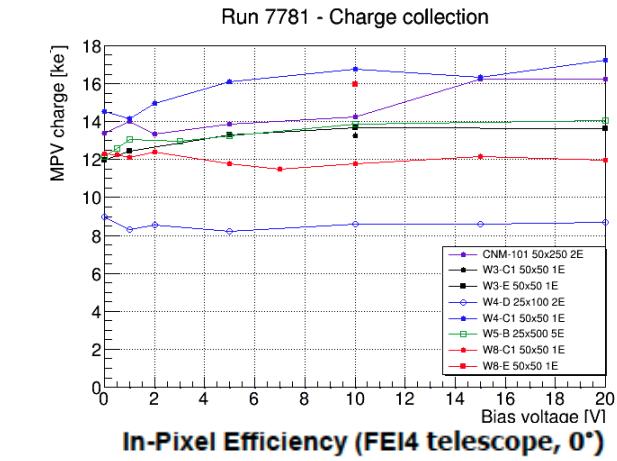
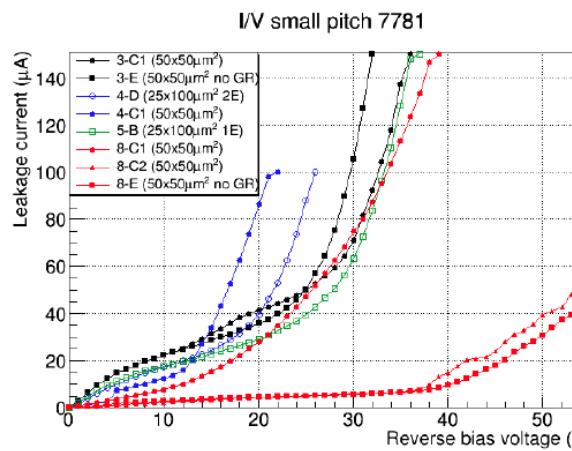
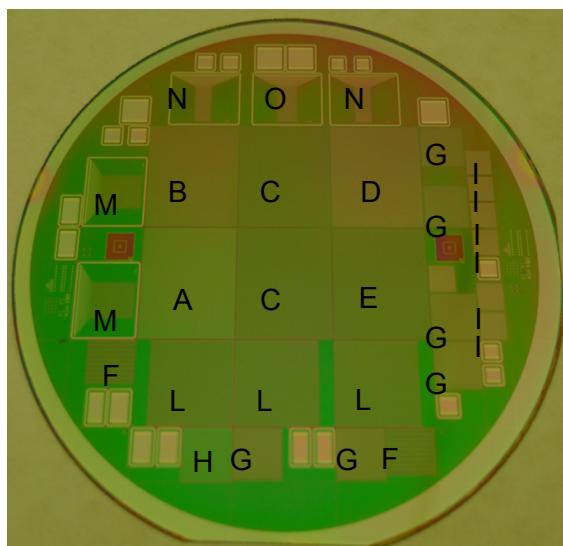
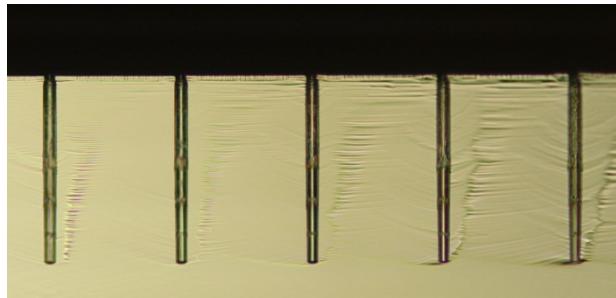
RD53A (25X100-1E)



Also available as 64x64 pixel arrays (CHIPIX65 and FE65-p2)

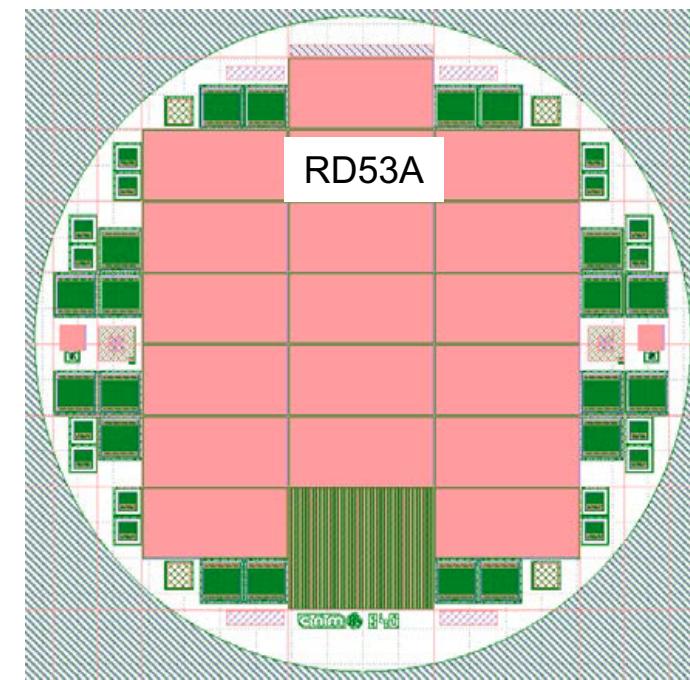
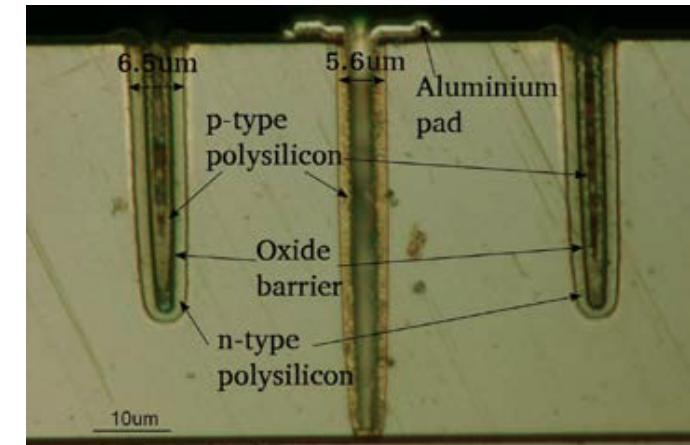
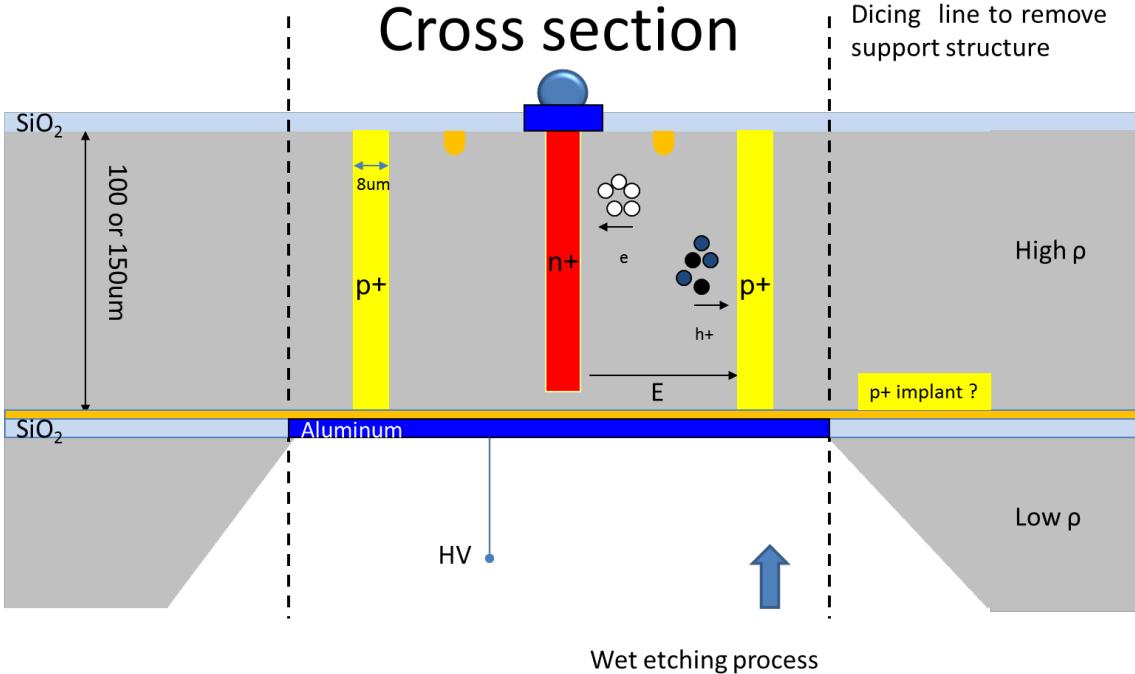
First small-pitch DS-3D at CNM

- Used at CNM for 1st small-pitch batch in 2015 (RD50 project)
 - FZ wafers, 230um thick, p-type (same wafers as IBL production)
 - Hole depth = 210 μm , Hole diameter = 8 μm , aspect ratio $\sim 26:1$



CNM single-side process on SOI wafers

G. Pellegrini, 27th RD50 Workshop, CERN, 2-4 Dec. 2015



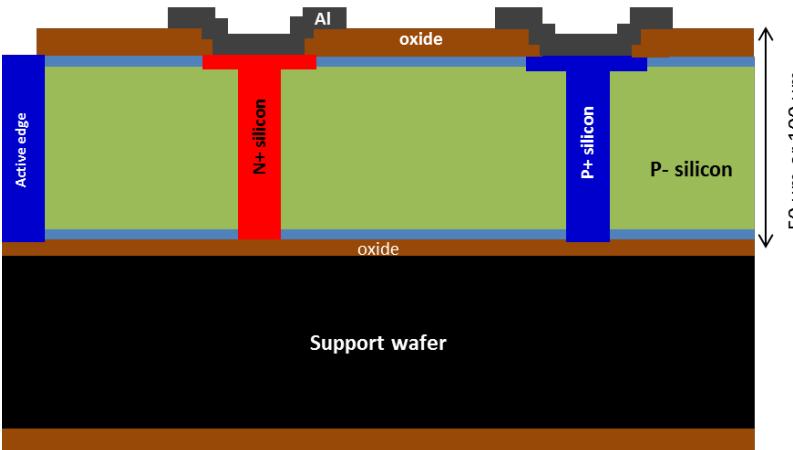
- Single-side process on thin SOI wafers developed at CNM since 2008 for different applications, here modified for back-side bias
- One batch under way with same layout as 1st batch with double-sided process, will be available soon
- Another batch launched with RD53A designs

3D Detector Status and Plans at SINTEF

Norwegian 3D Detector Team: Ozhan Koybasi, Angela Kok, Marco Povoli (SINTEF), Ole Rohne and Heidi Sandaker (U. of Oslo), Bjarne Stugu (U. of Bergen)

- New SINTEF Run 4 under processing (expected by March 2017)
 - SOI and Si-Si wafers with 100 µm and 50 µm thick sensors
 - 2 column types: fully passing (SOI) and partially passing (Si-Si) n-type columns
 - High aspect ratio holes (4-5 µm hole diameter, up to 100 µm depth)
 - Active edge sensors
- The cause of the extremely low wafer yield in Run 3 has been identified and addressed. Hoping that Run 4 will have a better yield.

SOI wafers



Si-Si wafers

