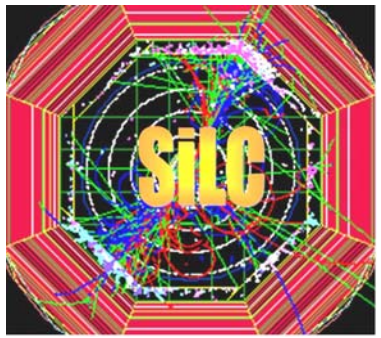
R&D on the new generation of large area Silicon tracking system

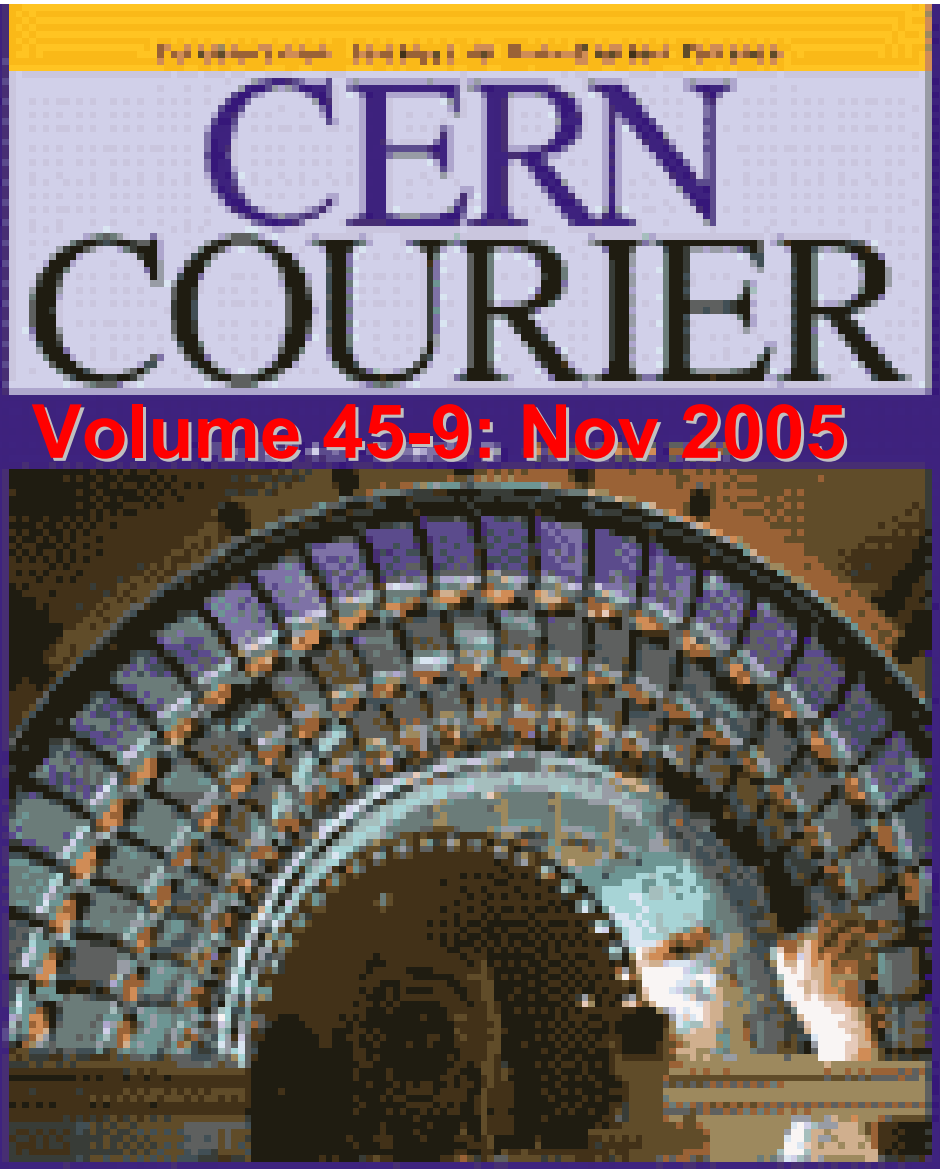


Meeting Japan-France, May 9-11, 2007, KEK

PARTICLE PHYSICS
JOINT LAB
JAPAN - FRANCE

Aurore Savoy-Navarro, LPNHE-UPMC/CNRS-IN2P3

Most of the material presented here is from the SiLC R&D collaboration

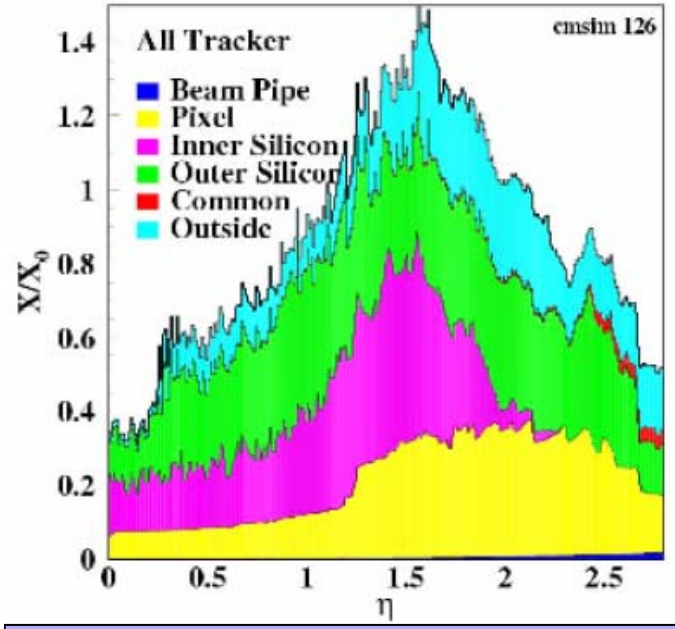


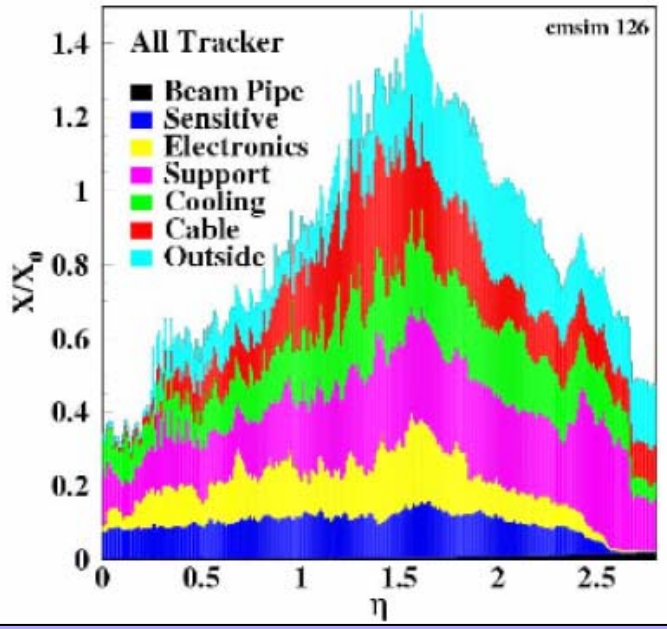
A lot to be already learned from LHC!

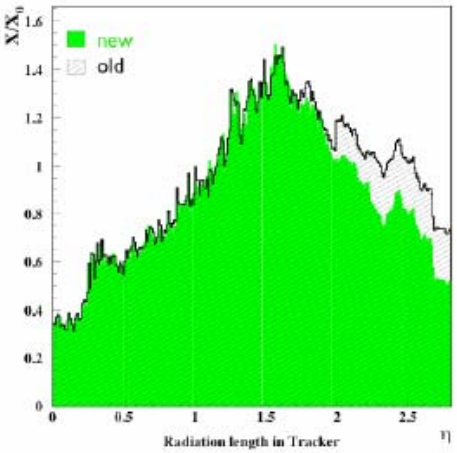
R&D on Si Trackers
¿ WHHHHYYYYYY ?

Material budget

- *Design goal in 1999: $X/X_0 < 1$*
- *Most of the material is electronics related (electronics, cooling, cable, ...)*
- *New description (with most importantly a better description of the bulkheads collecting the services behind the endcaps) predicts less material in the forward region*







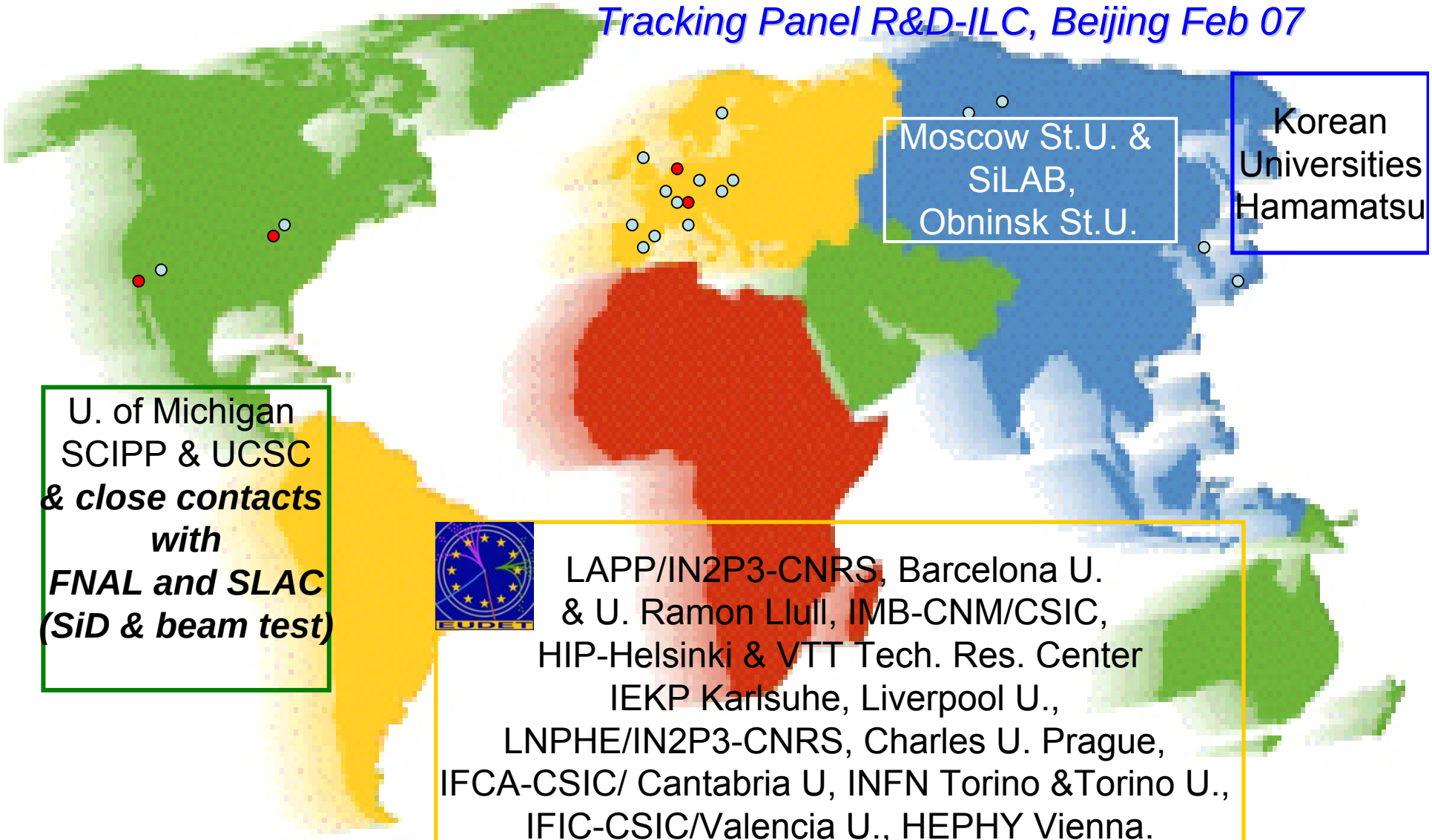
But material budget is not the ONLY reason

Both ATLAS and CMS experiments at LHC, have started to study the upgrade of their tracking systems
Many issues are addressed:

The new Silicon detectors (new pixels, strixels, new strips)
The new FE electronics
New data processing & triggering possibilities
The new mechanical structures

Even if there are clear differences in the machine functioning and
if environmental conditions are different by several aspects
there is a real synergy on many issues
sometimes for different reasons.
this talk will mainly concentrate on the R&D for ILC
but point out some of these synergies.

The SiLC Collaboration: *PRC-DESY May'03 & status report May'05, Tracking Panel R&D-ILC, Beijing Feb 07*



Moscow St.U. & SiLAB, Obninsk St.U.

Korean Universities Hamamatsu

U. of Michigan SCIPP & UCSC ***& close contacts with FNAL and SLAC (SiD & beam test)***

LAPP/IN2P3-CNRS, Barcelona U. & U. Ramon Llull, IMB-CNM/CSIC, HIP-Helsinki & VTT Tech. Res. Center IEKP Karlsuhe, Liverpool U., LNPHE/IN2P3-CNRS, Charles U. Prague, IFCA-CSIC/ Cantabria U, INFN Torino &Torino U., IFIC-CSIC/Valencia U., HEPHY Vienna. ***& close contacts with CERN and DESY***

SiLC: Silicon tracking for Linear Collider

Japan-France Si tracking 2007: KEK-LPNHE

Toru Tsuboyama, Yasuo Arai,
Osamu Tajima (KEK)
Takeo Kawasaki (Niigata)

Guillaume Daubard, Wilfrid Da Silva,
Jean François Genat, Didier Imbault,
Frédéric Kapusta, ASN

- ***Sensor R&D:***
  - ***New microstrip sensors made from larger wafer, thinner and with small pitch (HAMAMATSU HPK)***
  - ***Large pixels (starting with OKI via Italian teams)***
- ***Electronics R&D***
- ***Mechanics R&D & new materials: new module architecture and light but robust detector structure***
- ***Simulations for detector performances and Physics studies***
- ***Common interest on B Physics***

SiIC Collaboration main features:

- Generic R&D: representatives of GLD, LDC & SiD
- Worldwide
- Large expertise on all the R&D facets
- Synergy with LHC and LHC tracking upgrades
- Important R&D infrastructures in several Labs
- Silicon-oriented Research Labs: IMB-CNM, ETRI, SiLAB, VTT
- Close contacts with international Labs
- Collaboration with industrial firms
  (among which HPK)
- EUDET E.U. Infrastructure project involvement

Physics and Machine environment at the ILC are both imposing stringent conditions on the tracking system, namely:

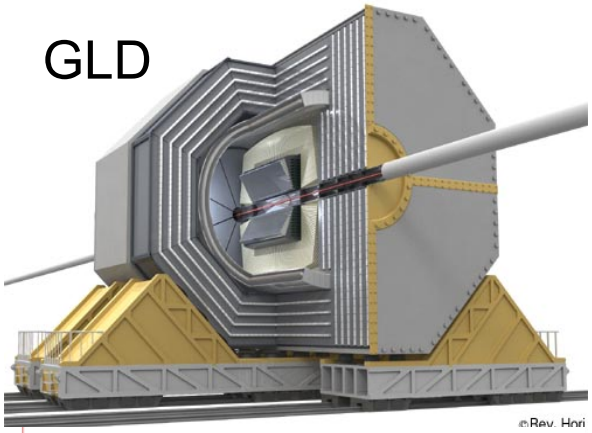
- high performance in momentum resolution and spatial resolution
- Low material budget
- Reliability, simplicity and easy to build, monitor and calibrate devices.
- Full coverage (No dead regions & **importance of End Caps/ Forward**)
- Easy to integrate in the detector and readout/DAQ architecture (part of particle flow)
- System able to handle very high magnetic fields (3 to 5 Teslas)

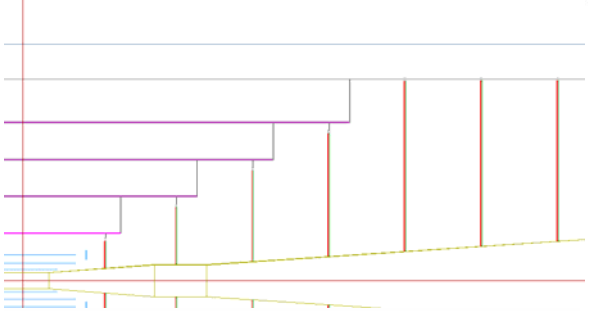
- **This leads to an active R&D for ILC large Silicon trackers, on:**
  - Mechanics R&D
  - Sensors R&D
  - Electronics R&D

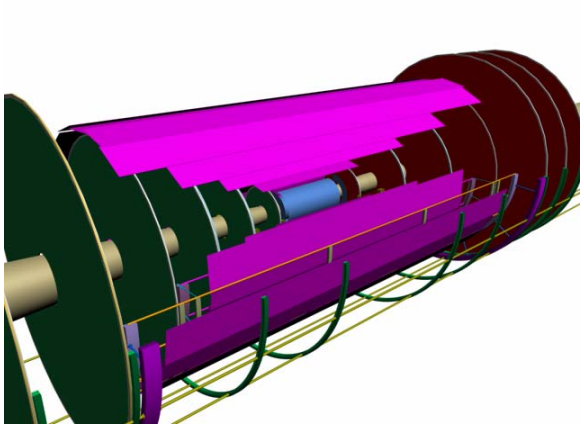
  Together with developing the needed tools:
  - Simulations
  - Lab test bench and test beams

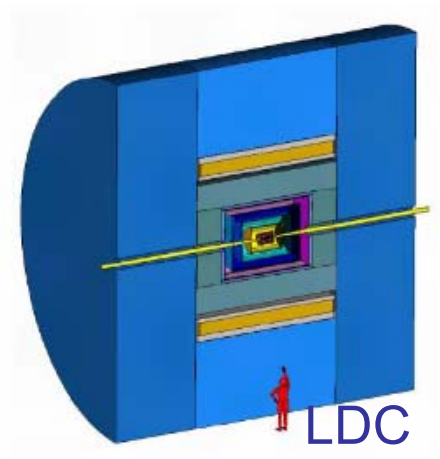
Keeping in mind all the issues listed above, for each of these R&D topics

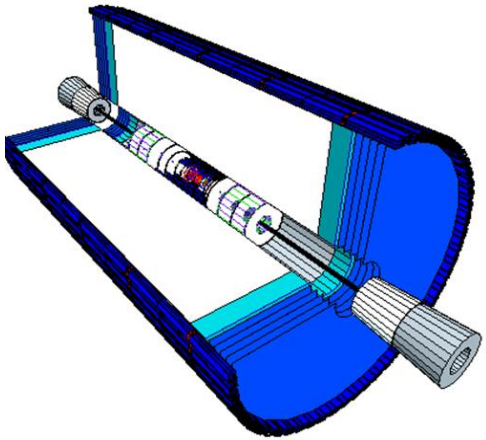
Role of Silicon tracking *or Silicon tracking what for?*



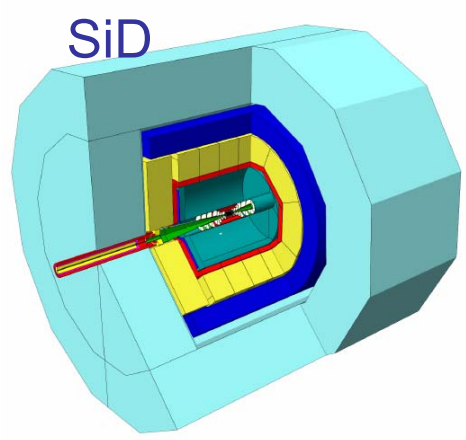


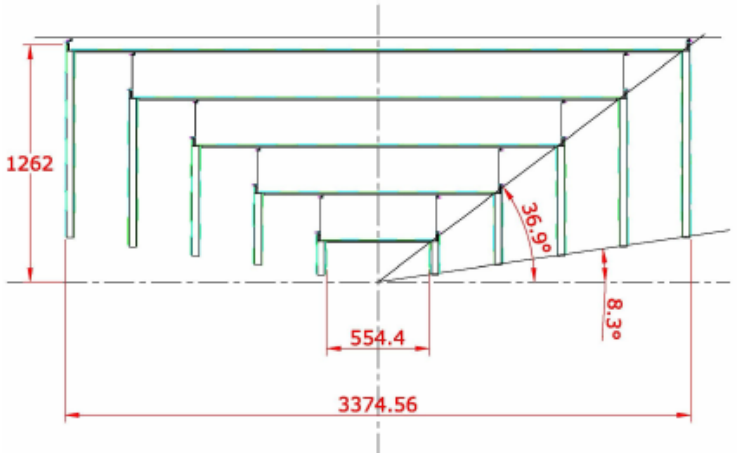




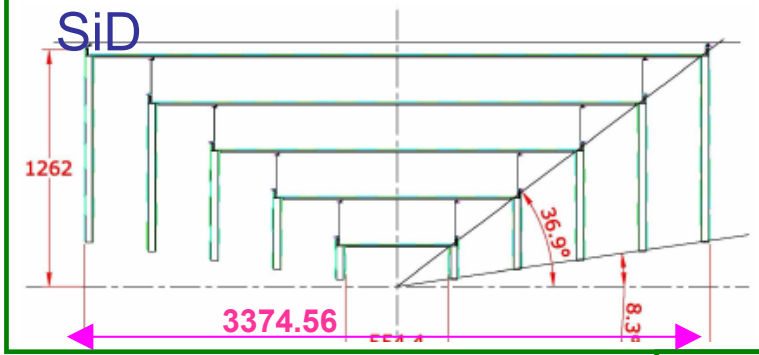


3 detector concepts & main difference:
The tracking strategy=TPC Yes or No

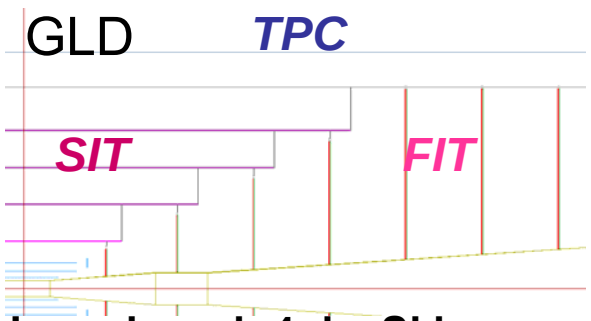




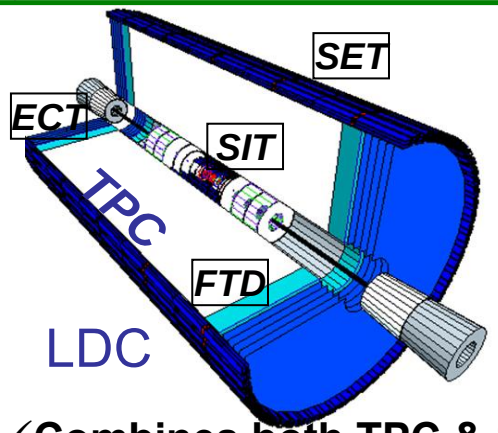
Role of Silicon tracking *or Silicon tracking what for? (cont'd)*

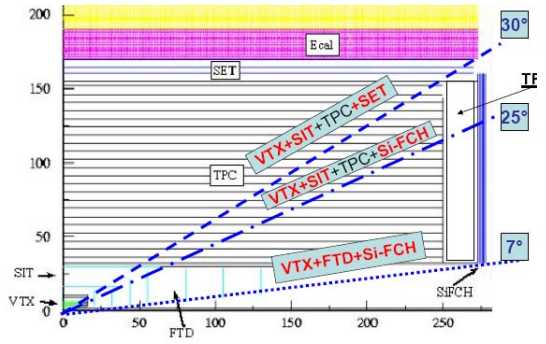


SiD concept: All-Silicon tracking strategy
Integrated Silicon tracker,
Barrel: more a '' sagitter '' than a true tracker?
with fully integrated Forward tracker:
Appealing for hermeticity & large angle Physics.



Inner barrel: 4 d.s Si layers
True tracker vs just a ''linker''
Pb: material budget in front of TPC?





Si Envelope:{SET+(SIT+FTD)+ECT}

✓Combines both TPC & Silicon tracking technologies
✓Each Si component LINKS 2 subdetectors (smoother transition)
✓Improves tracking overall performances (see simus)
✓Calibration of systematics & full coverage

Si Envelope is like stretching a all Silicon tracking into 2 parts: inner and outer ones and install a TPC in between.
SiLC:UNIQUE place to study/compare these various crucial tracking concepts

MECHANICS R&D

Teams: IEKP Karlsruhe, IFCA-CSIC/Santander, Korean Group, Liverpool U., LPNHE/IN2P3-CNRS, INFN-Torino & Torino U.

Why R&D on Mechanics?

The requirements on the next generation of large Silicon tracking systems are:

- low material budget,
- simplicity of the design
- easy to construct (automatization or semi-automatization, transfer to industry)
- New materials
- and robustness and stability
- stringent requirements on spatial requirements (alignment & positioning)
- and on hermeticity
- Integration issues (and push pull???)

CAD design studies on Si components

A series of preliminary CAD designs of the various components of the Silicon tracking system in an ILC experiment with an emphasis on

- simplifying as much as possible the overall design (limiting the number of different fundamental elements of the detector architectures (sensors and elementary modules or ladders))

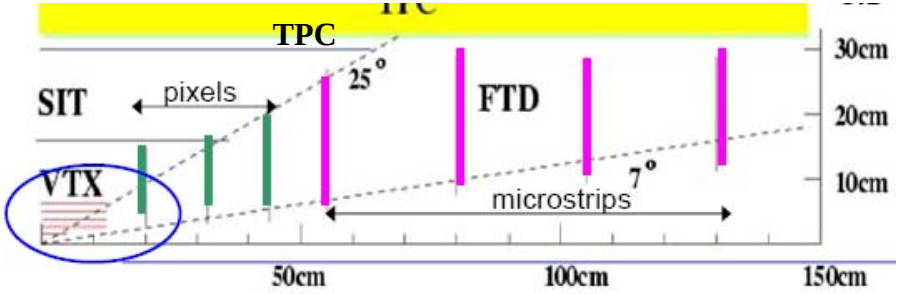
- and the main R&D objectives on Mechanics

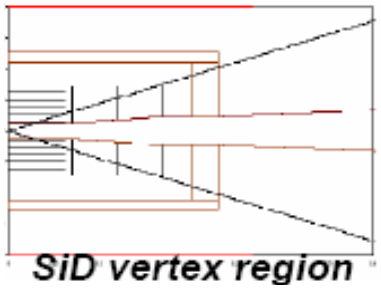
- Developing mechanical prototypes for preliminary mechanical studies and for test beams

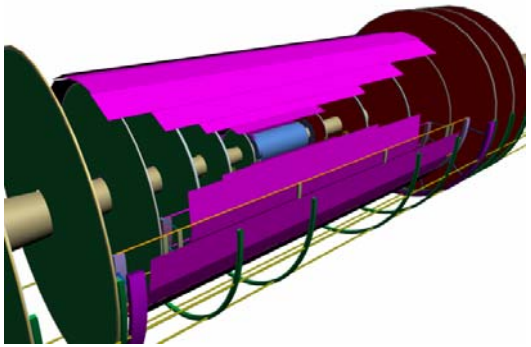
Important input for the detailed simulation (DB Geometry) and for building more realistic prototypes as for instance for thermo mechanical studies.

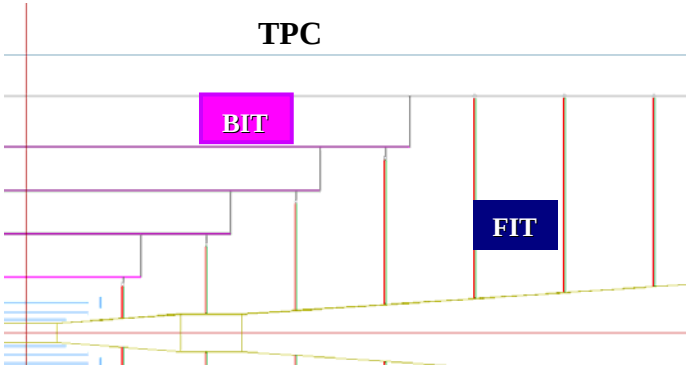
Example 1: The innermost layers

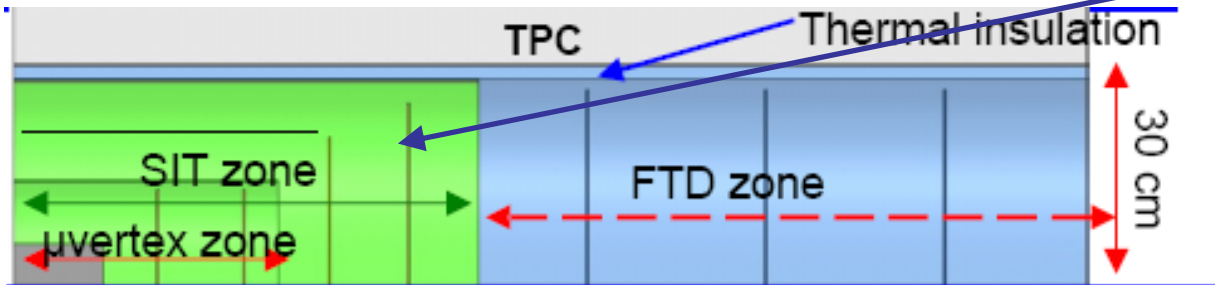
In GLD, LDC and SiD detector concepts the innermost part is done in a rather similar way: Si layers in barrel & disks in the forward/backward regions:









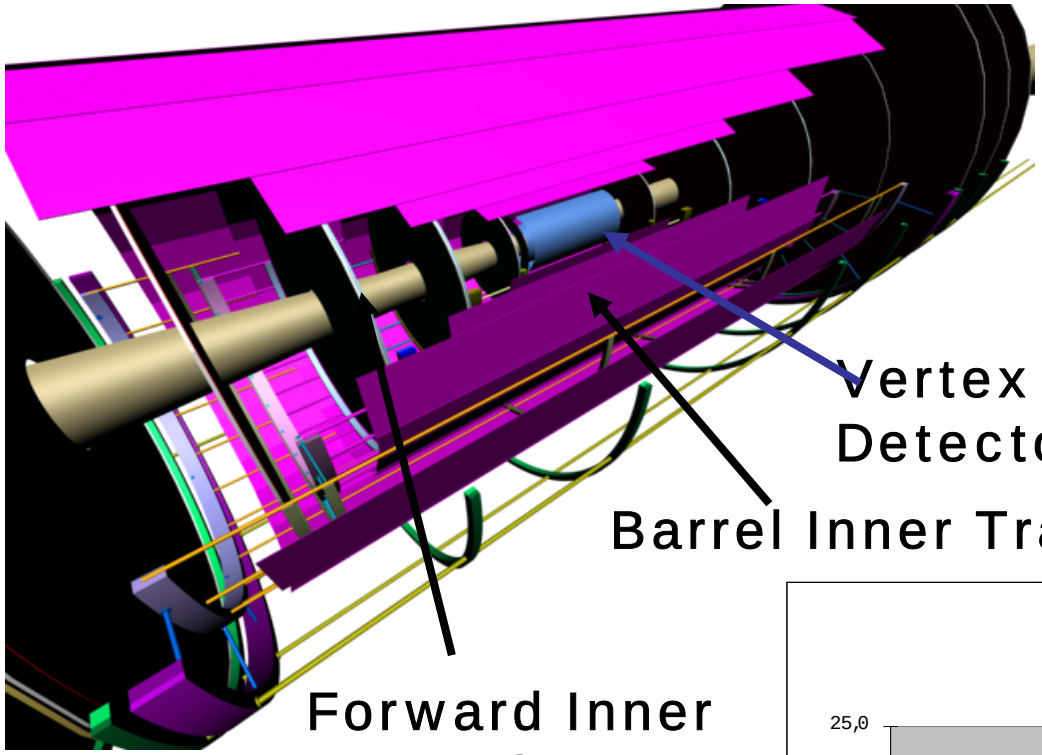


Korea, IFIC and UB

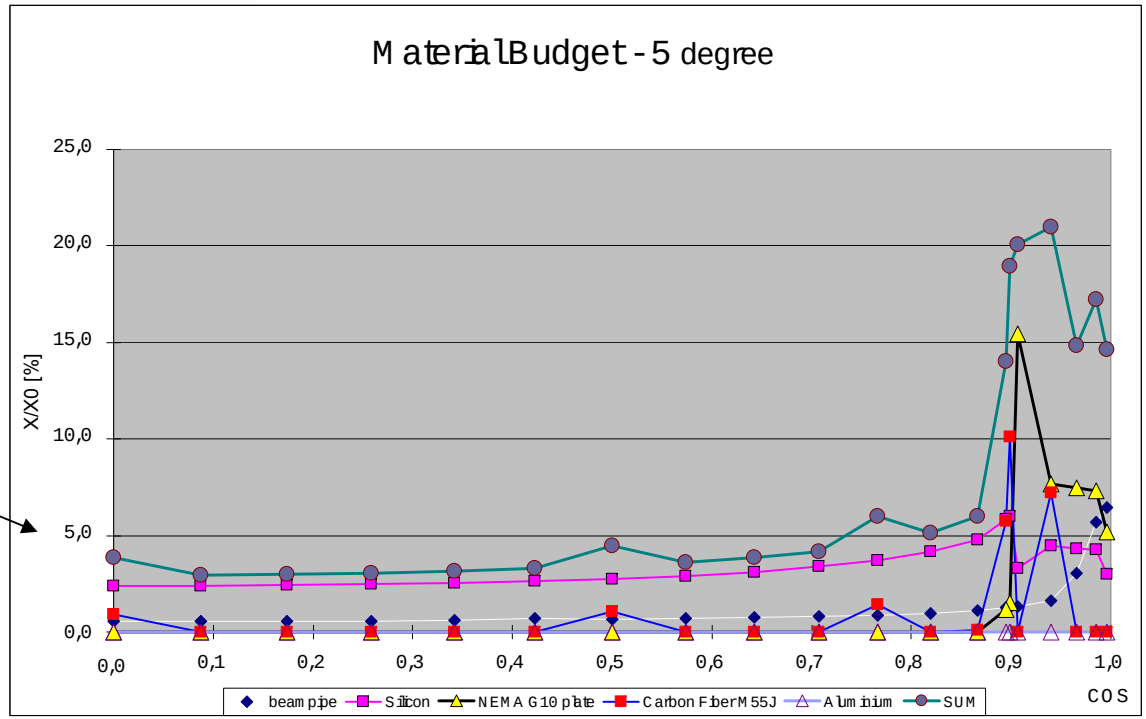
Thus the idea to extend the vertex detector as indicated in green region, borrowing the same sensor technology (pixels). SiLC studies: sensors & simulations

IT Mechanical Structure

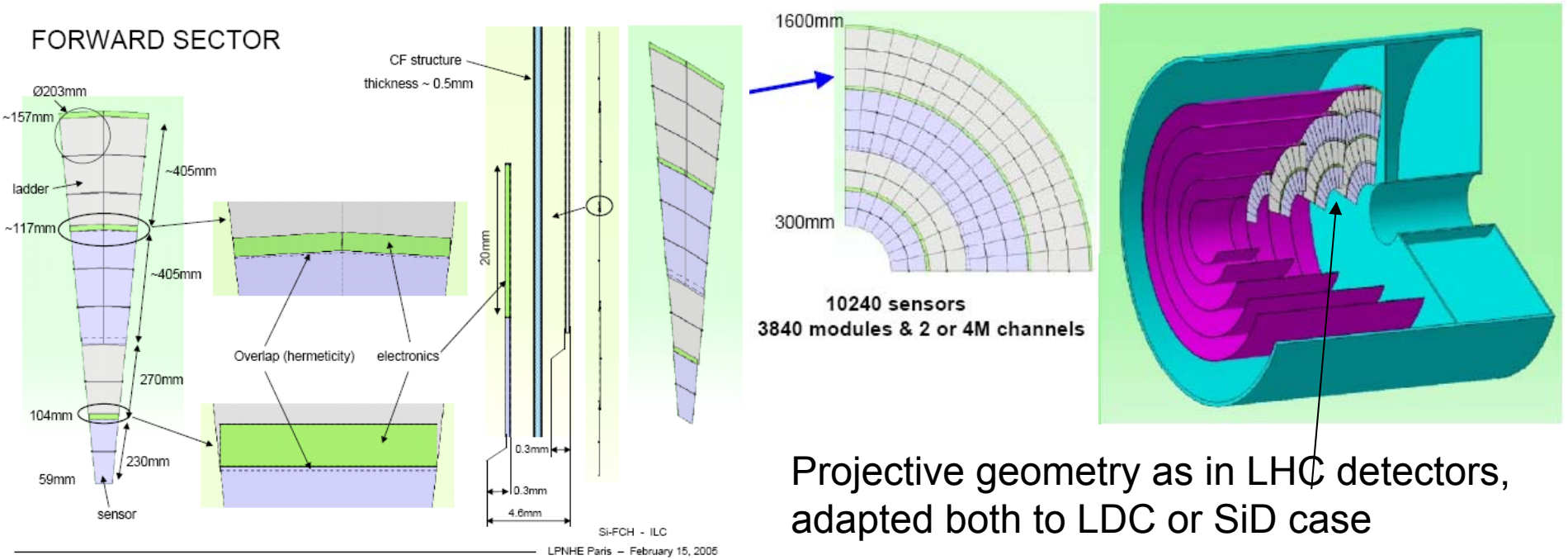
Korean Group, H.Kim et al.



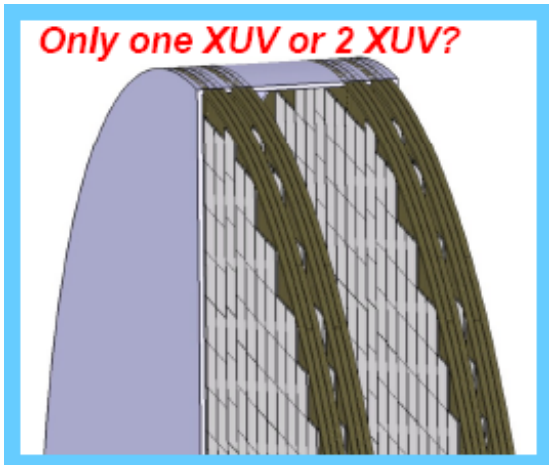
Beam pipe+Silicon+NemaG10plate
+ Carbon support+Al

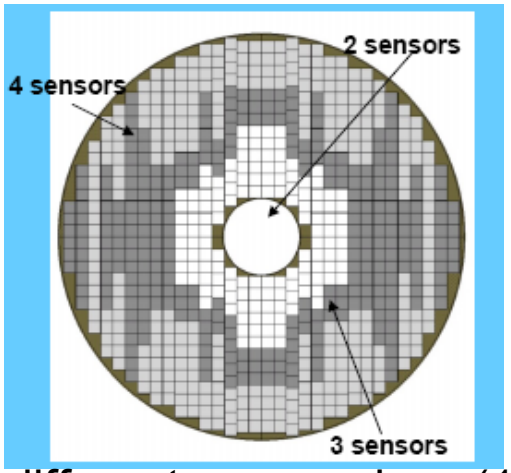


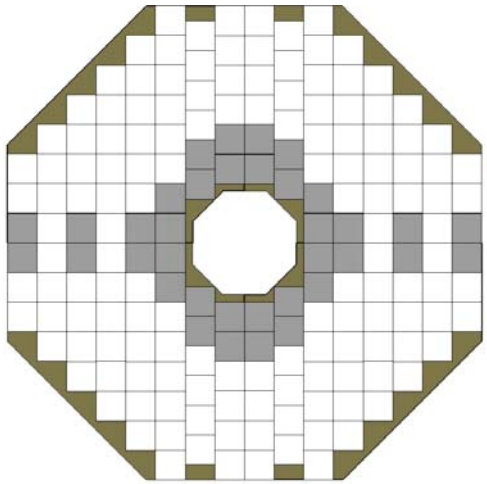
Example 2:CAD of the EndCap Si layers



Projective geometry as in LHC detectors, adapted both to LDC or SiD case







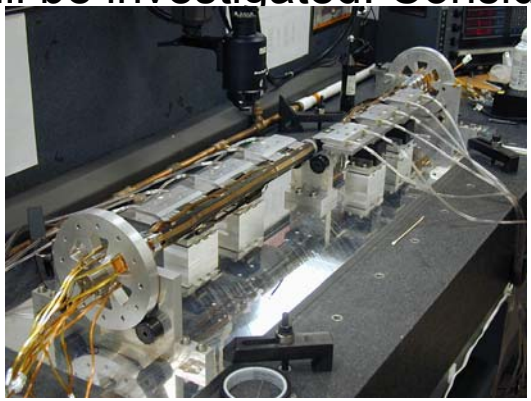
XUV design with different sensor sizes (10x10cm2 or 20x20 cm2)

A novel approach to construct elementary modules

(Liverpool U., T. Greenshaw & ASN, LPNHE-Paris)

Main quest: transparency & simplicity
Imply working on sensors, FEE,connectivity, mechanical structure, easiness to assemble (automatization issues)

Design & efficacy of Carbon fibre shells as a support structure for the Si tracker Will be investigated. Considerable expertise within SiLC.



Example 1: Liverpool designed & manufactured the supports for the L00 CDF layer (i.e.low mass cylindrical rigid structure of Radius = 1.5 cm and incorporating strips & cooling channels

Example 2: MICE Muon Ionisation Cooling Experiment
This support is at much larger scale: 50 cm diameter Carbon fiber ring

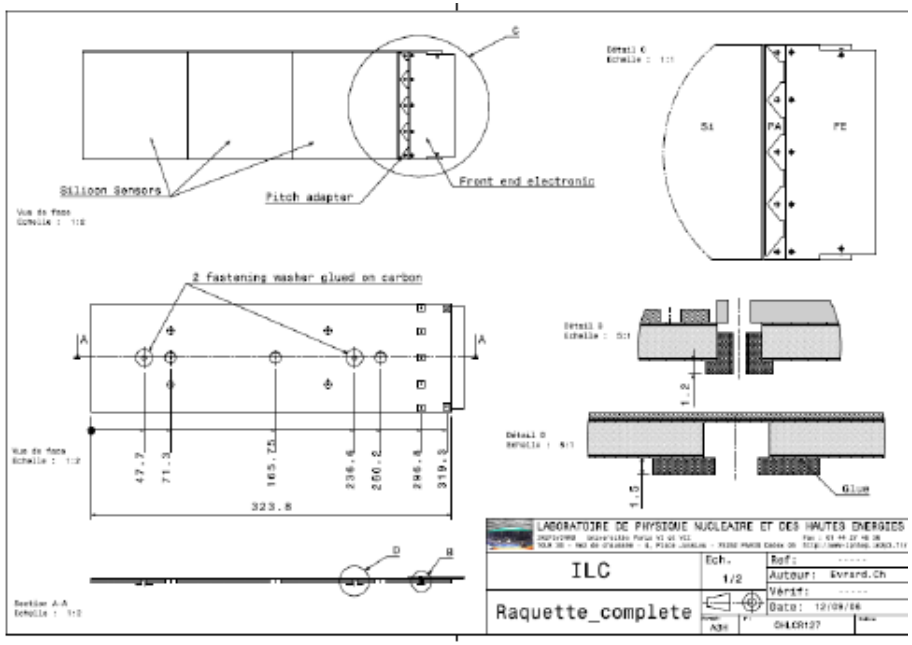
Studies of the support of Si trackers will be studied in 2 ways: sensors directly attached to a fiber shell Or sensors first assembled in 'ladders' , attached to a support frame

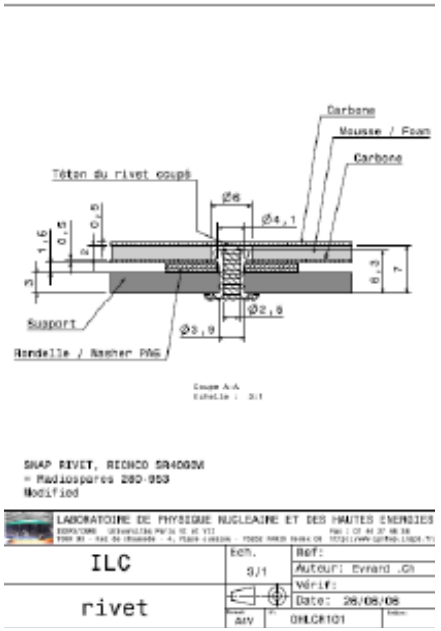
A novel approach to construct elementary modules

The ladder designs which will be investigated by the SiLC Collaboration include foam sandwich structures.

These are being studied for the vertex detector of the ILC by the LCFI group, who have demonstrated that ***both Silicon carbide and reticulated Carbon foams*** can be used to construct stable, extremely low mass ladders

A first step towards this type of ladder support structure is being experienced for the construction of the elementary modules for the forthcoming test beam in 2007.





COOLING *(Torino, LPNHE)*

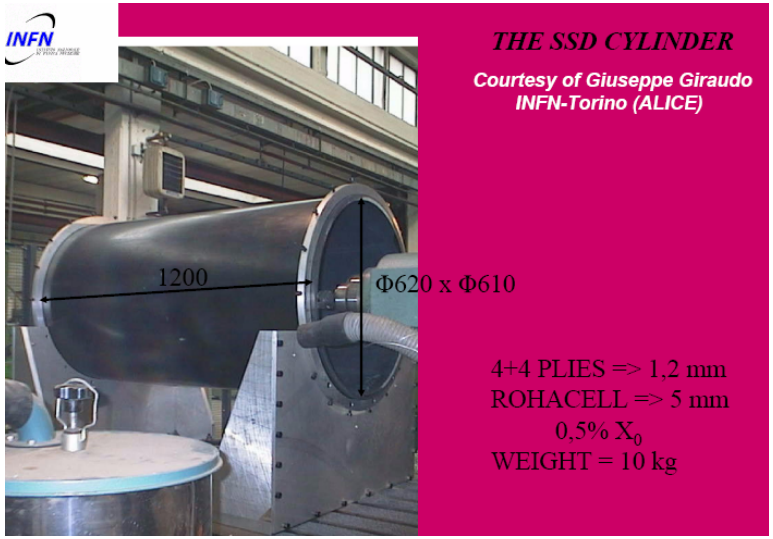
Hypotheses of work

- **At ILC Si tracker will be quite radiation safe**
- **Thus T°C up to 30°C on sensors are allowed and**
- **ΔT°C ~ 10°C**
- **From FEE electronics:**

  1mWatt per channel (certified by electronics R&D results)
- **Main source of warming up: the neighbours (still unknown??)**

Thus much better conditions than at LHC.

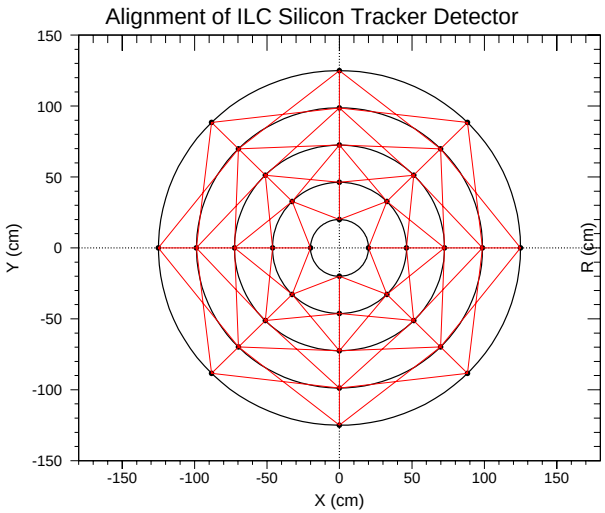
An insulating should be enough in order to protect from the external power dissipation and serving at the same time as Faraday cage

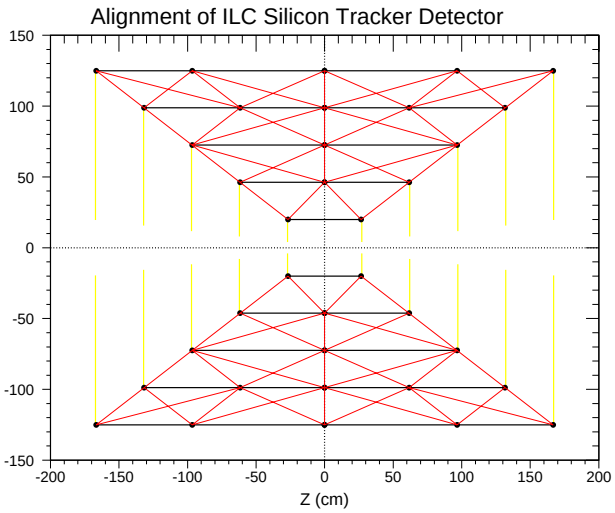


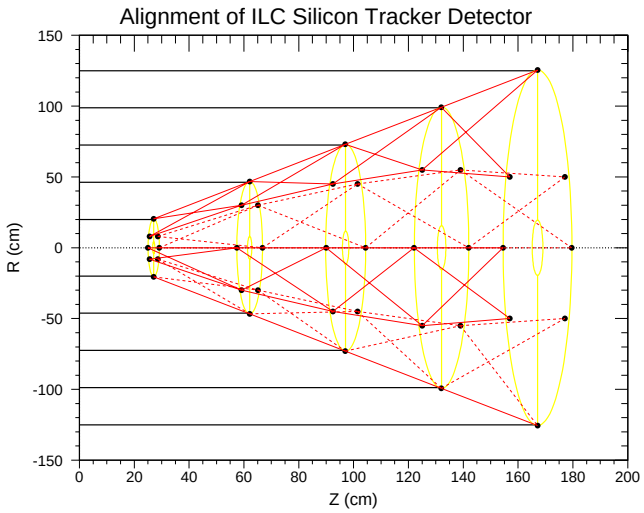
Alignment – FSI
(frequency Scanning Interferometer)

(H.J. Yang & K. Riles University of Michigan)

- **Measure hundreds of absolute point-to-point distances of tracker elements in 3 dimensions; based on development in Oxford University for the ATLAS SCT**
- Absolute distances determined using a Frequency Scanning Interferometer ("counting fringes") and an array of optical beam splits from a central laser.
- Grid of reference points overdetermined → Infer tracker distortions





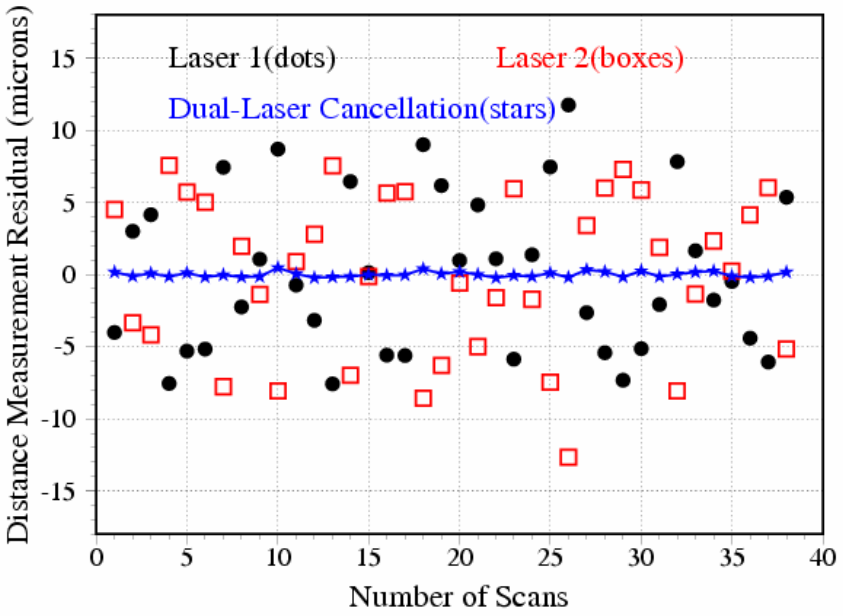


Alignment – FSI (cont'd)

- **In well-controlled ambient over distance of 10-60 cm: ~ 50 nm resolution** by using multiple-distance measurement technique. Vibration Measurement: 0.1-100 Hz, amplitude as low as few nm. *(*H.J. Yang, J. Deibel, S. Nyberg, K. Riles, Applied Optics, 44, 3937-44, (2005)

- **In real world**: temperature fluctuations /drift (refraction index) and vibrations affect distance measurement. **Single laser distance resolution degrades to 3-7μm.**

Dual-laser technique (Oxford, two independently chopped lasers, scanning over same frequency range in opposite directions) **restores precision to 0.2 μm**:



Si hybrid alignment system

- **The hybrid alignment system uses an IR laser beam traversing consecutive Si modules**

The beam serves as a reference with respect to which the modules get referenced. Remaining sensors are reconstructed using tracks in the overlap region. Subsequent track alignment reduces precision by 1 order of magnitude.

- **Based on successful experiences by AMS-I and CMS**
- **Sensor has to be slightly modified to allow transmission of the beam**
- **Si is almost transparent to IR light**. 200-300 μm of Si still yield a S/N~200 MIPs to IR light.

Advantages of this approach:

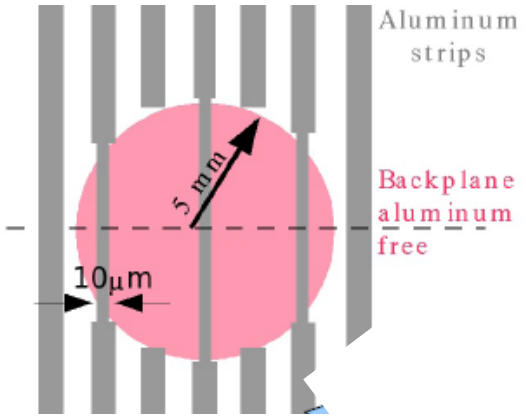
— **Minimum impact on system integration**

— **Straightforward DAQ integration ⇒ Alignment data is read out using Si DAQ**

— **Alignment system does not compromise tracker design: changes in geometry of the modules haveno impact in system precision**

Requirements of this approach:

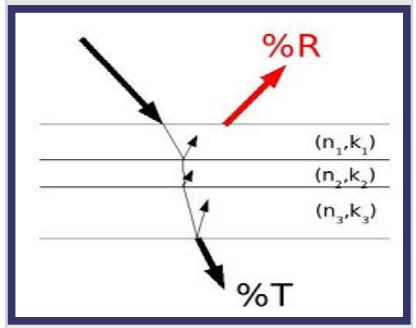
— Modifications of the sensor needed during production process. Removal of the **aluminum backelectrode locally** in the alignment window



Simulation of Si μ-strip sensors

- **Microstrip sensor simulated from an optical point of view**: study of the transmittance, reflectance and absorptance in the near IR.

The simulation includes: multiple reflections in all layers, absorption of the materials, dependence of refraction index on wavelength, deposition tolerances. Finally, the design is optimized around a specified wavelength.

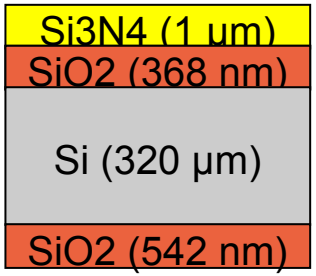


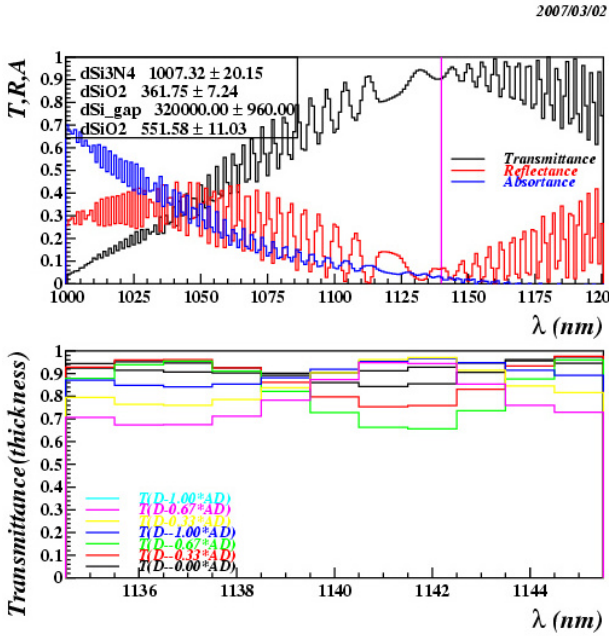
T+R+A = 1

- Aim is to achieve a transmittance as high as possible with moderate absorption (>30%)

Transmittance	90%	80%	70%	60%	50%	40%
# Sensors traversed	30	15	10	7	5	4

- Example: Typical DC sensor stack optimized for maximum transmittance at λ=1140 nm





Upper plot shows T,R,A for the sensor specified in the box. Calculated thicknesses ±tolerances are specified

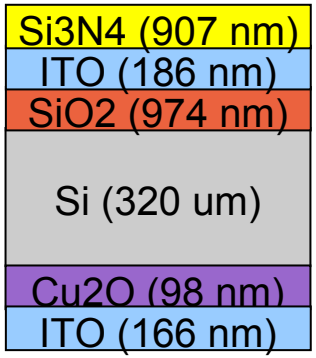
Bottom plot shows T in a narrow wavelength range, for thicknesses varied within tolerances

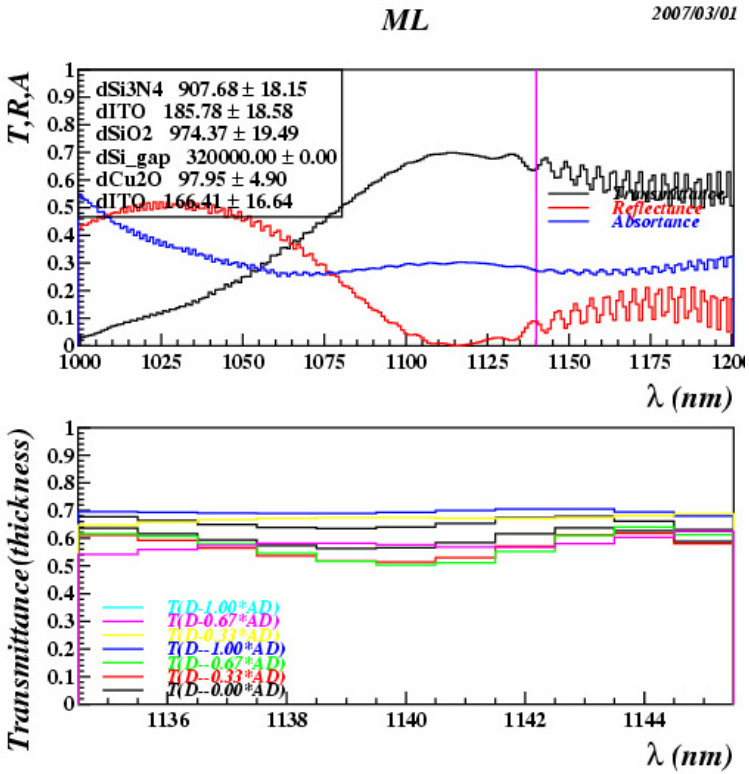
Note: Including the strips but neglecting diffraction effects produced by the “strip grating” the %T plot has to be rescaled by 0.8

(R & D with IMB-CNM)

• Collaboration of IFCA-Santander with IMB-CNM (IFAE)

• **Proposal to increase the transmittance of the Si sensor *substituting the Al by an IR transparent conductive oxide. Candidate: Indium Tin Oxide (ITO).***





• Another option we will rehearse, for a DC sensor, will be removal of the aluminum electrodes placed on top of the implant (across the alignment window). Charge can still be read with the implants. The performance is exactly the plot shown in the former transparency.

• Project with CNM has started. First prototypes will be built in June

· Prototype of 5 minimally modified sensors are being ordered to HPK

Alignment - comparison

Both approaches to the alignment system have complementary (when compared to each other and with respect to the track-based alignment) benefits and challenges.
SiLC is following the two approaches.

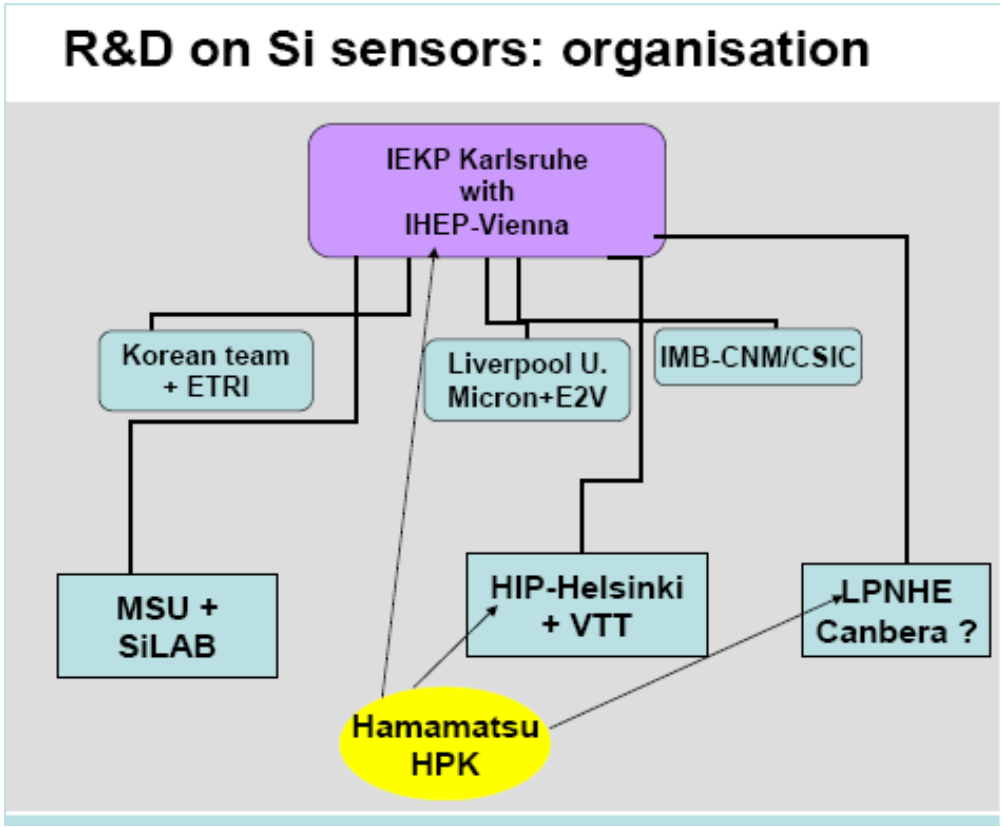
CHALLENGES:
- Both: Integration with the system
- The hybrid approach requires the development of sensors with optical properties.
- FSI relies on the mechanical transfer from retro-reflector position to active area.
- FSI is a more complex technique that requires its own DAQ system.

BENEFITS:
- Both: possiblity to resolve “fast” distortions
- FSI: measures arbitrary coordinates, constraints on “weak modes” of the track based alignment.
- hybrid: direct measurement of parameters that couple strongly to the sensor measurement.

SILC intends to test both on test beams in 2007 (1st HYBRID proto) and 2008 (FSI)

Sensors

Microelectronic Research Centers: CNM, ETRI, SILAB, VTT
Characterization Labs: CU Prague, HEPHY-Vienna, HIP-Helsinki, IEKP Karlsruhe, IFIC-Valencia, Korean Group, Liverpool, LPNHE-Paris
and close contact with industries: Hamamatsu, Micron, E2V, Korean firms, WIS-EDGETEK, Canberra, ...



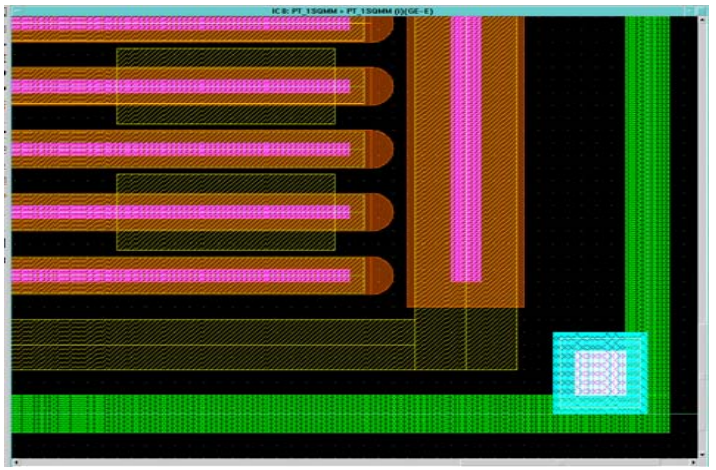
SiC Silicon µstrip Sensor Baseline

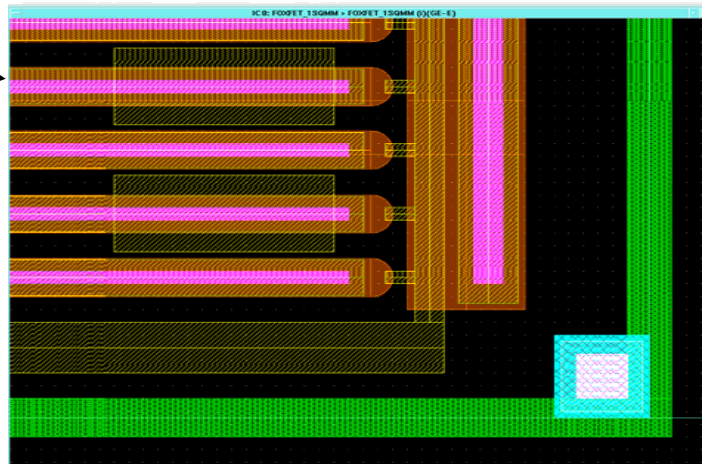
- **SiC sensor baseline**
  - FZ p-on-n sensors: n-bulk material, p+ implants for strips
  - high resistivity (5-10 kOhm cm)
  - Readout strip pitch of 50µm
    - Possibly intermediate strips in between (resulting 25µm pitch)
    - Smaller pitch becomes very complicated (Pitch adapter, bonding, charge sharing,…)
  - Thickness around 100-300µm
    - mostly limited by readout chip capabilities (S/N ratio)
  - **Low current:** <1nA per strip
    (Due to long integration time noise mostly defined by current and resistors)
- **Baseline for inner layers:**
  - 6” inch, Double sided, AC coupled
- **Baseline for outer layers:**
  - 8” (12”?) inch, Single sided, Preferably DC coupled(cheaper)

µstrip Sensor Baseline details:

Biasing Possibilities:

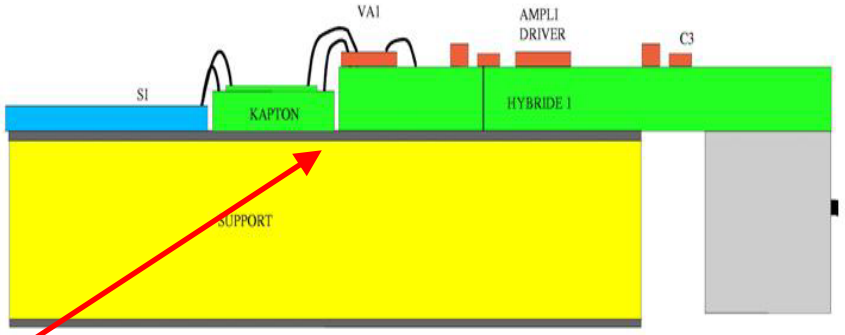
- bias resistor with **poly-silicon** (20 to 50 MOhm)
- **punch-through** (upper picture)
- or **FOXFET** biasing structure (lower picture)
  - Latter two have non-linear behaviour
  - But are cheaper



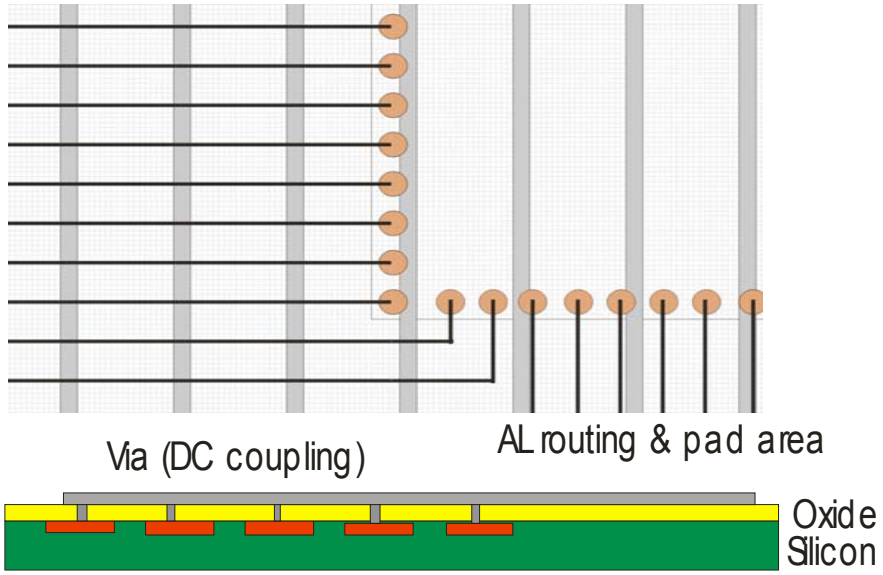


Minimize material budget

- Multiple scattering is crucial point for high-precision LC experiment
- Minimize multiple scattering by reduction of material budget
  - avoid old-fashioned way (pitch adapter, FE hybrid, readout chip)



- **Integrate pitch adapter into sensor**
  - Connectivity of strips to readout chip made by an additional oxide layer plus metal layer for signal routing
  - Readout chip bump-bonded to sensor like for pixels



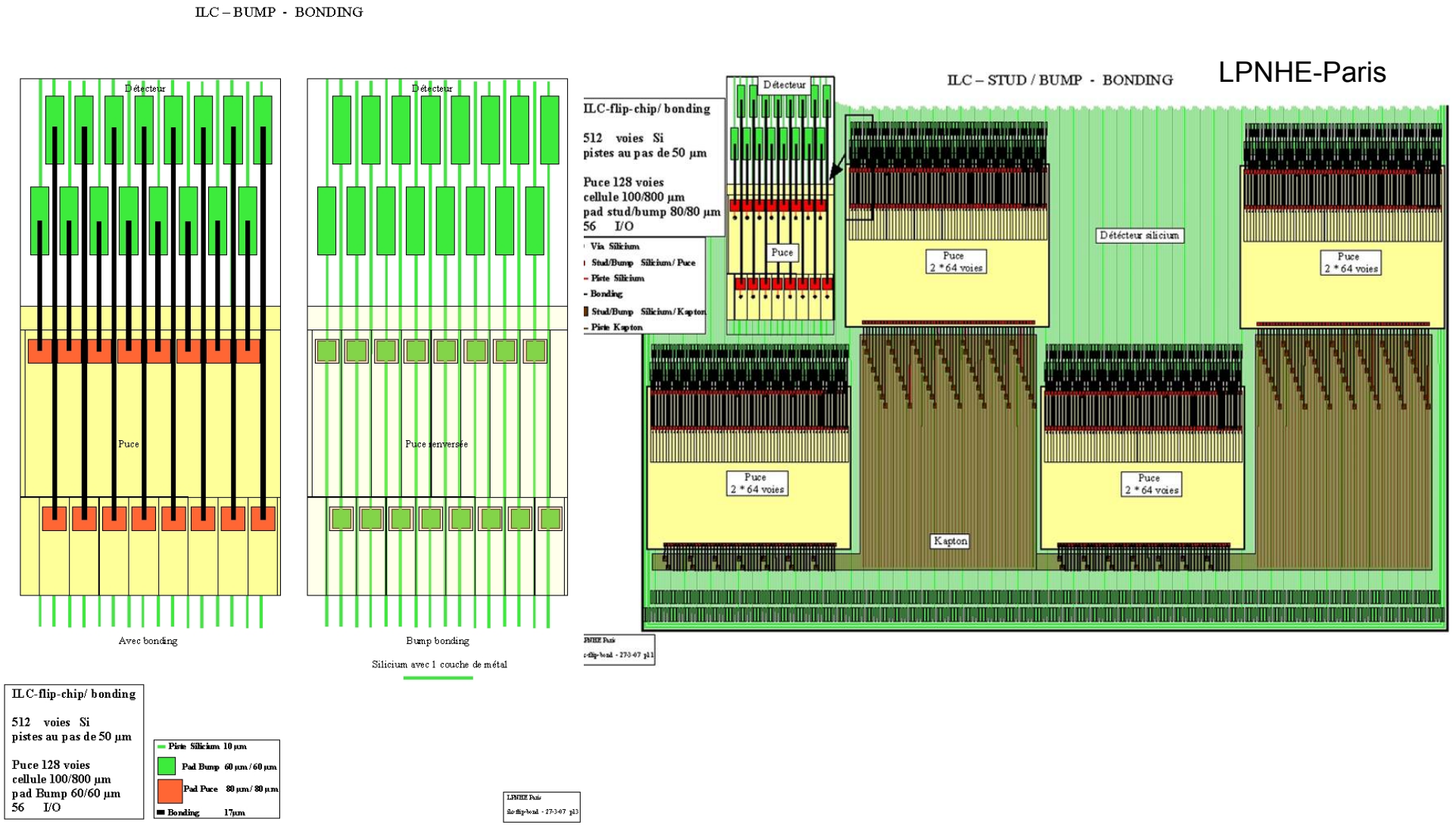
SiIC work program for sensor R&D

- Step 1 (2007)
  - Wafer thinning (100, 200, 300µm)
  - Use long strips (50 µm pitch)
  - Test new readout chips (DC coupling, power cycling)
  - Improve standardized test structures and test setups
- Step 2a (2008-)
  - Move from pitch adapter to in-sensor-routing
  - Test crosstalk, capacitive load of those sensors
- Step 2b (2008-)
  - Test 6” double sided sensors
- Step 2c (2008-)
  - 8” (12”) single sided DC wafer

Step 1 and 2a:

- Bump-bondable 128-channel chip available end 2007
- HPK agreed to provide a sensor design
- SiLC adapts strip to pad area
- HPK will process the sensor
- SiLC (Paris) provides chip
- HPK could bump bond chip to sensor
  - HPK is very interested to strengthen inhouse bumpbonding
    - In Bump
    - Flipchip
  - Stud-bonding (J. David, J.F Genat, F.Rossel)
- Testing begins 2008

“Inline pitch adapter” for SiLC UMC Chip



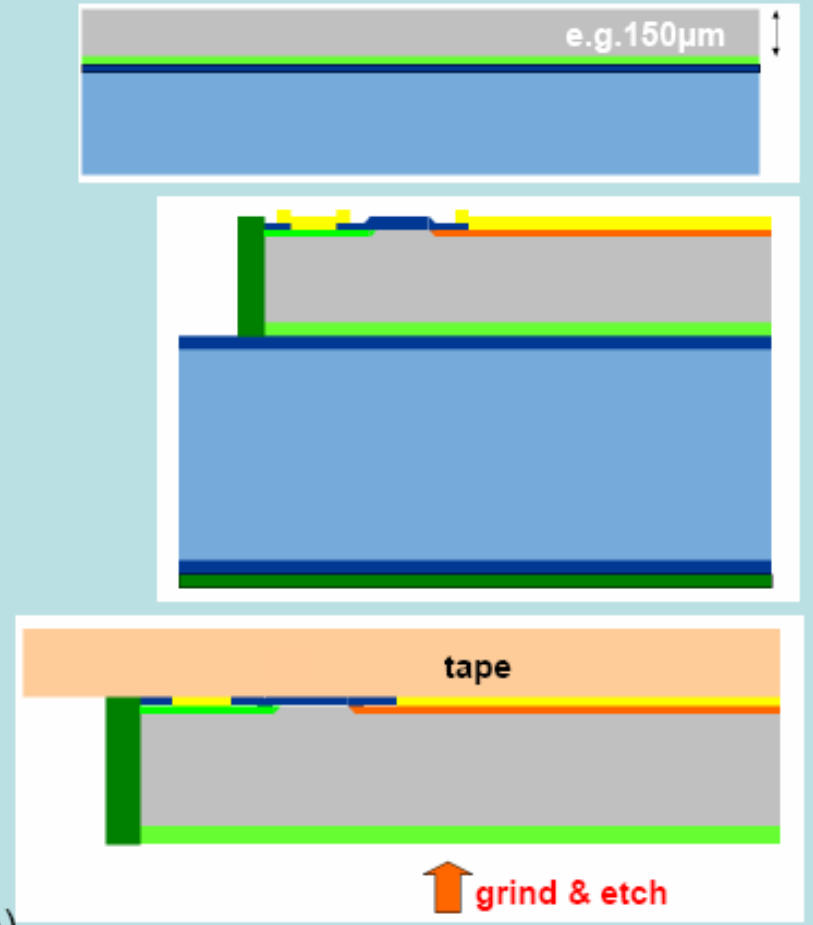
HPK

- Meeting with HPK's European Sales representant and Japanese engineer at VCI
- Several questions which have been answered by them (later by e-mail):
  - **Double sided processing (6")?** Not possible
  - **Cost difference AC-DC coupling**: AC is 40-50% more expensive
  - **Cost difference biasing (DC=100):** PT: 115; FOXFET : 120; Poly-Si : 130
  - **Minimal sensor thickness?** 200 micron (possible in 1 year from now)
  - **Maximum dielectric layer?** 1μm with SiO_2, maybe Polyimide in the future
  - **Trace metallization:** only Al with 0.9 μm thickness and minimum width of 3 to 4 μm; no other material for the time being (we asked for Copper)
  - **Larger Sensors:** 8-12" production possible via sub-contractor, but much more expensive; limited prototyping
  - **bump bonding:** Indium bump-bonding being developed within 1 year, 20 μm pitch
- HPK asked for an offer for 30 pcs SSD detectors with 50μm pitch

HPK proposal: Chip size of 95 x 95 mm
Thickness : 320 um
Strip : 50 um pitch (with one intermediate strip)
SSD type : single-sided DC type

Novel proposal: Edgeless Thin Detector

- Edgless Microstrip Thin Detector (VTT)
  - Starting point: two wafers bonded,
    - one is thinned, acting as sensor
    - the second is only a support structure, released at the end of the fabrication
  - Using DRIE, trenches are made, filled with doped poly
  - Detectors are diced with DRIE again.
  - Finally they are bonded to tape and the support wafer released.
  - End of the process: thin detector
    - Electrically connected without the need of using wire bonding;
    - Backside contact is made from the front through doped poly (dark green in the figure).

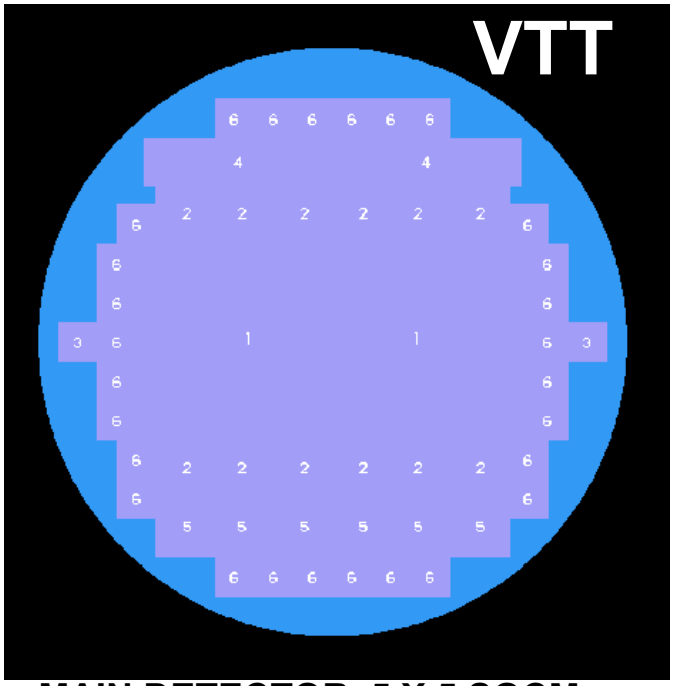


- Active edge (dead space≈20 µm) achieved through deep silicon etching & n-type poly fill
- Dicing: the chips are diced using deep Si-ething released from the support substrate

1st prototypes by July '07

At December SiLC Meeting HEPHY&VTT started to collaborate for mask design

- Design almost ready
  - Two main sensors on wafer
    - One sensor DC coupled
    - Other AC coupled with PT or FOXFET bias because of lack of polySi processing line
  - Vienna provided CMS-like ‘half-moon’ TS
- Now design verification
- Begin of processing soon



1. **MAIN DETECTOR, 5 X 5 SQCM**
2. *MEDIPIX2, 1.5 X 1.5 SQCM*
3. ALIGNMENT MARKS, 1 X 1 SQCM
4. **HALF MOON TEST STRUCTURE**
5. EDGELESS TEST STRUCTURES, 1.5 X 1.5 SQCM
6. BABY DETECTORS, 1 X 1 SQCM

Interest of 3D technology for:

(S)LHC = 3D pixels (in priority)

ILC: deep Silicon etching and via filling technologies are being applied for developing the next generation of µstrip sensors (3D planar tech) and the next step for FE detector embedded.

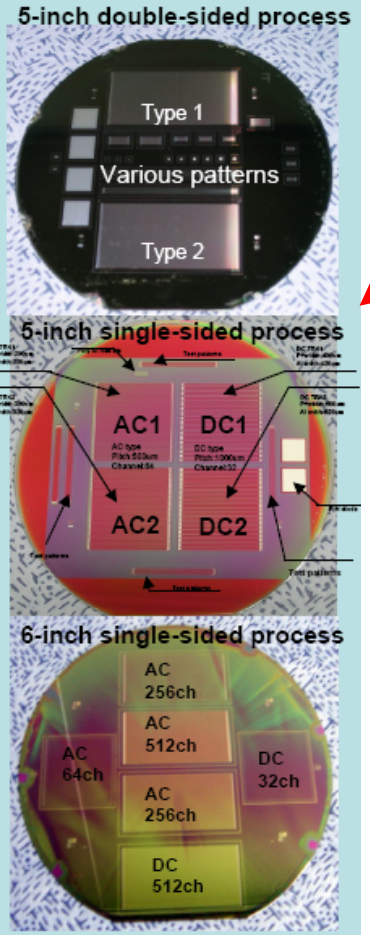
Latest R&D developments

- yield

type	DC-type	AC-type
single-sided	90%	80%
double-sided	< 30%	N/A

- fabrication line

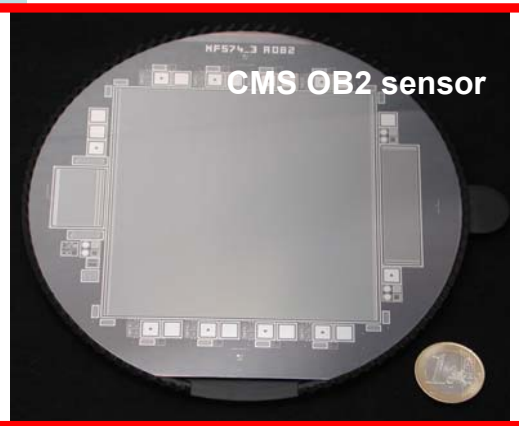
line	DC-type	AC-type
5 inch	double/single-sided	single-sided
6 inch	single-sided	single-sided (in progress)
8 inch	**thickness (725 um, can be thinned ~500 um)**	



SENSOR R&D in KOREA

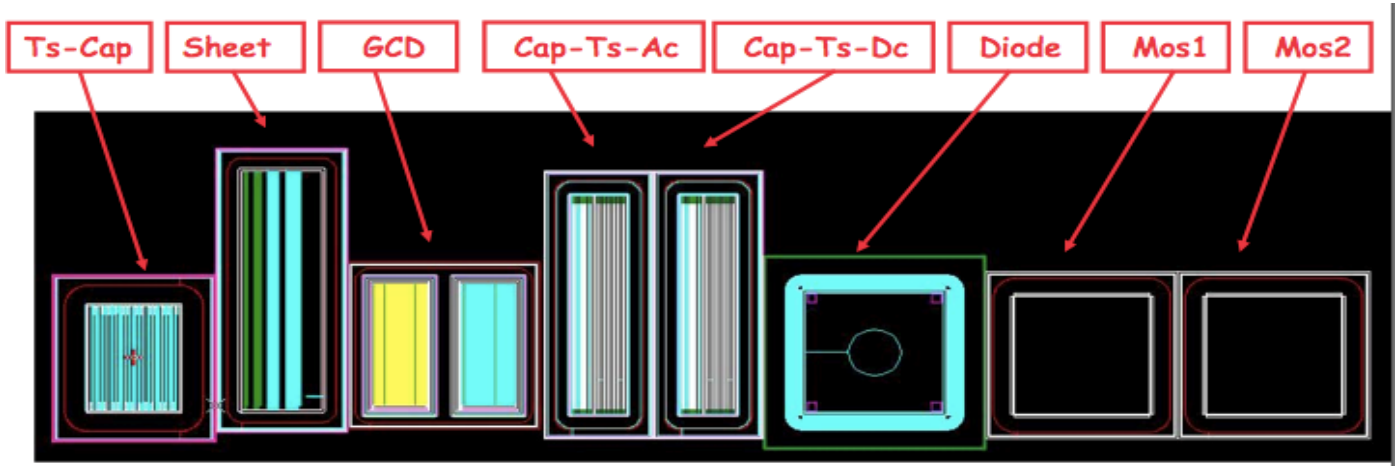
Launched collab Korea+HEPHY in Dec 2006

- Maximize size per wafer in a single sensor (approx. 10 x 10 cm^2), following SiLC 1st baseline.
- HEPHY provide a modified CMS design (with TS) for full 6” wafer (timescale: several months)
- Start in April 2007 (new financial year in Korea)



IET Warsaw

- Frank Hartmann established contact with *Institute for Electron Technology* (Jacek Marczewski) already three years ago
- Karlsruhe and Vienna are both in loose contact with them to develop test structures
  - Based on CMS ‘half-moon’
- They have experience with SOI and chip production, but not with fully depleted devices yet.
- Production of first batch has just started



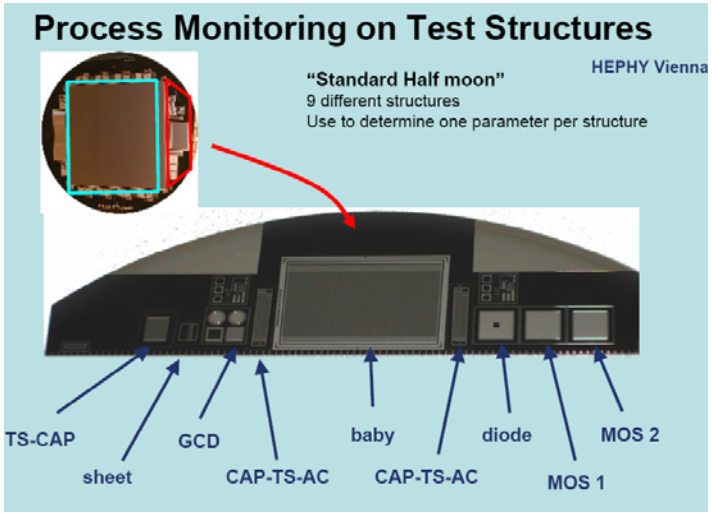
SiLC Present Status on sensors

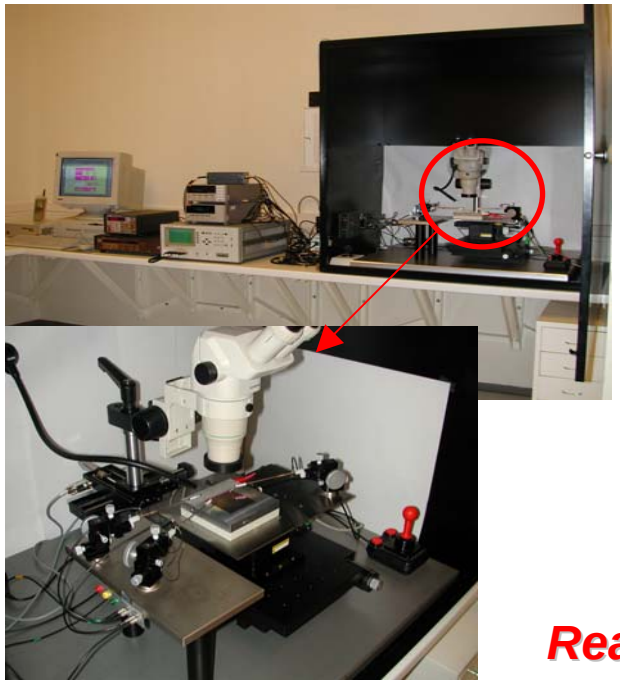
- Sensor baseline established:
  - FZ, p-on-n, high resistivity, 100-300um thick, 50um pitch
  - preferably DC coupled, otherwise biasing via PolySi, PT or FOXFET

- Discussion with several companies / institutes ongoing
  - VTT: design almost finished
  - Korea: 1st design has to come from us within next weeks
  - IET Warsaw: TS already in production
  - Canberra: Double sided 6'' available, have to be recontacted
  - ON Semiconductors: 1st visit next month?

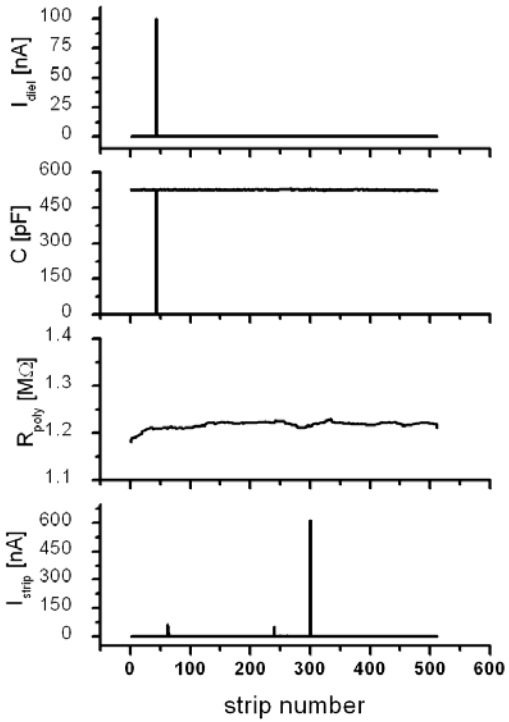
Silicon sensor expertise within SiLC

- Both, *Vienna* and *Karlsruhe* worked a long time already with silicon sensors
  - **DELPHI @ LEP**
  - **CDF @ Fermilab**
  - **CMS @ LHC**
- Experience in
  - Strip-by-strip characterization of Si strip sensor
  - Process monitoring with test structures
  - Proton irradiation facility in Karlsruhe



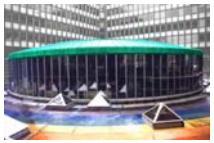


- **Global parameters:**
  - **IV-Curve:** Dark current, Breakthrough
  - **CV-Curve:** Depletion V, Total C.
- **Strip Parameters e.g.**
  - strip leakage current I_{strip}
  - poly-silicon resistor R_{poly}
  - coupling capacitance C_{ac}
  - dielectric current I_{diel}



Real asset for our R&D collaboration

130nm Digital Sampler chip: New results



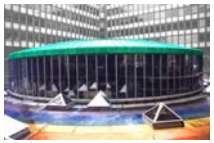
LPNHE-PARIS

FRONT-END GOALS

	This chip
•Full readout chain integration in a single chip	yes
Preamp-shaper	yes
Trigger decision (analog sums)	yes
Pulse Sampling: Analog pipe-lines	yes
On-chip digitization: ADC	yes
Buffering and pre-processing: Centroids, Least square fits,	no
Lossless compression and error codes	no
Calibration and calibration management	no
Power switching (ILC timing)	no

CMOS 130nm	2006	yes
CMOS 90nm	2007	no
512-1024 channels envisaged		4 channels

J.F.Genat 2, D. Fougeron 1, R. Hermel 1, H. Lebbolo 2, **T.H. Pham 2**, R. Sefri, 2, A. Savoy-Navarro 2 (*1 LAPP Annecy, 2 LPNHE Paris)*



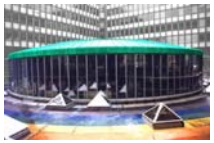
FRONT-END IN 130nm

130nm CMOS:

- Smaller
- Faster
- More radiation tolerant
- Lower power
- Will be (is) dominant in industry

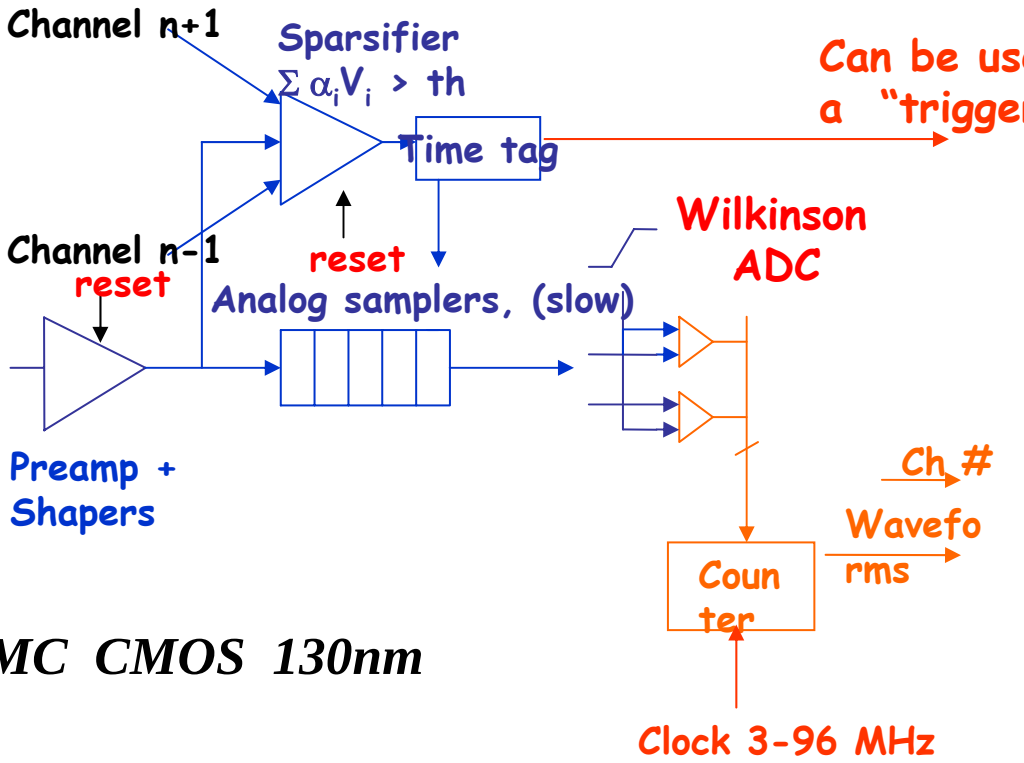
Drawbacks:

- Reduced voltage swing (Electric field constant)
- Leaks (gate/subthreshold channel)
- Models more complex, not always up to date
- Crosstalk (digital-analog) to be cautious with.



LPNHE-PARIS

FRONT-END IN 130nm

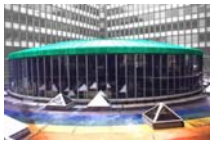


UMC CMOS 130nm

TARGETED

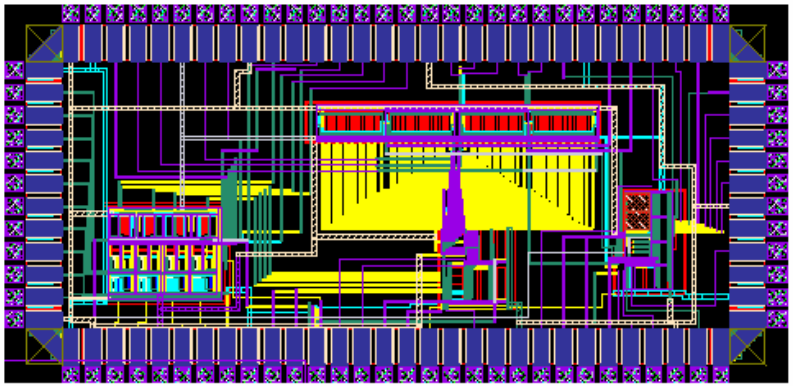
Amplifier/Shaper : 20 mV/MIP
Sparsifier: threshold on analog sum
Sampler : 16-deep
ADC : 10-bit

Noise measured with 180nm
CMOS : 375 + 10.5 e-/pF@3 μs shaping, 120μA (preamp + shaper)

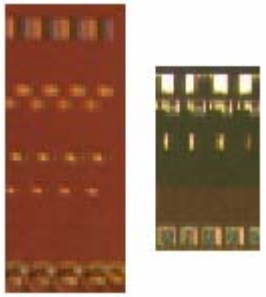


LPNHE-PARIS

SILICON

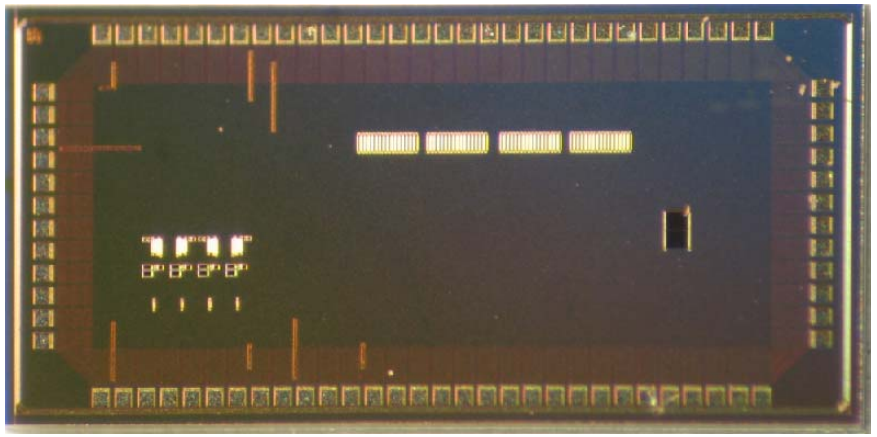


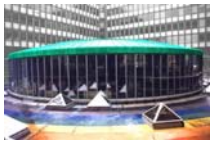
Layout of the 130nm chip including sampling and A/D conversion



180nm 130nm

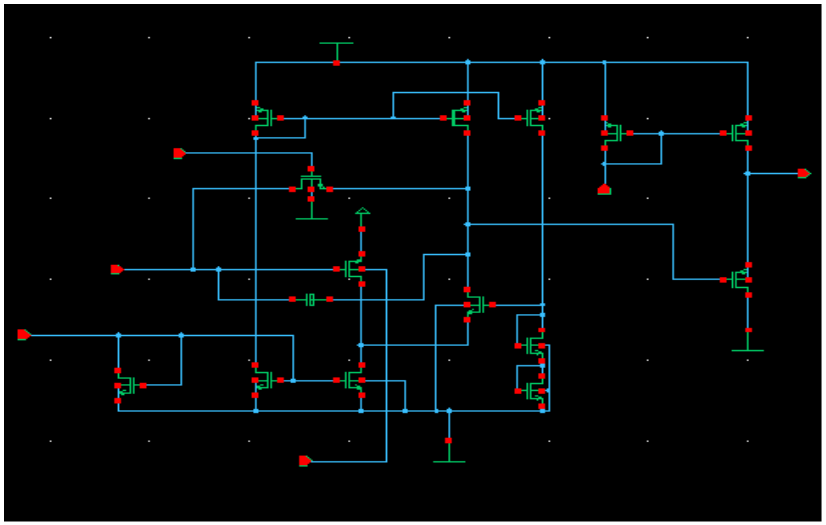
Picture





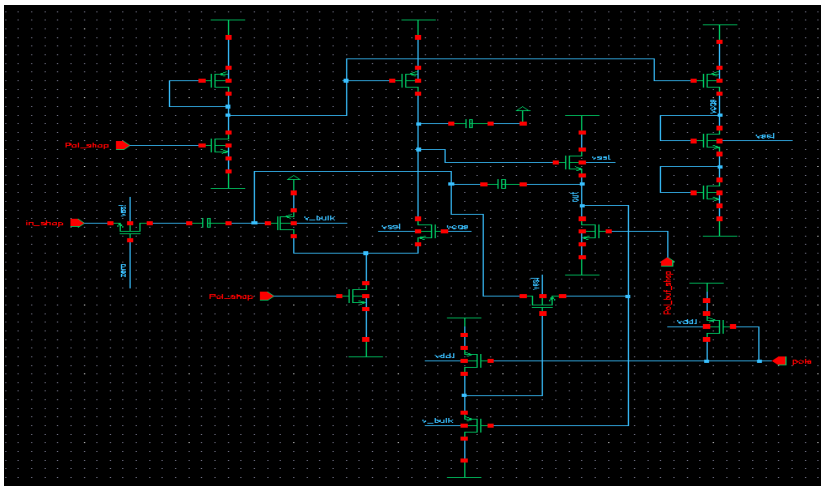
PREAMPLIFIER

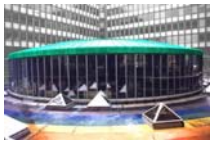
Gain: 28.5mV/MIP
3.3V Input transistor:1.5mm/0.5µm
gm = 1.5 mS/ ~70 µA
Feedback capacitance = 133 fF
Dynamic : 25 MIPs
(linearityy = 1% at 25MIPs)
Noise@70 µA = 1000e$^-$ + 25e-/pF



SHAPER

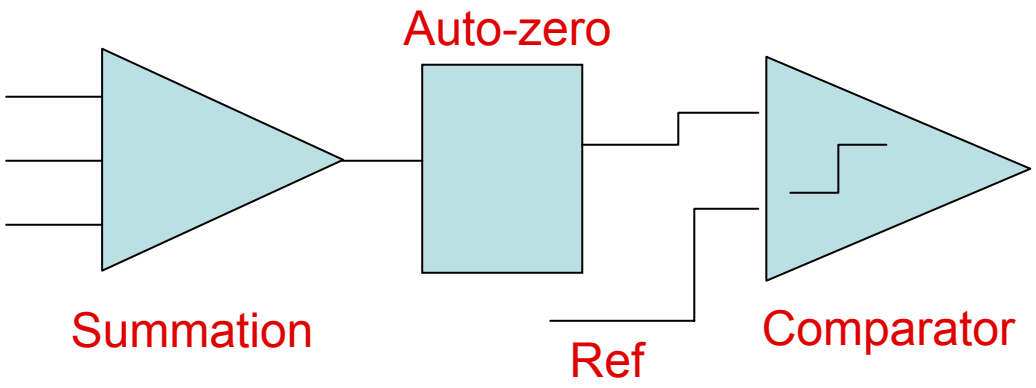
RC-CR Filter
Adjustable shapping time:0.7µs -> 3µs
noise@700ns = 335+22e$^-$/pF
noise@3µs = 305+16e-/pF
Dynamic : 20 MIPS





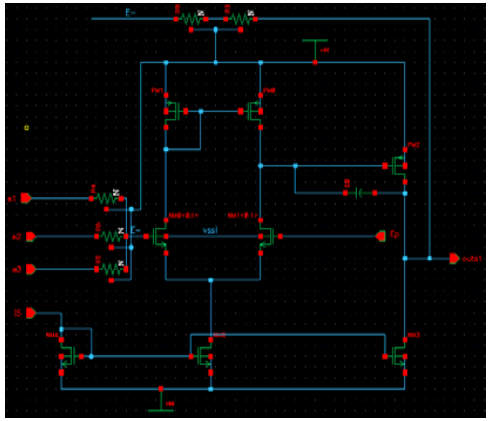
LPNHE-PARIS

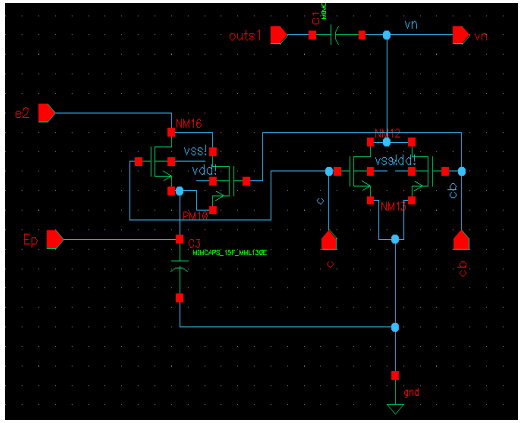
SPARSIFIER READOUT

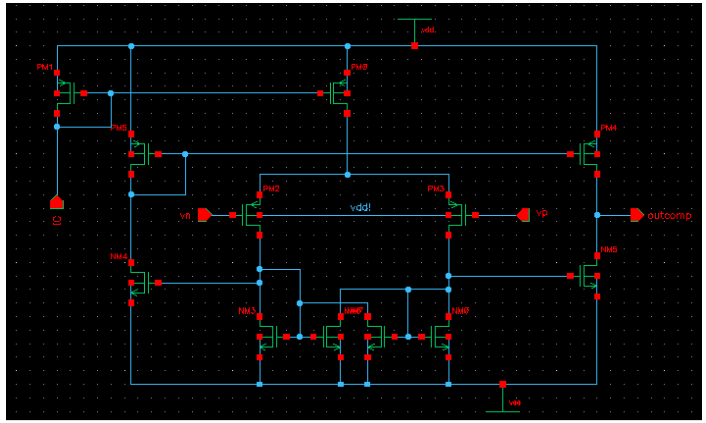


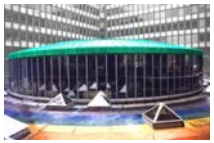
+ Resolution ~ 0.1mV

+ Response time = 186ns









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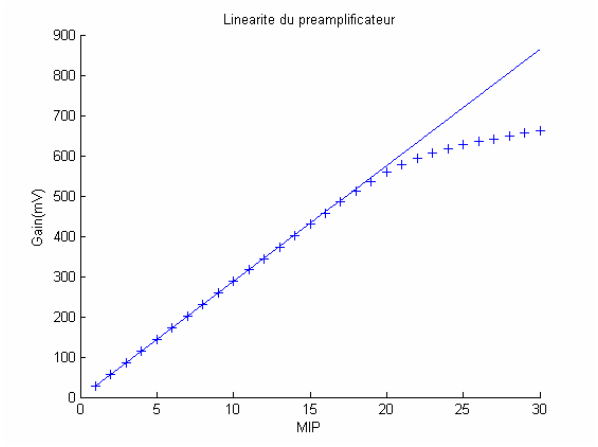
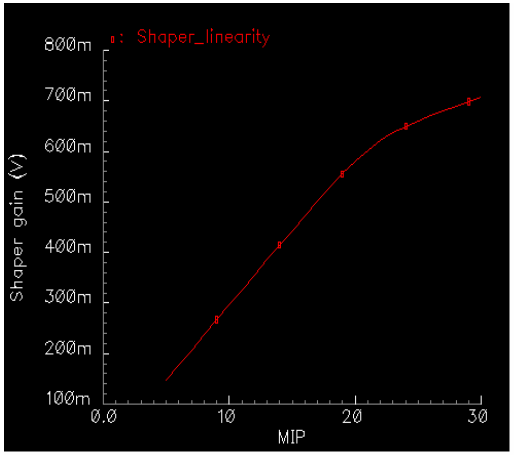
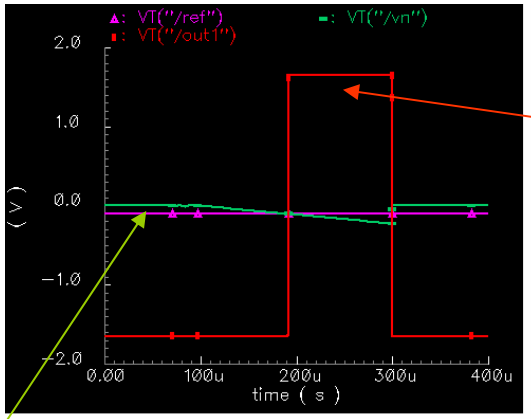
SIMULATIONS: LINEARITIES



Linearity of preamplifier



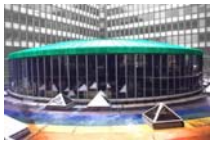
Linearity of shaper



Read channel

Summation response

Sparse readout



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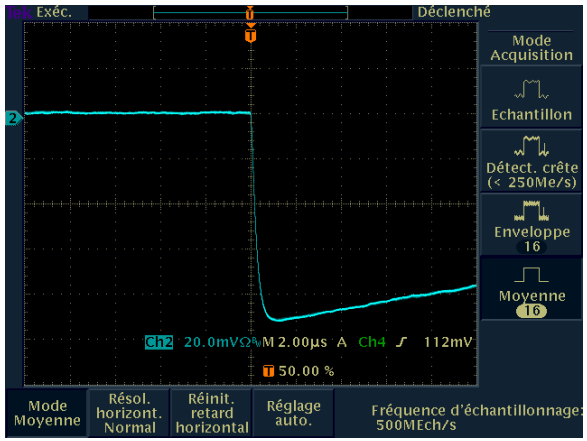
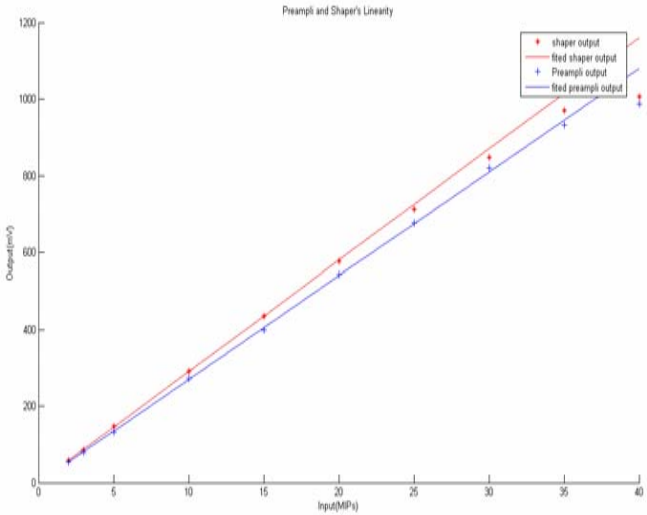
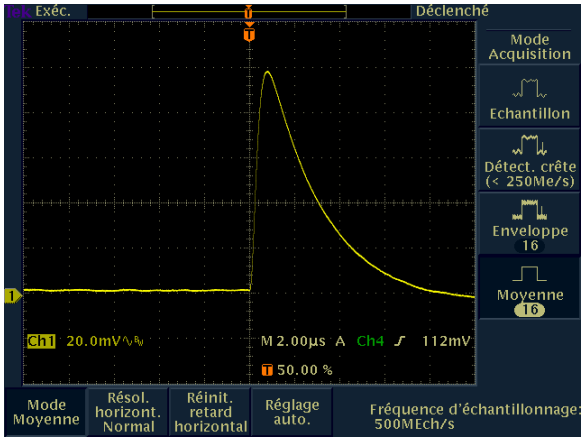
MESURES: GAIN – LINEARITY

Preamplifier's output







Shaper's output

Preamplifier :

Gain = 27mV/MIP

Dynamic = 25MIPs (<1%)

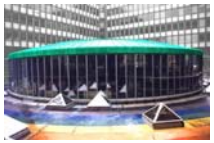
= 30MIPs(<5%)

Shaper :

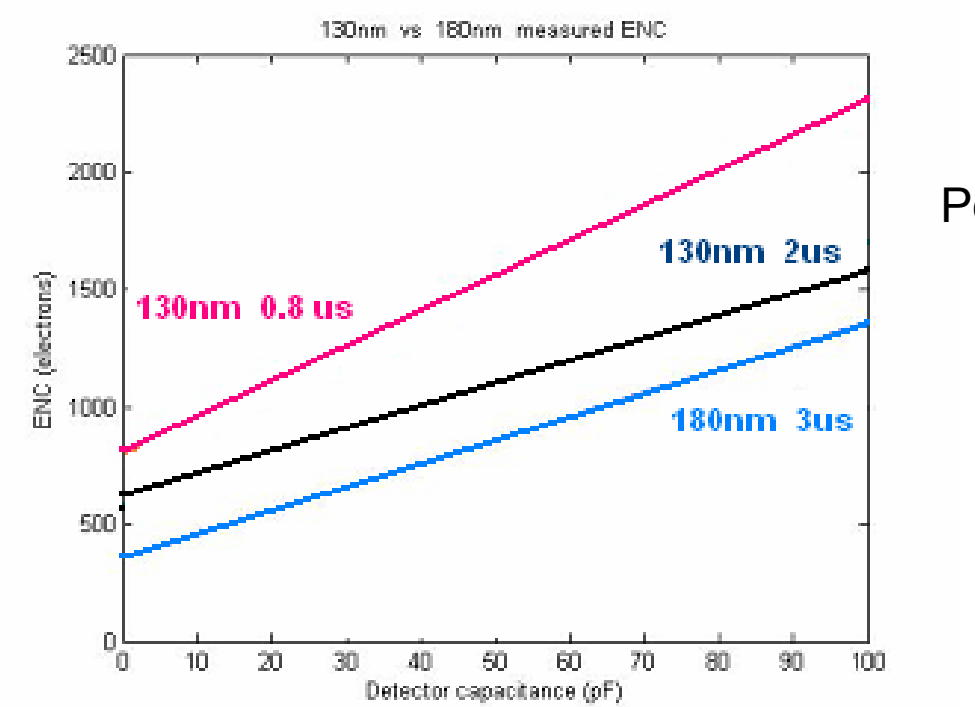
Gain = 29mV/MIP

Dynamic = 20MIPs(<1%)

= 30MIPs(<5%)



NOISE RESULTS



Power (Preamp+ Shaper) = 290 **m**W

Noise:	130nm @ 0.8 **ms** :	850 + 14	e-/pF	
	130nm @ 2 **ms** :	625 + 9	e-/pF	625*sqrt(2/3 **ms**)=510 **e-/pF**
	180nm @ 3 **ms** :	375 + 10.5	e-/pF	

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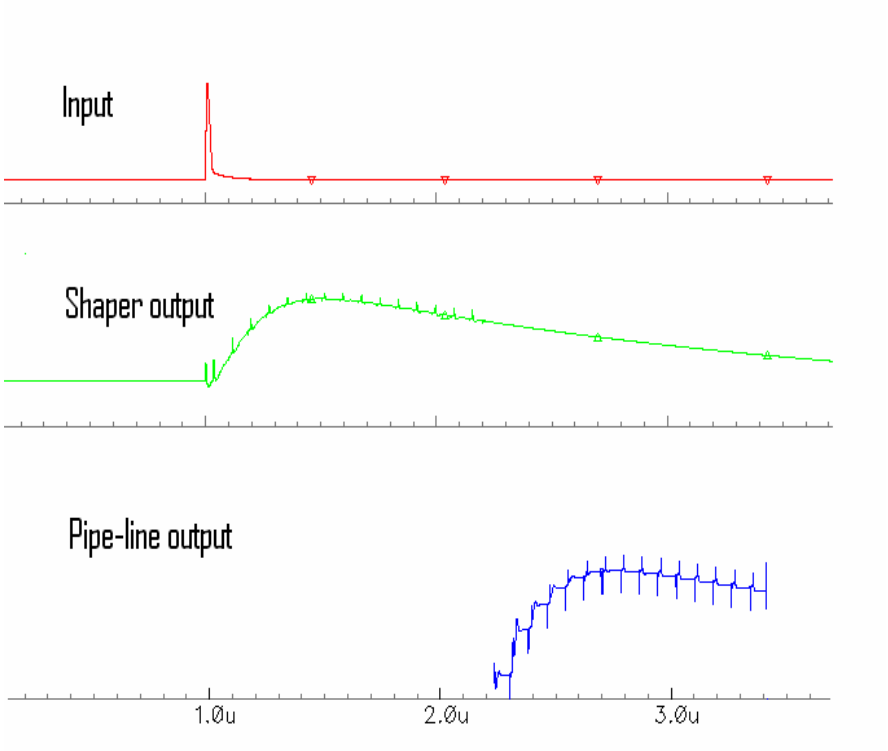
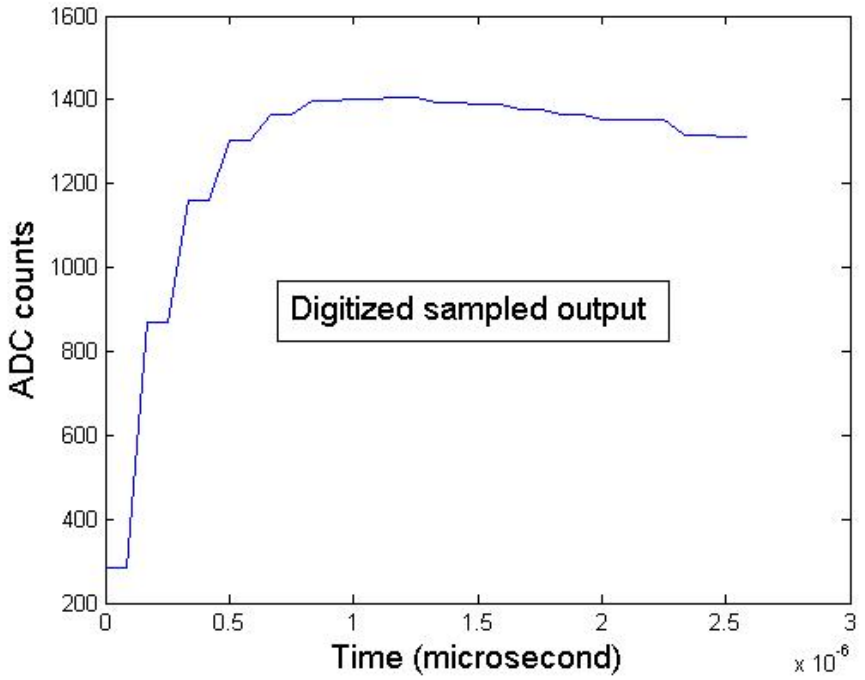
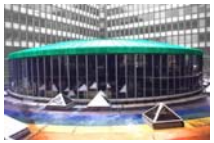
ANALOG PIPELINE OUTPUT



Simulation of the analog pipeline



Measured output of the ADC



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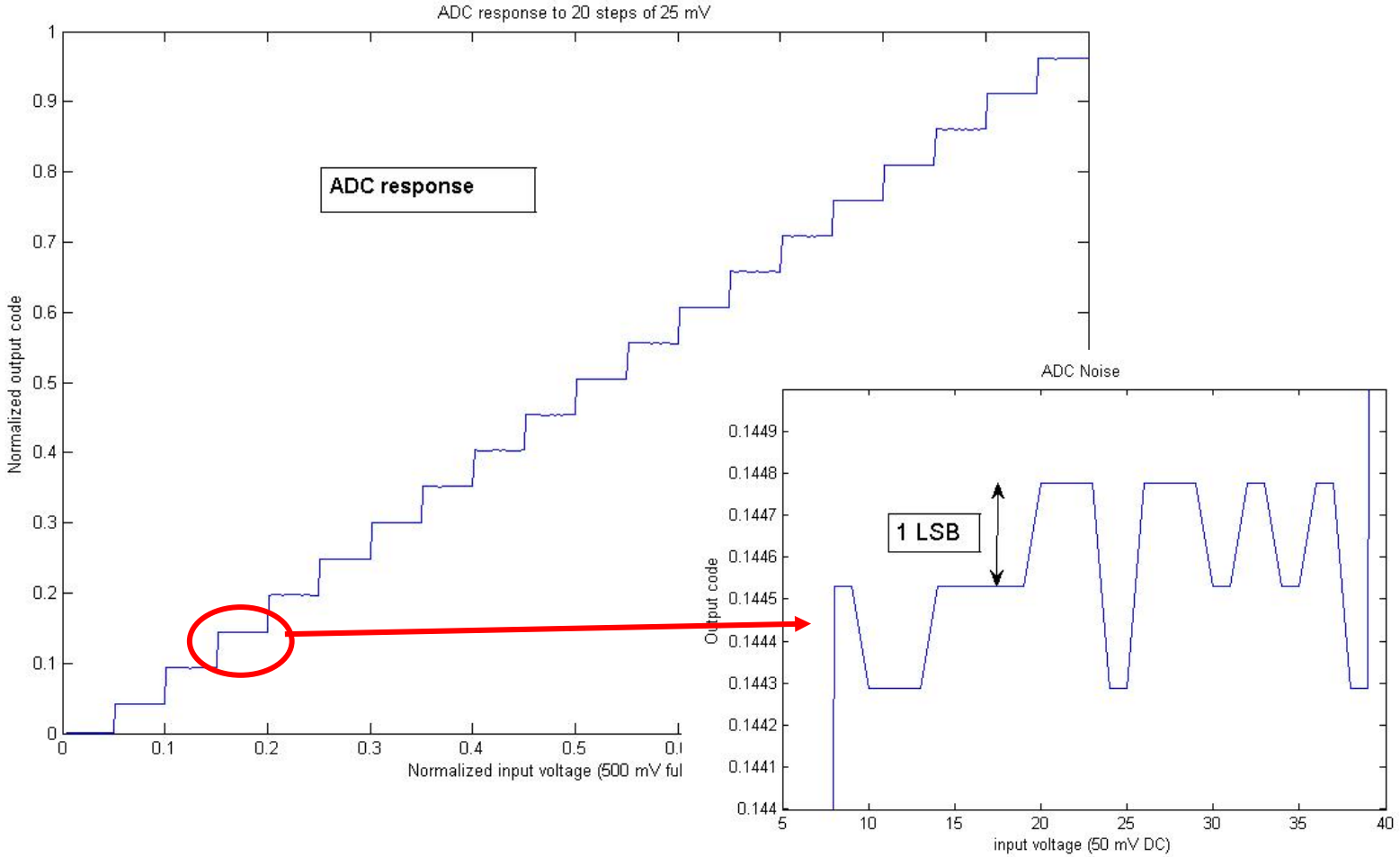
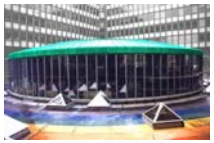
ADC





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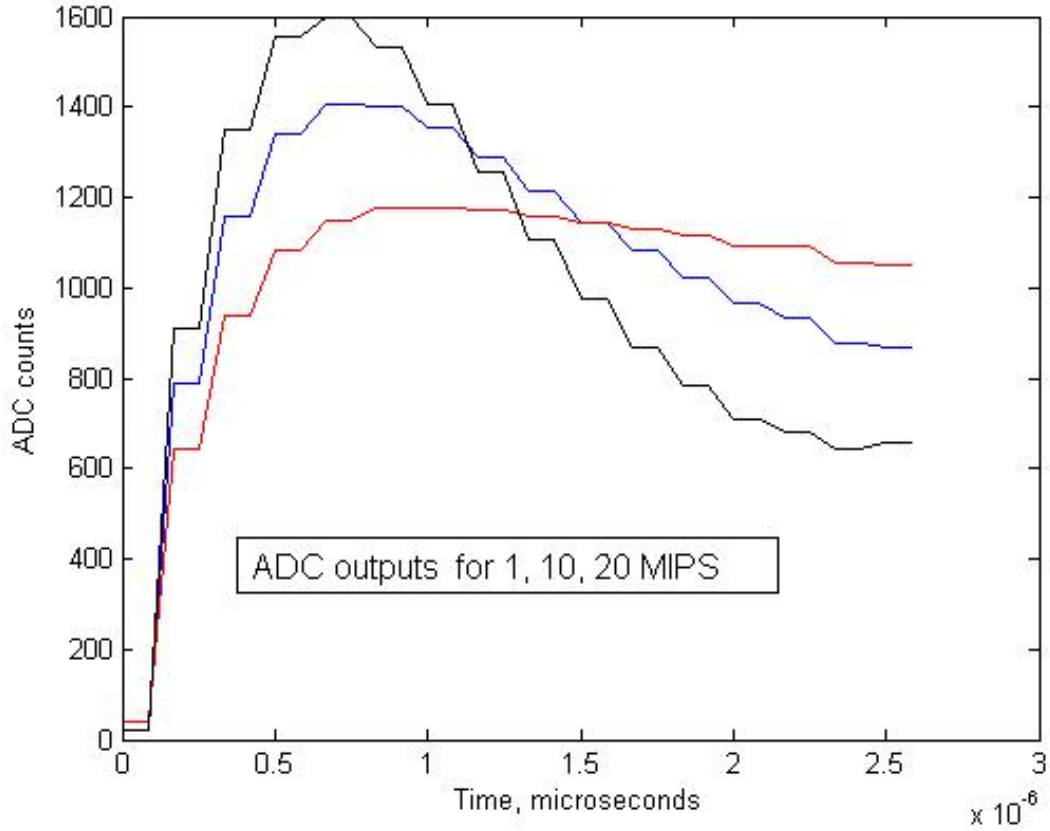
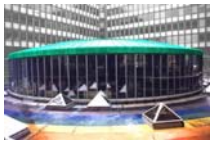
Sampler + ADC



Waveform biased by the output pad parasitic capacitance (~ 1pF)
Chip130-2 under tests: buffer between sampler and ADC



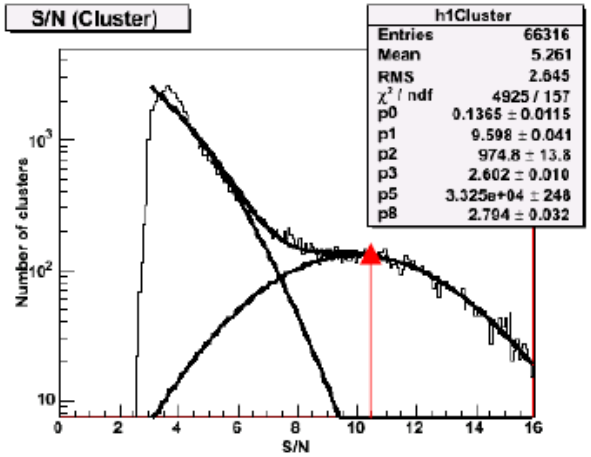
LPNHE-PARIS

130-1 NEXT TESTS

Measure ADC extensively

- Linearities integral, differential
- Noise fixed pattern, random
- Speed maximum clock rate

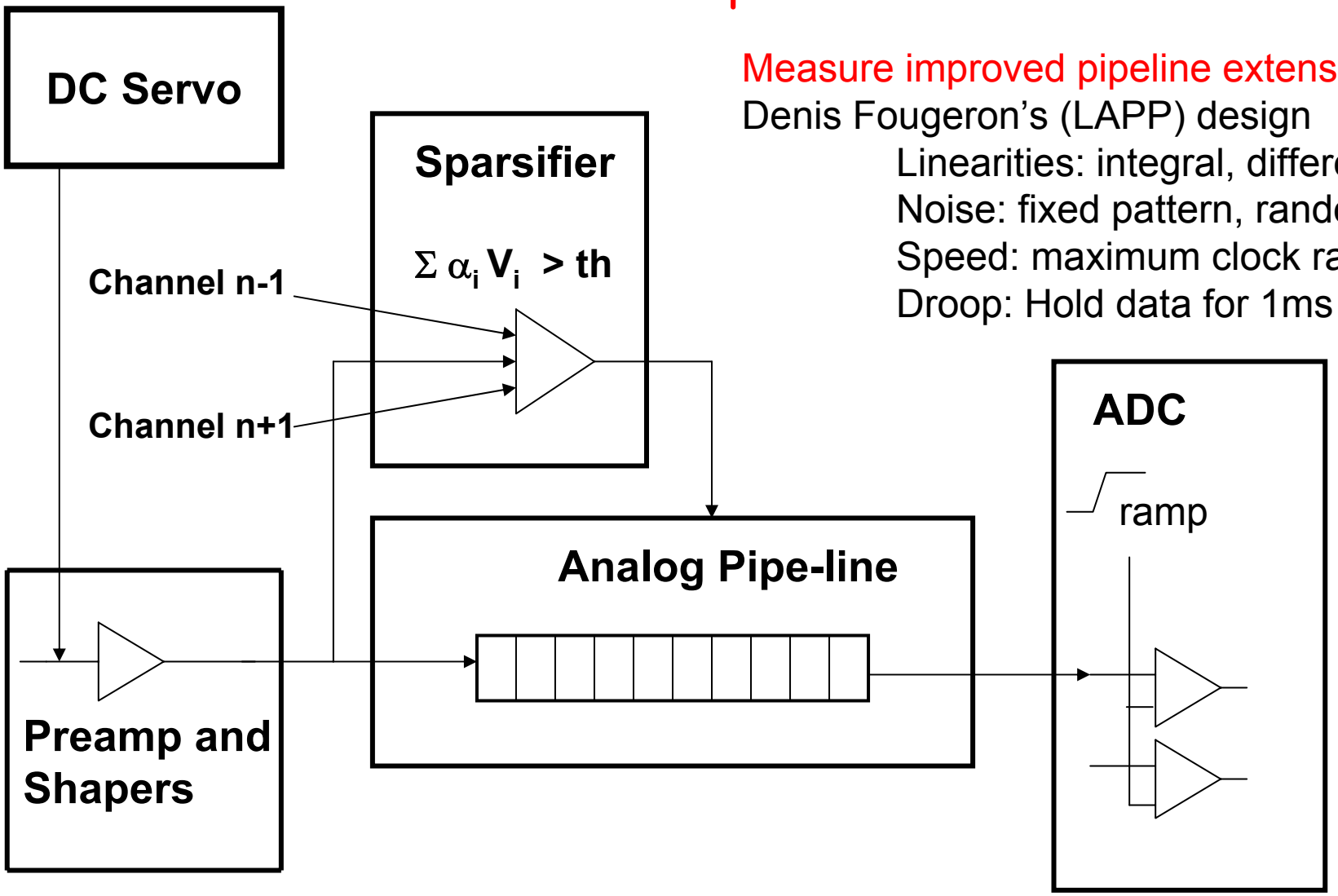
Effective number of bits (ENOB)



First tests with a detector and radioactive Source with 180nm prototype chip as FE, at Lab test bench
Now being tested at DESY in June as well as the new 130nm chip.

Therefore FULL characterization

130nm Chip 2



Measure improved pipeline extensively

Denis Fougeron's (LAPP) design

- Linearities: integral, differential
- Noise: fixed pattern, random
- Speed: maximum clock rate
- Droop: Hold data for 1ms at ILC

Next chip

Equip a detector, thus first "large" production

- Lab test bench and 2007 beam-tests
- 130nm chips 1 + 2 128 channels

  - Preamp-shapers + sparsifier
  - Pipeline
  - ADC
  - Digital
  - Calibration
  - Power cycling

TESTS of Detector prototypes

- Lab test bench
- Beam tests in preparation

➢ 2007:

June 3-15 at DESY (ladders + new FE chips)

October 10-23 at H6-SPSCERN (proto with new HPK sensors, new 130 nm chips, cooling + alignment protos)

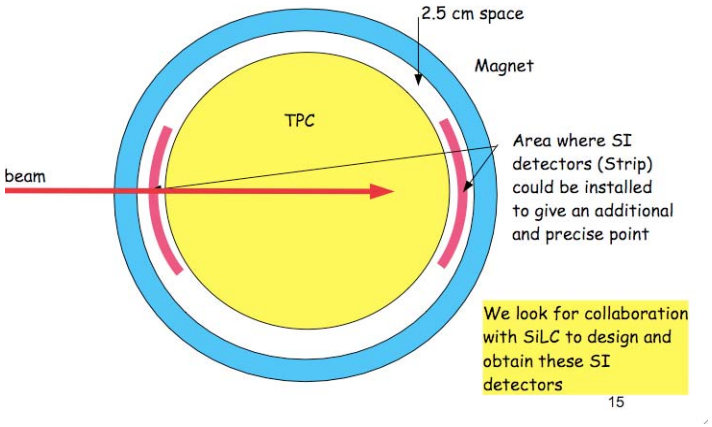
End of year: first try with TPC test beam at DESY

➢ 2008:

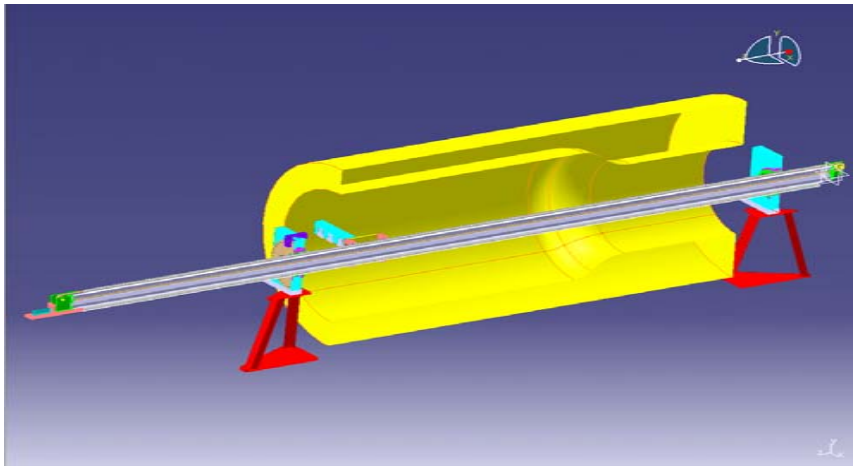
Move to FNAL

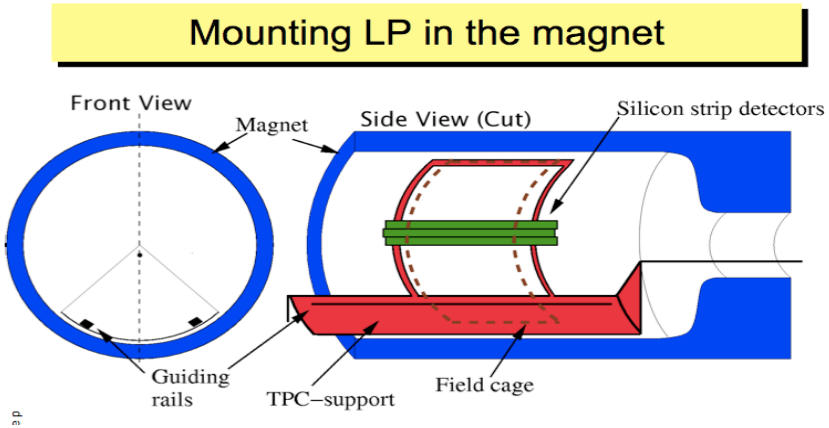
Prototype fully equipped with 130nm-126ch chips

Silicon Envelope test with TPC

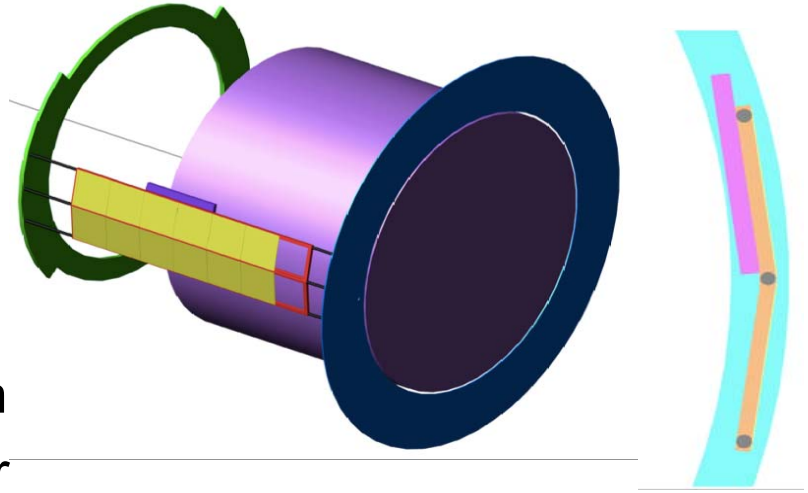


- **Magnet already at DESY**
- **TPC Support structure movable; Si modules should be mounted onto this structure**
- **Timescale:**
  - Construction of TPC Field Cage until autumn 2007 by commercial company
  - First beam test until end of the year



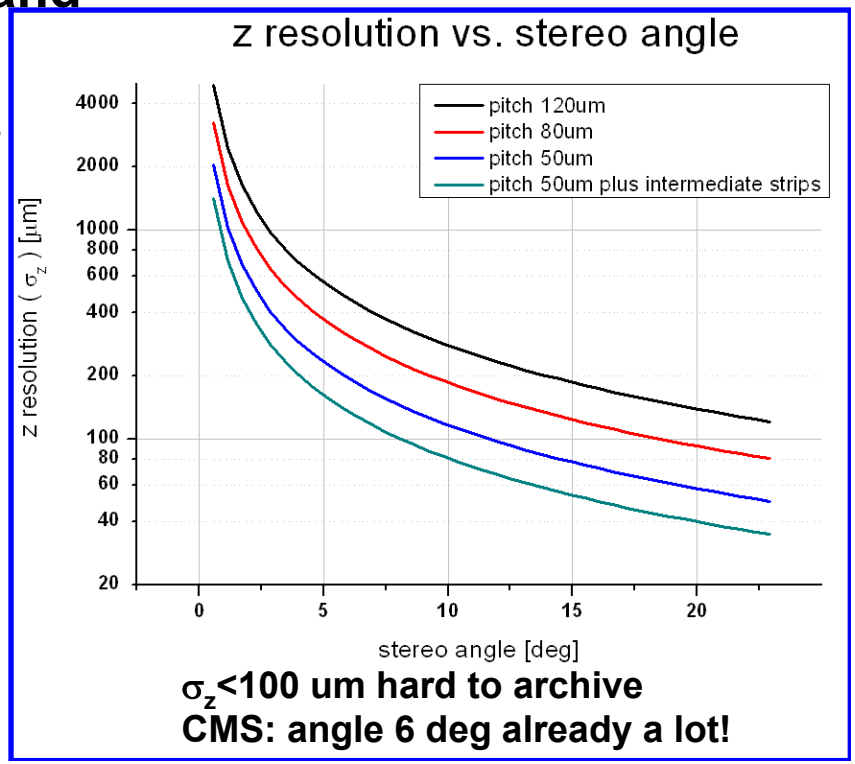


- **Long ladder in z Direction**
- **Stereo modules with two sensors**
- **Resolution requirements still unclear:**
  - R-Phi: 10-50 µm
  - Z: 50-250 µm
- **Stereo angle responsible for z resolution**
  - Optimal z resolution when stereo sensor perpendicular to R-phi sensor
- **Crucial Point: Space between magnet and TPC: 2cm**
  - Large stereo angle needs more space
  - Sensors perpendicular?



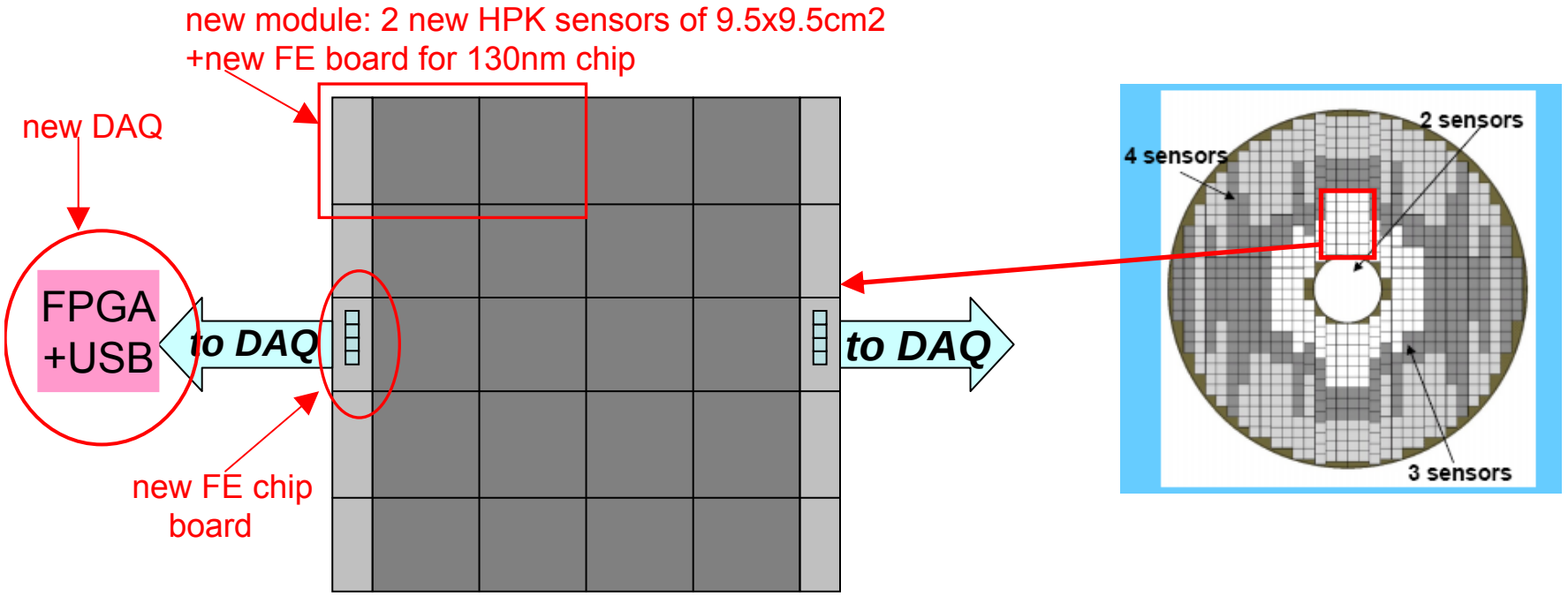
r-Phi pitch [um]	resolution sigma [um]
120	35
80	23
50	14
50*	10

* with intermediate strips



σ_z<100 um hard to archive
CMS: angle 6 deg already a lot!

New prototype for CERN test beam Octobre 2007



Equipped with new sensors from HPK, and the first prototyped FE chip in 130nm just a few channels + VA1 for reference
Will be installed in H6 beam at SPS-CERN (Oct 10-23, 2007)
Plus 3 ladders also under fabrication for the DESY test beam in June 3-15, with the same readout but.They will be used as part of the beam telescope.
Combined test with calo?

Synergies with (S)LHC

From F. Hartmann's Talk in "CMS Sensor upgrade Workshop" (Feb, CERN) revised & completed (ASN)

piece	development	reason & realization ILC	reason & realization SLHC	synergy	problems
sensors					
	8"	large area	large area	YES	
	3D	has specific applications	radiation hardness	YES	no industry standard
	MCz	not neeed	radiation hardness	NO	
	Thinning	multiple scattering	Vdep;power, multiple scattering, no need for thick cause CCE degradation	YES	Signal
	n-in-p, n-in-n	not needed	Depletion after SCI starts from top	NO	
	double sided	save MB	not applicable, radiation damage	NO	Not a real issue for ILC (small areas only)
	Strixel sensor	Perhaps interesting for innermost layers (occupancy)	Occupancy	NO ??	To be discussed
	DC	chip must cope with switch off and GND on strip	current too high	NO ??	To be studied even for ILC
	edgeless sensors with 3D for edges	no need for overlap => large area	high voltage stability	YES	no industry standard
electronics/ chip					
	small feature size 90/130/180nm	low power consumption	low power consumption	YES	
	radiation	no issue; standard libs	special libs needed	NO	
	timing	1-3µs (slow)	~10 ns FAST	NO	
	electronics on chip (CMOS,bump bonding)	multiple scattering; power	multiple scattering; power	YES	Under development
	Ladders with strips≥10cm	OK apart from innermost regions	not usable	NO	Noise ~ C critical for SLHC
Mechanics	Large structure, module, new material solutions	Requested for decreasing X/X0	Requested for decreasing X/X0	YES	New material and simplified construction
	Cooling and insulation	Insulation from outside	Strong cooling constraints	YES/NO	some feedbacks for both
	Alignment	High spatial precision	High spatial precision	YES	Equally important for 2
Simulation	Important in many ways			YES	
Test bench & beam test	Important in many ways			YES	

TO CONCLUDE:

- New Physics Signatures are expected to include heavy quarks and/or τ-leptons Tagging of 3rd generation fermions is required to find these new phenomena.
- Tracking devices play an essential role in this, especially the Silicon detectors, that are becoming preponderant technology
- ATLAS, CMS, LHCb, ALICE made an incredible jump forward in developing sophisticated Silicon based tracking systems covering areas up to 200 m2.
- A new generation of Si trackers is already demanded,
- Both for the LHC upgrade(s) and for ILC.
- With a lot of new technological challenges to be overcome
- This demands a close collaboration with high tech industries.

❖ **The synergy between R&D for LHC upgrades and ILC is one of the key of success to achieve these R&D goal.**

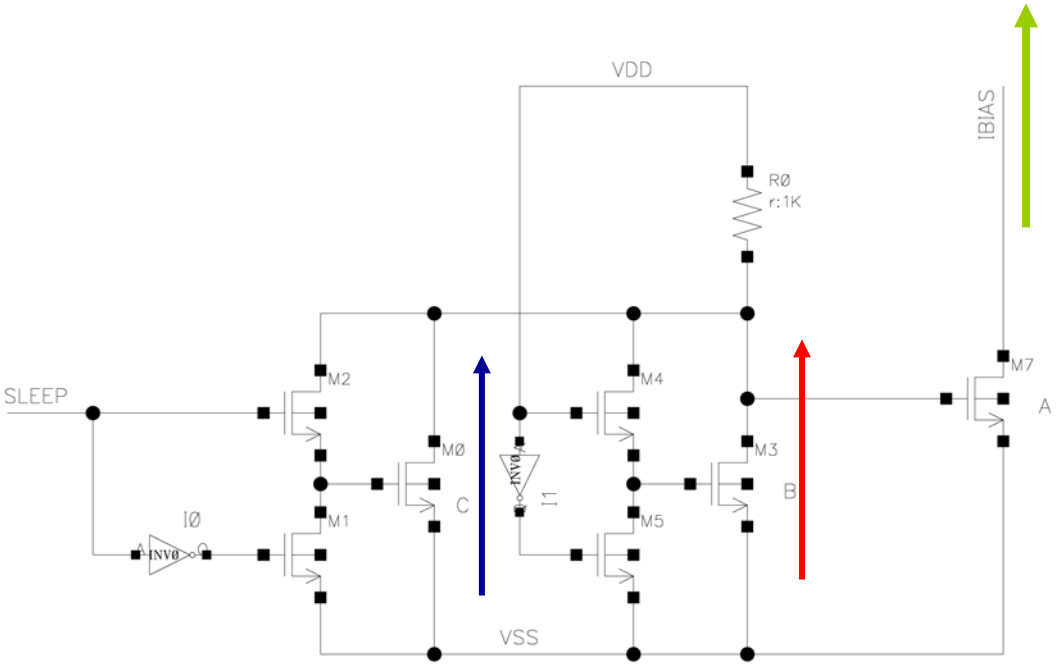
❖ **There is a valuable and large expertise in several crucial aspects of the Silicon-based tracking technology in Japan**

We look forward to succeed expanding Japan-France collaboration in all these challenging goals

Backup slides

Power cycling

Switch the current sources between zero and a small fraction (10^{-2} to 10^{-3})



This option switches the current source feeding both the preamplifier & shaper between 2 values to be determined by simulation.
Zero or a small fraction (0.1% - 1%) of biasing current is held during « power off ».

Zero-power option tested on 180nm chip with 2 ms recover time constant