Status of the setup: cosmic runs

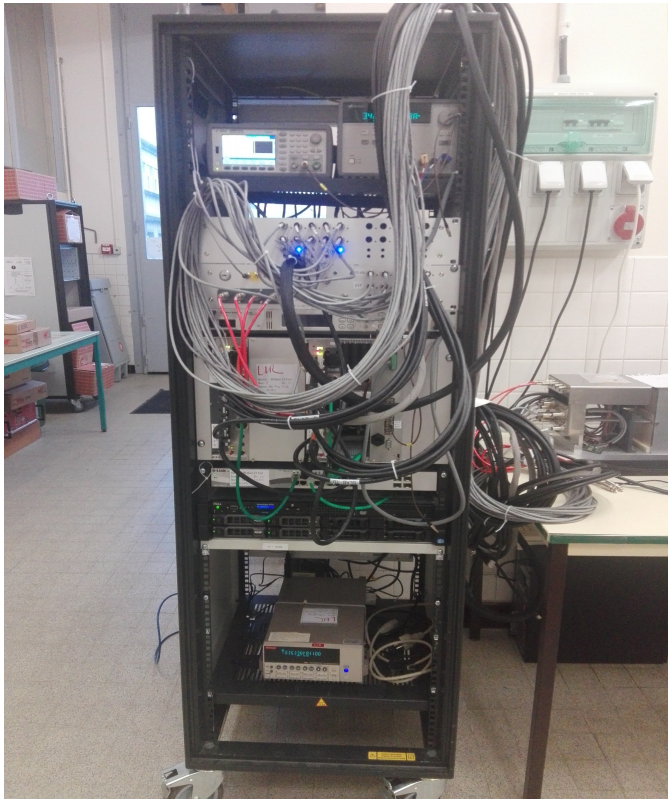
- Timing / DAQ
- Setup at LAL
- Preparing for cosmics
  - First try → ADC == 4 problem
  - Slow Control Optimization
  - Spill & FindNoisy optimization
  - Threshold optimization
- Results

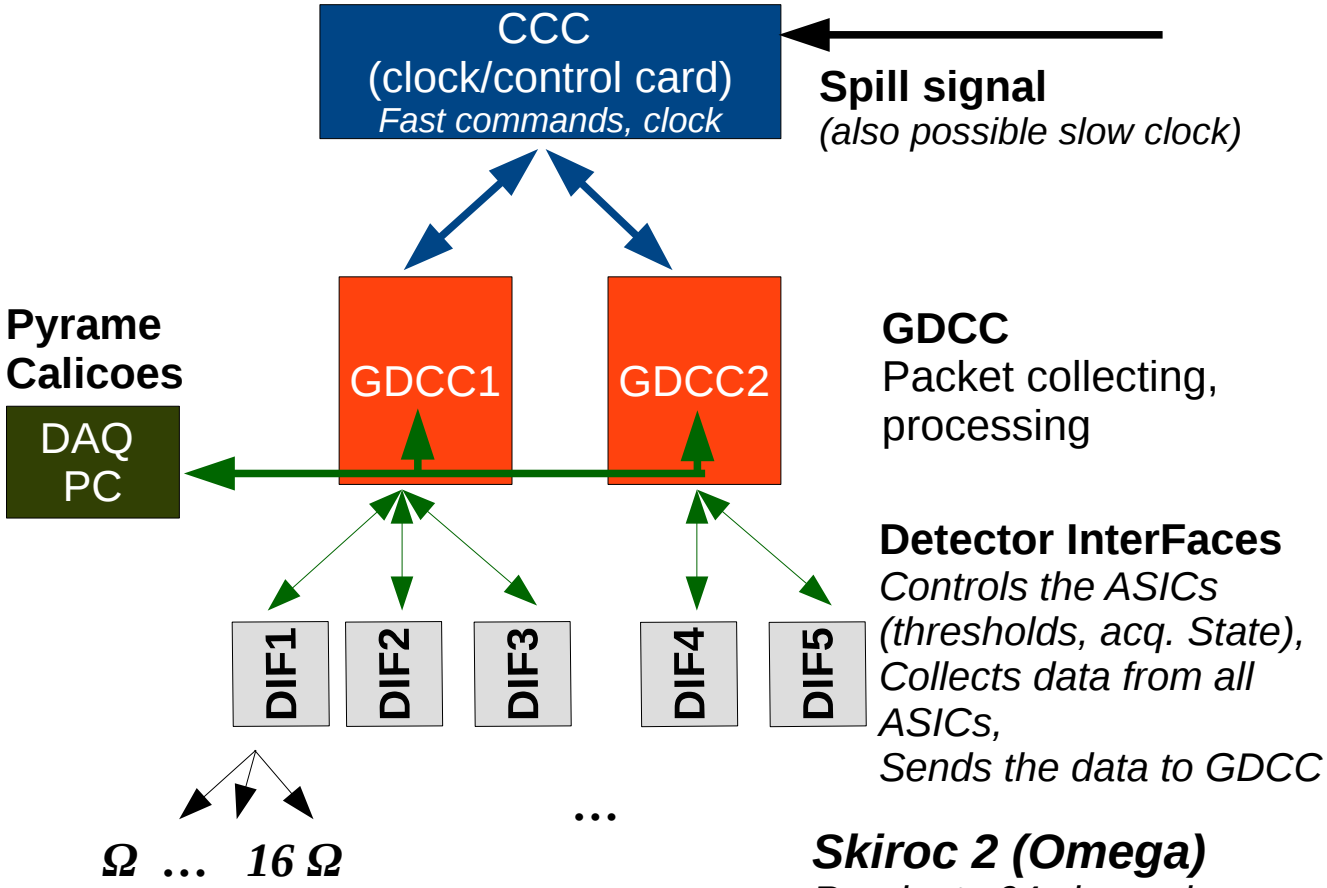
SiWLC ECAL Beam Test Readiness Meeting

A. Irles, LAL, 24th April 2017

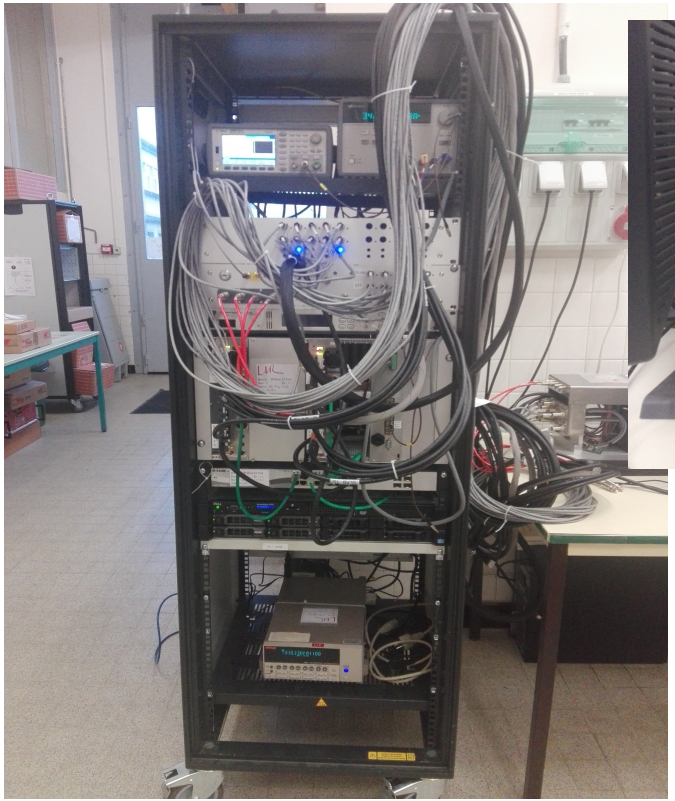
AIDA 2020 CALICE HIGHTEC P2IO Physique des 2 Infinis et des Origines LAL LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

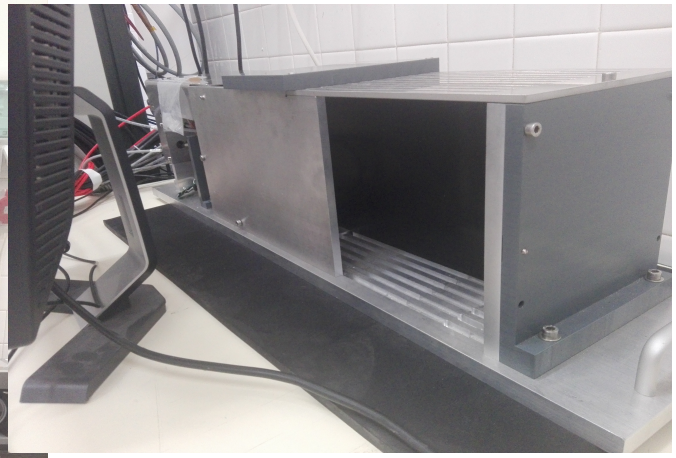
DAQ & electronic setup schematics

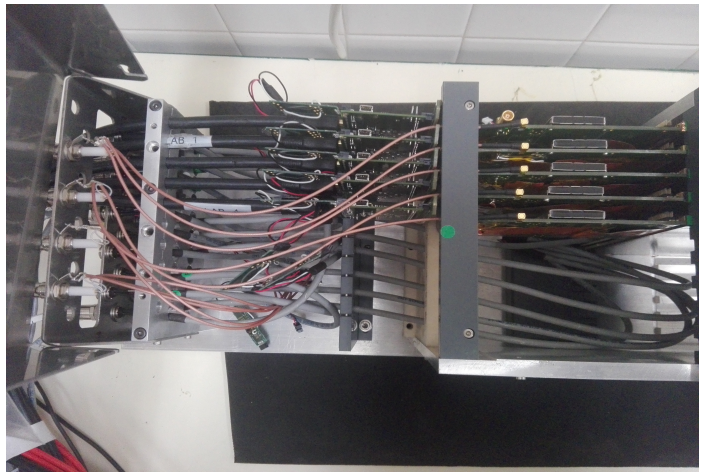


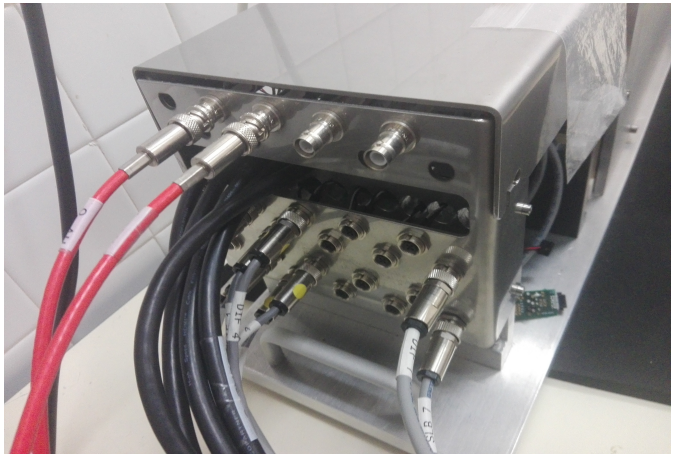


Testbench(es) 2017



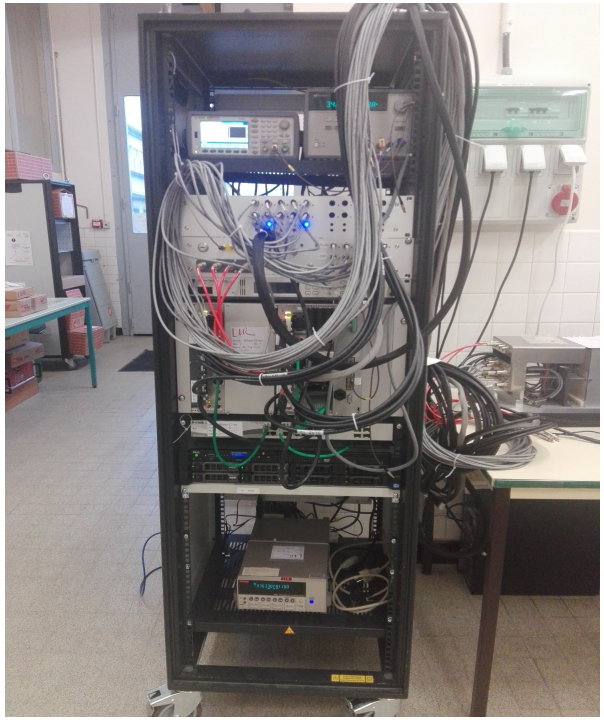


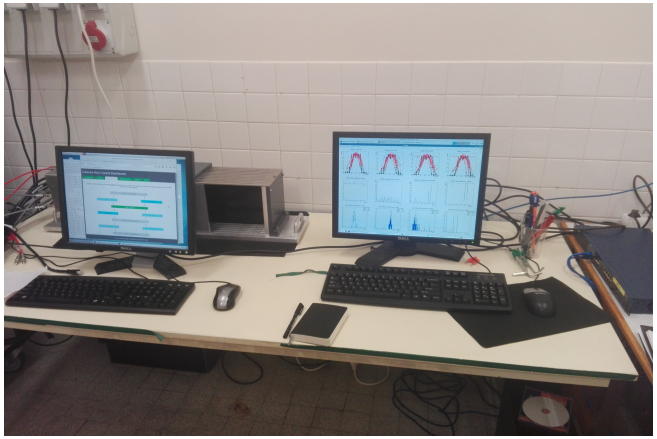


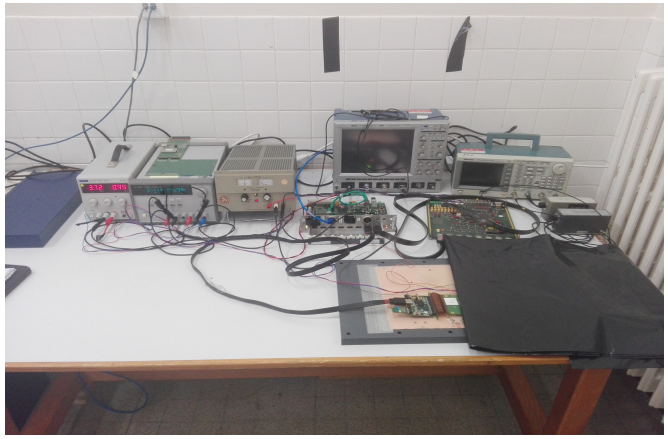


Prototype equiped with **5 FEV10 modules** with 16 chips **(skiroc 2)**, 64 chn each = 5120 chn.

LLR rack with all servers and electronics -> plug and play

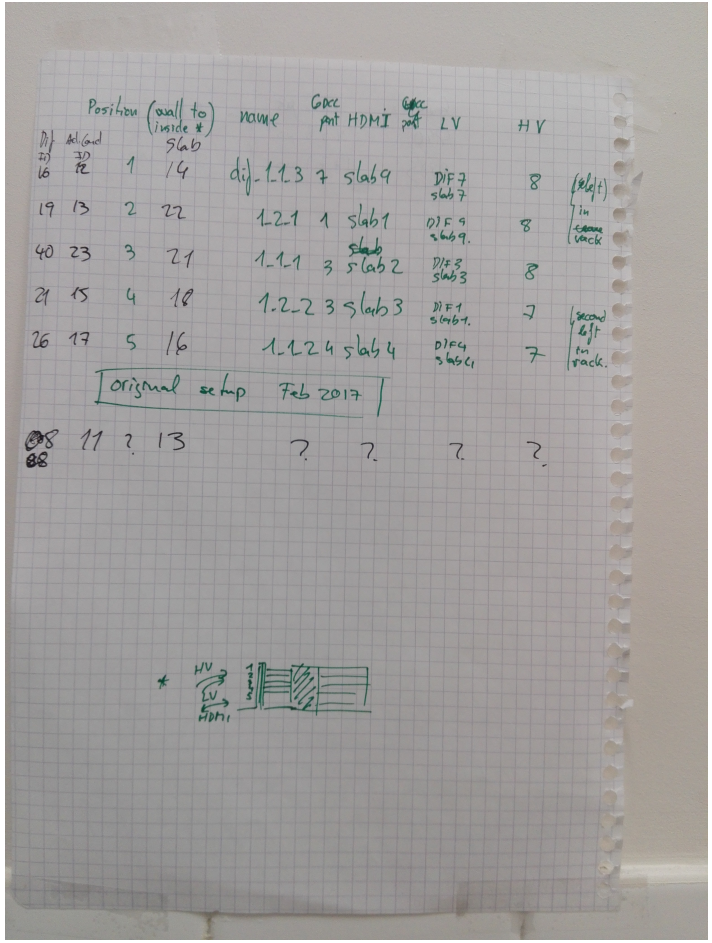






- Two testbenches together (from left to right)
  - Electronic rack for the prototype
  - Control PC of the proto
  - Prototype itself (5120 calorimeter cells behind a 15” screen)
  - Monitoring PC (used for both testbenches)
  - Testbench of single modules (FEV8)
- Weeks of work together with engineers from LAL, LLR and OMEGA

Setup at LAL (slides CALICE + picture)

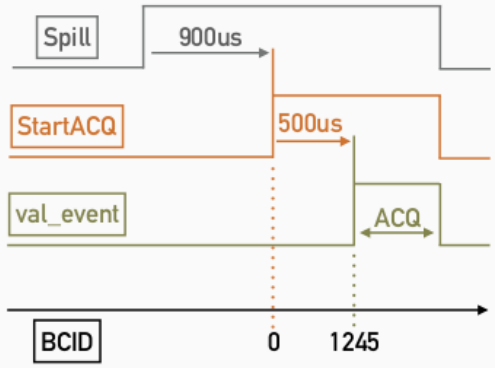


SK2/2A timing

With the current setup: spill length ≠ acqusition length:

1. Spill starts the acquisition window: reset and power ON
2. 900 μs delay for power to stabilize
3. StartACQ starts the acquisition and BCID counter

but triggers are only accepted within the "val_event" window, which is delayed by 500 μs to avoid triggers induced by StartACQ



Real acqusition length: spill length − 1.4 μs!

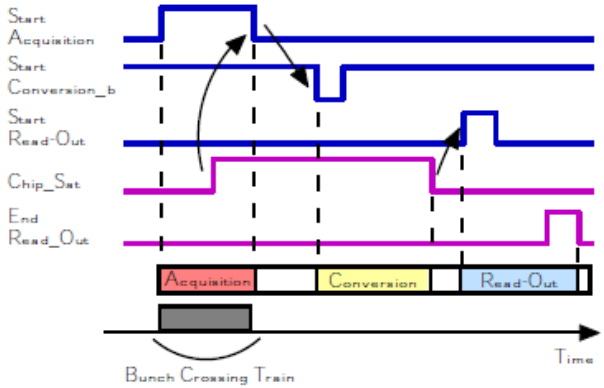


Figure 6: Global sequencing with chip full during acquisition

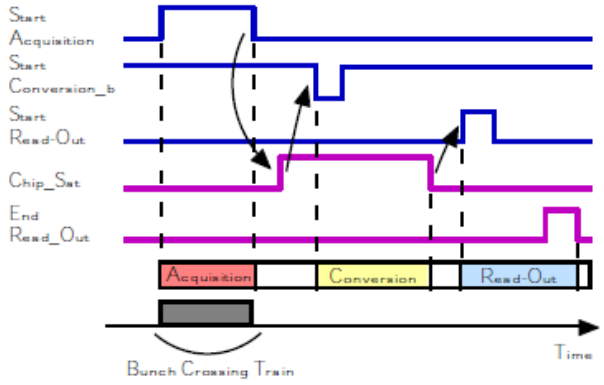


Figure 7: Global sequencing with chip not full during acquisition

Cosmic run preparation

- Optimization of the slow controls: **compensation capacitance**
  - the **compensation capacitance** should prevent overshot and ripple at the output of the preamplifier. According to the value one may trig (or not) on the primary pulse or an overshot.
  - Default 4pF. Tested 1pF and 6pF. With 1pF we lost a full slab (dif 1_1_2)
  - Final chose **6pF** → need to redo the optimization of the hold value.
- Optimization of the slow controls: **feedback capacitance =1.2pF (high Gain)**
- Find Noisy channels –> Find Noisy algorithm
  - Iterative algorithm that goes from very high DAC value to down masking iteratively the channels with
- Scurves (chose of the value of threshold of the fast shaper)
- Spill optimization
  - If readout takes longer than the time when the next spill arrives we get in troubles (a start spill always reset both the ROCs and the data buffers in the DIF)
  - A full memory chip (noisy channel) takes 12ms to be readout. Readout is in parallel.

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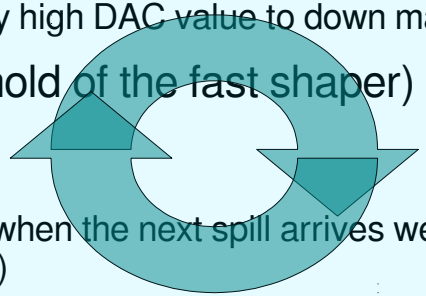
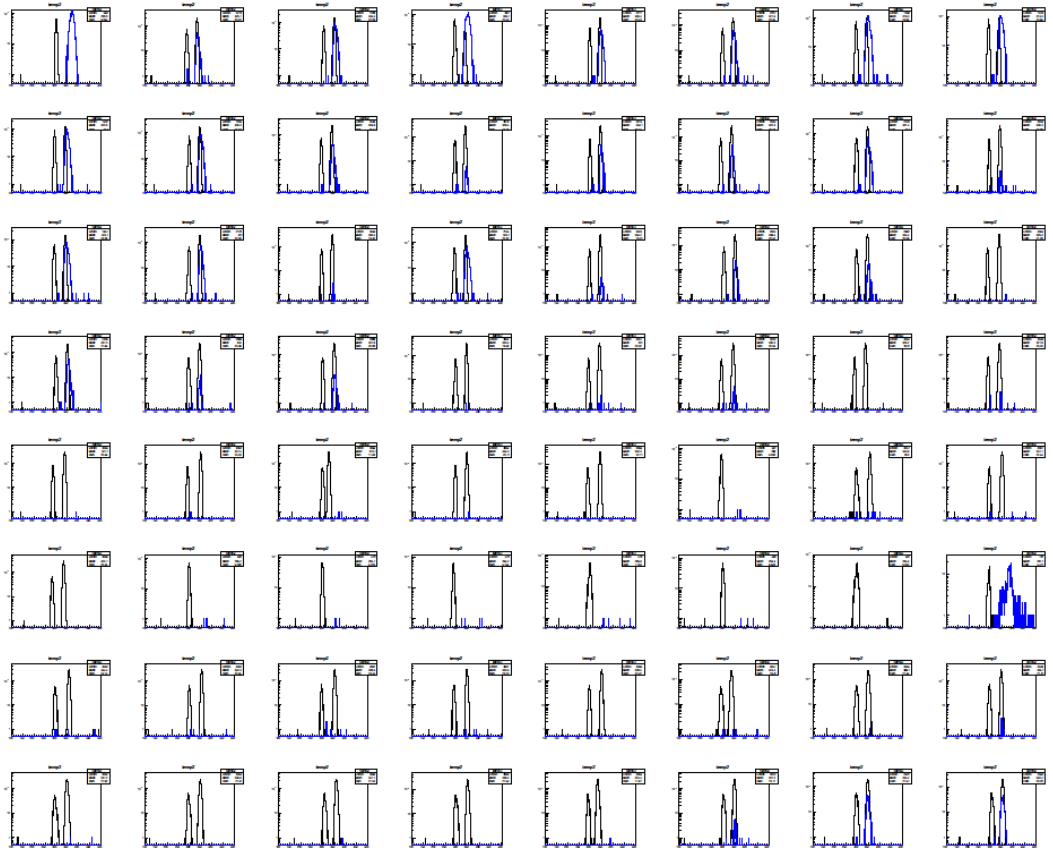


Cosmic run preparation

- First cosmic test: Spill 2Hz, width 2ms (2-1.4), DAC = 250, 2 days of data taking.
  - Allow me to not explain why these values for parameters.
- Results for 1 chip (report, page 8)
  - **signal (hit bit =1)**
  - pedestal (hit bit = 0)



Cosmic run preparation

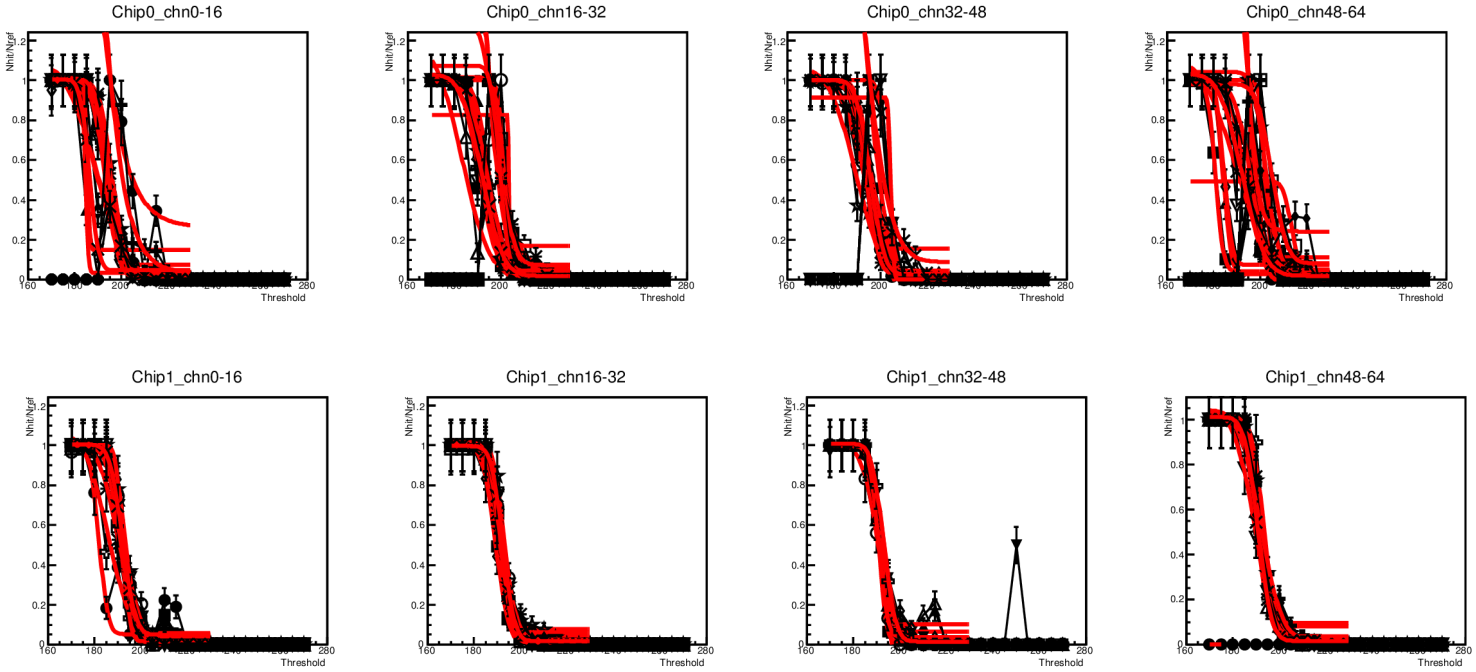
- The double/triple peak is (Remi's studies on 2015-16) are strongly correlated to events with channels with ADC = 4 (overflow).
- Filtering these events the double/triple peak pedestal structure dissapears → but also the statistics.
- FindNoisy Algorithm does not finds these channels → because events with ADC = 4 are filtered!

Cosmic run preparation

- I have “run” an FindOverflowed algorithm and are always the same channels in all DIFS...
  - all chips: channel 37
  - chip 2, 10 --> channels 41-47
  - I disabled the preamps, not only the trigger output.
- Then the Find Noisy works fine,

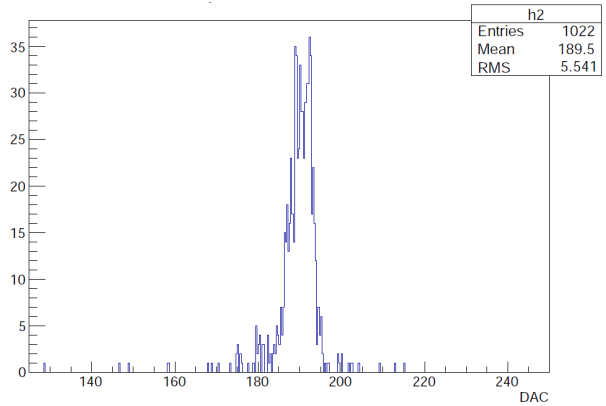
  but it also shows some systematical findings
  - chip 1, 9 --> channel 5
  - chip 2, 10 --> channels 48-53
  - chip 8, 16 --> channels 3, 9
- Masking summary (in top of those from above)
  - DIF 1_1_1 chips 5,6,7,8 masked.
  - 4-6 channels per DIF for the others (in cosmic position... some of them may be cosmic events?)

- After the masking → scurves with safe spill configuration: 2Hz, 2ms width.
- Results chip 0,1, dif 1_2_2

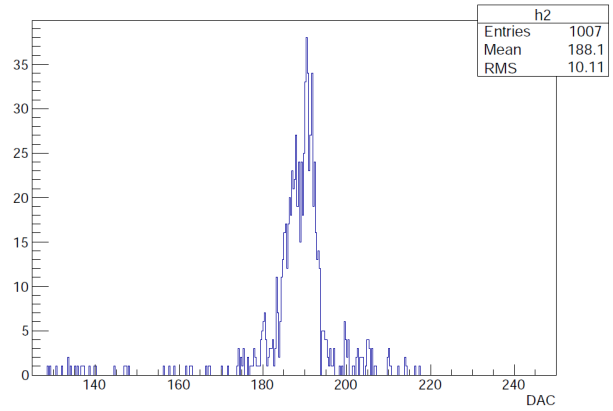


- Results for all difs → Final choice DAC = 230

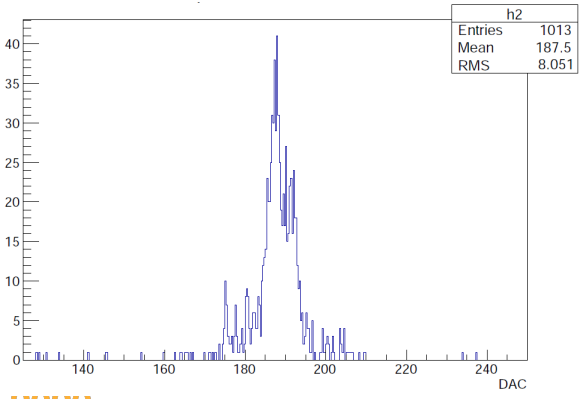
- DIF 1_1_1



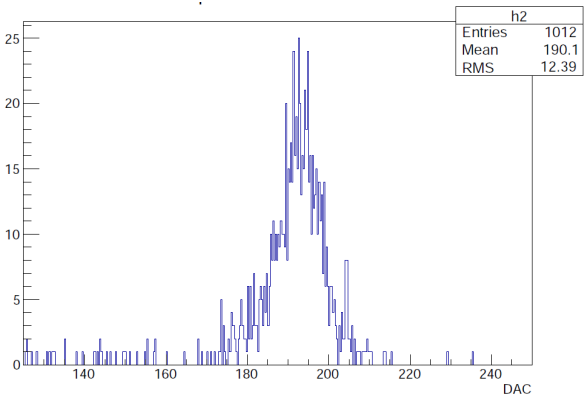
- DIF 1_1_2



- DIF 1_2_1



- DIF 1_2_2



Spill optimization

- Several tests.
  - Spill Freq, width, distance bewteen end spill and start spill.

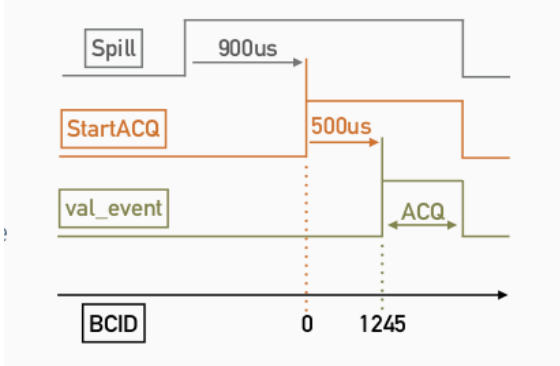
- 2Hz, 2ms, 498ms OK
  2Hz, 2.5ms, 497.5ms OK
  2Hz, 3ms, 497ms BAD
  2Hz, 5ms, 495ms BAD

- 5Hz, 2ms, 198ms OK
  5Hz, 2.5ms, 197.5ms OK
  5Hz, 3ms, 197ms BAD
  5Hz, 5ms, 195ms BAD

- 10Hz, 2ms, 98ms OK
  10Hz, 2.5ms, 97.5ms OK
  10Hz, 3ms, 97ms BAD
  10Hz, 5ms, 95ms BAD

- **BAD** means that the cosmic runs are populated of events with pedestal entries considered as triggers … (retriggering?)

- Final choice **10Hz, 2.5ms, 97.5ms**



- If bad → seen during the conversion
  - Output example of Data integrity checks done during conversion.
  - For wrong spill configurations we always observe ~3% of spills with extra bits in BCID and ~3% of spills with different hit bits for low and high gain

```
DATA INTEGRITY SUMMARY
total number of spills = 58
TOTALGOOD  93.1034 %   are spills with acceptable data
bad -- 0 %   have bad data size
bad -- 0 %   have more than 15 SCA
bad -- 0 %   have bad chip number
bad -- 5.17241 %   have extra bits in BCID
bad -- 1.72414 %   have extrabits in low gain.
bad -- 0 %   have extrabits in high gain
bad -- 0 %   have different hit bit for low and high gain
bad -- 0 %   bad number of SCA or channels
```

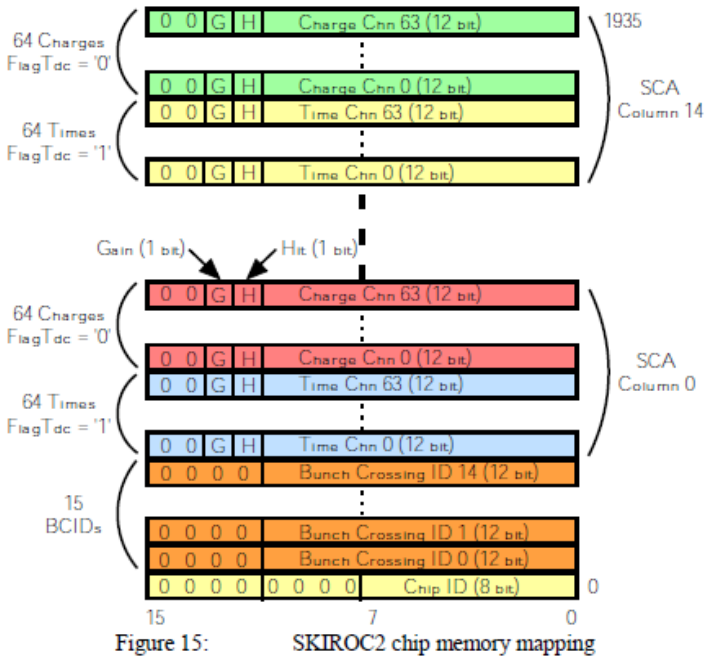


Figure 15: SKIROC2 chip memory mapping

Cosmic run for the weekend

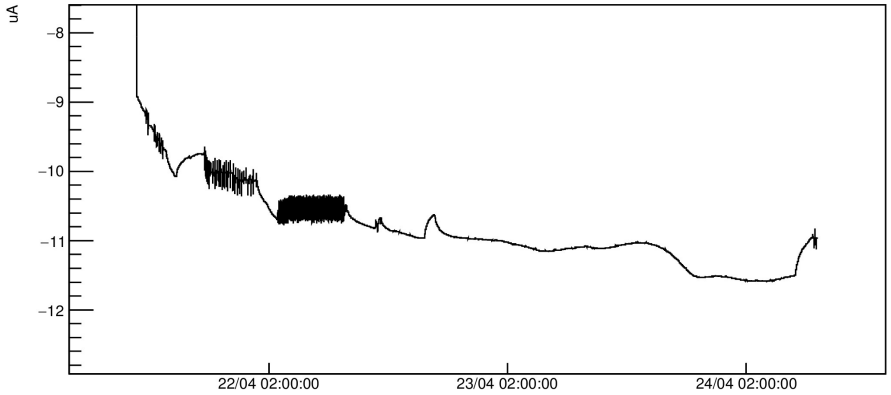
- DAC = 250, spill 10Hz, 2.5 ms (1.6 active), Masked overflowing and noisy.
- Expected ~ 450 MIPS per channel.
- MIP (historically) at ~ 70 ADC counts.
- Analysis very basic:
  - Pedestal == ADC with hitbit = 0.
  - MIP == ADC with hit bit = 1.
  - Pedestal is subtracted SCA by SCA.

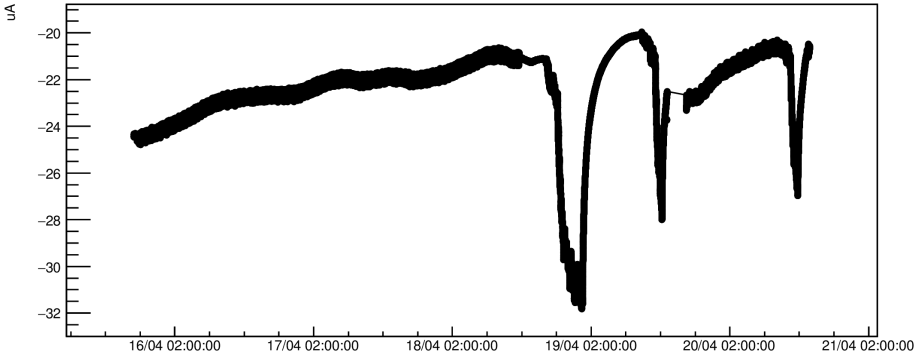
- https://owncloud.lal.in2p3.fr/public.php?service=files&t=613222d739a05515808ab7cf89d46b18

SLAB commisioning (ongoing)

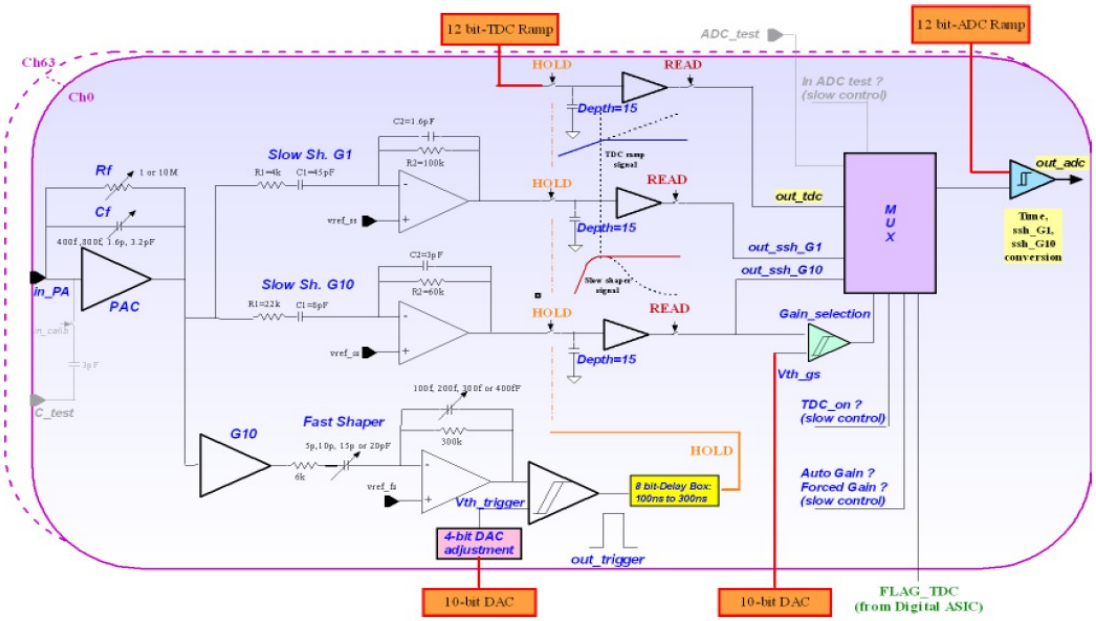
- Automatize procedure to:
  - Find Overflowing
  - Find Noisy (done... to be optimized, to be merged with the FindOverflowing ?)
  - Scurves → find threshold
  - Spill ?
  - Holdscans, scurves with pulse injection
- Most of the points are partially covered (pieces here and there) but we need to converge to something stable and share it between LLR and LAL
  - Not possible before friday because of the ADC == 4 issue that made very difficult the understanding of the noise.

Backup slides


uA
−8
−9
−10
−11
−12
22/04 02:00:00
23/04 02:00:00
24/04 02:00:00

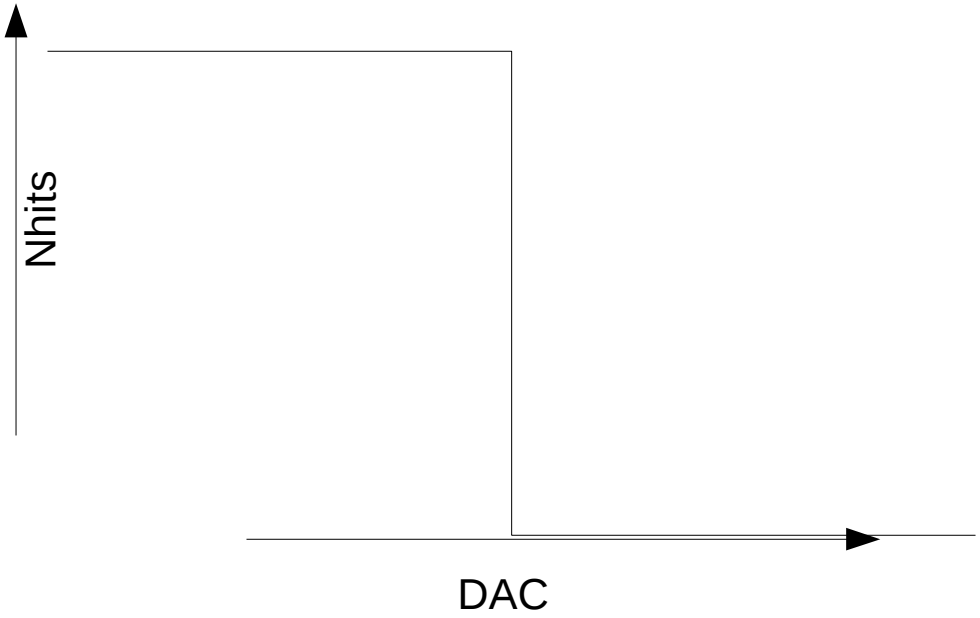

uA
−20
−22
−24
−26
−28
−30
−32
16/04 02:00:00
17/04 02:00:00
18/04 02:00:00
19/04 02:00:00
20/04 02:00:00
21/04 02:00:00

Determination of the pedestal of the fast shaper threshold → Scurves

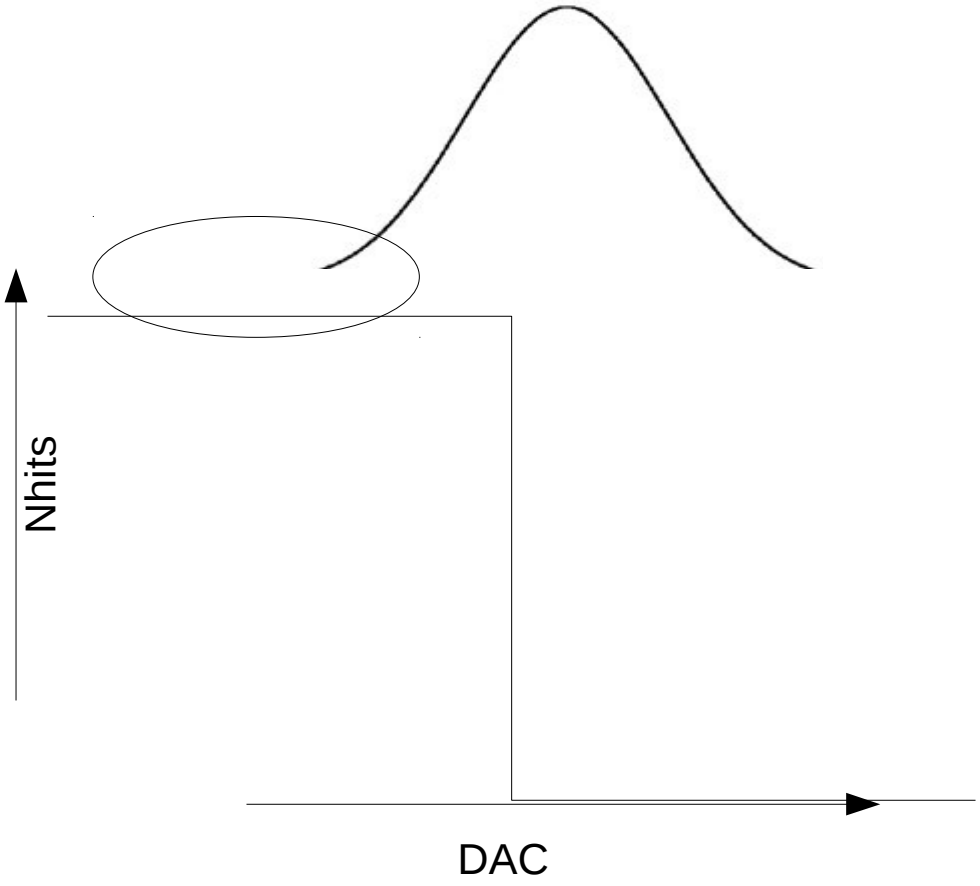


Determination of the pedestal of the fast shaper threshold → Scurves

- SCA = 0



Determination of the pedestal of the fast shaper threshold → Scurves



- SCA = 0
- SCA > 0
  - For low values of the threshold → “saturation”: in SKIROC/SPIROC, there is a Rising Edge detector... If a discriminator output is always set to 1, the detector doesn't see any rising edge, therefore the chip does not write anything.
  - Can be removed from the analysis by requiring
    BCID > val_evt_bcid + 15
    Needed?
  - Every SCA has different pedestal.

Determination of the pedestal of the fast shaper threshold → Scurves