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Futur Crystal Data Readout for AGATA using Futur Electronics (STARE)

IFIC/MILANO/ CSNSM/IPHC Collaboration

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AGATA Crystal Data Readout in Futur Electronics

- AGATA data rate : 50 kHz per core
- Project Definition Standard data readout through Ethernet.
- Network Band Width : 10 Gbps.
- Look for TCP/IP interface embedded inside an FPGA
- After several months of research. Here are what we found :

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AGATA Crystal Data Readout in Futur Electronics

10 Gb TCP IP Research and Development

- 10 Gb UDP interface from a third party inside a Xilinx Chip : **150 k€**
- Very expensive impossible to buy out of our budget.

- More research and here what we found:
- 10 Gb TCP/IP interface from IN2P3 collaboration inside an Altera : 10 k€
- Good affordable but not compatible with Xilinx, needs Altera expert engineering. No one from CSNSM knows about Altera technology. Kept as a B plan version.

- More research and here what we found:
- 10 Gb TCP/IP interface from Zurich university developped by a phd-student.

- Full TCP/IP inside a Xilinx Chip : **0 K€**

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AGATA Crystal Data Readout in Futur Electronics

10 Gb TCP IP Research and Development

- Person in charge in Zurich university : David Sidler.
- Open source code.
- No guarantee and no maintenance but continuous upgrades and feedback to developper to improve code is mandatory. Discussion and help is possible.
- No financial expense but add name in all publications where the interface is used.

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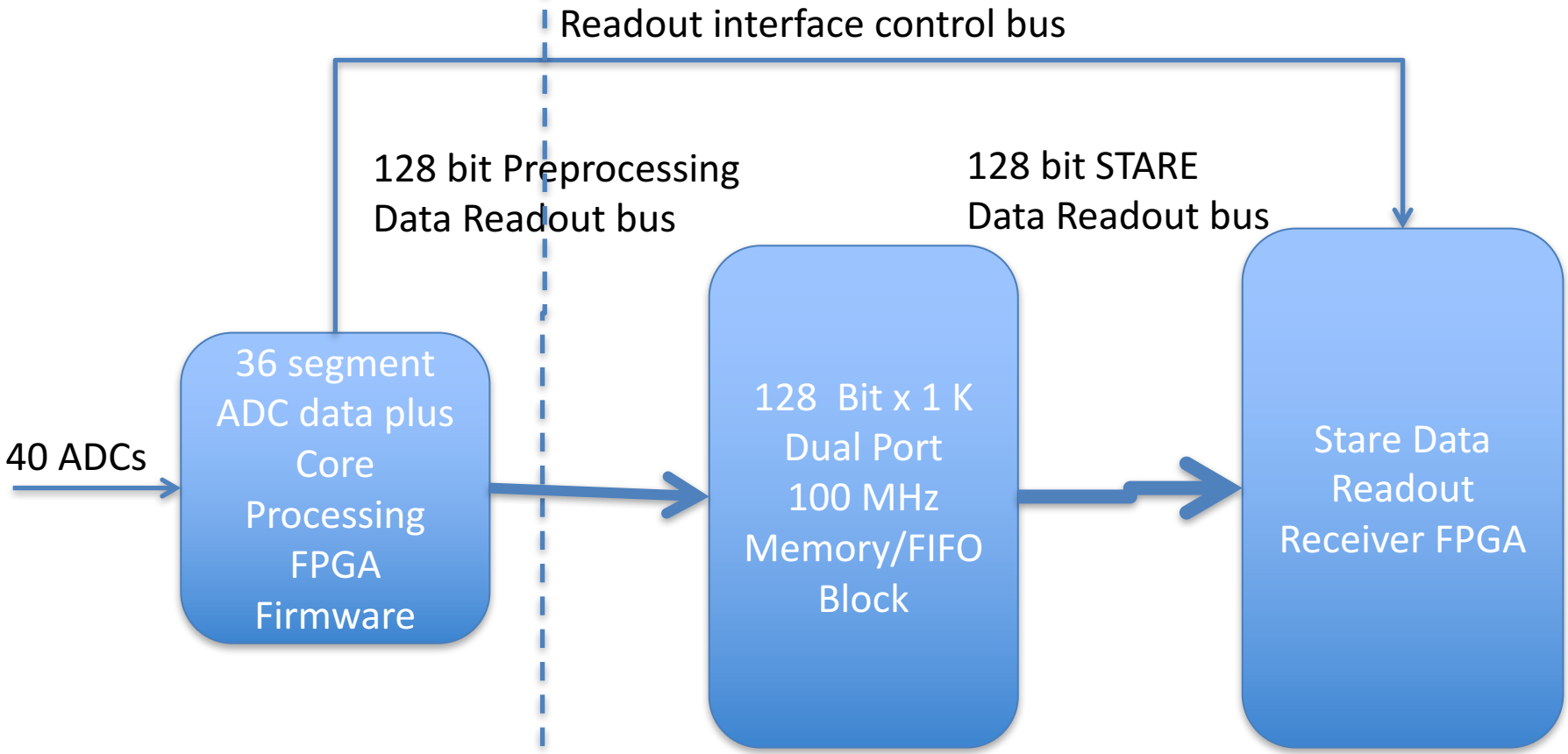
10 Gb TCP IP Research and Development

- **What's next :**
- Xilinx evaluation board purchase to qualify the code.
- Interface the EB with the CSNSM 10 Gb network data flow and validate the TCP/IP for AGATA DAQ.
- Check for the best architecture to integrate the TCP/IP. Either in the preprocessing FPGA or inside an independant board.
- Design the AGATA data Readout interface prototype.
- Integrate the prototype with the preprocessing board.
- Production and tests.
- **What's needed: MANPOWER (waiting for an engineer).**

AGATA Crystal Data Readout in Futur Electronics

10 Gb TCP IP interface Block Diagram



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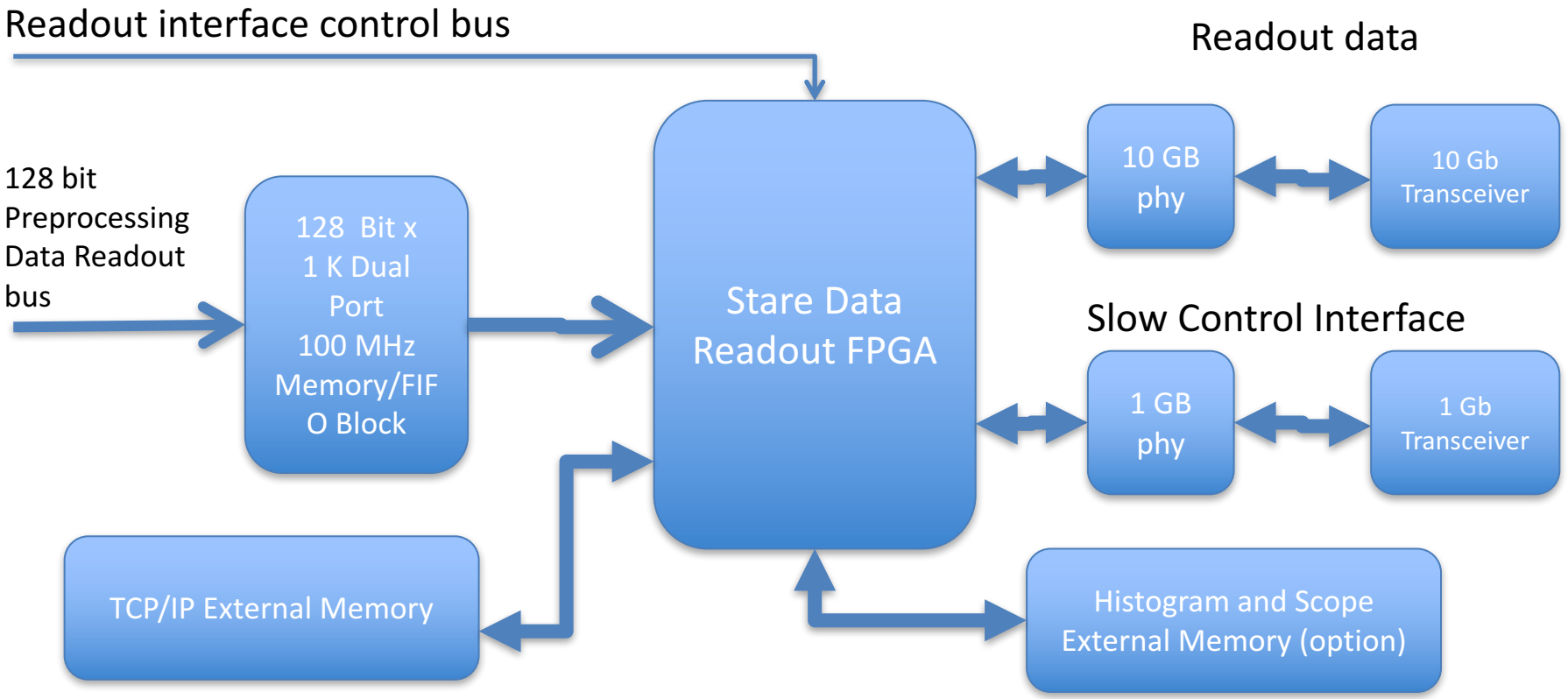
STARE Block Diagram



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AGATA Crystal Event Data in Futur Electronics

- Data Readout (From Preprocessing to Pizza Box) Requirements
- AGATA data rate : 50 kHz per core
- ADC Data rate 14 bits @ 100 MHz = 1,6 Gbps per channel = 100 M Words of 16 bits
- Continuous cristal data rate (40 channels): 64 Gbps = 4 Gword of 16 bits
- Need to reduce raw ADC data to 10 Gbps.
- Network Band Width : 10 Gbps = 640 M words of 16 bits.
- For full crystal data transfer @50 kHz we can send 12,8 kWords of 16 bits/ crystal/event (≈ 300 W/segment/event)

AGATA Crystal Data Readout in Futur Electronics

- Data Readout (From Preprocessing to Pizza Box) Requirements
- For continuous channel trace transfer acquisition is 10/1,6 = 6 channels.
- For 2 continuous core signals = 3,2 Gbps = 200 Mw of 16 bit
- Reference Example: For a gamma ray of 1 MeV 1 core and 2 segments are hit.
- How much data can be sent if 1 core and 2 segments trigger plus 2 x 4 neighbors (11 channels 1/4 crystal) ?
  - Assume 10 us is the Trace length then 4 x 1024 data are collected from the triggered channels (2 core +2 segments) = 4kw of 16 bits.
  - Plus 8 x 256 points x 16 bits from 8 neigbours recording 2,5 us of trace for PSA. Total :2 kw of 16 bits
  - Total number words per event is 6 kw of 16 bits
  - This means that another event during can be processed in parallel which means 2 core channels plus 2 more segments in parallel.
  - This gives a total of 12 kw of 16 bits

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AGATA Crystal Monitoring in Futur Electronics

- Full FPGA online Monitoring (Chipscope on Ethernet)
- Continuous channel trace for noise and maintenance and problem tracking.
- Hardware Inspection Lines using ethernet scope boxes
- GUI Facility to monitor and modify crystal parameters.
- It is important to have spy eyes on all the data processing from Preamplifier to Data Flow

- Thank you