



# Report for Sept 2017 AGATA Week

## Phase 0 Digitisers

*Work of Patrick Coleman-Smith and Andy Hill*

*Presented by Ian Lazarus*

*PreProcessing slides from Xavier Lafay*

*Advanced phase 1 slides from Andres Gadea*

# Repairs to phase 0 digitisers

- **Since last AGATA week:**
  - 5 repairs
    - 3 Segment modules (1 still at DL/just shipped)
    - 2 Core modules
  - Attempted to repair 10 segment ADC cards (previously removed from faulty modules).
    - Bought 10 off V2Pro FPGAs and swapped.
    - Aim is to get some spares.
    - 5 repairs were successful.



# Status of phase 0 digitisers

- **Core Modules:**
  - 27 at GANIL
  - 1 at ORSAY
  - 1 at Daresbury Laboratory
- **Segment Modules**
  - 26 at GANIL
  - 2 at Daresbury (*including 1 repaired and ready to send*)
  - 1 at ORSAY



# PRE-PROCESSING ELECTRONICS MAINTENANCE

## HARDWARE

Agata Project

Agata France 10-11 July 2017

X. Lafay/N. Karkour / D. Linget

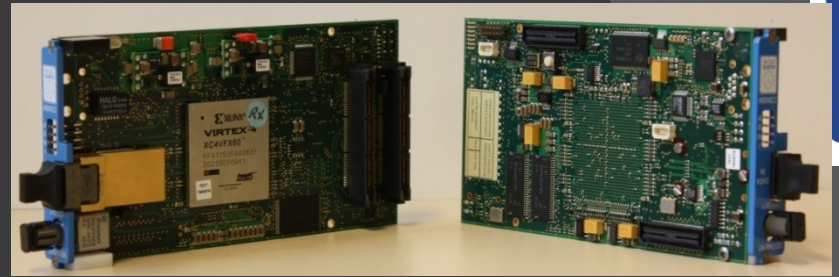
- Segment board status V2.21 (hardware and firmware)
- 168+1 installed cards @ Ganil
- 29 Core board status V2.1r2
- (hardware and firmware) never installed

• Total 198 cards

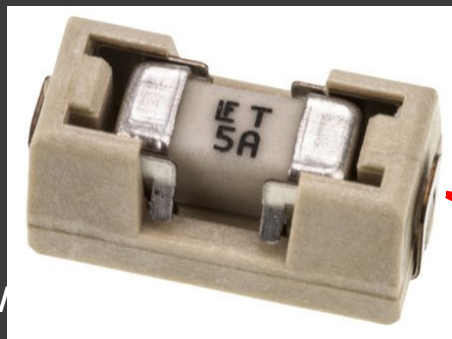
- Carrier board V3 (IPNO) V4 (CSNSM)
  - CSNSM Production : 24 cards
    - 23 are Installed @ GANIL
  - IPNO production : 33 cards
    - 25 cards: Installed @ GANIL

• Total : 48 cards

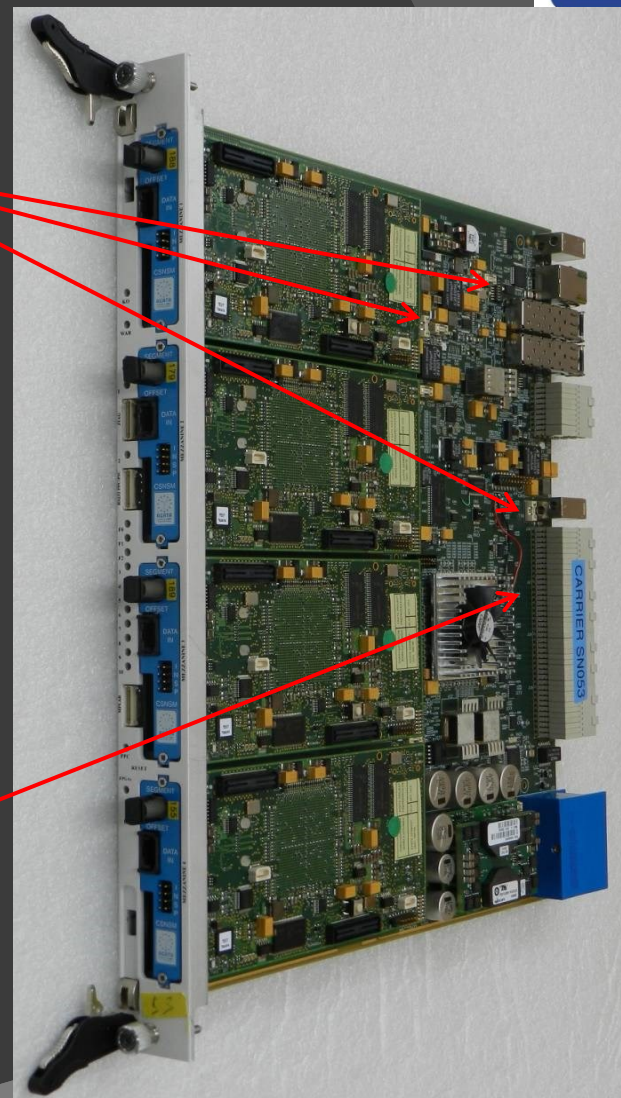
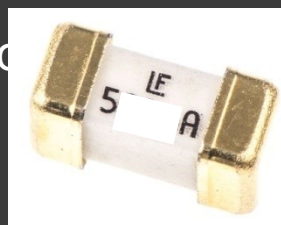
+ 2 carrier V3 @ Orsay's TestBench (with segments)



# • PreProcessing Hardware



- 2015 → Finally some new
- Fuse sockets reliability decreases with time. Bad contacts are formed and/or oxidation . Fuse series resistors increases, Final Voltage supply decreases..
- Patch (known since 2008) : solder fuses directly to pcb.
- Made on preproduction @ Padoue not to V3 IPNO nor V4 CSNSM
- ALL carriers V3 et V4 concerned.
- few cards modified → OK
- 10 fuses per carrier (total of 480 fuses were unsoldered and resoldered back)



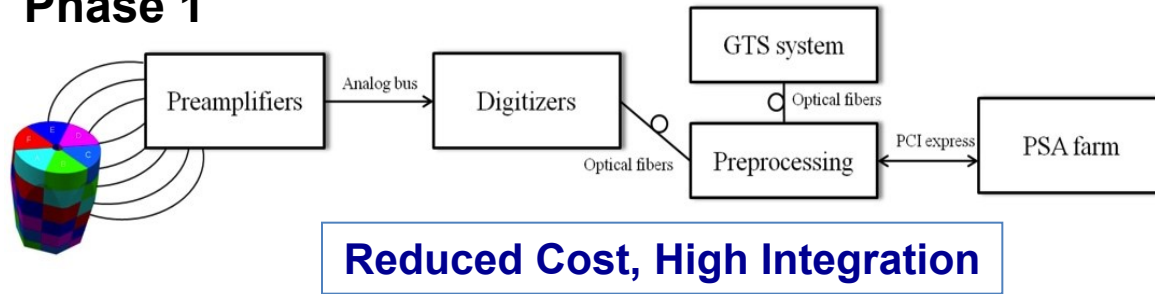
- 48 cards modified, Trip to GANIL in 2016

## • ATCA Carrier maintenance

- Lot of time consuming even few cards can take enormous time. Some reasons :
  - Orsay test bench quality deteriorates.
    - Synchronisation Master/Slave
    - Clocks (suspicions on TCLK board)
    - Digitiser heat (new cooling system arrived)
  - Hectic pulser to generate 36 signals.
  - Old pizza boxes for DAQ fails very often.
  - Servers and programs fail to connect to Hardware.
  - Every power up procedure can take from 5 minutes to 1 day or never.
  - Manpower problems to spend to repair test bench and to look after the cards. IPNO will help, training is necessary (but needs a stable testbench)
- **Fuse modification has improve the stability of the system**

# Advanced Phase 1 Electronics Maintenance

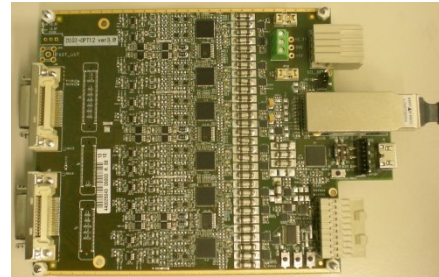
## Phase 1



## PCI Pre-Processing Card GGP



## ADC Card



## Control Card



## Pre-Processing

- GGP (EDA-002264- pre-processing + EDA-02266 transceivers plug-in)
- Repairs managed by INFN-Padova (Contact Person R.Isocrate)
- Issues with heat dissipation identified in some cards.
- Repairs to be done
  - 4 EDA-002264 (3 FPGA + 1 DC/DC replacements)
  - 1 EDA-02266 (DC/DC replacement)
- Procurement of FPGAs for replacement completed

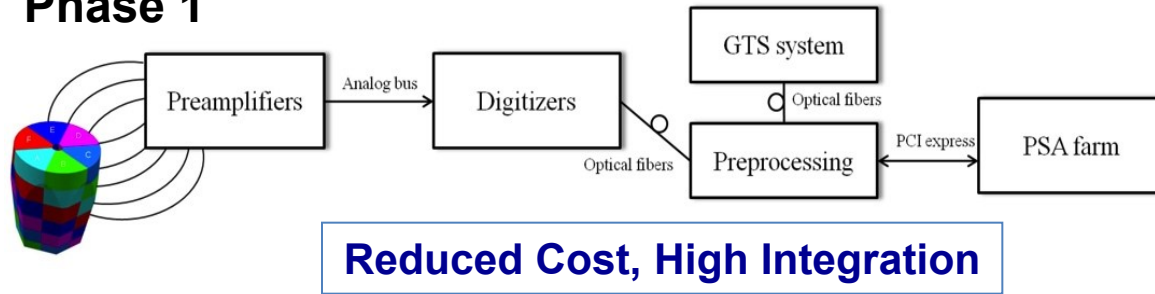
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INFN-Padova INFN-Milano INFN-LNL  
IFIC-Valencia ETSE-Uni.Valencia



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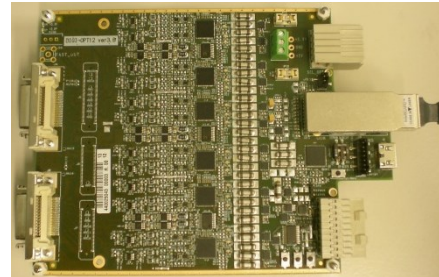
## Phase 1



## PCI Pre-Processing Card GGP



## ADC Card



## Control Card



## DIGIOPT-12 Digitizer

- DIGIOPT12 cards repairs managed by A.Pulia (INFN-Milano) 1 repair done in 2017.
- Control Card repairs managed by INFN-Padova and IFIC
- Power Supply Units and backplanes repair managed by ETSE-Valencia.
  - Issues with Temperature in the PS units. Few units replaced. Solution under evaluation.
- Mechanics maintenance managed by ETSE-Valencia and IFIC-Valencia

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