Report on the R&D on electronics for 2020 and beyond: Introduction to the new R&D on electronics

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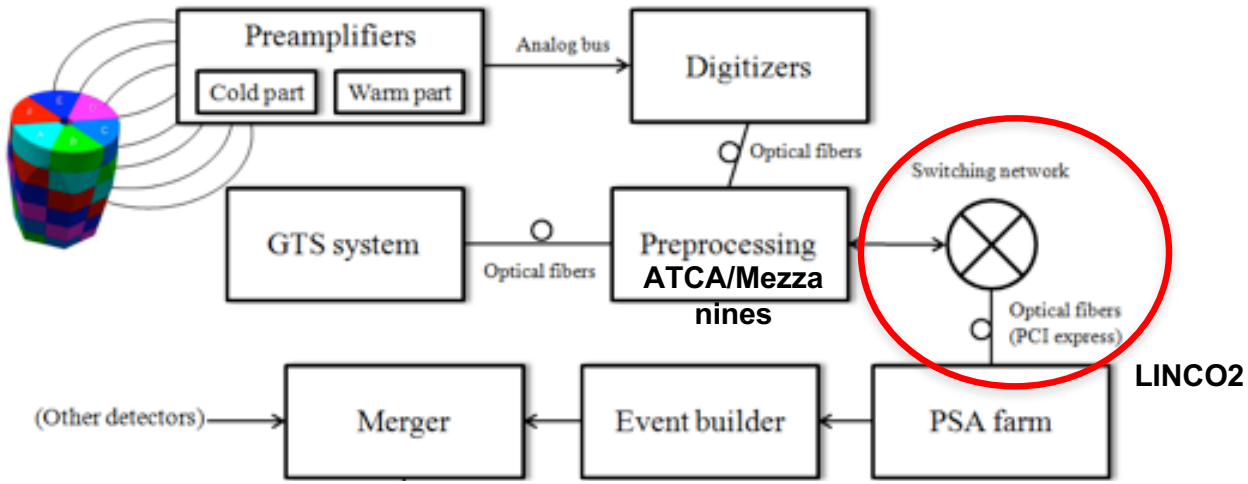
Outline

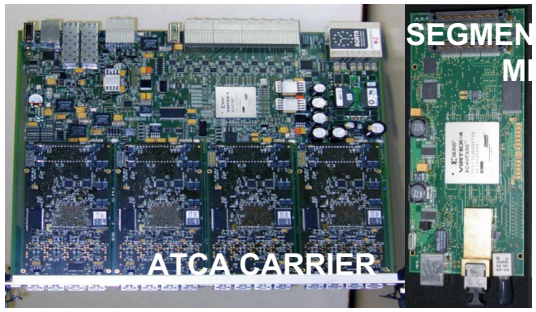
- AGATA Electronics Evolution
- Found issues
- Guidelines for R&D initiative
- On going Technical Proposal

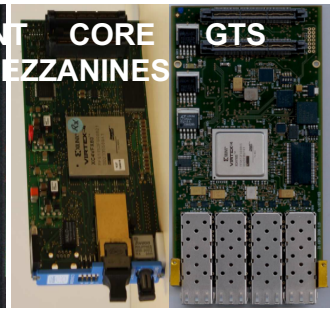
AGATA Electronics Evolution

AGATA Electronics Phase 0/Early1



23 to 25 channels available



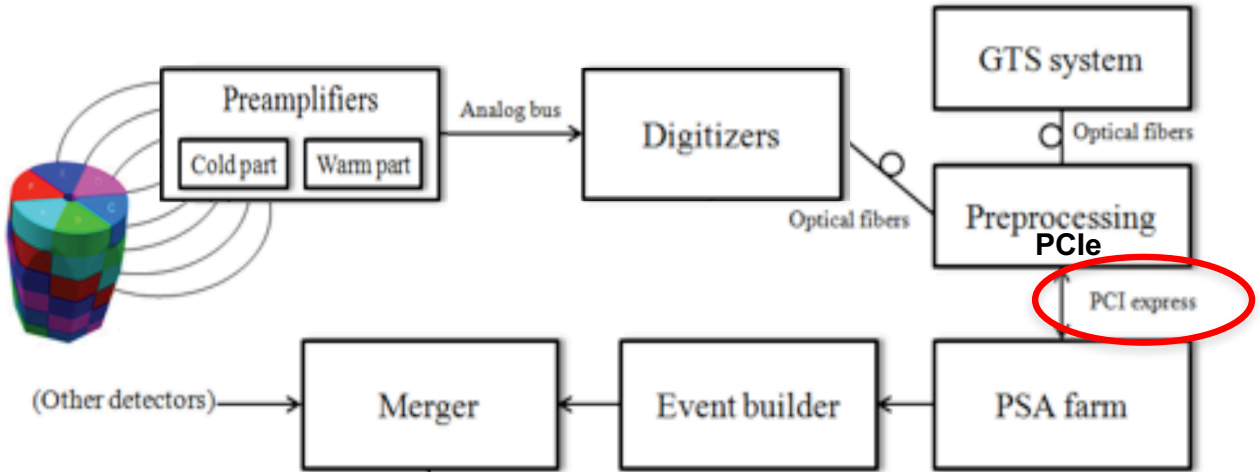


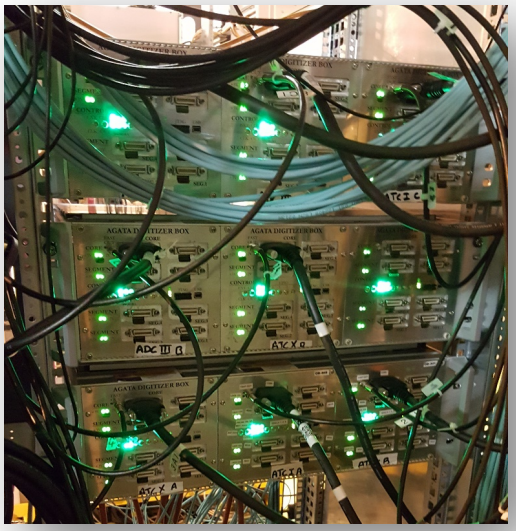
IPHC Strasbourg Uni.Liverpool STFC Daresbury IPNO, CSNSM-Orsay INFN-Padova

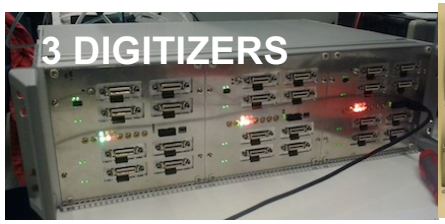
AGATA Electronics Evolution

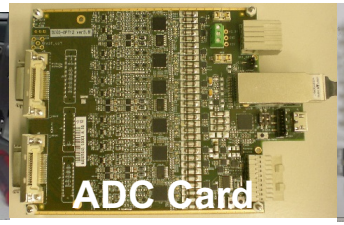
AGATA Electronics Advanced Phase 1

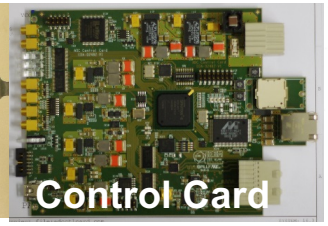
Up to 13 channels available

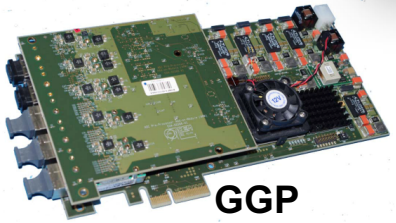












GGP Card

INFN-Milano INFN-Padova INFN-LNL IFIC-Valencia ETSE-Uni-Valencia

AGATA Electronics Evolution

Up to 38 channels available for AGATA
Up to 45 detectors by end of GANIL campaign

New production batch of Adv. Phase 1 electronics
10 channels + spares

We need to go to 60 channels

More Adv. Phase 1 channels?
New electronics?

Known issues

Several issues faced in AGATA Electronics evolution

At least:

- Component procurement due to obsolescence (transceivers, IC, …)
- Compatibility issues, i.e. GGP and workstations
- Difficulties in maintenance and repairing
- Costs
- …

But we need to think in view of AGATA Phase 2

More Adv. Phase 1 channels?
New electronics?

Electronics R&D

Guidelines for the R&D

Recommendation of experts evaluation for Advanced Phase 1 (2012)

- **New R&D Phase to improve integration** and reduce data transmission using large number of optical links.
- **Model of FEE production with an R&D phase at least on every construction phase of AGATA**. This model also reduces considerably the maintenance costs since the expensive early electronics might be replace with time by cheaper newer one.
- **Compatibility with the existing electronics and with the GTS is considered a basic requirement.**

Guidelines for the R&D

FEE Group discussions identified the following lines of R&D

1. Possibility of **higher integration and power consumption reduction** in the AGATA **core and segment pre-amplifier**. Exploring the **ASIC technology** for the AGATA pre-amplifiers.
2. Possible **integration of the Digitizer and the ADC** in the spirit of the Digital Pre-amplifier module.
3. **Improvement in the Digitizer ENOB** by using **16 Bit FADC's (or beyond)**. This will allow to enlarge the energy range without endangering the energy resolution, specially in the high gain section that might go easily to an 8 MeV range.
4. Possibility of increasing the ENOB **using more complex pre-processing algorithms on the evaluation of the baseline**.
5. Possibility of **higher integration in the Digitizer control Card** for remote settings of the Digitizing cards.
6. Pre-Processing improvements: considering the **possibility to integrate the pre-processing of a full cluster in a single card.**

Guidelines for the R&D

Lines of R&D cont'd

7. Study of the **possibility to locate Digitizer an pre-processing electronics together in the neighbourhood of the AGATA Clusters**, using short links and avoiding long optical fibers
8. **Improvements in the GTS protocol** increasing the **number of leaves** in the tree and possibly defining **"qualifier bytes"** for complex triggers.
9. Development of the **Hardware and Software trigger processor** able to cope with the necessities of AGATA and all complementary instrumentation beyond Phase 1.
10. Exploring the **possibility of using Ethernet capacity** to transfer data from experimental hall to the computer room **avoiding dedicated interfaces**.
11. Exploring the **use of high capacity Ethernet network to remove customized cards** inside computer farm.
12. **Explore if some high level processing algorithm can be moved** from the FPGA to computer farm.

After **January 2016** Town Meeting on R&D for AGATA Electronics, the **AMB and ASC encouraged the development of a medium term solution for processing an ATC and with Ethernet readout**, while **long term developments with ASIC (Digital Pre-amplifiers)** shows technical difficulties that **need further development**.

On going Technical Proposal(*)

Proposal objective: to build a scalable and stable Back End Electronics and DAQ (Electronic Data Acquisition) system for AGATA beyond phase 1 and track the best technical solutions for the full 4π array

Important issues

- Interface between front end electronics and servers should **not rely on any specific hardware interface**.
- Simplified and autonomous electronic modules to **ease maintenance** and **minimize impact of possible rework due to obsolete components** in future.
- **Highly integrated solution** to ease the installation in experimental area.
- **Readout** based on **high bandwidth network technology** (up to 10 Gb/s per crystal).
- **Stable and scalable architecture** of the AGATA BEE&DAQ architecture (for which the necessary performances must be fulfilled from 45 up to 180 crystals)
- **Modularity** to allow for the use of new technologies when available and suitable for the objectives of cost reduction and higher integration.

(*) Information from the working document for the R&D on electronics for AGATA Phase 2.

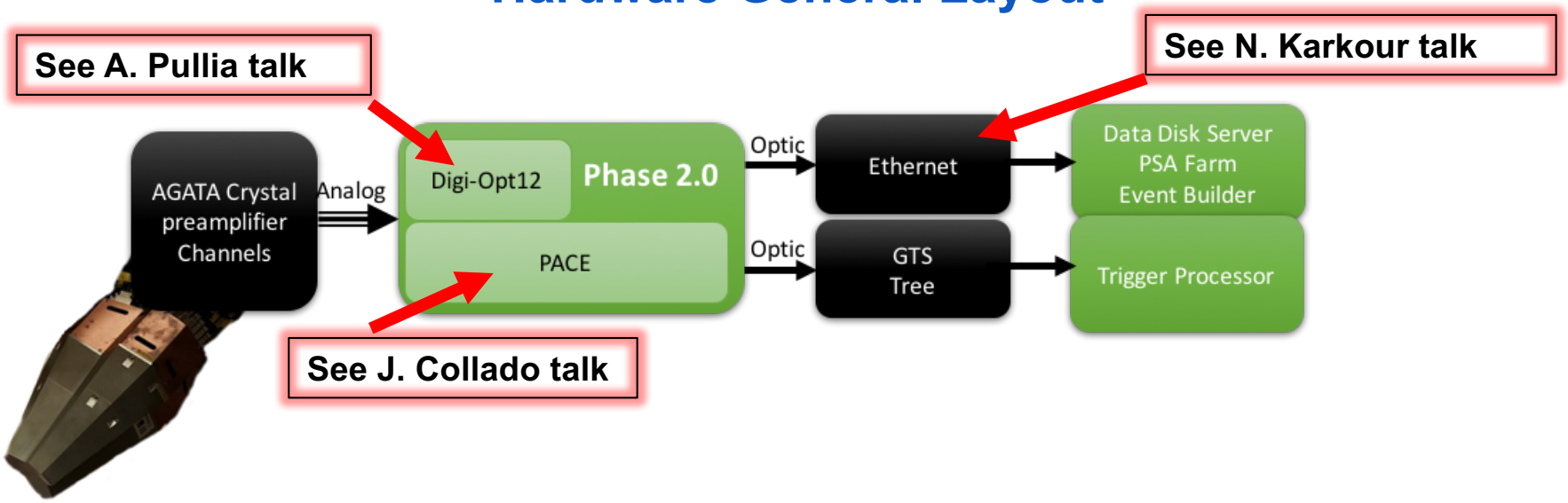
On going Technical Proposal

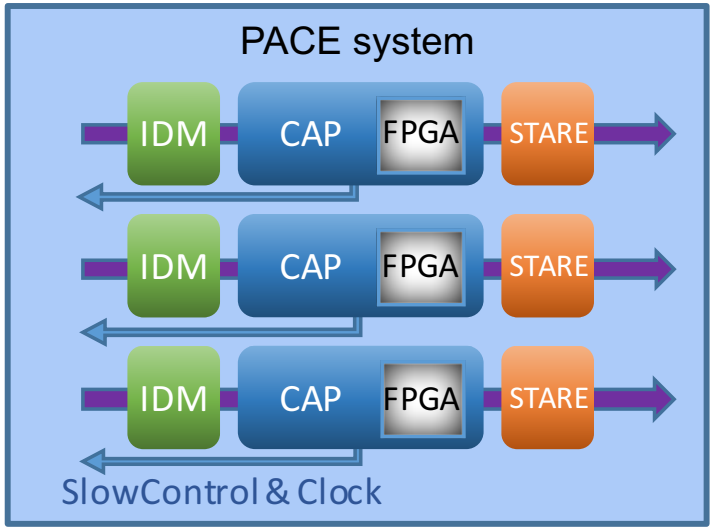
Important issues (cont'd)

- **Maintenance** of the system **by external companies highly recommended** to insure it through the life of the experiment independently of man power fluctuations in the collaboration.
- **Possibility to have a portable version** to install them in Scanning area, Acceptance Test labs, Host labs for detector maintenance labs so that results can be compared using the same instrumentation between experimental area and labs.
- **Built-in self tests and built in embedded software** so that the system can work **without network access to servers and complicated infrastructure**.

On going Technical Proposal

Hardware General Layout





PACE: Processing and Control over Ethernet
IDM: Input Data Mezzanine
Aggregates data to reduce the number of connections from DigiOpt12 to CAP
CAP: Control and Processing
Integrates the Control Card and GGP functionalities
STARE: Serial Transfer Acquisition Readout over Ethernet
Possible 10 Gb/s Ethernet connection mezzanine. Otherwise integrated in CAP.
GTSO: GTS Output
GTS leaf mezzanine

On going Technical Proposal

Hardware production

Construct during the design phase **the industrial production procedure with a private company** who can be **able to maintain, produce and buy** in advance specific components.

Objective: ensure that **every subsystem contains** the following items:

- **complete** design **description** document
- **manufacturing files** including all the special mounting notes and different constraints
- **purchase documents, ATP and ATR** (Acceptance Test procedure and report)
- **List of short lifetime parts**
- **Integration** documents and all the **production procedures**

On going Technical Proposal

Hardware maintenance

The **company** responsible for maintenance

- must insure **on the shelf enough spare parts**
- be able to **furnish** the AGATA collaboration **enough items to replace defected ones**
- must have **3rd level of Maintenance expertise** (visual verification, test bench tests, and power supply verifications plus JTAG programming test procedure) in order to repair defected cards. If the repair does not succeed, then help can be envisaged from the partners who designed the product.

On going Technical Proposal

Firmware General Layout

Firmware should integrate the **functionalities** of
- present **Control Card and GGP**
- **others** interesting for the physics, system maintenance, etc.
  - **preprocessing algorithms**
  - **oscilloscope mode**
  - …
- several ip's to develop

See L. Charles talk

Software General Layout

May need development but still under discussion

On going Technical Proposal

Documentation

- **All the work** should be **well documented** and available for future needs
- All this information, including user manuals, repairing manuals, technical descriptions, CAD files, VHDL codes, software, should be **placed in a computer space publicly accessible to all members of the collaboration**

Management

- General Coordination: A. Gadea (IFIC, Valencia)
- Hardware Coordination: V. González (TeDRA-ETSE, Valencia)
- Firmware Coordination: Strasbourg
- Software Coordination: not yet decided

Thank you for your attention