Agata Week 2017
Electronics phase 2
Ctrl & Processing f/w

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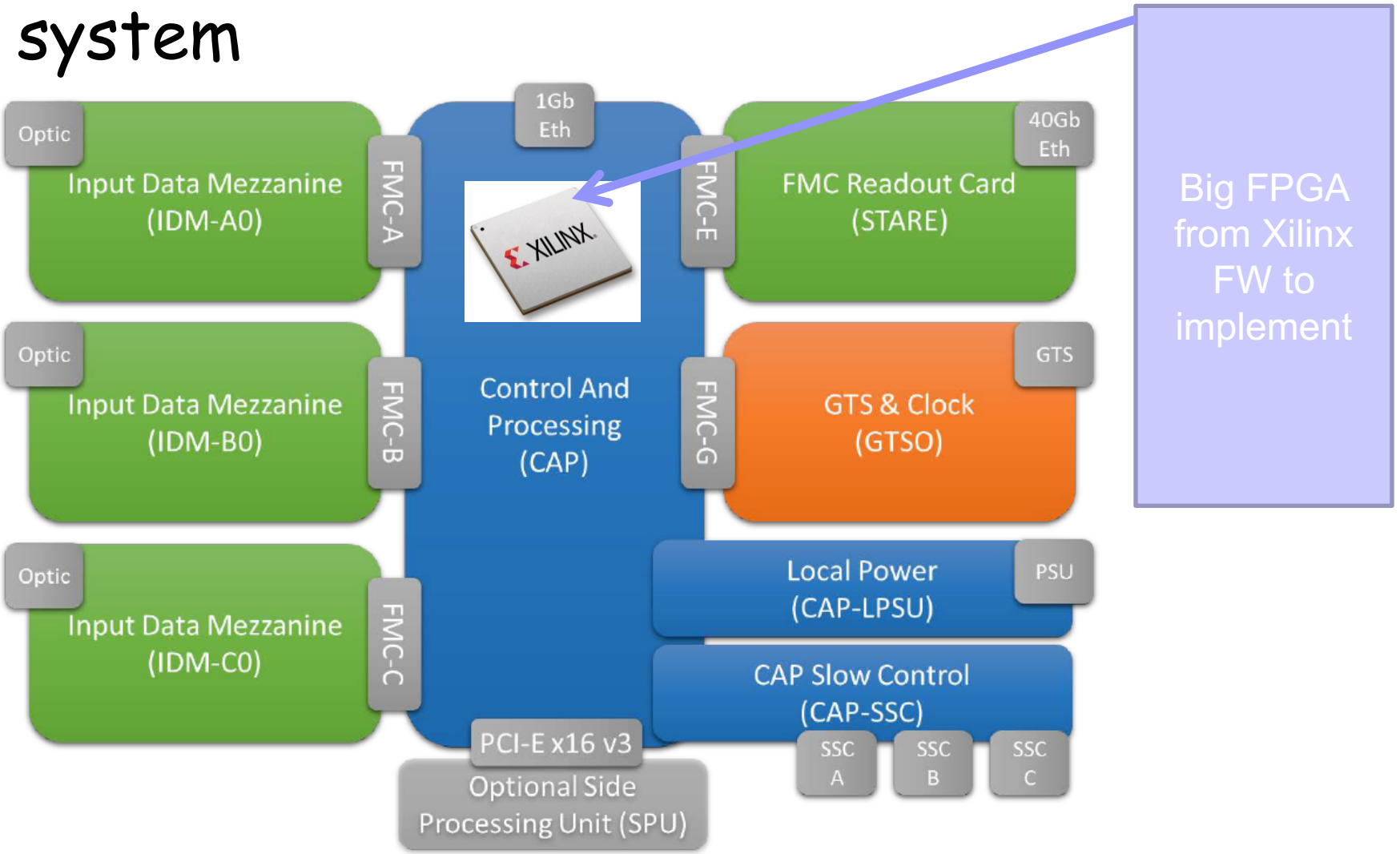
Outline

- Introduction
- Contributions from IPHC
- Todo list (at short & middle term)

Intro - General

- Remind of the schematic of the PACE system



Intro - General

- Functionalities to be implemented into the FPGA from the CAP board
- The FPGA should be well sized
  - The FGPA should be quite large to fit the whole logic
  - Checking & choice of the component done by Valencia
- The current GPP f/w could not be re-used
  - We have to perform the f/w design from scratch

Intro - General

- 5 main interfaces
  - Channels Receiver
    - Reception of the digitized channels coming optically from 3 IDM mezzanines designed by Valencia
    - 3 IDM ⇔ 3 crystals ⇔ 3 x 36 channels in all
    - Interface done by Valencia and include
      - Deserialization
      - Alignment
      - Buffering
      - Control signals
        - To indicate that the channels data are ready for the next block
        - From the slow control for initialization stage

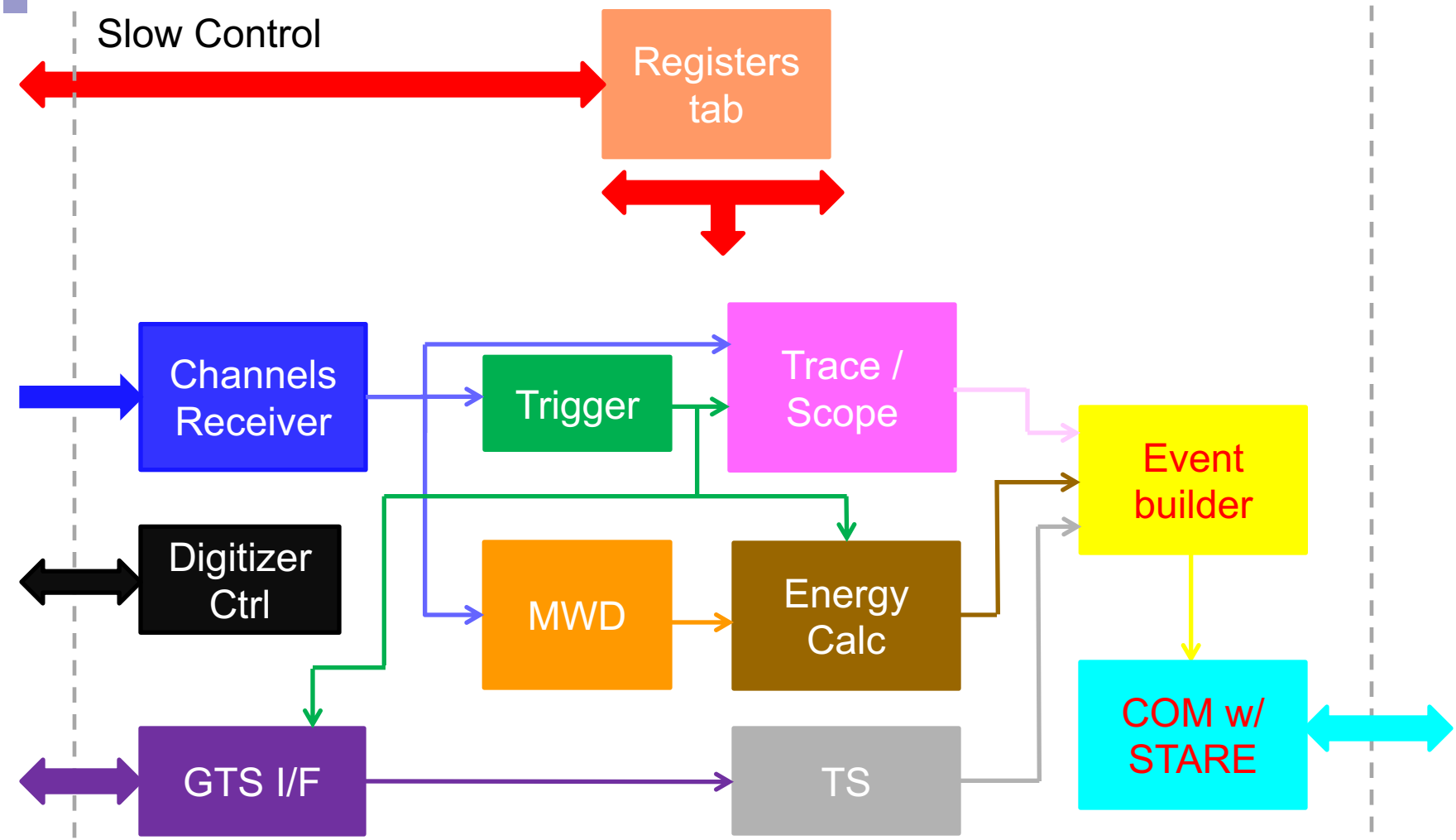
Intro - General

- Interface with the FMC readout board (STARE) designed by CSNSM
  - Communication path should be defined
    - Buffering via an external memory seems necessary before transferring data packets to the STARE board
- GTS interface
  - Available from NEDA project
  - Need to identify which person to contact
  - To be re-used and integrated in the global f/w
- Digitizer Controller
  - Which link?
  - Which config? offset, gain, internal settings ADC…
    - Depends on the choice of the component

Intro - General

- General Slow control
  - Useful to configure
    - All internal registers
    - IDM board (Digitizer) via the Digitizer Controller block
    - Registers tab should be well defined with an address range per functionality
  - Best option
    - 1 Gb-Eth / Ipbus interface
      - Link & protocol used for configuring and monitoring in the DAQ systems from CMS Upgrades phase 1 & 2
    - If BW should be saved on STARE board, the Ipbus interface could be extended to transfer channel data in scope mode
      - To do long trace analysis
      - To configure properly the channel settings (trigger, MWD) before an acquisition run

Intro - Simplified block diagram



Contributions from IPHC

- Dev of the f/w and a part of the s/w
  - Based on our experience in nuclear physics from
    - Past
      - TNT2 card still used
      - Digitizer from Agata Phase 0 in Stand Alone Mode => re-use of the algos from TNT2
    - Present: Stella project for nuclear astrophysics
      - DSSD acquisition from 96 channels split on 4 AMC boards plugged in one microTCA crate
      - Ipbus readout
      - Migration of the algos from TNT2 to Kintex-7 FPGA
      - In operation at Orsay
  - Based on our CERN activities
    - Notably Ipbus used in CMS Tracker Upgr. Ph. 1 & 2

Contributions from IPHC

- Dev in interaction with the contributors
  - CSNSM concerning the readout part
    - COM FPGA(CAP) ⇔ FPGA(STARE)
      - External memory for buffering
    - Def of the data format
    - Def of the acquisition modes
      - Energy mode
      - Scope mode
      - Mix-mode?
    - Scope mode seems important for diagnostic purposes
      - Dev of a versatile & flexible s/w plug-in for displaying sampled data or processed data
        - Need requests from the users to define the features and limitations of the tool to dev
        - A doodle will be early proposed by E. Legay

Contributions from IPHC

- Valencia for the Channels Receiver
  - Deserializing, alignment of the channel data
    - Test bench with an eval kit from Xilinx
  - Integration of this block in the global f/w
- People from NEDA project for the GTS I/F
  - Need to identify the person(s)

Todo list (at middle term)

- Task1: writing of a working document
  - Which will be iterated

Todo list

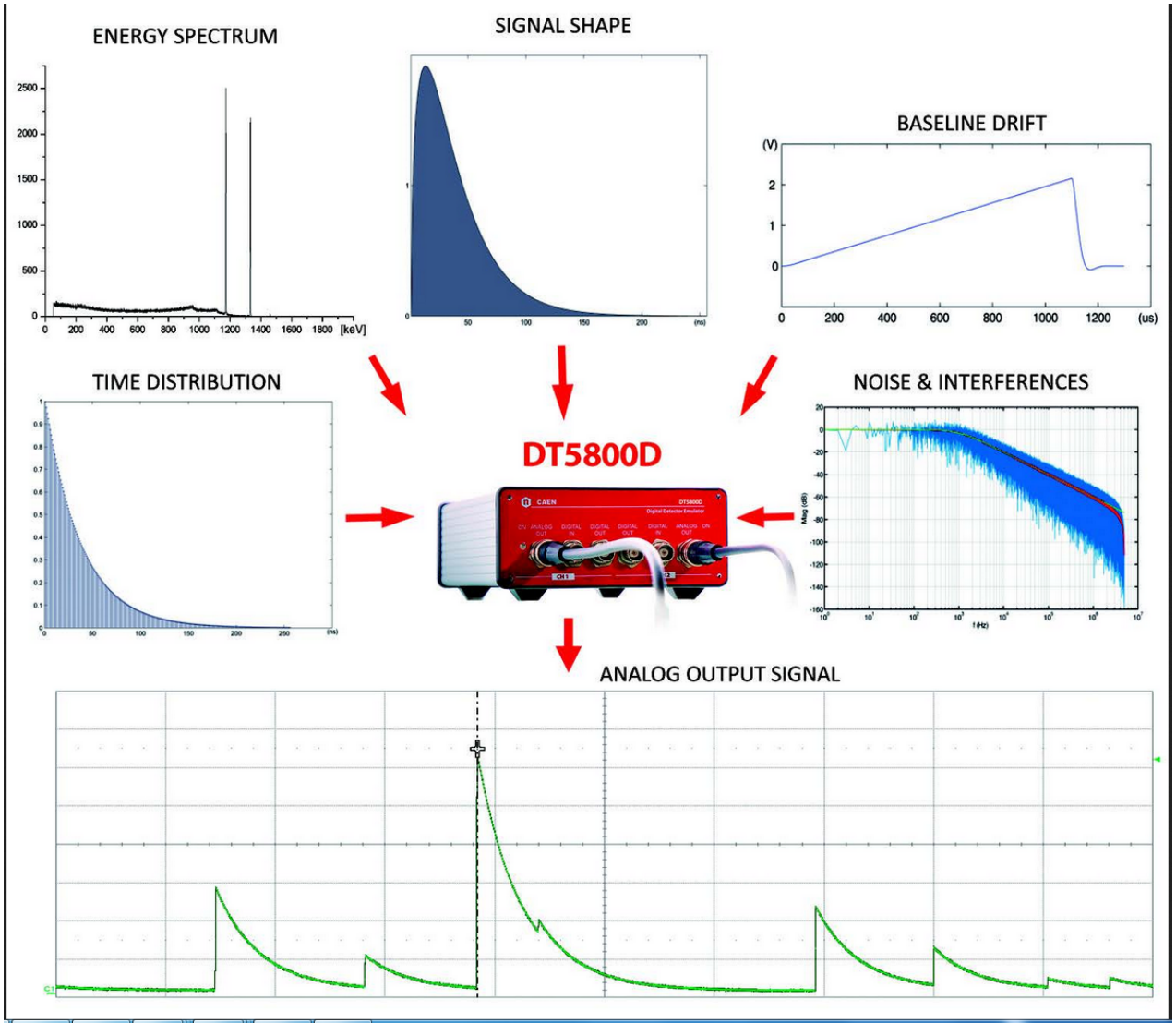
- Task2: migration of the algos
  - Towards the evaluation kit chosen by Valencia
  - Dev of scalable code to generate n instances of algos derived from TNT2 (MWD & Trigger) via generic parameters
  - Utilization reports from Vivado Tool from Xilinx
    - Check if the stats match the stats from Valencia
  - Performance measurements of the digitizer
    - Add Gb-Eth/Ipbus interface to acquire data?
      - Need a data format for the test bench
    - Comparison of the performances against
      - The current electronics
      - Others boards (TNT2, etc.)

Todo list

- Task2: MWD improvements
  - Other implementations are possible but need to be tested and compared
    - Eg. Bipolar mode avoiding the BLR (baseline restorer)
    - Christian could test it in s/w
      - Need same data set from Agata experiments for cross verification
    - FW coding and checking on board
  - Note: our team has the Desktop Digital Detector Emulator DT5800 from CAEN

Todo list

DT5800D from CAEN



Todo list

- Task3: Trigger improvements
  - Pulse discrimination of individual channel
  - At the beginning of dev => Re-use of this one from TNT2
  - Do some s/w models exist?
    - Which could be tested by Christian before beginning a FW migration

Todo list

- Task4: Compression algo
  - Should be done on the f/w before transferring data packets to STARE
  - Zero suppress
  - Were some models already studied?