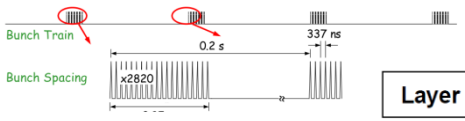
CMOS for HEP experiments :
Focus on ILC vertex detector

- ILD VXD requirements
- Axis of CMOS Pixels Sensors R & D

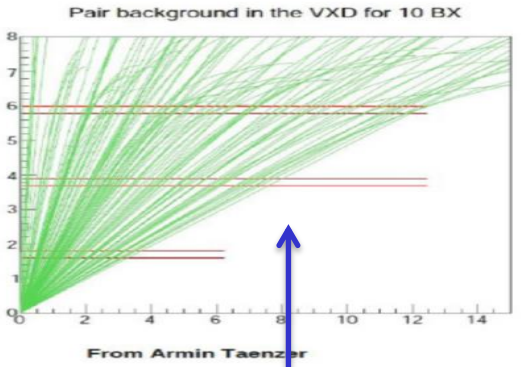
Reminder: ILD Vertex Detector requirements (DBD @ 500 GeV)



#Hits/cm^2/BX with anti-DID (Detailed Baseline Design)

Layer	1	2	3	4	5	6
0.5 TeV	6.3±1.8	4.0±1.2	0.25±0.11	0.21±0.09	0.05±0.03	0.04±0.03
1 TeV	11.8±1.0	7.5±0.7	0.43±0.13	0.36±0.11	0.09±0.04	0.08±0.04

cf. A. Perez *Preliminary results on recent beam backgrounds estimation in ILD (with and without antiDID)*



- Physics: Mat. budget and granularity

$$\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$$

(a & b parameters)

  - $\sigma_{R\phi}$ ~ 3 μm (pitch ~ 17 μm)
  - O(0.15%X_0/layer) + 0.14%X_0 (beam pipe)
- Experimental constraints
  - Occupancy (Beam background)

~ 5 part/cm^2/BX ⇨ few % occupancy max ?

  - Radiation hardness :

O(100 kRad) & O(1x10^{11} $n_{eq\ (1MeV)}$) /yr

  - Power dissipation :

~ 50 mW/cm^2 ⇨Power cycling, ~3% duty cycle

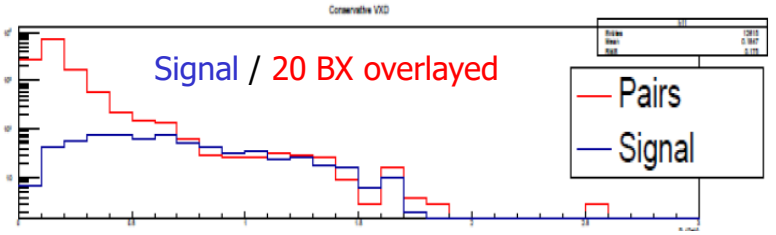
Beam background

- Low momentum (10-100 MeV/c) real tracks !
- uncertainties on M.C. simulations / final geom.

⇨ Safety factors needed (> x5)

- Vertex detector roles:
  - ⇨ b/c/τ-tagging
  - ⇨ Stand alone tracking capabilities (low pT)
  - ⇨ VTX/Jet charge determination, etc.
- Lower occupancies means
  - ⇨ Reduced combinatorial to reduce fake tracks
  - ⇨ Reduced pile-up for physics analysis

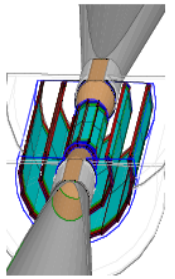
$\chi^{\pm}$ pair prod.



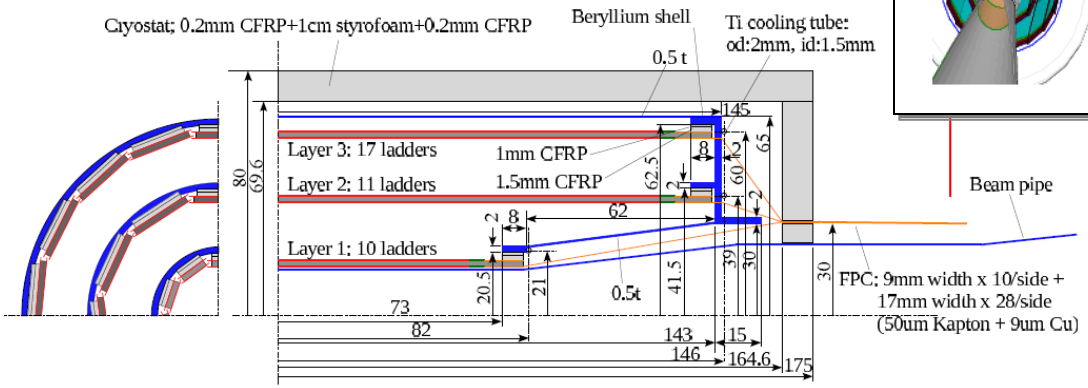
G.Voutsinas (DESY), ECFA 2016

⇨ Strong motivations to get reduced occupancy / faster read-out

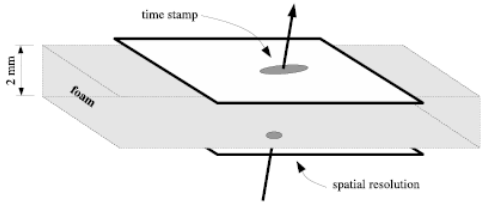
ILD: Vertex detector

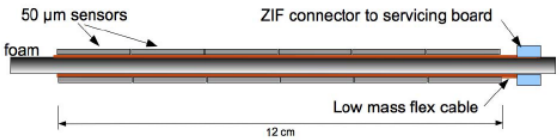


- Layout (DBD geometry):
  - Long Barrel approach
  - Radius: ~15 mm – 60mm
  - 3 x double sided ladders
    - Optimize material budget / alignment.
    - Stand alone tracking improvment
    - Background tagging capabilities
    - Other option: 5 single sided layers
  - Layers 1 & 2:
    - Priority to read-out speed & spatial resolution
    - Small pixels: 17 x 17 / 33 μm^2
    - Binary charge encoding
    - Read-out time ~ 50 / 8 μs
    - σ_{sp} ~ 3 / 5 μm
  - layers 3 – 6
    - Optmized for power comsumption
    - Large pixels (25/35 x 35 μm^2)
    - 3-4 bits charge encoding
    - Read-out time ~ 60 μs
    - σ_{sp} ~ 4 μm



	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ (μs)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6	10
Layer 3	37	125	0.96	4	100
Layer 4	39	125	0.95	4	100
Layer 5	58	125	0.91	4	100
Layer 6	60	125	0.9	4	100



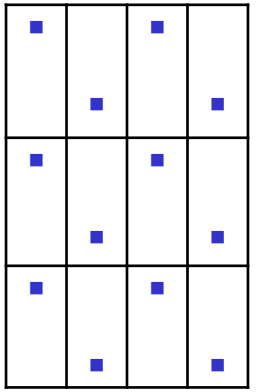


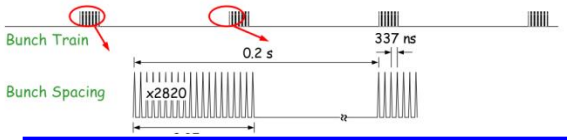
The occupancy : squaring the circle

- How to decrease occupancy if needed ?

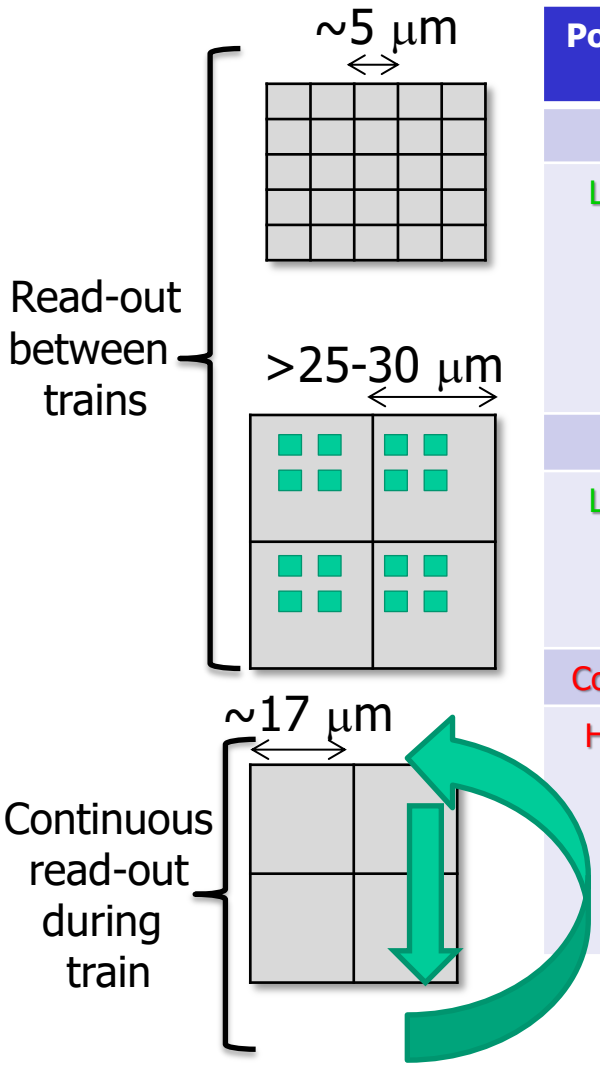
$$\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$$

  - Increase read-out speed ?
    - Enlarge pixel pitch ⇨ deteriorate spatial resolution (⇨ 2-3 bits instead of 1 bit output ?)
    - Elongated pixels ⇨ improved read-out speed while keeping resolution not degraded too much
    - Increase power consumption
  - Smaller pitch ?
    - More pixel to read ⇨ decrease read-out speed ⇨less bunch time stamping
    - Effective if it compensates the number of superimposed BXs in one read-out
  - Decrease cluster multiplicity ? (BB tends to have large incident angles)
    - Full depletion / sensitive thickness : helps a bit (marginal effect)
    - Multiplicity – pitch – depletion – angle relation ⇨ multi-parameter space
  - Increase inner radius ?
    - Not really an option: Deteriorate σ_{IP} ⇨ $\sigma_{d_0}^2 = \frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}$
  - Increase B field ?
    - Not really a free parameter
  - Technology progress : the way to go ?
    - e.g. smaller feature size ⇨ less power consumption, more memories in pixels, etc.
    - Go lower than ~100 ns/row read-out time ? (more parallelism, asynchronous read-out, etc.)





Read-out strategies vs resolution/occupancy



Power	Time resolution	Spatial resolution	Advantages	Caveats
Fine pixels (e.g. FPCCD)				
Low	1 complete train	~ 1 μm	Spatial Resolution Hit separation Beam background tagging capabilities ? (cluster shapes)	⇨x16 #pixels to read-out in 200ms ⇨No time stamping ⇨Occupancy issues ?
In pixel circuitry to store hits with time stamping (e.g. chronopixels, SOI)				
Low	Single or few bunches (>~ 0.5 μs)	>~ 5 μm	Hit time stamping Well suited to outer layers	⇨BX time stamping storage in conflict with granularity
Continuous read-out during train (e.g. DEPFET, CMOS): rolling shutter or priority encoding.				
High	Few to 10s bunches (5-50 μs)	~ 3 μm	Time & spatial resolution compromise	Power cycling mandatory ? ⇨F(Lorentz) ~ 10^5 grams ⇨Distribute 100s Amps shortly before train ⇨heat cycles the ladders.

⇨ Figures may evolve significantly with R&D and access to new technologies
e.g. feature size ⇨Power, read-out speed, granularity, etc.
⇨Different options / room for mixed strategies ?
e.g. double sided ladders: 1-fast / 1-precise

Typical occupancy rate (layer 1, with DBD rates)

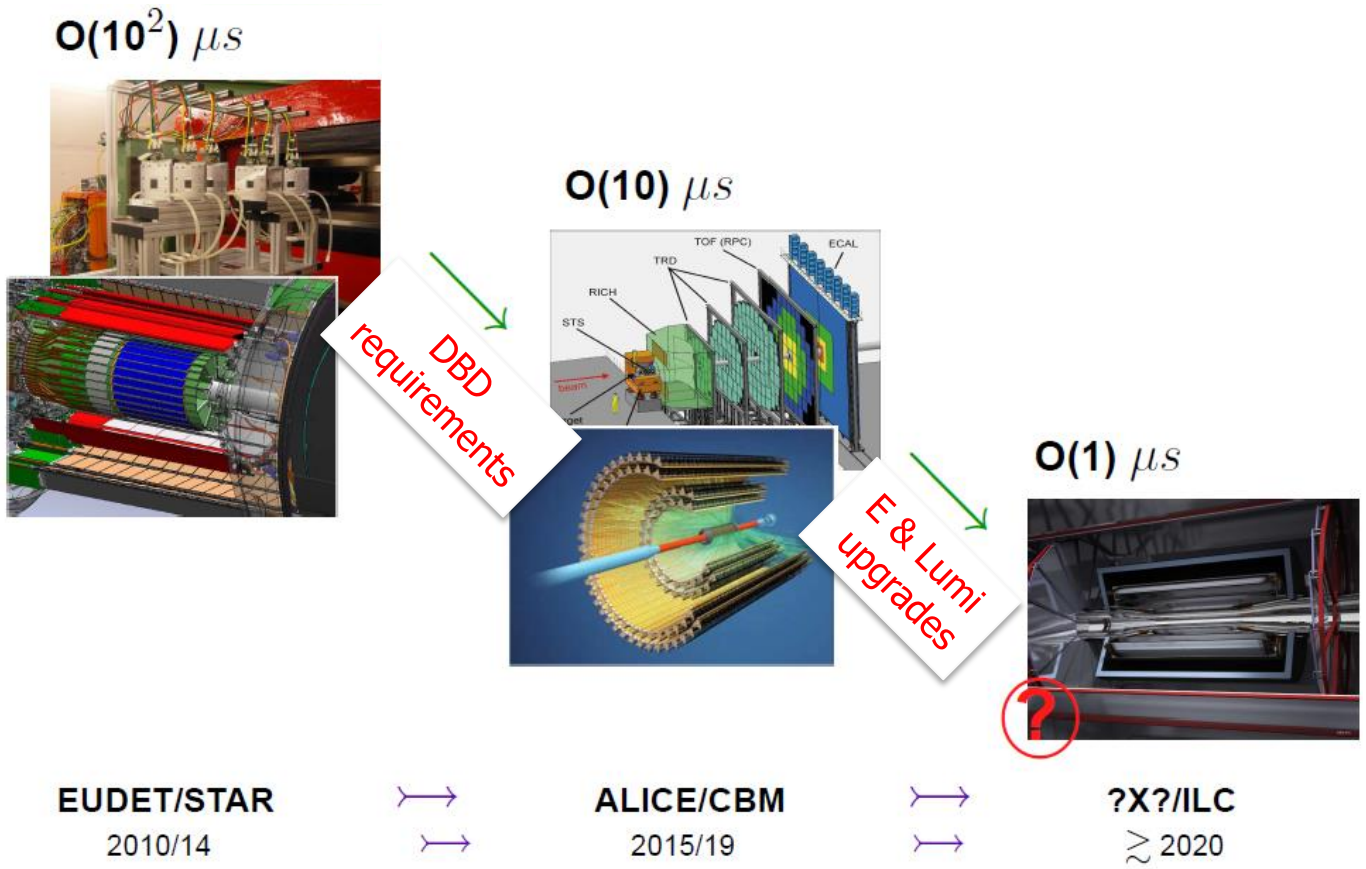
Pixel pitch	σ_{sp}	Read-out Time / time resolution	Assumed average cluster multiplicity	Lumi Mode (bunch Per train)	BX time spacing	√s	Assumed Expected Background	Expected background with safety factor 5	Occupancy	remarks
(μmxμm)	μm	(μs)	# pixels	B/train	ns	GeV	#hits/cm²/BX		w.o./w safety	
17x17	~3	50	5	Baseline (1312)	554	500	6	30	$8x10^{-3}$ / $4x10^{-2}$	DBD
17x17	~3	50	5	Upgrade (2625)	**366**	500	6	30	$1x10^{-2}$ / $6x10^{-2}$	Lumi upgrade
17x17	~3	50	5	1312	554	**250**	3	15	$4x10^{-3}$ / $2x10^{-2}$	250 GeV
17x17	~3	50	5	2500	366	**1000**	10	50	$2x10^{-2}$ / $1x10^{-1}$	1 TeV
17x17	~3	**25**	5	Baseline (1312)	554	500	6	30	$4x10^{-3}$ / $2x10^{-2}$	DBD X 2 faster
22 x 22	**~4**	4	5	Baseline (1312)	554	500	6	30	$1.5x10^{-3}$ / $8x10^{-3}$	Async. Read-out
25 x 25	**~5**	**1BX**	**3**	Baseline (1312)	554	500	6	30	$1x10^{-4}$ / $5x10^{-4}$	Bunch stamping
5 x 5	**~1**	**1 train**	**6**	Baseline (1312)	554	500	6	30	$1x10^{-2}$ / $6x10^{-2}$	Fine pixel BB tagging

Occupancy = (#hits/cm²/BX) x <mult> x (pitch)² x (r.o.time) / (BXtime) x safety

5 part/cm²/BX ⇨17x17 μm² pitch, cluster mult. ~5, 50 μs read-out time @ 0.5TeV on Layer 1 ⇨ ~ 1 %

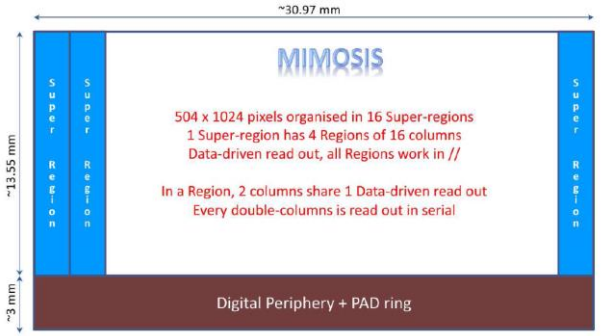
Read-out speed roadmap

- How to improve read-out speed ? while keeping
  - a spatial resolution in the 3-5 μm range
  - a material budget per layer in O(0.1-0.2)% X_0 range
  - a controlled power consumption and a controlled data flow.



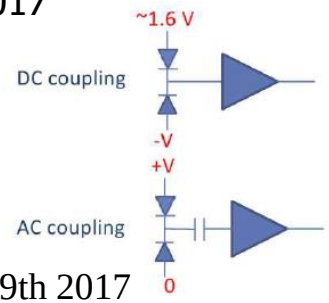
CMOS R&D : CBM-MVD

- Asynchronous (fast) read-out architecture
  - MIMOSIS = based on ALPIDE pixel readout (ALICE-ITS upgrade)
- Specifications:
  - σ_{sp} ~ 5 μm
  - r.o. time ~ 5 μs
  - Enhanced data flux: ~1.6 Gbits/cm^2/s (peak) ⇨ x 60 ITS rate
    - Revisited digital circuitry (data sparsification & transfer logic)
  - Enhanced radiation hardness: O(10 Mrad) & O(10^{14} $n_{eq(1MeV)}$)

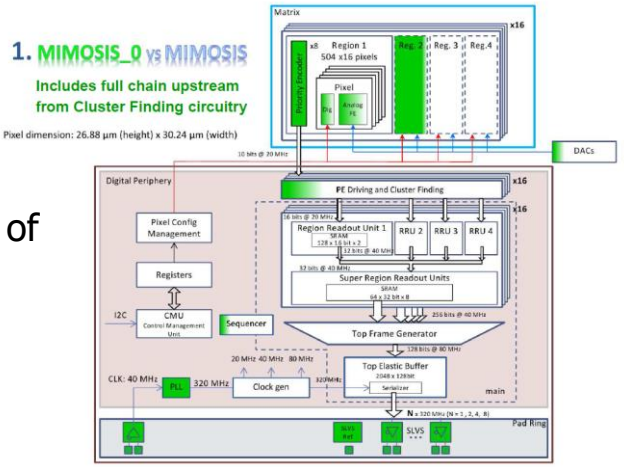


Pixel array & digital periphery developed in //

- MIMOSIS_0
  - Timing study of the data driven readout circuitry
  - DC & AC coupling foreseen to compare performances
  - Chip submitted in May 2017

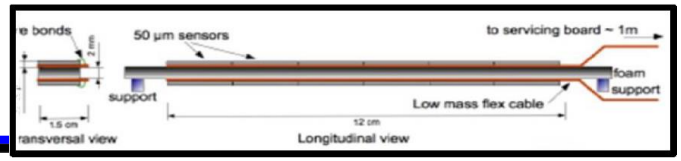


- Digital Periphery
  - Design underway
    - ✓ Physical implementation of the different block
    - ✓ Timing vs Chip length
    - ✓ Data rate
    - ✓ Power estimation
  - 1st full scale prototype ~ 2018

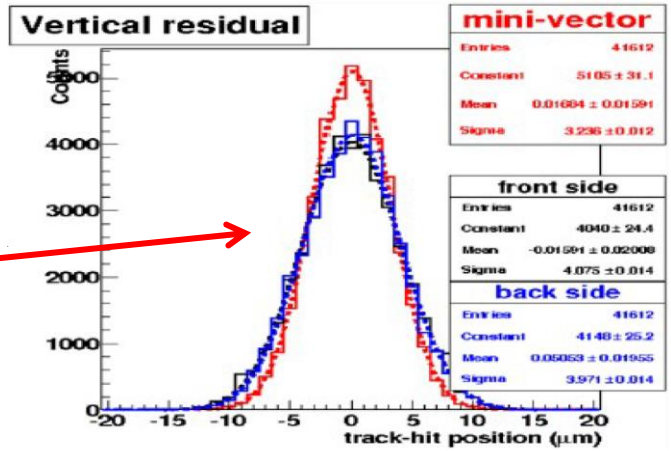


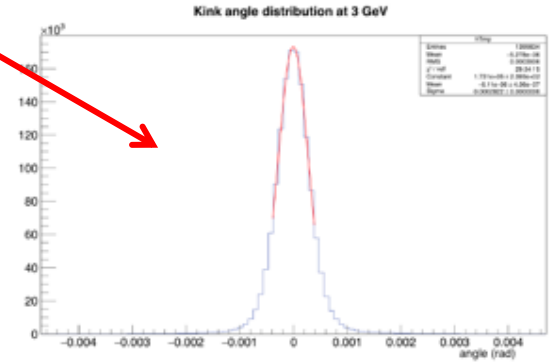
Final preproduction sensor in early 2020

Integration: PLUME collaboration



- Plume collaboration (Bristol, DESY, IPHC)
  - Double sided ladders with minimized material budget
- Plume 01 prototype (fab. 2012)
  - 2x6 Mimosa-26 on 2 mm foam SiC
    - <mat.budget> ~ 0.6 % X_0 + Air cooling
  - Successfully validated in test beam
    - Mat. budget checked in test beam with kink angle in sensitive area: Mes = 0.47±0.02 % X_0 (0.45 expected) (B.Boitrelle PhD)
- Plume 02 prototype ⇨ Reduced mat. Budget
  - Cu flex cable (0.42 % X_0)
    - 2 modules functional, 2 more expected
  - Al flex cable (0.35 % X_0)
    - 4 modules. Connectors issue ⇨ fix in 2017
  - 6 ladders expected (2 fabricated)
    - Modules functional. Tests ongoing in 2016
- Application: Beast @ SuperKEK-B
  - BEAST: beam background measurement For Belle II
    - Different detectors in inner volume
    - System integration being done at DESY with the other sub-systems
    - 2 Plume Ladders will be installed in 2017
- Next step: ≠ chips on each side





⇨ Ladders close to ILC mat.budget specifications

Towards smaller feature size: 180 nm ⇨110 nm

- Motivations
  - Small pixel dimensions
  - Faster read-out
  - Reduced power consumption
  - Other tech. options matters (# metal layers, deep P-well, etc.)
- Asynchronous read-out (à la ALPIDE from ALICE-ITS)
  - Extend ALPIDE architectures
    - Larger areas, power saving, uniformity, robustness while keeping low mat.budget, sp. resolution
  - Potential Benefit: Power cycling may not be necessary
    - Alignment issues ?

  ⇨ Ultimate read-out speed potential of O(few μs)
- New options
  - TowerJazz offers a mixed 110/180nm CIS process
    - 2017: submit prototype
  - 2 other CMOS factories offer access to 110 nm
    - Discussions with foundries going on (with CEPC)

⇨ Smaller feature size offers opportunities to get closer to ILC bunch tagging

ILD-VXD design options

- ILD-VXD Options DBD

	R (mm)	$\lvert z\rvert$ (mm)	$\lvert\cos\theta\rvert$	σ (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6	10
Layer 3	37	125	0.96	4	100
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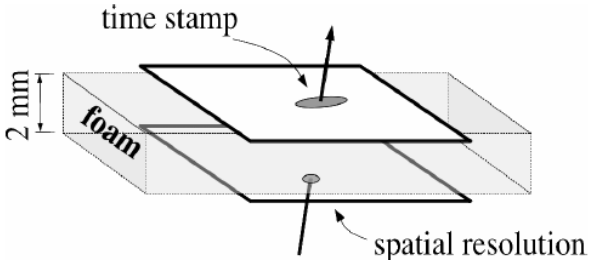
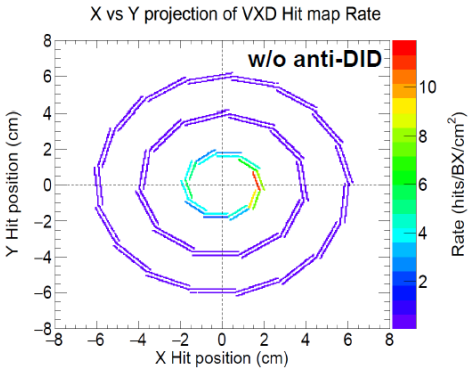


- CPS option achievable with our present knowledge
  - A la PLUME double sided ladders
    - Mat. Budget ~ 0.3-0.4 % X0 / ladder
  - A la ALPIDE/MIMOSIS option
    - 6 Layers with 22x22 μm^2 ⇨ σ~<4 μm & 4 μs

Software studies

LC Vertex Detector Workshop 2017
https://agenda.linearcollider.org/event/7450/



- **Alignement studies on th VXD**
  - Loic Cousin PhD (http://www.iphc.cnrs.fr/Loic-COUSIN.html)
  - Double sided ladders will help
  - Alignement with beam background tracks seems doable
- **Beam background MC production (Preliminary)**
  - A. Perez Perez
  - Goal:
    - New ILD software
    - Complete new MC production
    - Study background in the different detectors
    - Study different geomerties (anit-DID)
  - Results
    - Aniti-DID effect is moderate
    - Background mostly coming from central region (~75%). Backscatterd ~25%, VXD+beam pipe ~5%

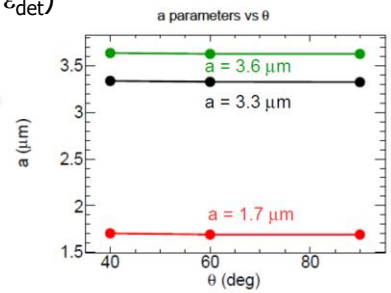
Layer	Units	DBD Prev	This Prod w/o antiDID	This Prod w/ anti-DID
1	Hits/BX/cm^2	6.32 ± 1.76	5.75 ± 0.02	4.35 ± 0.02
2		4.00 ± 1.18	4.05 ± 0.01	2.60 ± 0.01
3		0.25 ± 0.11	0.177 ± 0.001	0.137 ± 0.001
4		0.21 ± 0.09	0.134 ± 0.001	0.113 ± 0.001
5		0.04 ± 0.03	0.038 ± 0.001	0.031 ± 0.001
6		0.04 ± 0.03	0.033 ± 0.001	0.027 ± 0.001

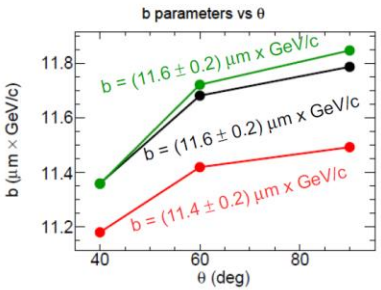
- **Analytical Tool to study design options: *Guariguanchi***
  - A. Perez, J. Baudot, Qian-Yuan LIU, A.B., M.W.

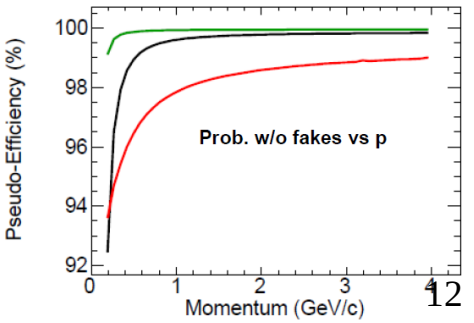
✓ **Inputs**
- Geometry + material budget (multiple scattering)
- Detector performances (σ_{sp} + $t_{r.o.}$ + ε_{det})
- Salt and Pepper beam background

✓ **Output**
- Impact parameter resolution
- Tracking pseudo-efficiency

- L1: 2.8 µm/ 50 µs, L2: 6 µm/10 µs, L3-6: 4 µm/ 100 µs (DBD)
- L1: 1.0 µm/800 µs, L2: 6 µm/0.5 µs, L3-6: 4 µm/ 4 µs
- L1-6: 4 µm/ 4 µs







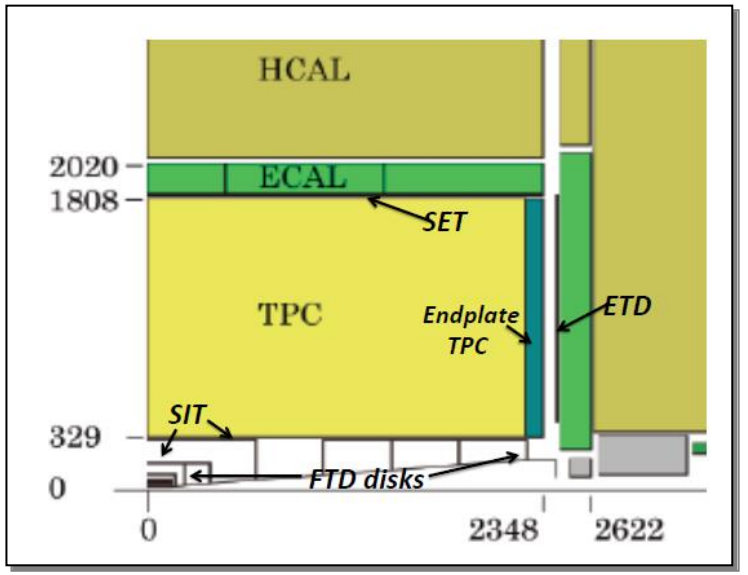
$$F\,a \oplus b / p\beta \sin^{3/2}\theta$$

Pixelated SIT ?

- Idea (beeing discussed in ILD)
  - Current design (Strips)

Barrel system				
System	R(in)	R(out)	z /mm	comments
- SIT	153	300	644	2 silicon strip layers $\sigma = 7\mu m$

SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
153	368	0.910	R: σ=7.0,	307.7 (153.8)	0.65
300	644	0.902	z: σ=50.0	σ=80.0	0.65



  - Replace it by pixels: no technology showstopper a priori.
    - Possibly double sided pixels to get 4 hits
    - ~ same material budget and σ_{sp} ~ 5-7 μm
    - Occupancy expected to be small: local peak occupancy (inside jets) needs to be checked

⇨ Seems doable with MIMOSIS approach (~5 μm + few bunches (1-4) time stamping)

- Pros
  - Time stamping of tracks and better resolution
    - Either fast detector (O(BX)) or memory buffer with read-out between train
    - Moderate expected occupany could allow read-out between train
  - Track seeding for pT >~150 MeV

⇨ Track seeding + time stamp should help to disentangle physics tracks from beam background

Summary

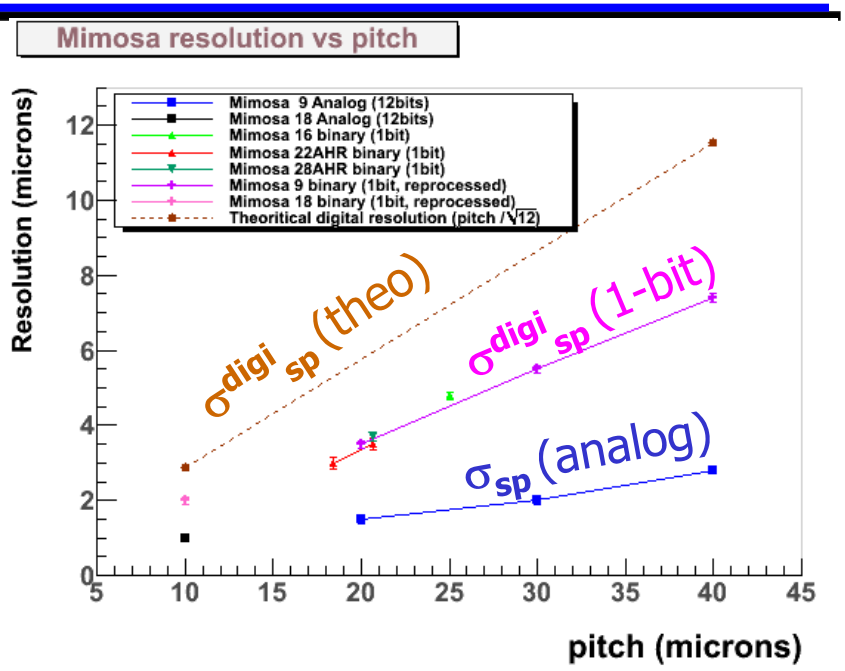
- ILD VXD requirements
  - The VXD challenges in the coming years:
    - Parameters space optimization = refining the requirements
    - Integration issues (EMI, Power & cooling, mechanics, data flux, etc.)
  - CPS offers a very good compromise in terms of:
    - Spatial resolution
    - Read-out speed
    - Material budget
    - Power consumption
    - Radiation hardness

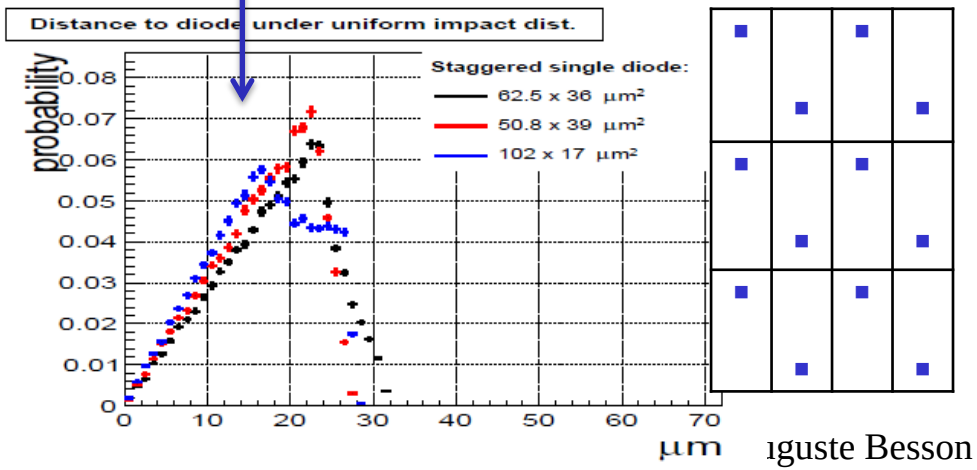
- Still room for new ideas and improved performances
  - CPS Technology still evolving
  - Combining technologies ?
  - New geometries ?
  - Disks and SIT ?

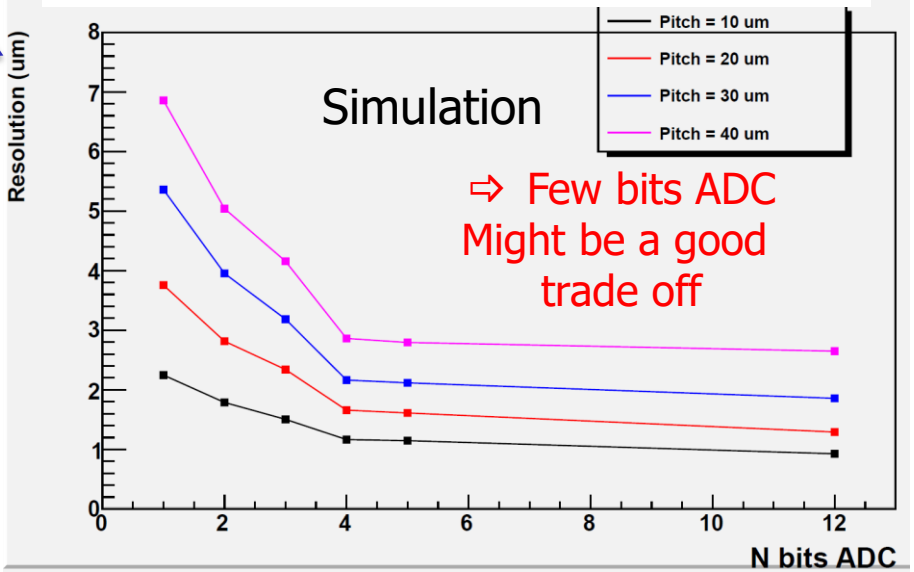
Back up

Resolution and pitch: what CPS can offers

- Resolution governed by
  - Pitch
  - S/N & Collecting diode
    - Charge sharing
    - epi. thickness, resistivity, etc.
  - Signal encoding (binary or ADC)
- Pitch impact
  - $\sigma_{sp} \propto$ pitch (~linear)
- Signal encoding
  - e.g. σ_{sp}(1bit, ~17 μm)
  ~ σ_{sp}(2bits, ~23 μm) ~ 3 μm
- Staggered pixels
  - Preserve resolution in both direction







Short term: CBM-MVD

- CBM-MVD @ FAIR (~2019-2020)

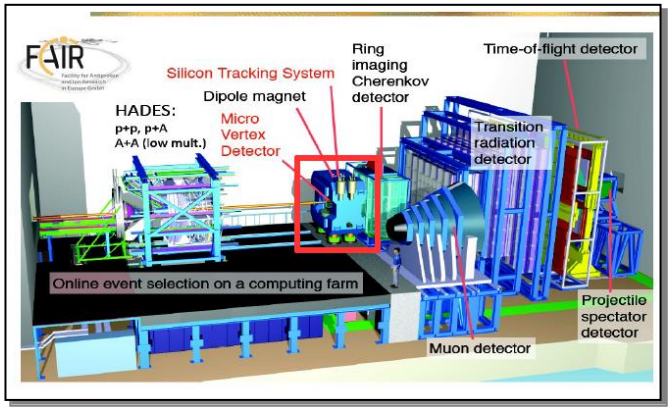
  0.18 μm deep P-well, based on ALPIDE design.

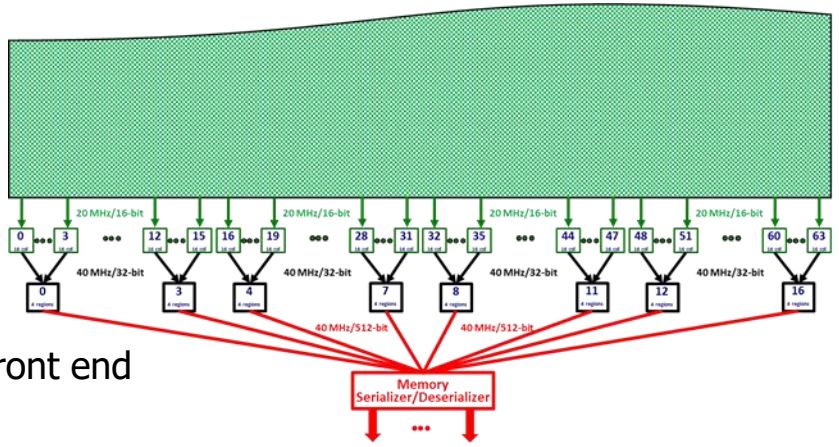
  – Requirements & Design
    - Pitch ~ 22x33 μm^2 ⇨ σ_{sp} < 5 μm ;
    - Time resolution = 4 μs
    - 4 stations of CPS
    - x2 Data transmission rate (up to x10 for local hit density)
    - peak hit rate @ 7 x 10^5 /mm²/s ⇨ >2 Gbits/s

    ⇨ more buffer & serializer
    - Rad.tol. x 10 w.r.t. ALICE-ITS : 3x10^{13} n_{eq}/cm^2/yr & 3 MRad/yr (with replacement every year)
    - Vacuum compatible & Negative temp. operation

  – Status
    - ongoing design
    - Pixel + priority encoder designed
    - digital part ongoing
    - Amplifier modified w.r.t ALPIDE

  – 1st testing chip MIMOSIS
    - 64 col x 512 rows chip to tests architecture / front end
    - Submission: Feb. 2017

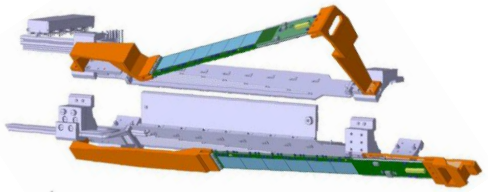


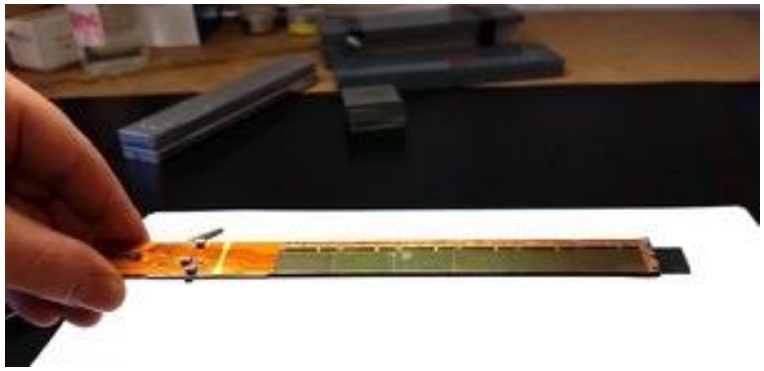


⇨ architecture adaptable to a fast sensor for an ILC vertex detector

Other development: PLUME for BEAST 2@ SuperKEK-B

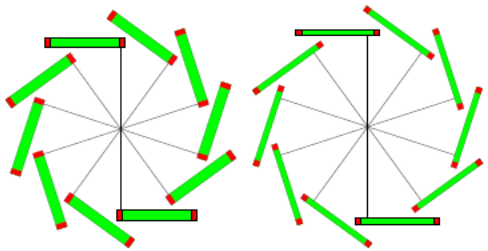
- Goal: beam background measurement For Belle II
  - Different detectors in inner volume
- Spin-off for ILC:
  - operation of PLUME ladders in real conditions
  - Exploiting the minivectors produced to help reconstructing soft electron trajectories
- Plume 02 prototype ⇨ Reduced mat. Budget
  - Cu flex cable (0.42 % X_0)
  - 2 ladders functional, 2 more for spares by June
- Timeline:
  - Q4 2017: Installation & comissioning
  - Q1 2018: Start of data taking
- Next steps:
  - finalize Al flex cable (0.35 % X_0)
  - Beam test @ DESY in 2017-18

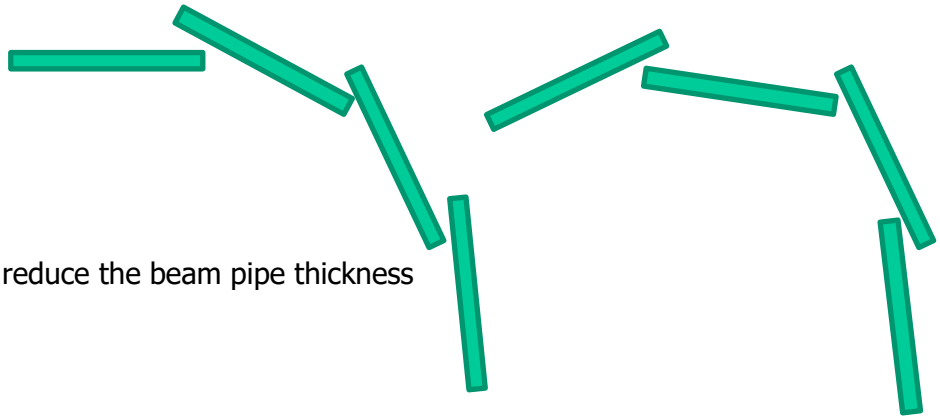




Geometries ?

- Long barrel vs endcap disks
  - Double sided ladders : added value in standalone tracking
    - -> helicoidal geometry ?
    - Mat. budget vs acceptance issues ?
    - Read-out periphery (techno. dependant)
- Spacing in double sided layers (2mm ⇨ 1.5mm ?)
    - Large spacing: more rigidity, more angular resolution
    - Small spacing: Mini-vector building, Mat.Budget
- Number of ladders
  - Probably 10 in Layer 1-2 ?
  - 1 or 2 radius ?
    - Mat. budget vs acceptance (low pT) trade off
- Beam pipe
  - 500 μm Be @ R = 1.5 cm
  - Mechanical constraints: Reducing the Radius allows to reduce the beam pipe thickness
- Faraday cage ?
- Revisiting numbers ?
  - All accepted numbers tends to become a tradition (i.e. one forgets their origin)
    - e.g. power, a ⊕ b parameters, geometry, read-out speed, etc.



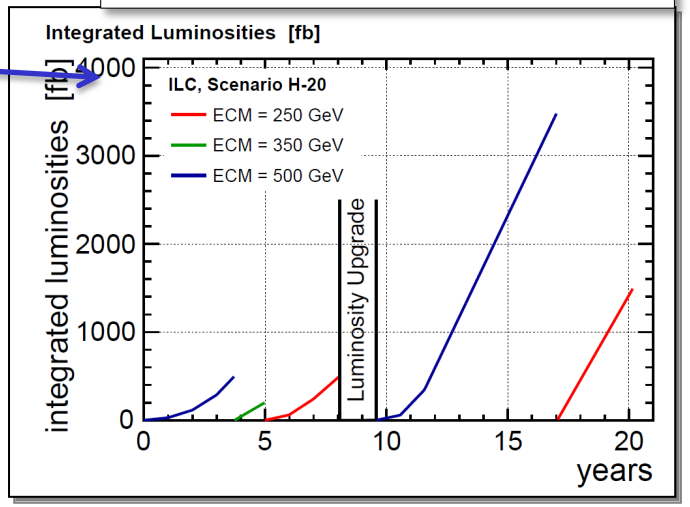


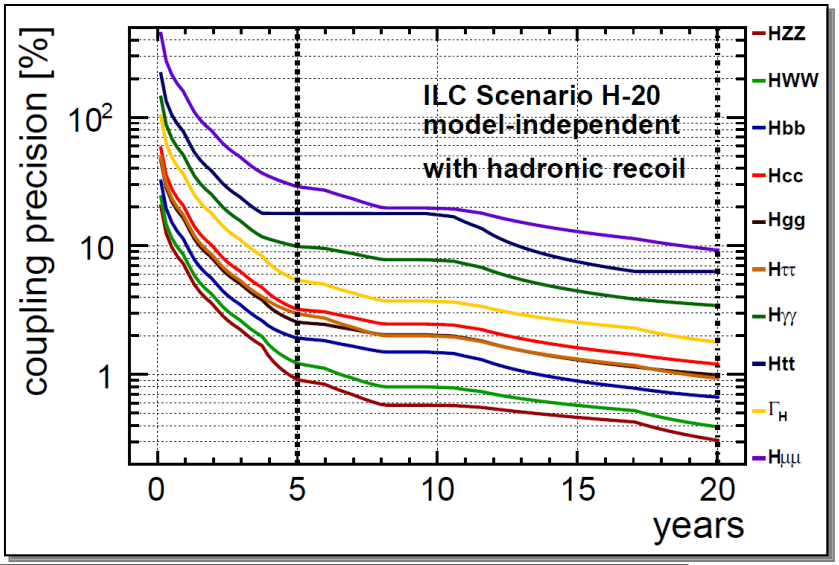
⇨ cf. A. Perez *Analytical tool to study vertex detector configurations*

Ramping scenarios: √s = 250 GeV/500 GeV ?

ILC Operating scenarios
T. Barklow et al. ILC-NOTE-2015-068

- Standard scenario
- LCWS 2017 (Morioka):
  - Ramping scenario starting @ √s = 250 GeV is considered very seriously
- What are the consequences for the VXD ?
  - Significant Beam background reduction expected
- Typical values:
  - 500 GeV ⇨250 GeV will divide #hits/cm²/BX by ~ 2
  - BUT:
    - Luminosity scenarios are different
    - Enhanced luminosity @ √s = 250 GeV would counter balance the Decrease of background due to lower energy.
    - LEP/SLD history: L was finally much higher than the baseline



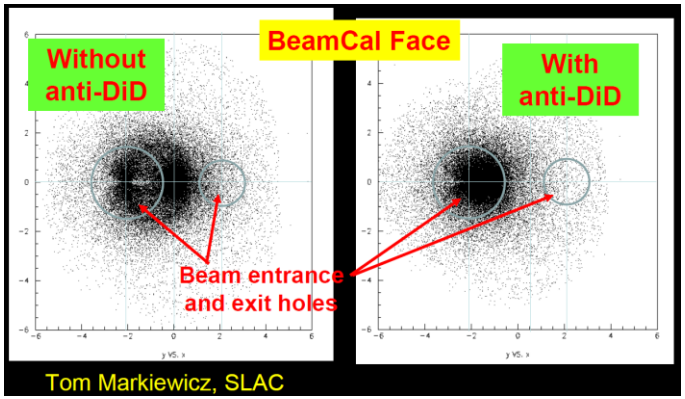


⇨ A running scenario starting with √s = 250 GeV does not change that much the picture

Anti-DID and IR configurations

LC-DET-2012-081
Conceptual Design of the ILD Detector Magnet System

- Idea: Additional Dipole located in the outer radius of the main solenoid
- Expected effect
  - Dipole field ~0.035 T @ z = 3 m)
    - guides particles in the forward region
  - Forward detectors: reduces background significantly
  - VXD: Reduces backscattered particles



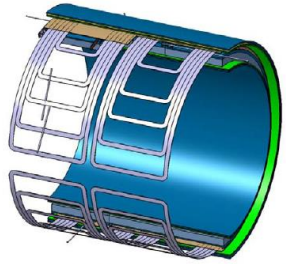


Figure 13: 3D view of the anti-DID (version 1).

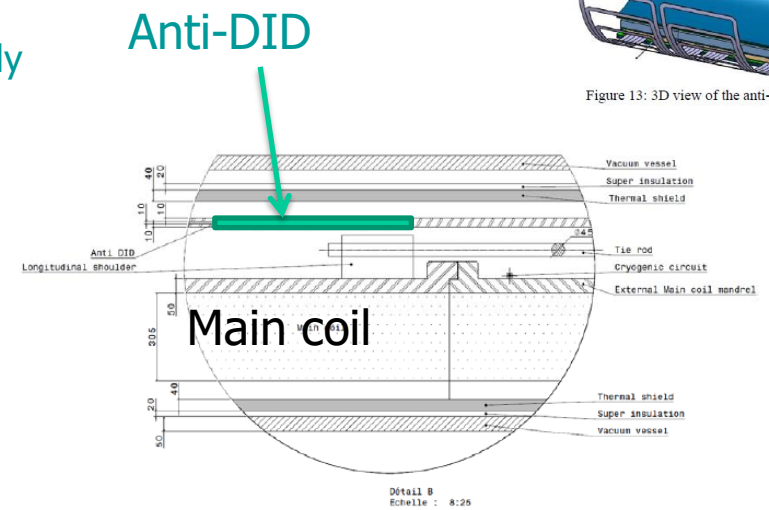


Figure 15b: Integration of the anti-DID in the cold mass (detail B).

  - Effect on the luminosity due to the spreading of the beam ?
- Task force in ILD (ongoing)
  - Explore the different design options
    - Cost & design studies
  - A priori: VXD not expected to drive the final decision
    - Order of magnitude: < Factor 2 effect.
    - Needs to be confirmed
  - New MC samples beeing produced and analyzed (cf. A.Perez talk)

ILC parameters (DBD)

			Baseline 500 GeV Machine			1st Stage	L Upgrade	E_{CM} Upgrade	
								A	B
Centre-of-mass energy	E_{CM}	GeV	250	350	500	250	500	1000	1000
Collision rate	f_{rep}	Hz	5	5	5	5	5	4	4
Electron linac rate	f_{linac}	Hz	10	5	5	10	5	4	4
Number of bunches	n_b		1312	1312	1312	1312	2625	2450	2450
Bunch population	N	$\times 10^{10}$	2.0	2.0	2.0	2.0	2.0	1.74	1.74
Bunch separation	Δt_b	ns	554	554	554	554	366	366	366
Pulse current	I_{beam}	mA	5.8	5.8	5.8	5.8	8.8	7.6	7.6
Main linac average gradient	G_a	MV m^{-1}	14.7	21.4	31.5	31.5	31.5	38.2	39.2
Average total beam power	P_{beam}	MW	5.9	7.3	10.5	5.9	21.0	27.2	27.2
Estimated AC power	P_{AC}	MW	122	121	163	129	204	300	300
RMS bunch length	σ_z	mm	0.3	0.3	0.3	0.3	0.3	0.250	0.225
Electron RMS energy spread	$\Delta p/p$	%	0.190	0.158	0.124	0.190	0.124	0.083	0.085
Positron RMS energy spread	$\Delta p/p$	%	0.152	0.100	0.070	0.152	0.070	0.043	0.047
Electron polarisation	P_-	%	80	80	80	80	80	80	80
Positron polarisation	P_+	%	30	30	30	30	30	20	20
Horizontal emittance	$\gamma\epsilon_x$	µm	10	10	10	10	10	10	10
Vertical emittance	$\gamma\epsilon_y$	nm	35	35	35	35	35	30	30
IP horizontal beta function	β_x^*	mm	13.0	16.0	11.0	13.0	11.0	22.6	11.0
IP vertical beta function	β_y^*	mm	0.41	0.34	0.48	0.41	0.48	0.25	0.23
IP RMS horizontal beam size	σ_x^*	nm	729.0	683.5	474	729	474	481	335
IP RMS veritcal beam size	σ_y^*	nm	7.7	5.9	5.9	7.7	5.9	2.8	2.7
Luminosity	L	$\times 10^{34}$ cm^{-2}s^{-1}	0.75	1.0	1.8	0.75	3.6	3.6	4.9
Fraction of luminosity in top 1%	$L_{0.01}/L$		87.1%	77.4%	58.3%	87.1%	58.3%	59.2%	44.5%
Average energy loss	δ_{BS}		0.97%	1.9%	4.5%	0.97%	4.5%	5.6%	10.5%
Number of pairs per bunch crossing	N_{pairs}	$\times 10^3$	62.4	93.6	139.0	62.4	139.0	200.5	382.6
Total pair energy per bunch crossing	E_{pairs}	TeV	46.5	115.0	344.1	46.5	344.1	1338.0	3441.0

½ gradient
Initial Higgs factory

Baseline

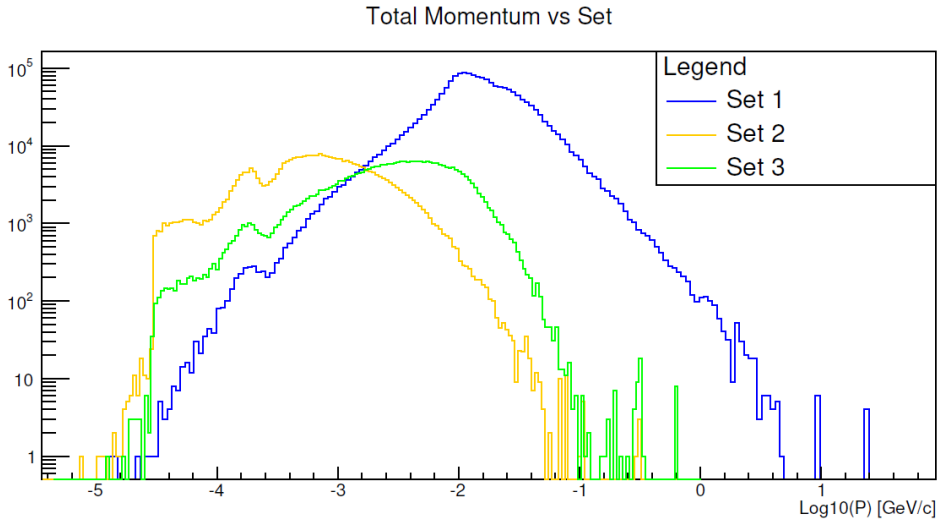
½ length
(Option 1e phase)

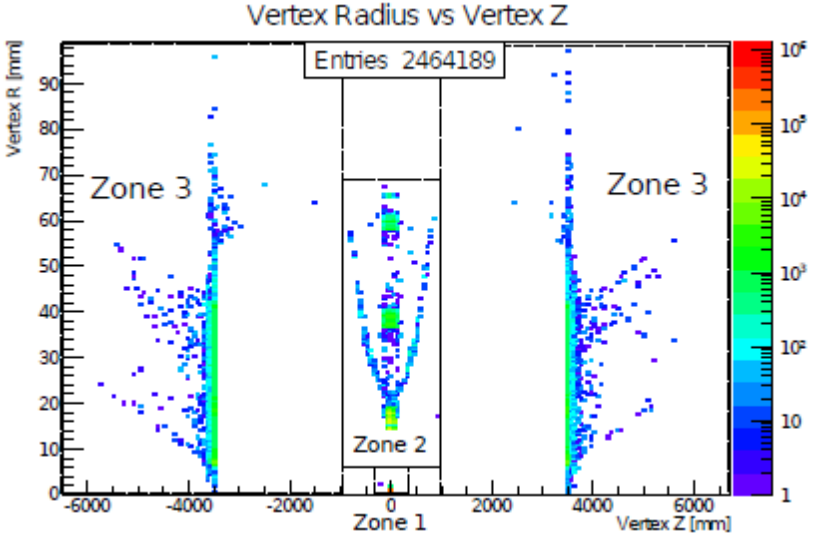
Lumi
upgrade

1TeV upgrade

Beam background features.

L.Cousin PhD



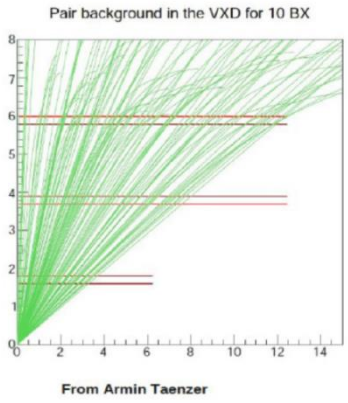


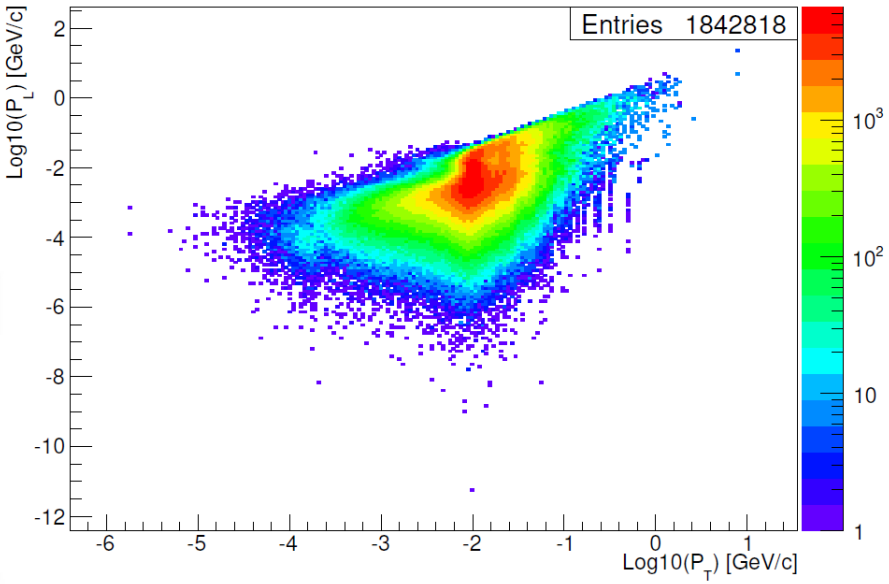
- Origin of background:

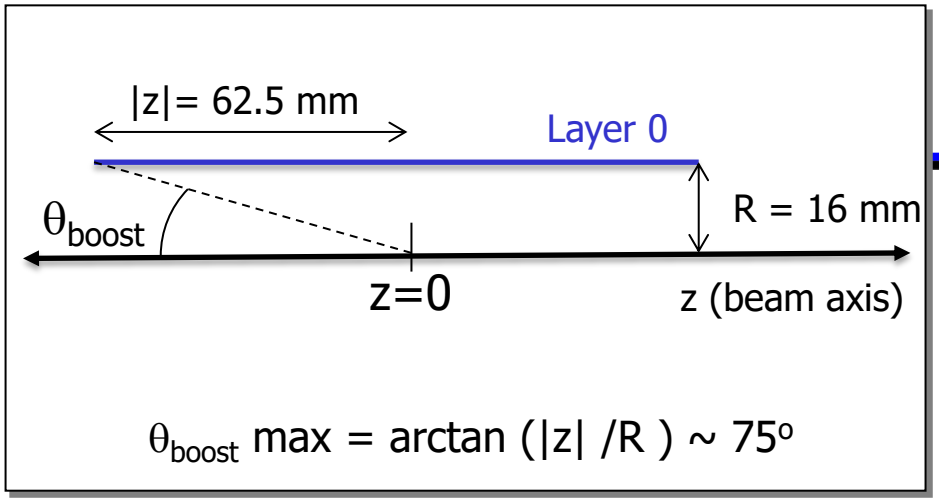
Zone 1 = interaction region
Zone 2 = detector region
Zone 3 = backscattered particles

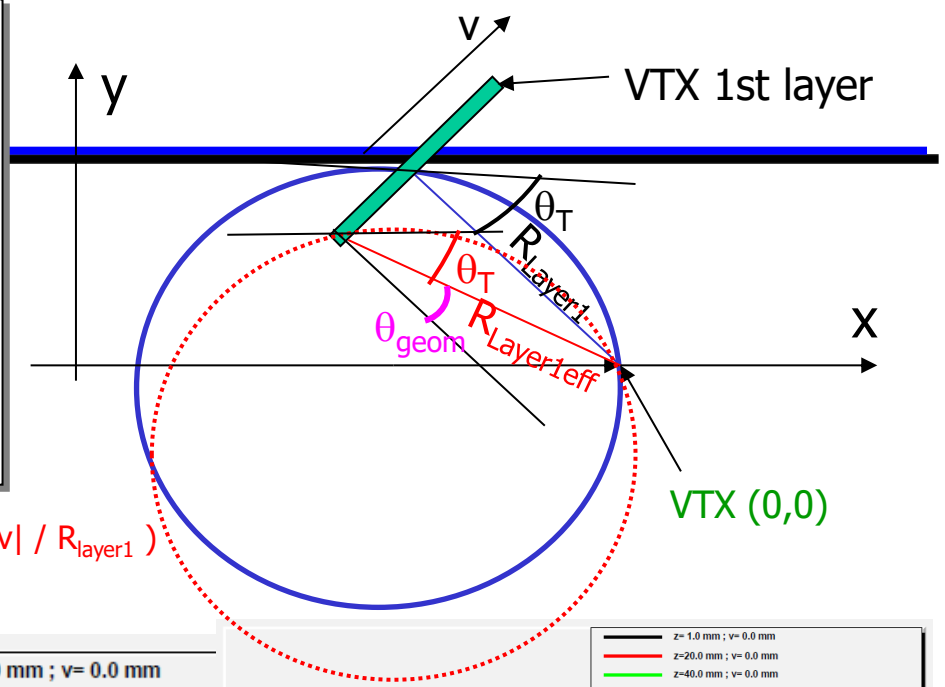
⇨ Most background is coming from IR
⇨ Typical pT ~10-100 MeV
⇨ They are real tracks !

(pT ~8 MeV to reach Layer 1)
(pT ~30 MeV to reach Layer 6)

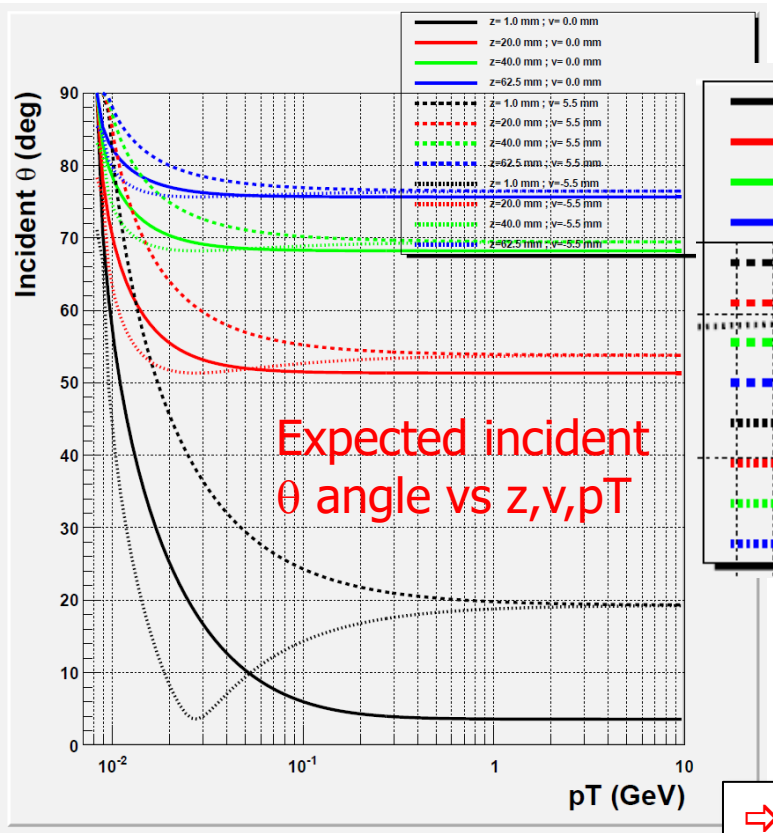


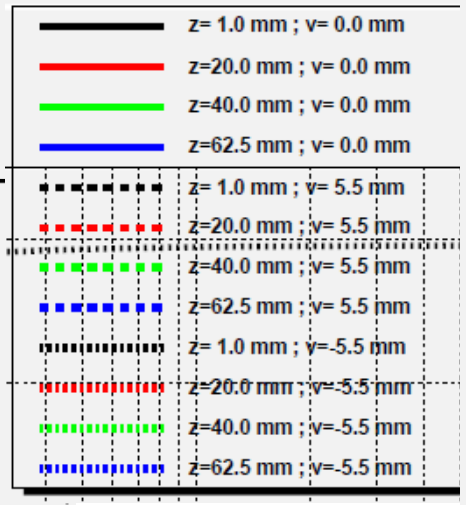




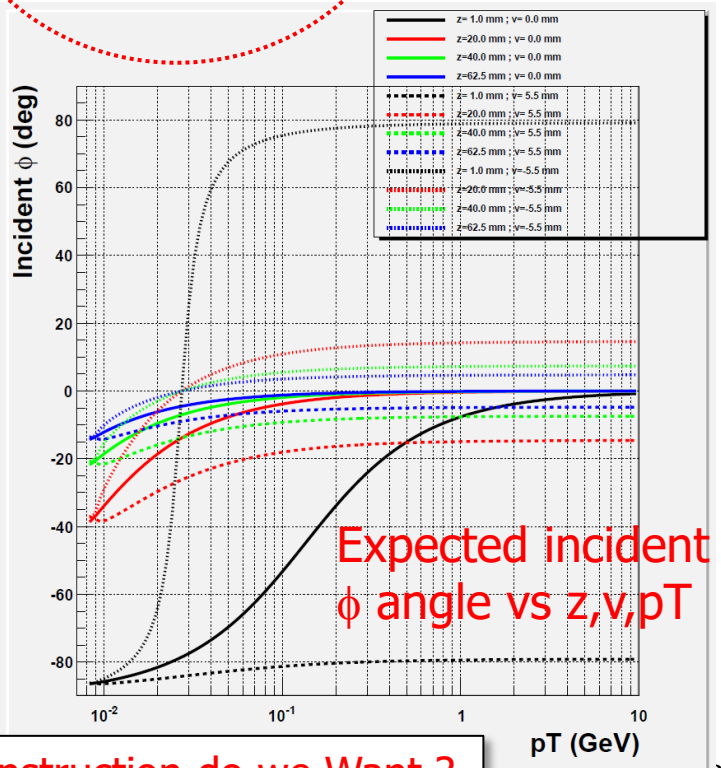


θ_T effective = $(\pi/2)$ - Arccos $(0.3.\times B\times R_{layer1eff}/(2\times pT)$) ± arctan ($|v| / R_{layer1}$)





θ-ϕ-pT
For particles coming from IR



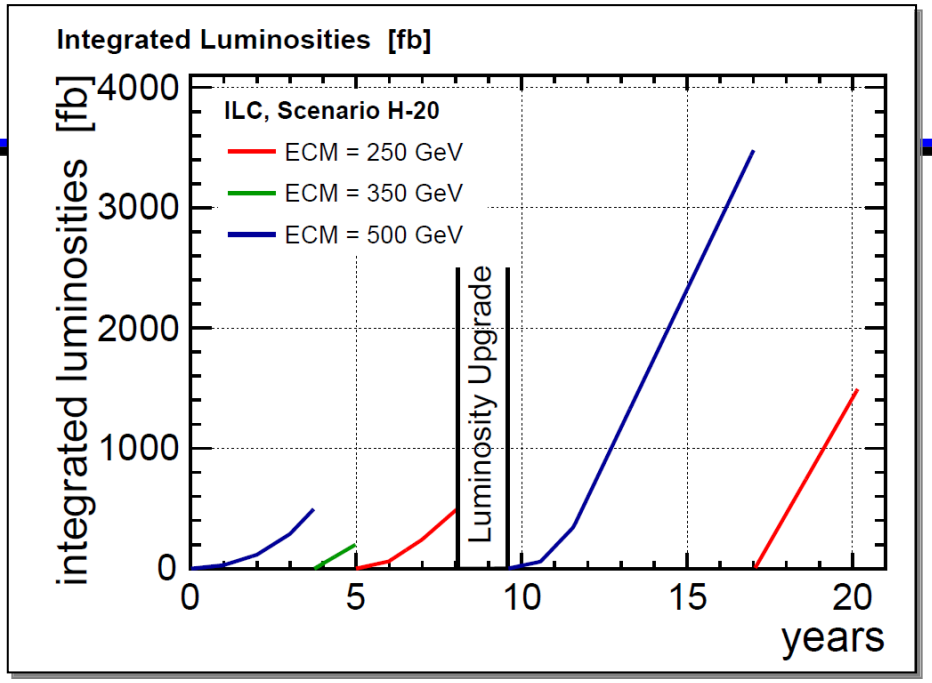
⇨ Which min pT reconstruction do we Want ?

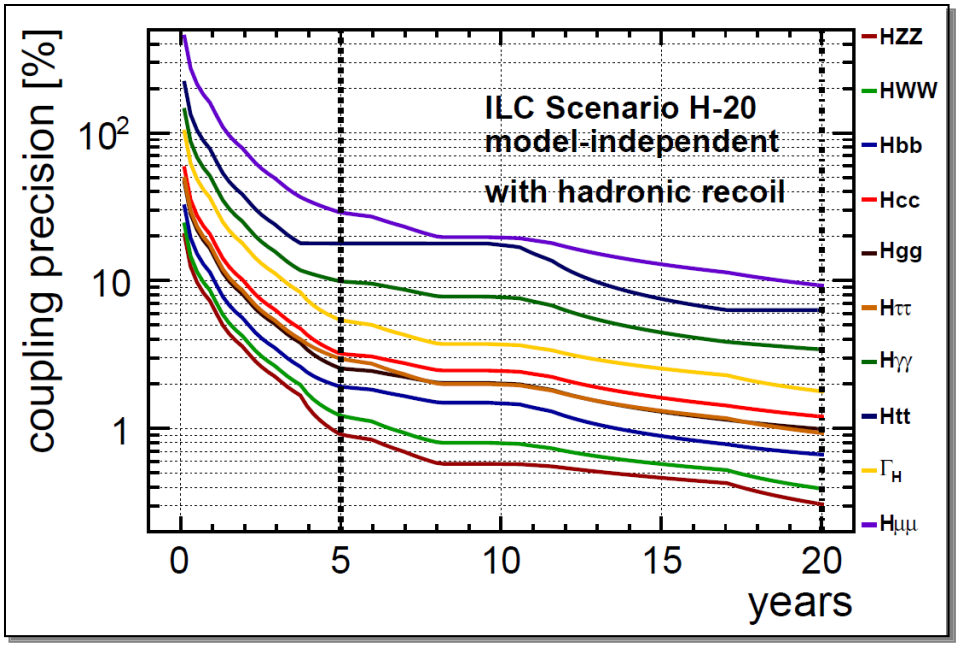
ILC Running scenarios

Physics Case for the International Linear Collider
K. Fuji et al. ILC-NOTE-2015-067

ILC Operating scenarios
T. Barklow et al. ILC-NOTE-2015-068

Topic	Parameter	Initial Phase	Full Data Set	units
Higgs	m_h	25	15	MeV
	$g(hZZ)$	0.58	0.31	%
	$g(hWW)$	0.81	0.42	%
	$g(hb\bar{b})$	1.5	0.7	%
	$g(hgg)$	2.3	1.0	%
	$g(h\gamma\gamma)$	7.8	3.4	%
		1.2	1.0	%, w. LHC results
	$g(h\tau\tau)$	1.9	0.9	%
	$g(hc\bar{c})$	2.7	1.2	%
	$g(ht\bar{t})$	18	6.3	%, direct
		20	20	%, $t\bar{t}$ threshold
	$g(h\mu\mu)$	20	9.2	%
	$g(hhh)$	77	27	%
	Γ_{tot}	3.8	1.8	%
	Γ_{invis}	0.54	0.29	%, 95% conf. limit
Top	m_t	50	50	MeV ($m_t(1S)$)
	Γ_t	60	60	MeV
	g_L^γ	0.8	0.6	%
	g_R^γ	0.8	0.6	%
	g_L^Z	1.0	0.6	%
	g_R^Z	2.5	1.0	%
	F_2^γ	0.001	0.001	absolute
	F_2^Z	0.002	0.002	absolute
W	m_W	2.8	2.4	MeV
	g_1^Z	8.5×10^{-4}	6×10^{-4}	absolute
	κ_γ	9.2×10^{-4}	7×10^{-4}	absolute
	λ_γ	7×10^{-4}	2.5×10^{-4}	absolute
Dark Matter	EFT Λ: D5	2.3	3.0	TeV, 90% conf. limit
	EFT Λ: D8	2.2	2.8	TeV, 90% conf. limit





Sustainable occupancy rate ?

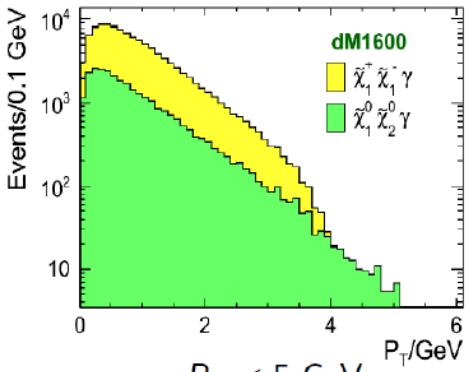
- Study by G.Voutsinas (DESY) cf. 31.05.2016 **ECFA 2016**

⇨ ≠r.o. time configurations tested

Chargino cross-section study

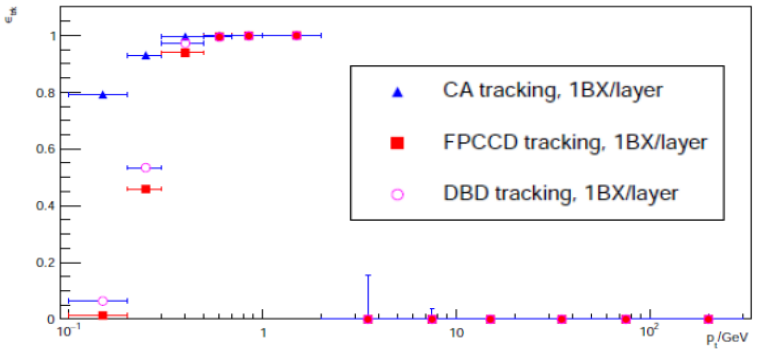
M_h=124 GeV

δm(chargino – neutralino) 1.59GeV

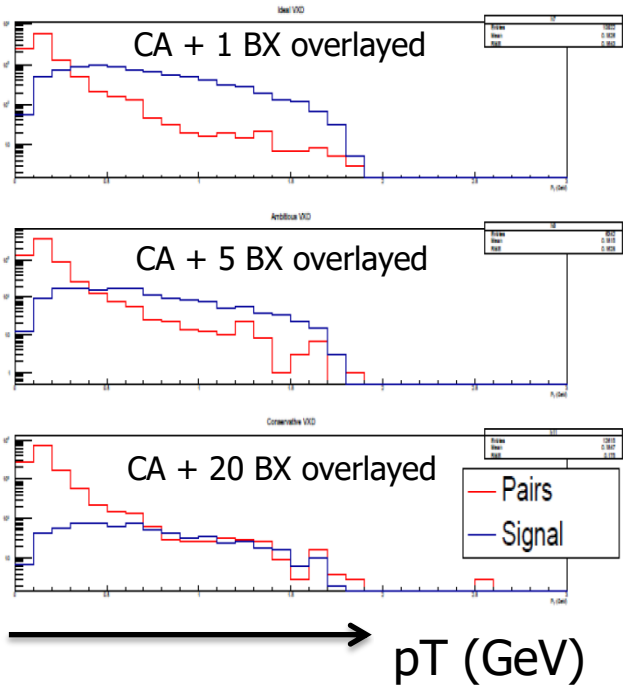


$P_T < 5$ GeV

	DBD VXD		Ideal VXD		Conservative VXD		Ambitious VXD	
layer	σ_{sp} (μm)	σ_{time}(μs)	σ_{sp} (μm)	σ_{time}(BXs)	σ_{sp} (μm)	σ_{time}(μs)	σ_{sp} (μm)	σ_{time}(μs)
L1 / L2	3 / 6	50 / 10	3/ 3	1 / 1	4 / 4	4 / 4	3 / 3	1 / 1
L3 / L4	4 / 4	100 / 100	3 / 3	1 / 1	4 / 4	8 / 8	3 / 3	2 / 2
L5 / L6	4 / 4	100 / 100	3 / 3	1 / 1	4 / 4	8 / 8	3 / 3	2 / 2



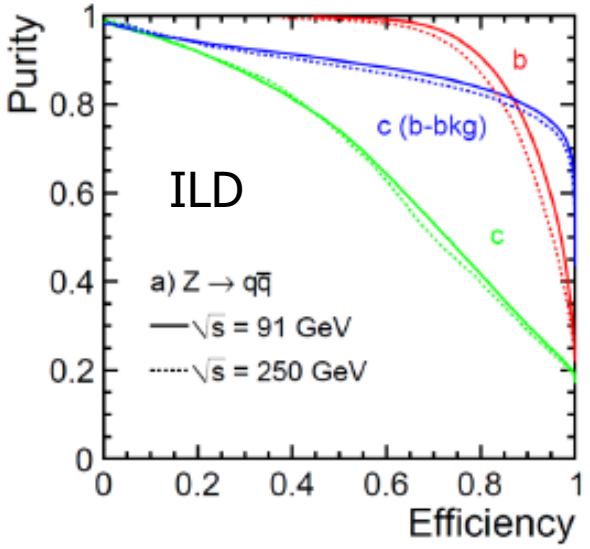
⇨ Track seeding in the VTX helps low momentum track efficiency

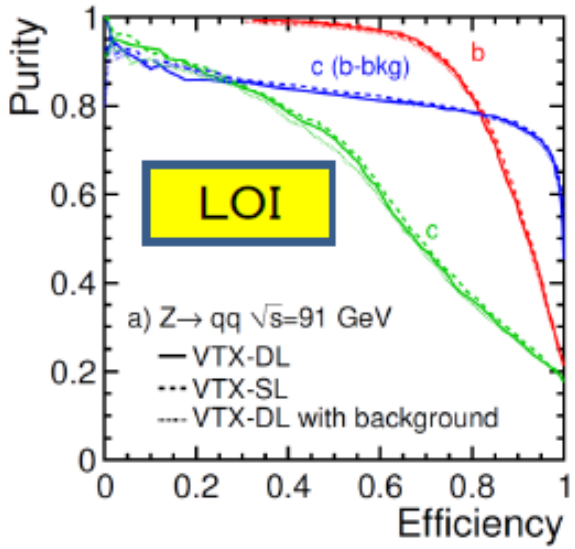


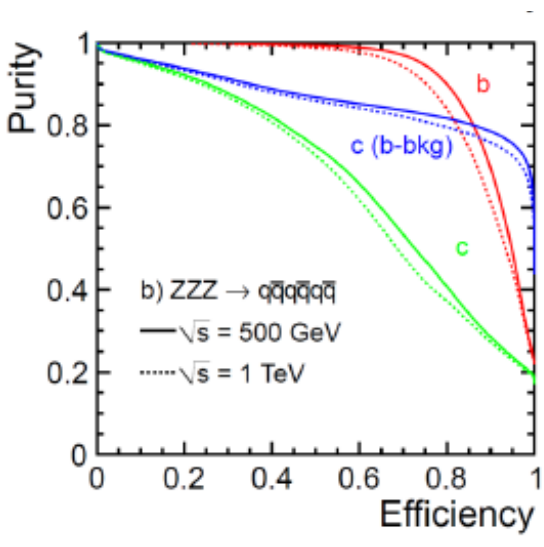
⇨Faster read-out do help to disentangle "Tracks signal" from tracks coming from BB

Expected Vertex performances (2) : Flavor tagging

- ILD example
- Full simulation
- Multi-variable tagging algorithm (BDT)
  - LCFIplus
- Continuous improvements

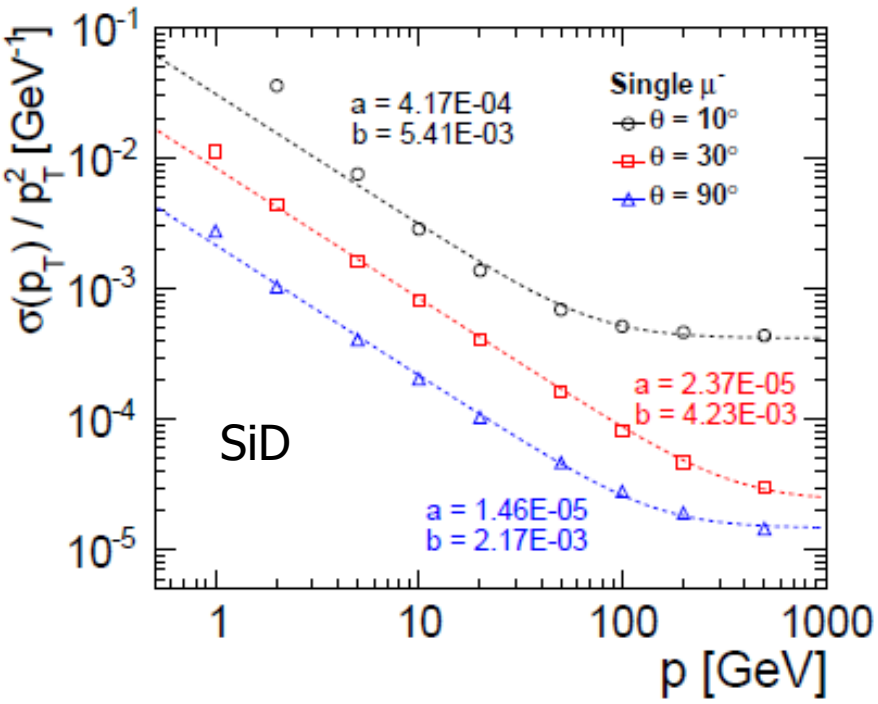


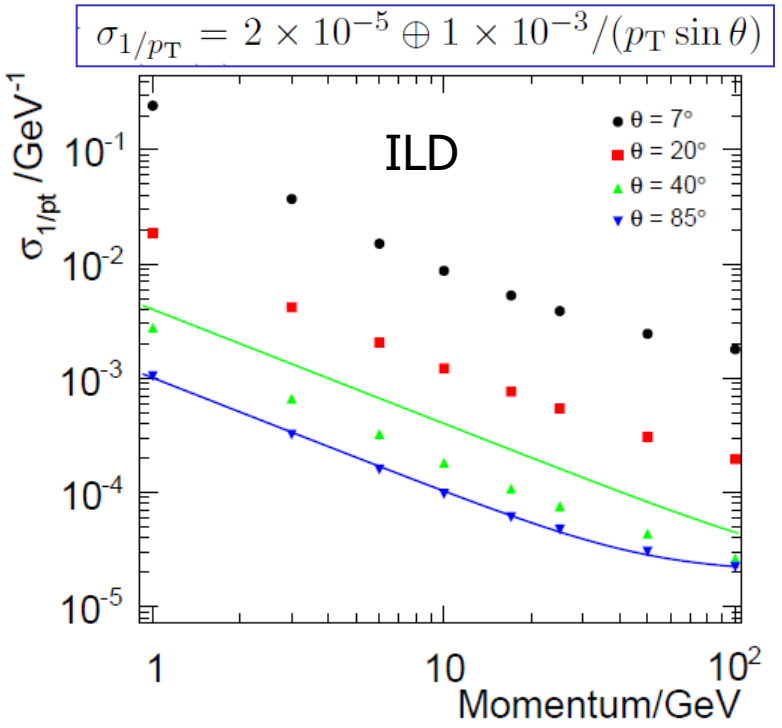




Expected Tracking performances

Single muons events : Normalised pT resolution for different polar angles

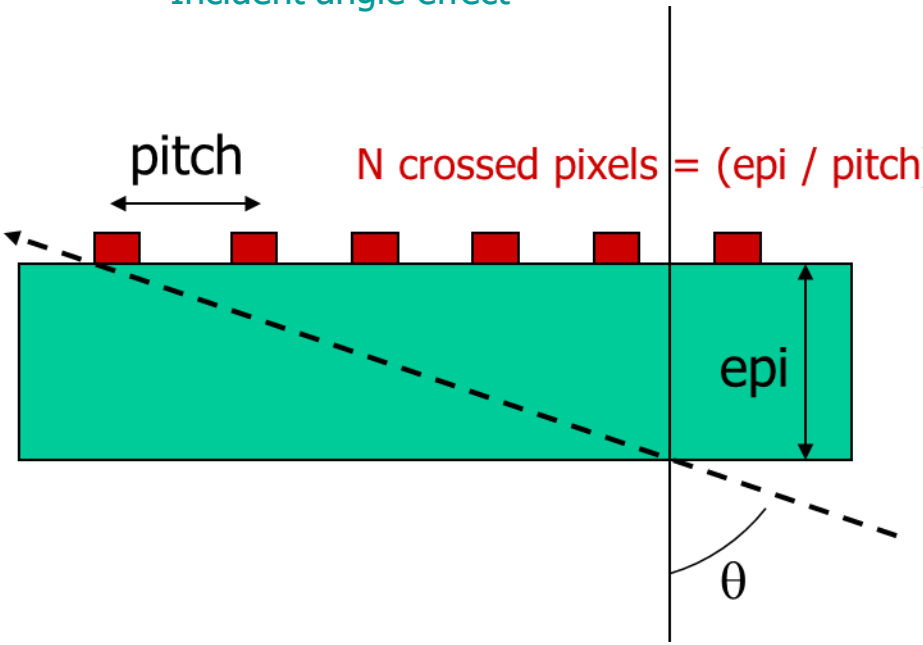




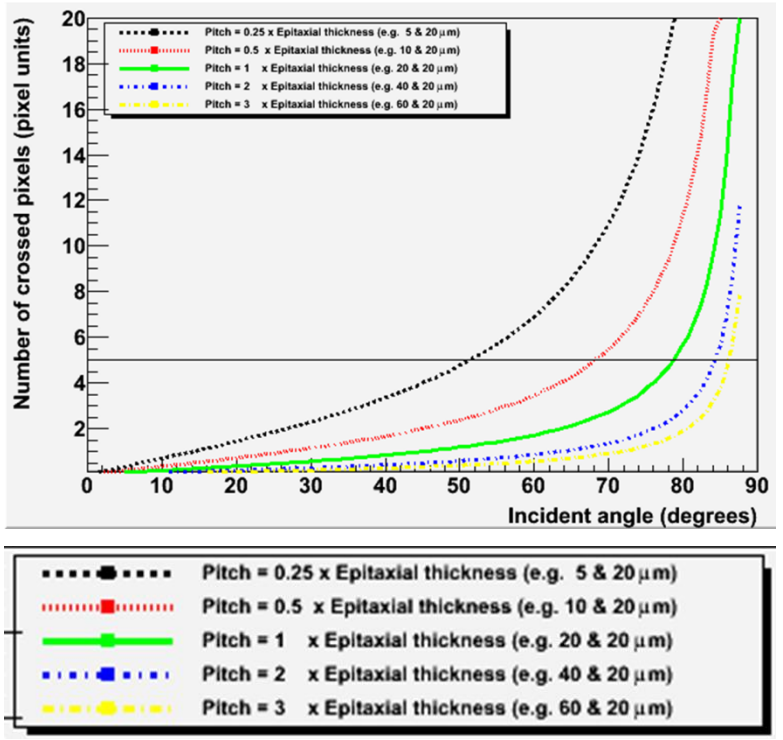
- SiD:
  - better @ high pT
  - robustness in high density tracks environment
- ILD:
  - better @ low pT
  - dE/dx capabilities (TPC)

Multiplicity discussion

- 1 hit ≠ 1 pixel fired
  - Typically 1-4 for perpendicular particles
- ⇨ Depends on:
  - Threshold applied on discriminators
  - Charge sharing
    - Smaller for fully depleted technologies
    - Increases with sensitive thickness
  - Incident angle effect

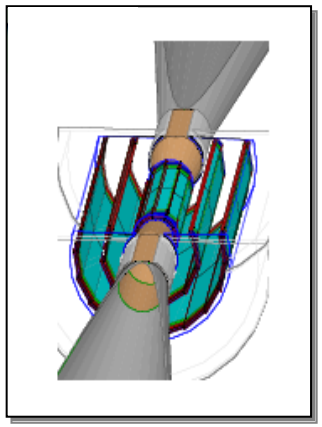


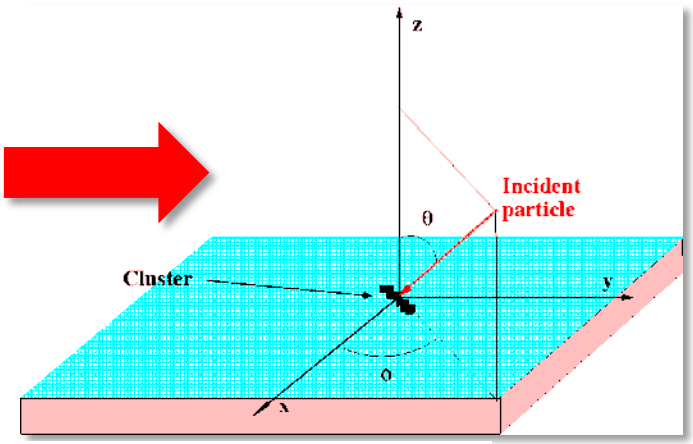
Crucial parameter: pitch / epitaxial layer thickness



e.g. :
20 μm pitch, 20 μm thickness, θ= 70°
⇨ 3 crossed pixels ⇨ ~ x3 occupancy

Beam background properties in the local frame of the sensors



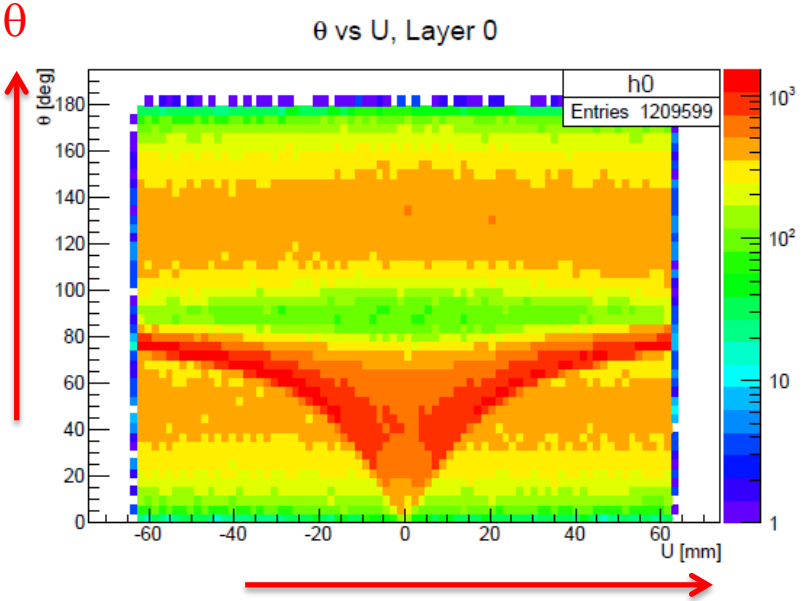


- Background properties:
  - z-ϕ-θ correlations ⇨ Elongated clusters
  - Use cluster shape to tag/reject beam background ?
  - easier for small pitch

& large sensitive thickness

Beam background simulation (with anti DID)

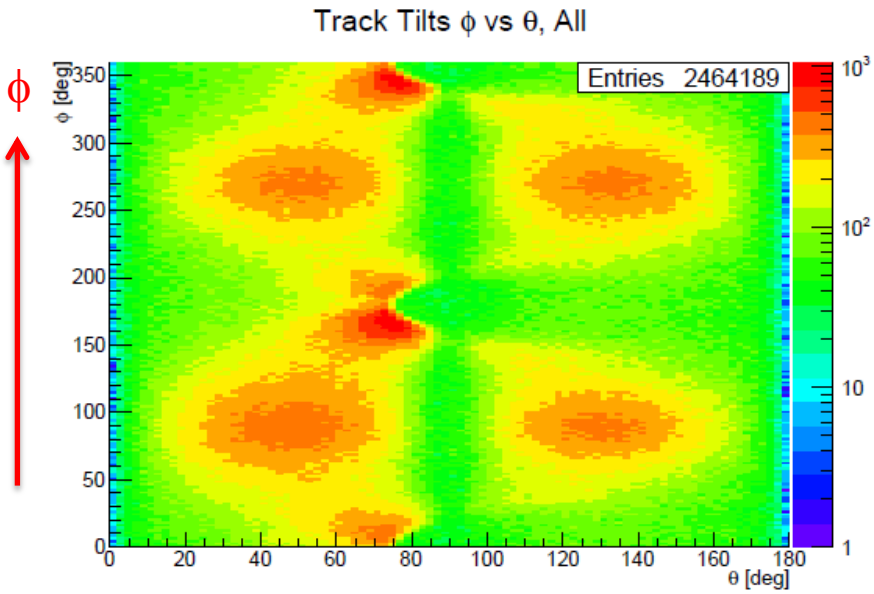
θ



(L.Cousin PhD, IPHC)

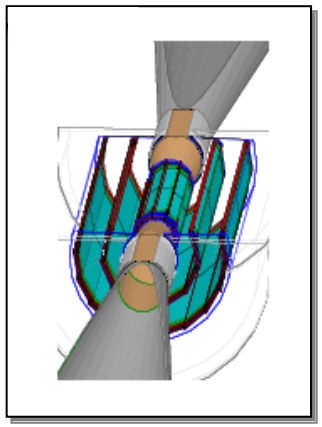
Beam axis

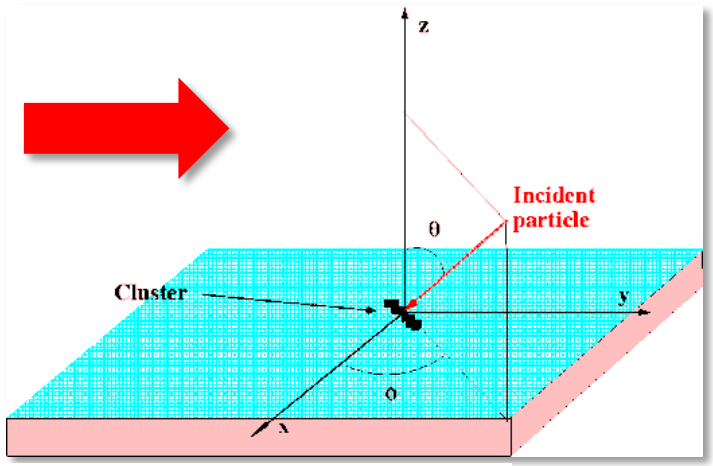
ϕ



θ

Beam background properties in the local frame of the sensors



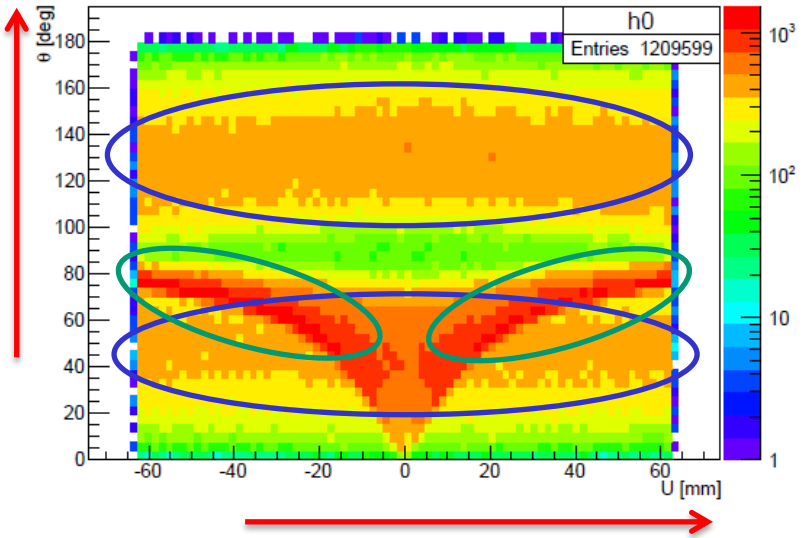


- Background properties:
  - z-ϕ-θ correlations ⇨ Elongated clusters
  - Use cluster shape to tag/reject beam background
  - old idea for small pitch

1 hit Bckgd

Loopers (low pT)

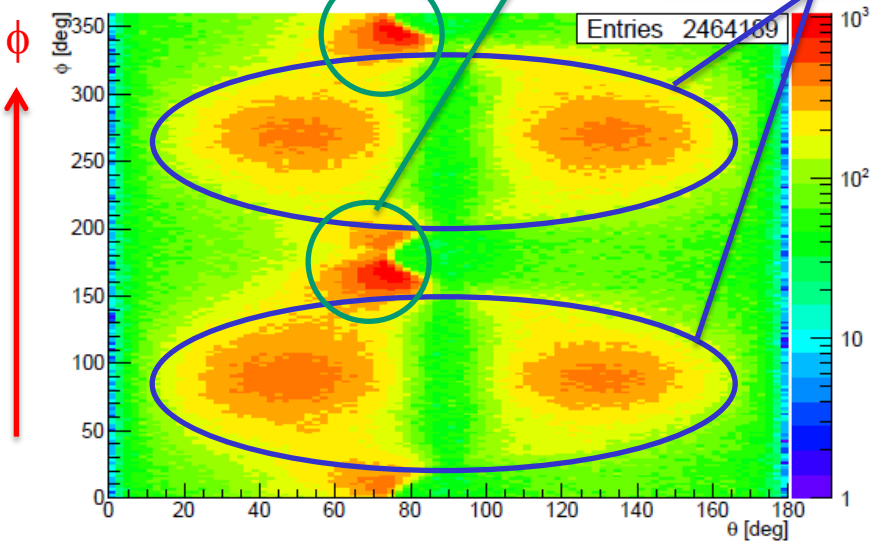
θ



(L.Cousin PhD, IPHC)

Beam axis

ϕ



θ