# Development of Vertex Detector for ILC

Proposal of SOI sensor for ILC: SOFIST

**SO**I sensor for **Fi**ne measurement of **S**pace and **T**ime

**Miho Yamada (KEK)**

yamadami@post.kek.jp

and SOI PIXEL R&D Group

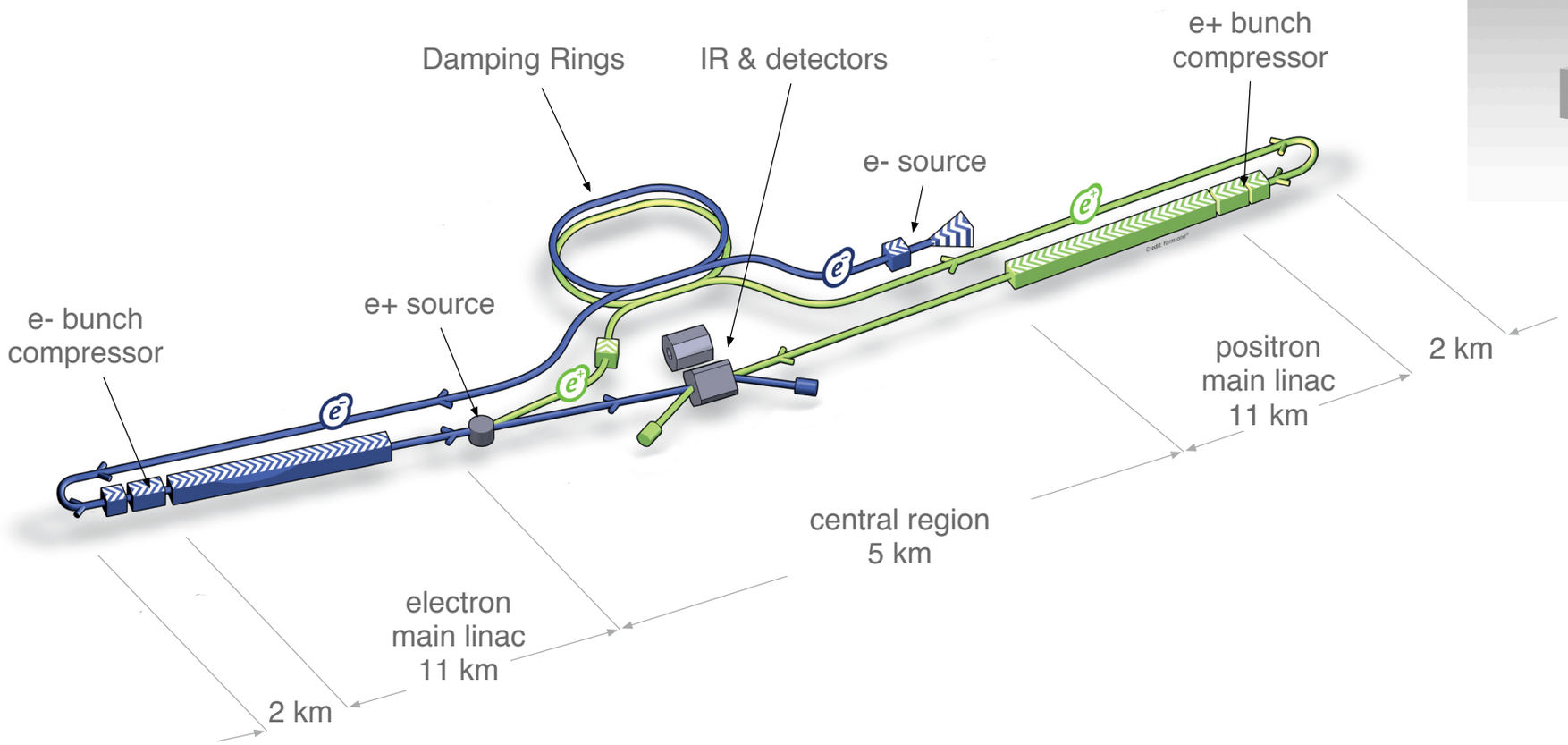
SOI Satellite Meeting, Strasbourg, France

May. 9th, 2017

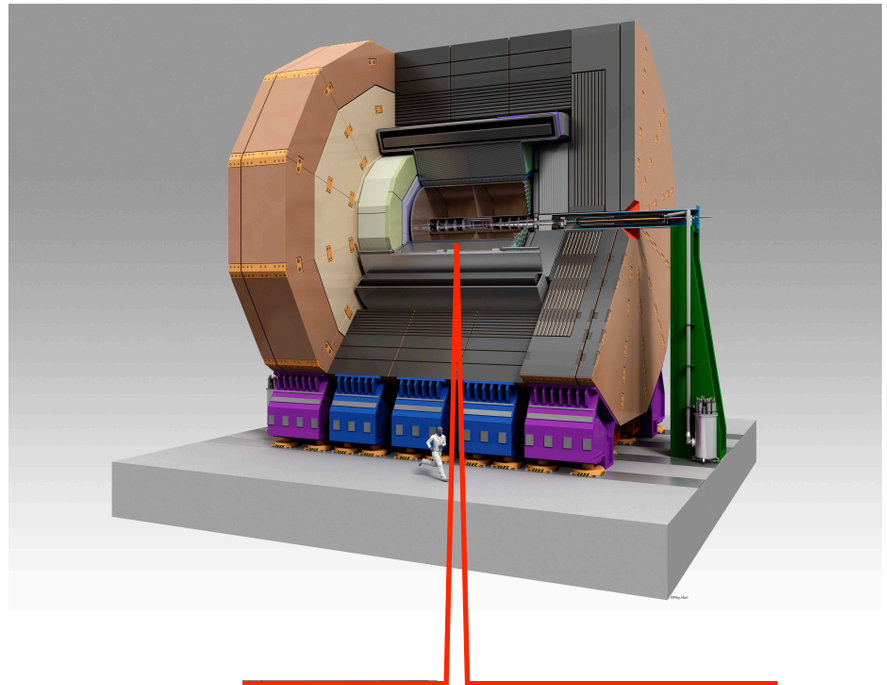
# ILC Experiment

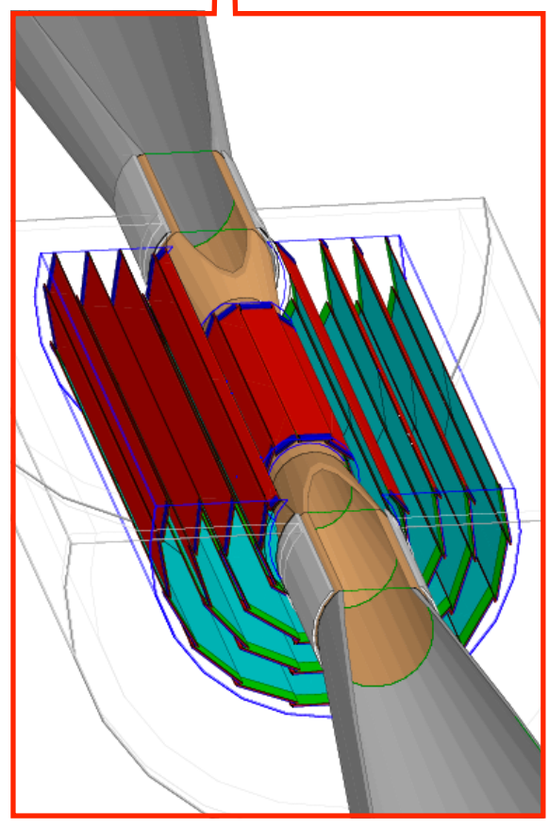
## ILC Experiment

- $e^+e^-$ linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for beyond the Standard Model




ILC detector concept (ILD)





Vertex detector geometry (VTX-SL)

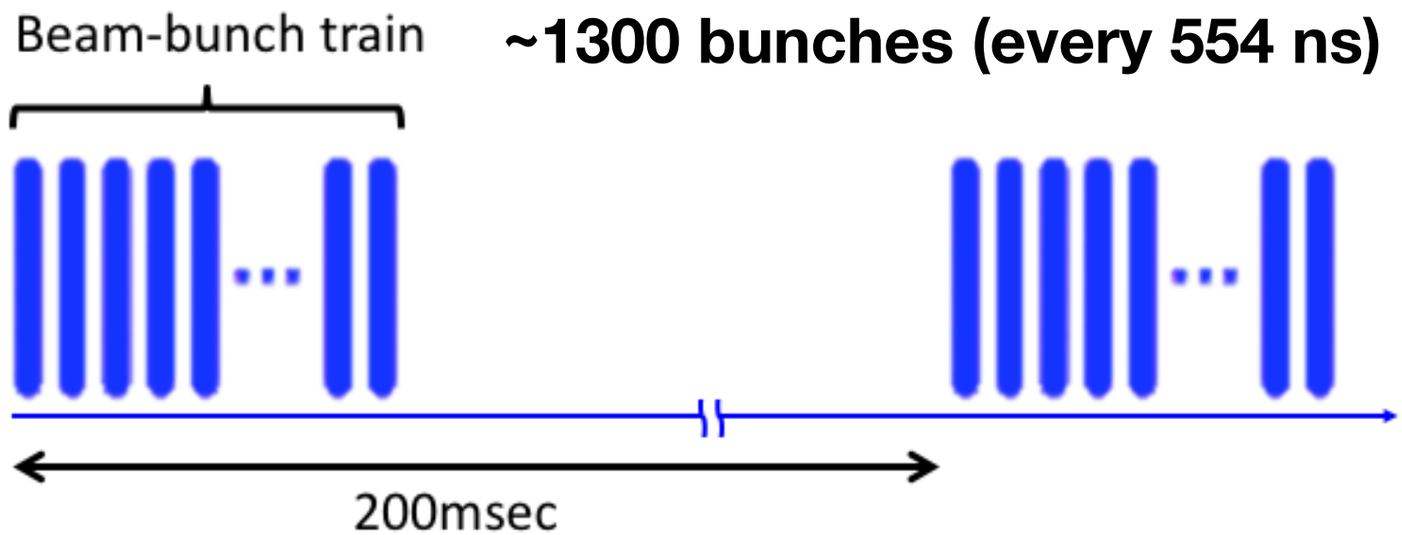
ILC TDR vol.4: Detectors
ILD Concept Group, T. Abe et al., arXiv:1006.3396 [hep-ex].

# ILC Vertex detector

**Requirements:**

1) Single point resolution: better than 3 $\mu$m
   Pixel size: ~20 × 20 $\mu m^2$
2) Time resolution: single-crossing (554 ns interval) time resolution
3) Detector occupancy: < 2 %
4) Low material budget: $X \leq 0.1 - 0.2$ % $X_0$ / Layer
   corresponds to ~ 100 - 200 $\mu$m Si, including supports, cables and cooling
   low-power ASICs (~ 50 mW/cm$^2$) + gas-flow cooling
5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < $10^{11}$ 1MeV $n_{eq}$ / cm$^2$ / year

We are designing and evaluating prototype pixel sensor with SOI technology to fulfill the requirements.




ILC TDR v4 Detector
LC Vertex / Tracking R&D 2nd Nov. 2015

# Functions for ILC Vertex Detector

**Necessary functions for the ILC vertex detector:**

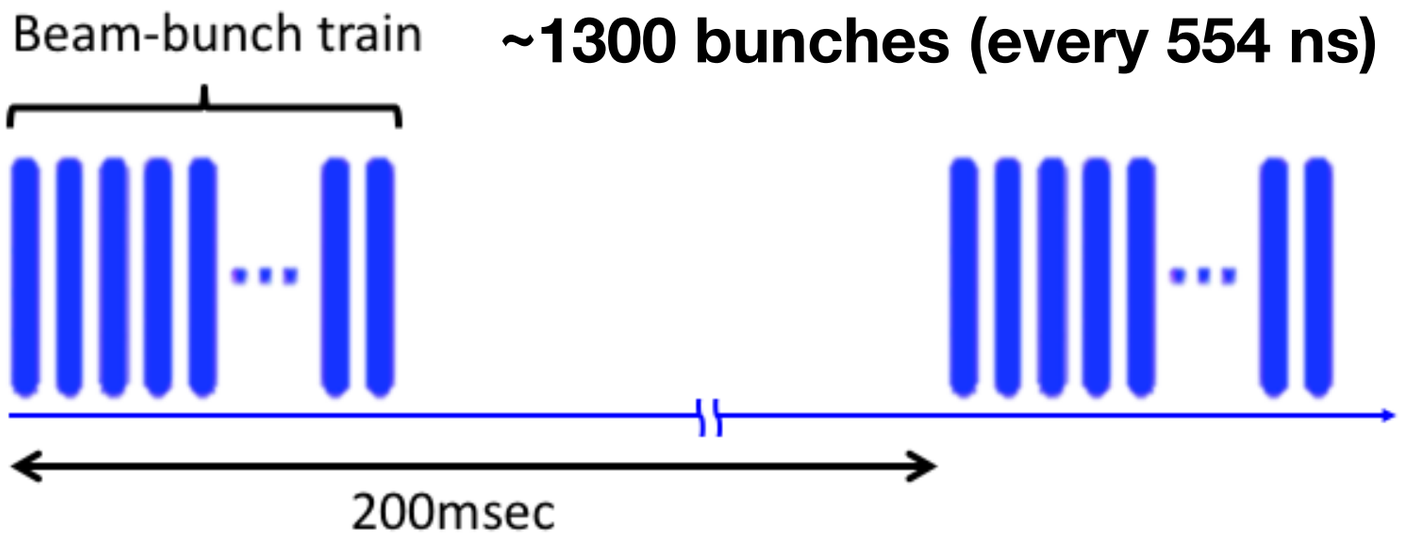
- Single point resolution
  Pixel size: less than 20 $\mu$m
  Calculate weighted center of charges (Charges are spread among multi pixels).
  → Record an analog signal of a hit.

- Timing resolution
  Bunch crossing occurs every 554 ns in 1-msec-long bunch train with an interval 200 ms.
  Identify a collision bunch of a hit to reconstruct a event.
  → Record a time stamp of a hit.

- Detector occupancy
  Hit information have to hold during 1 beam-bunch train.
  Increase detector occupancy.
  → Need multiple memories

- High speed data transfer
  Data have to be send to backend before next bunch train injection.
  → Reduce a data to transfer.

We designed a prototype pixel detector SOFIST.



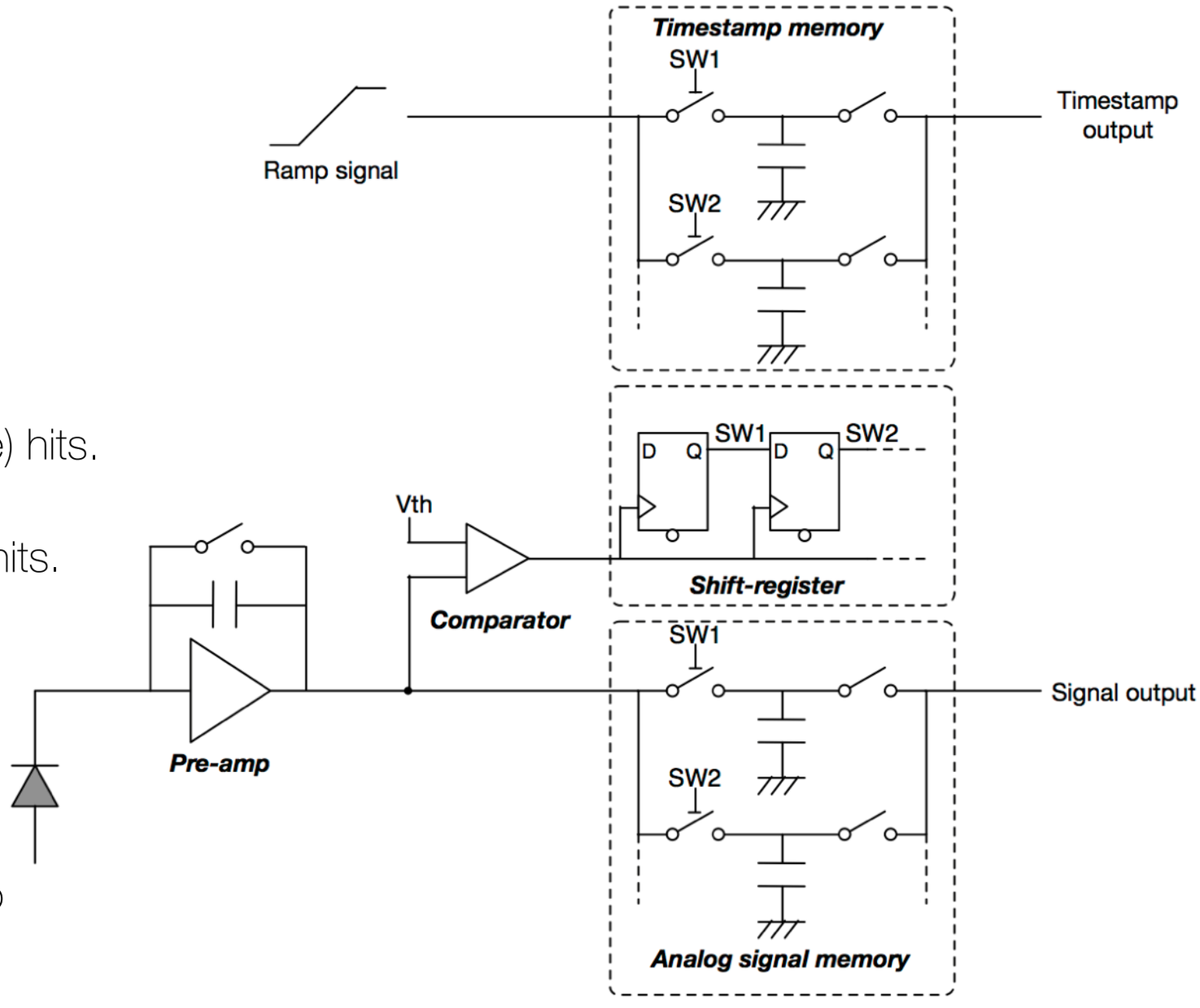
# Architecture of SOFIST

## In a Pixel

- Pre-amplifier
- Comparator
  Keep the analog signal and time stamp
  if a signal exceeds a threshold $V_{th}$.
- Shift register
  Latch for multiple memories.
- Analog signal memory
  Store signal charges up to two (or more) hits.
- Time stamp circuit
  Store time stamps up to two (or more) hits.

## On Chip

- Column ADC
  Digitize analog signal and time stamp.
- Zero-Suppression logic
  Extract hit pixels and reduce the data to transfer to backend.

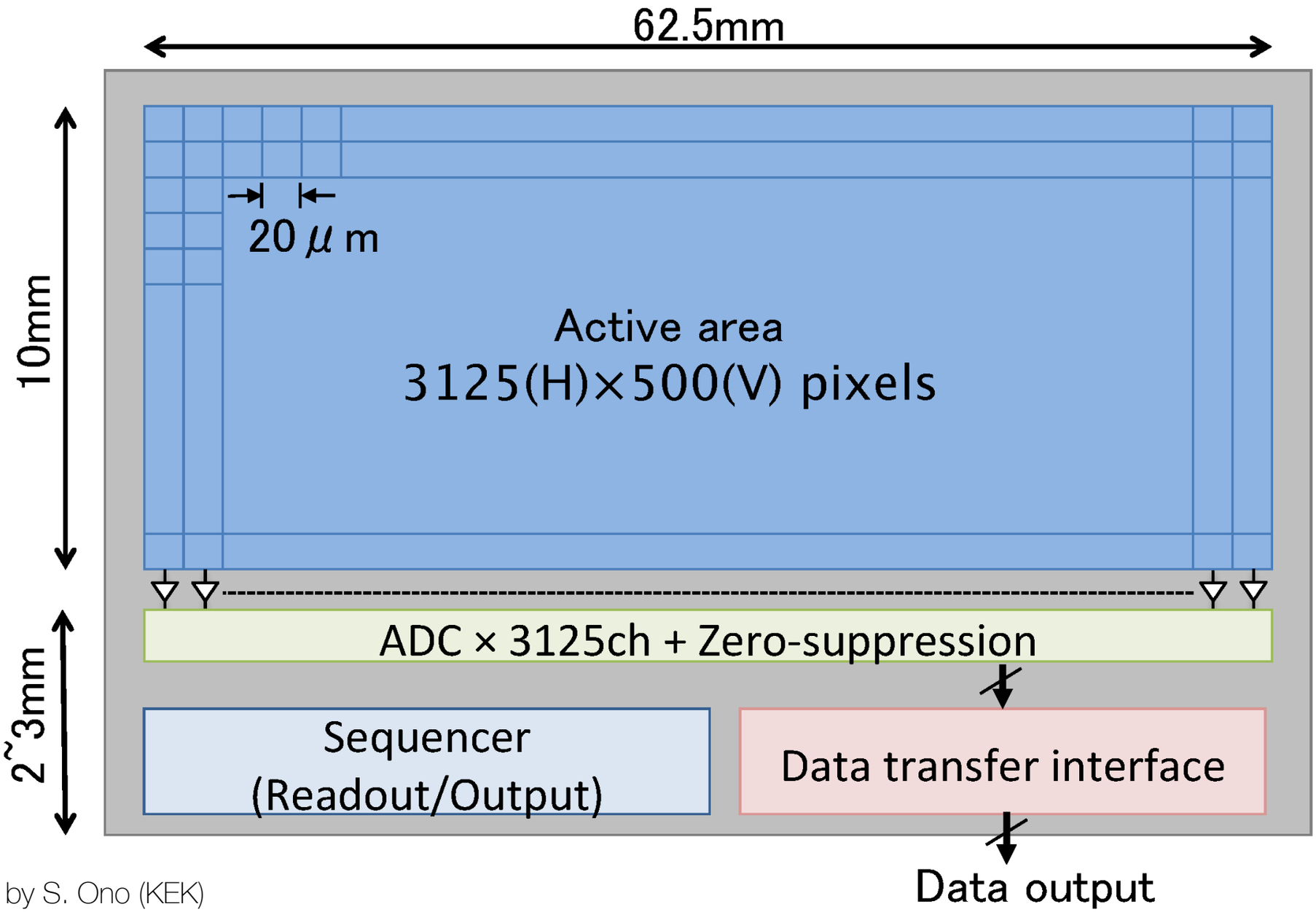



Designed by S. Ono (KEK)

# SOI sensor for ILC: SOFIST

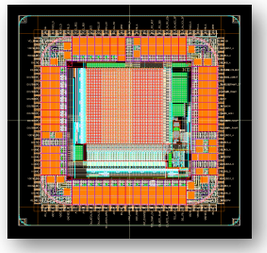
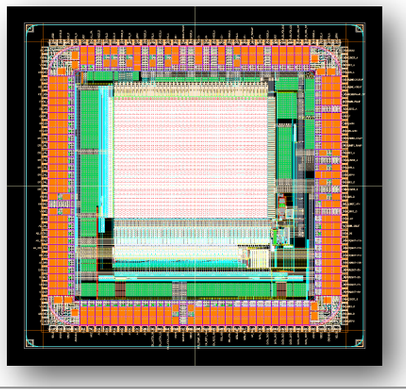
**SOFIST**: SOi sensor for Fine measurement of Space and Time

Conceptual SOI pixel sensor for the ILC (inner most layer of the vertex detector).




Designed by S. Ono (KEK)

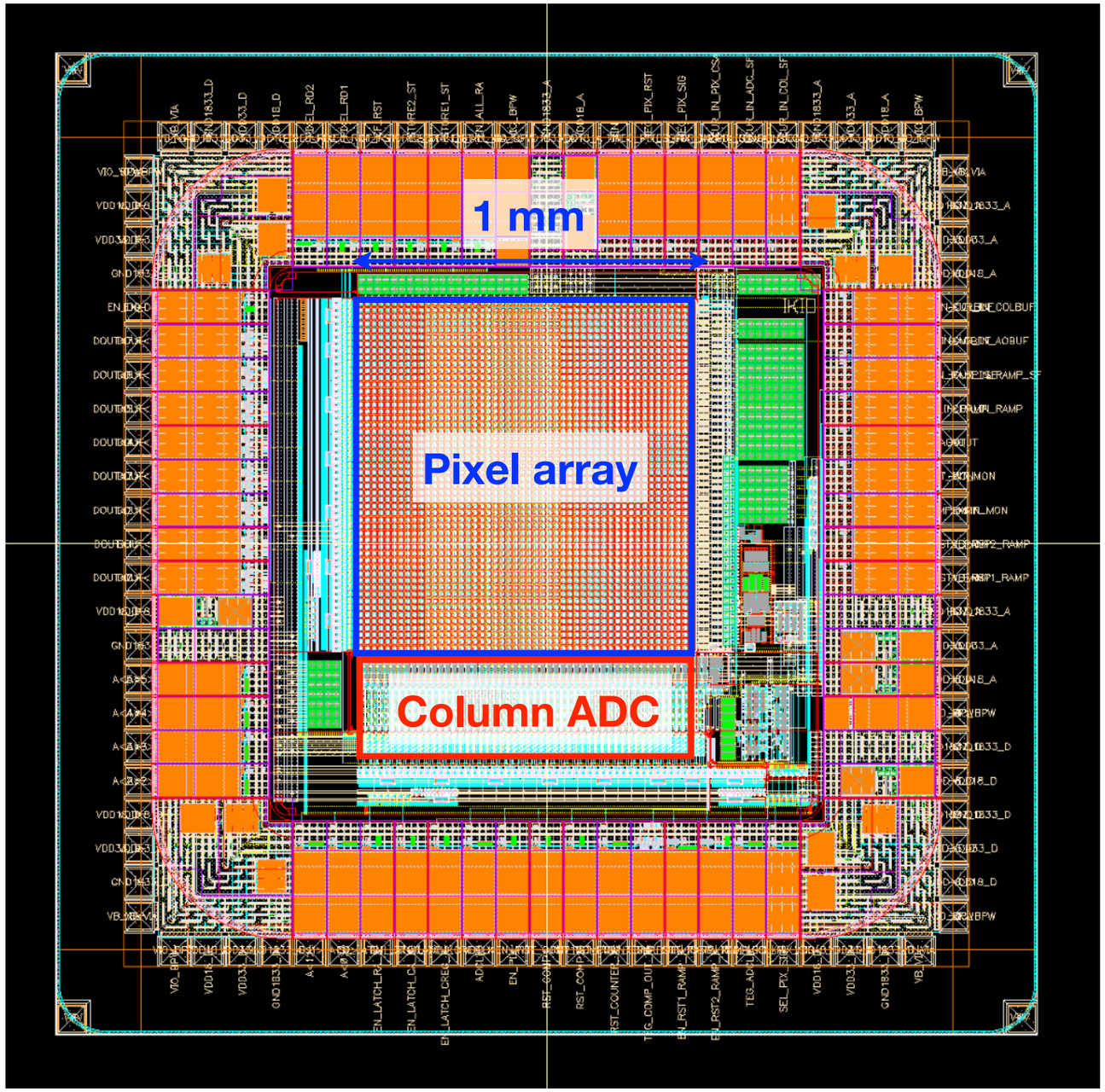
# SOFIST

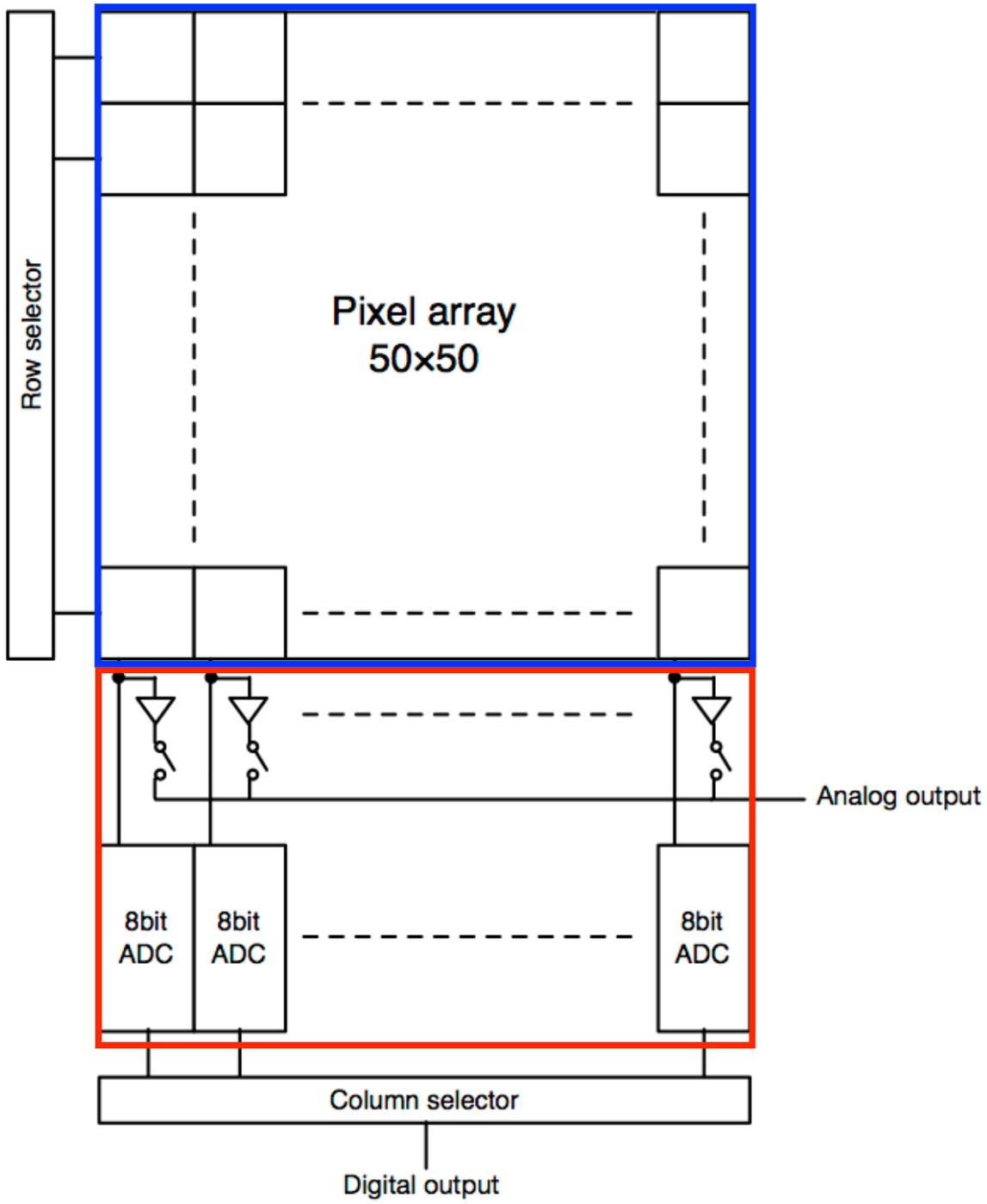
| | MX1850 | MX2040 | MX2xxx | |
|---|---|---|---|---|
| SOFIST | ver.1 | ver.2 | ver.3 | ver.4 (3D) |
| |  |  | Under design | Upper Chip<br>Under design<br>Lower Chip |
| Chip Size ($mm^2$) | 2.9 × 2.9 | 4.45 × 4.45 | 6 × 6 | 4.45 × 4.45 |
| Pixel Size ($\mu m^2$) | 20 × 20 | 25 × 25 | 30 × 30 | 20 × 20 |
| Pixel Array | 50 × 50 | 64 × 64 (Time Stamp)<br>1 × 64 (Analog Signal) | 128 × 128 | 64 × 64 |
| Functions (Pixel) | Pre. Amplifier (CSA)<br>Analog signal memory (2 hits) | Pre. Amplifier (CSA)<br>Comparator (Chopper inverter)<br>Shift register (DFF × 2)<br>Analog signal memory (2 hits)<br>or<br>Time stamp memory (2 hits) | Pre. Amplifier (CSA)<br>Comparator (Chopper inverter)<br>Shift register (DFF × 3)<br>Analog signal memory (3 hits)<br>Time stamp memory (3 hits) | Pre. Amplifier (CSA)<br>Comparator (Chopper inverter)<br>Shift register (DFF × 3)<br>Analog signal memory (3 hits)<br>Time stamp memory (3 hits) |
| Functions (On Chip) | Column ADC (8 bit) | Column ADC (8 bit)<br>Zero-suppression logic | Column ADC (8 bit) | Column ADC (8 bit) |
| Wafer | FZ *n* -type (Single SOI) | Cz *p* -type (Double SOI) | FZ *p* -type (Double SOI) | FZ *p* -type (Double SOI) |
| Wafer Resistivity (kΩ·cm) | 2 ≤ | 1 ≤ | 3 - 10 | 3 - 10 |
| Status | Delivered (Dec. 2015)<br>Under evaluation | Delivered (Jan. 2017) | Under desing (Submit June 2017) | Under desing (Submit June 2017) |

0.2 $\mu$m FD-SOI CMOS process by Lapis Semi. Co. Ltd.

# SOFIST ver.1

# SOFIST ver.1




Pixel size: 20 × 20 $\mu m^2$
Chip size: 2.9 × 2.9 $mm^2$
Active area: 1.0 × 1.0 $mm^2$ (50 × 50 pixels)
Wafer: FZ *n*-type, Single SOI, 500 $\mu$m thickness

# SOFIST ver.1

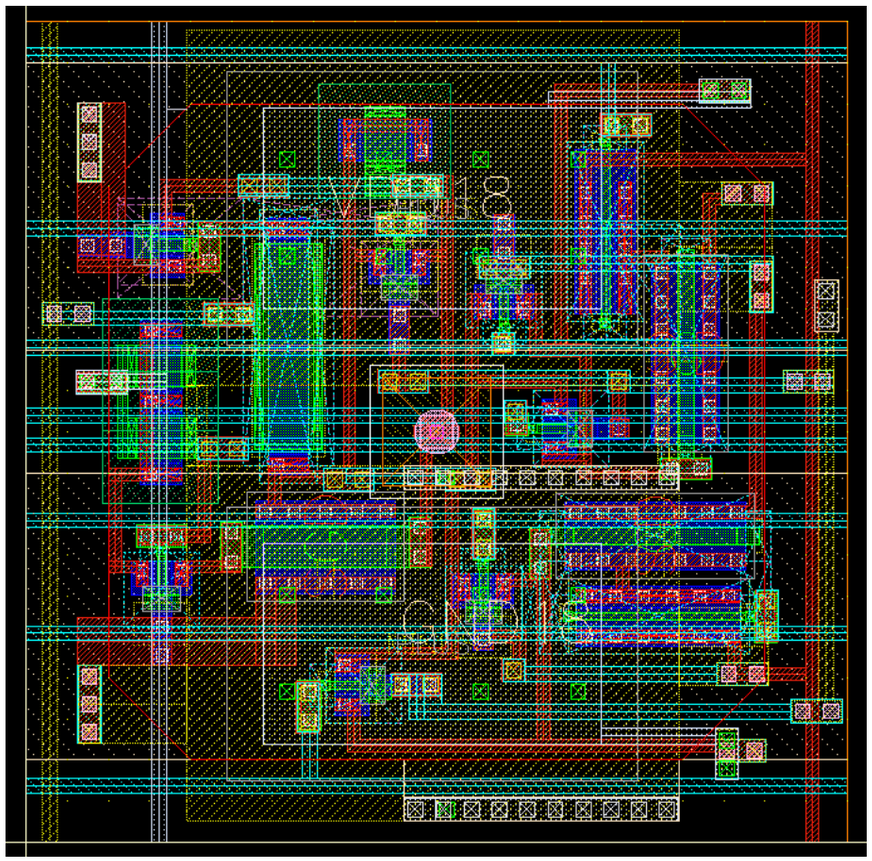
**Pixel**

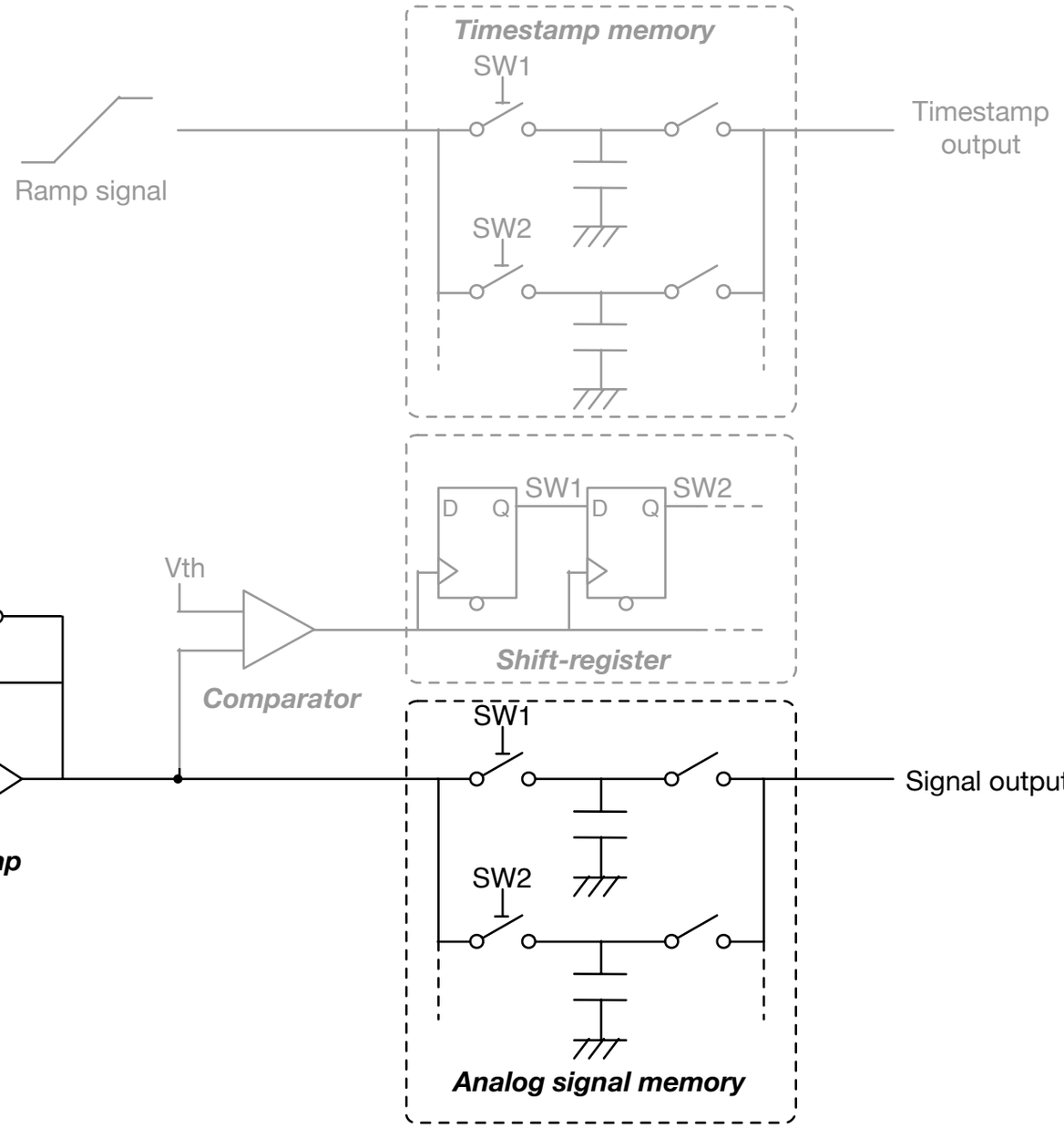
- Pre. amplifier (Charge sensitive amplifier)
  gain: 0.12 V/MIP (assuming 50 $\mu$m thick sensor)
- Analog signal memories (two memories)

**On chip**

8 bit column ADC

Pixel size: 20 × 20 $\mu m^2$





# Beam Test

## SOFIST ver.1 Beam Test with FPIX2

at Fermilab Test Beam Facility (Jan. 20th - Feb. 8th, 2017)


**Beam**

120 GeV proton beam
1 spill: ~4 sec

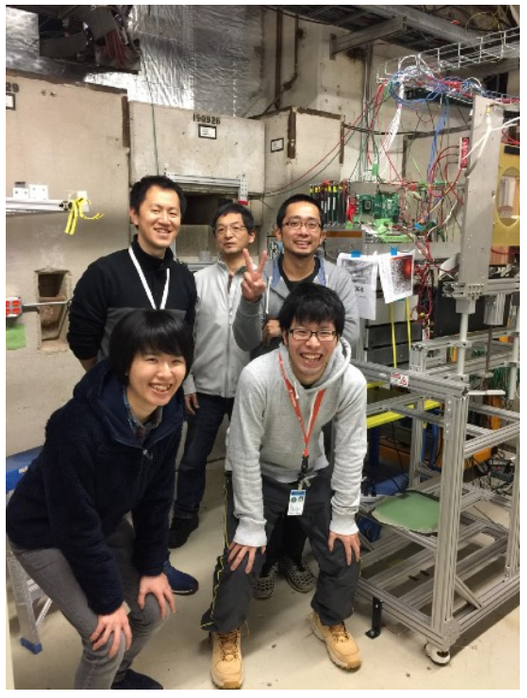
**Evaluation**

- **S/N ratio**
- **Position resolution**

**Colleagues**

SOFIST (KEK):
T. Tsuboyama, M. Togawa, S. Ono and M. Yamada

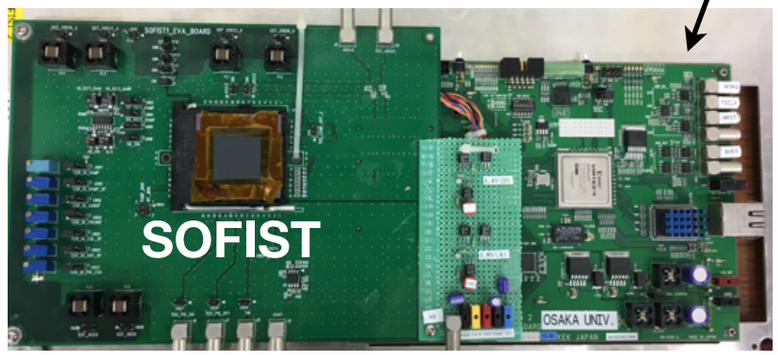
FPIX (Univ. Tsukuba):
D. Sekigawa and S. Endo



# Setup

**Trigger**: ATLAS upgrade pixel sensor (FE-I4) && Scintillator (Downstream)
(Some data were taken by coincidence of two scintillators for checking the DAQ system.)
**DAQ rate**: ~300 events/s

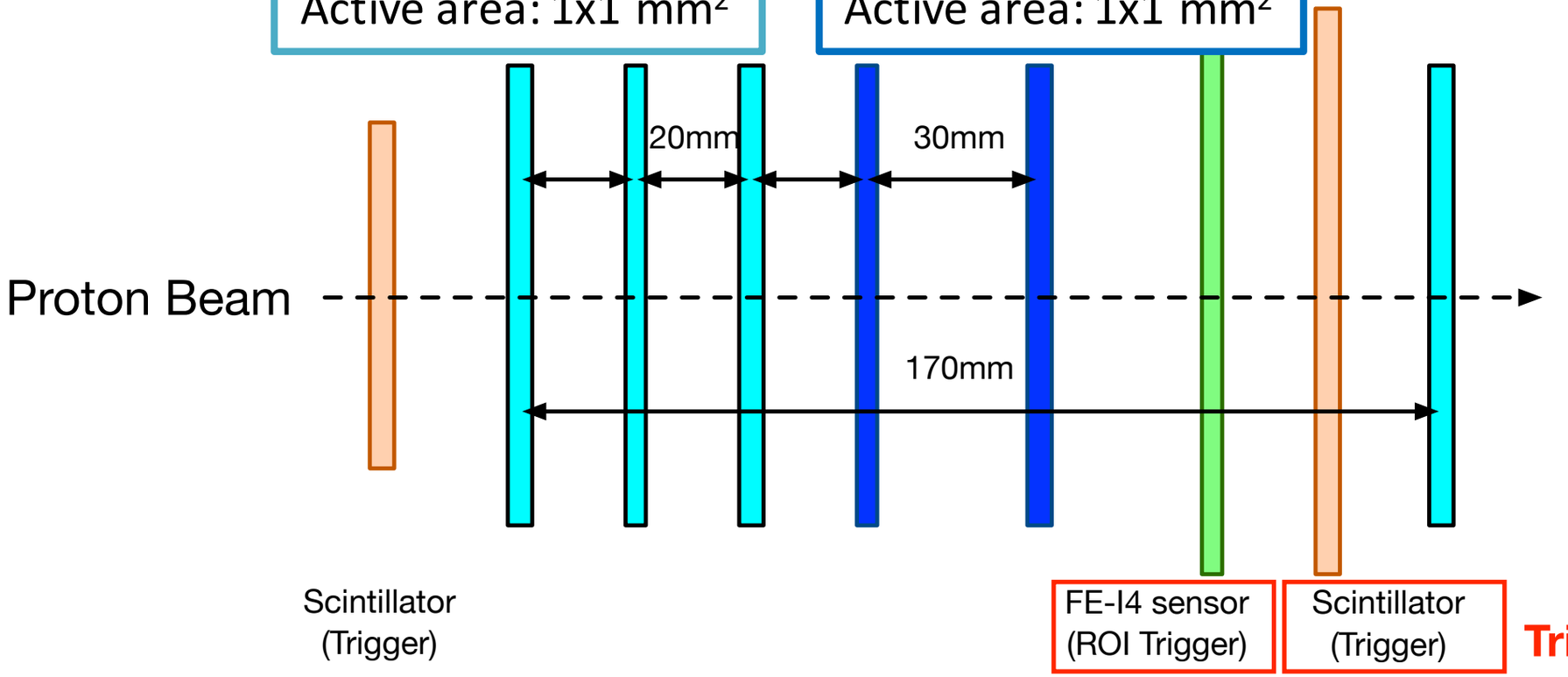
DAQ board (SEABAS2)

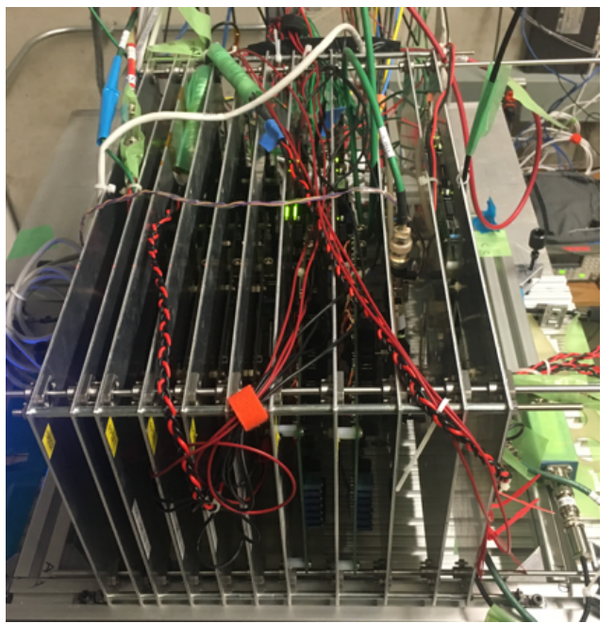



Telescope for SOFIST
Reconstruct track with four layers of FPIX2.

**FPIX2**
Pixel size: 8x8 μm²
Active area: 1x1 mm²

**SOFIST ver.1**
Pixel size: 20x20 μm²
Active area: 1x1 mm²

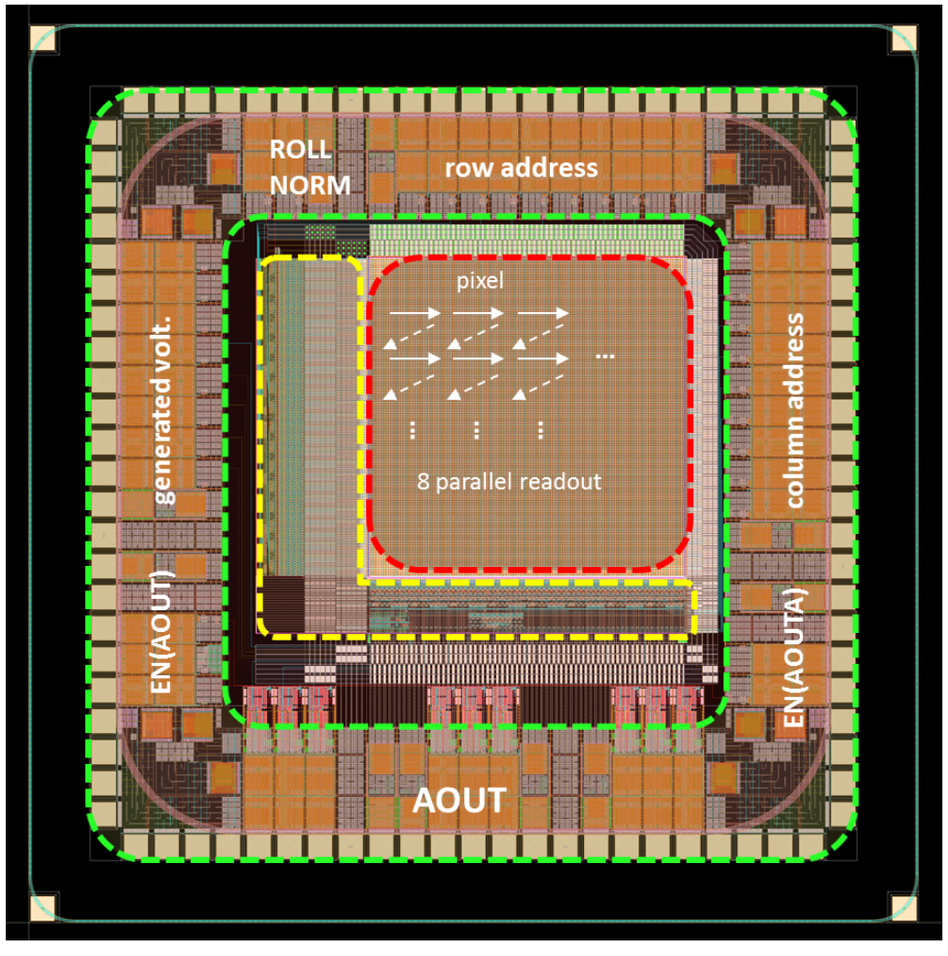


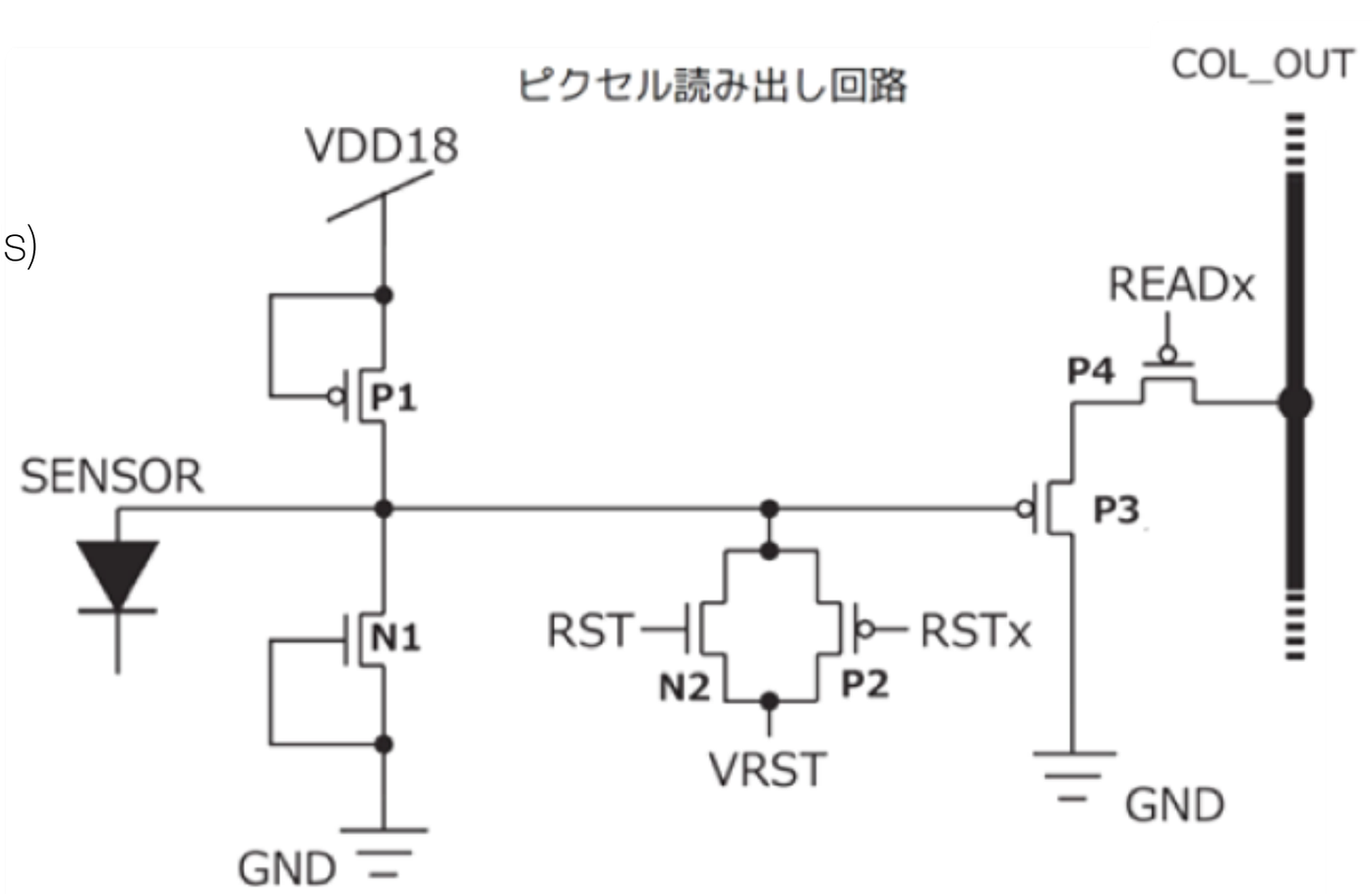



# FPIX2

## FPIX2 (SOI Pixel sensor)

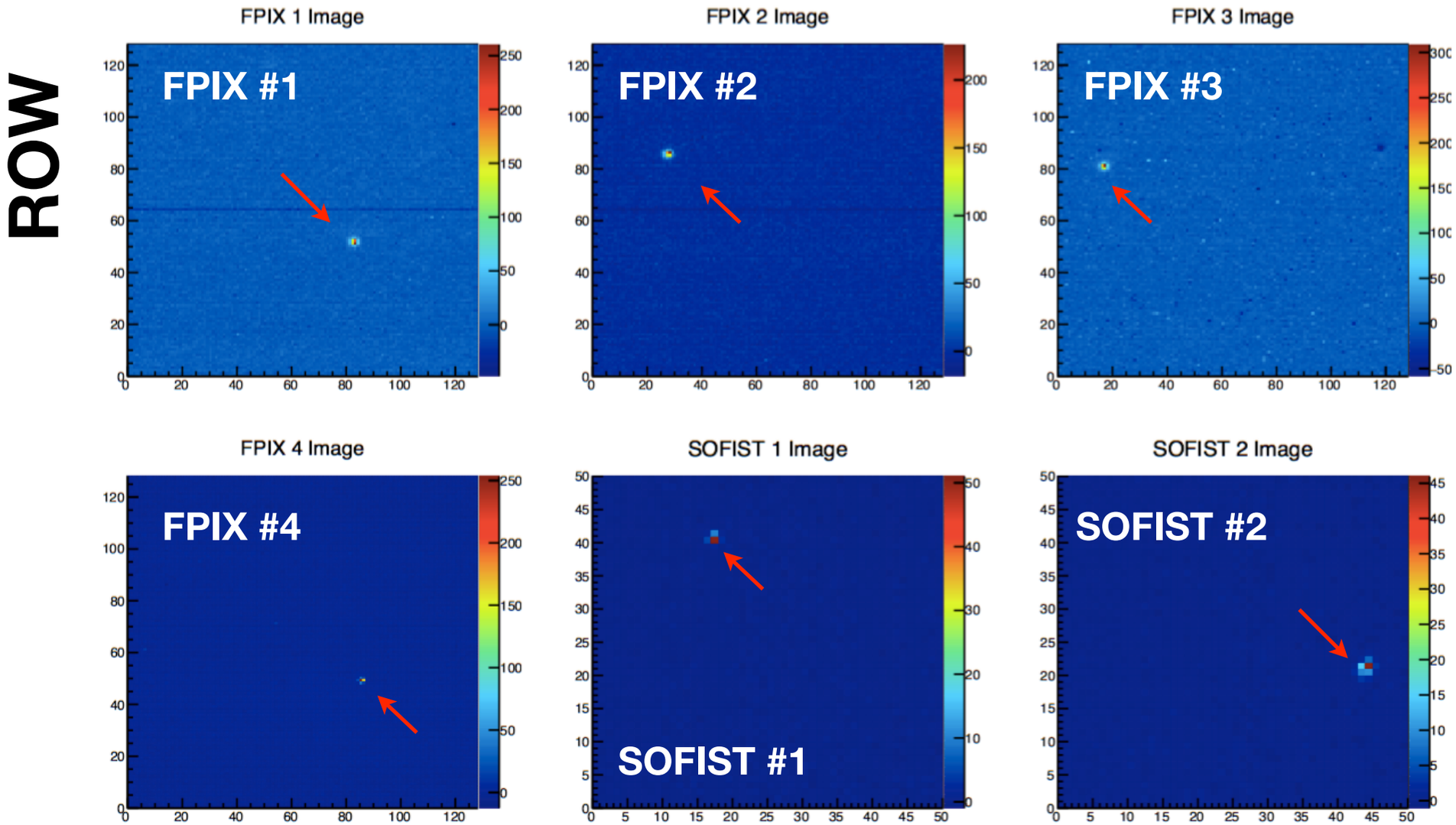
- Chip size: 2.9 × 2.9 mm$^2$
- Single-SOI (FZ *p*-type, 500 $\mu$m)
- Pixel size: 8 × 8 $\mu$m$^2$
- Active area: 1024 × 1024 $\mu$m$^2$ (128 × 128 pixels)
- Readout: Rolling shutter, 8 line parallel
- 1 ms frame time
- External 12 bit ADC (SEABAS2)



# Event Display

They are already subtracted their pedestal.




**FPIX2**
HV = 70 V (not fully depleted ~400 $\mu$m)
Reset cycle = 1 ms

**SOFIST ver.1**
HV = 130 V (fully depleted ~500 $\mu$m)
Reset cycle = 10 $\mu$s

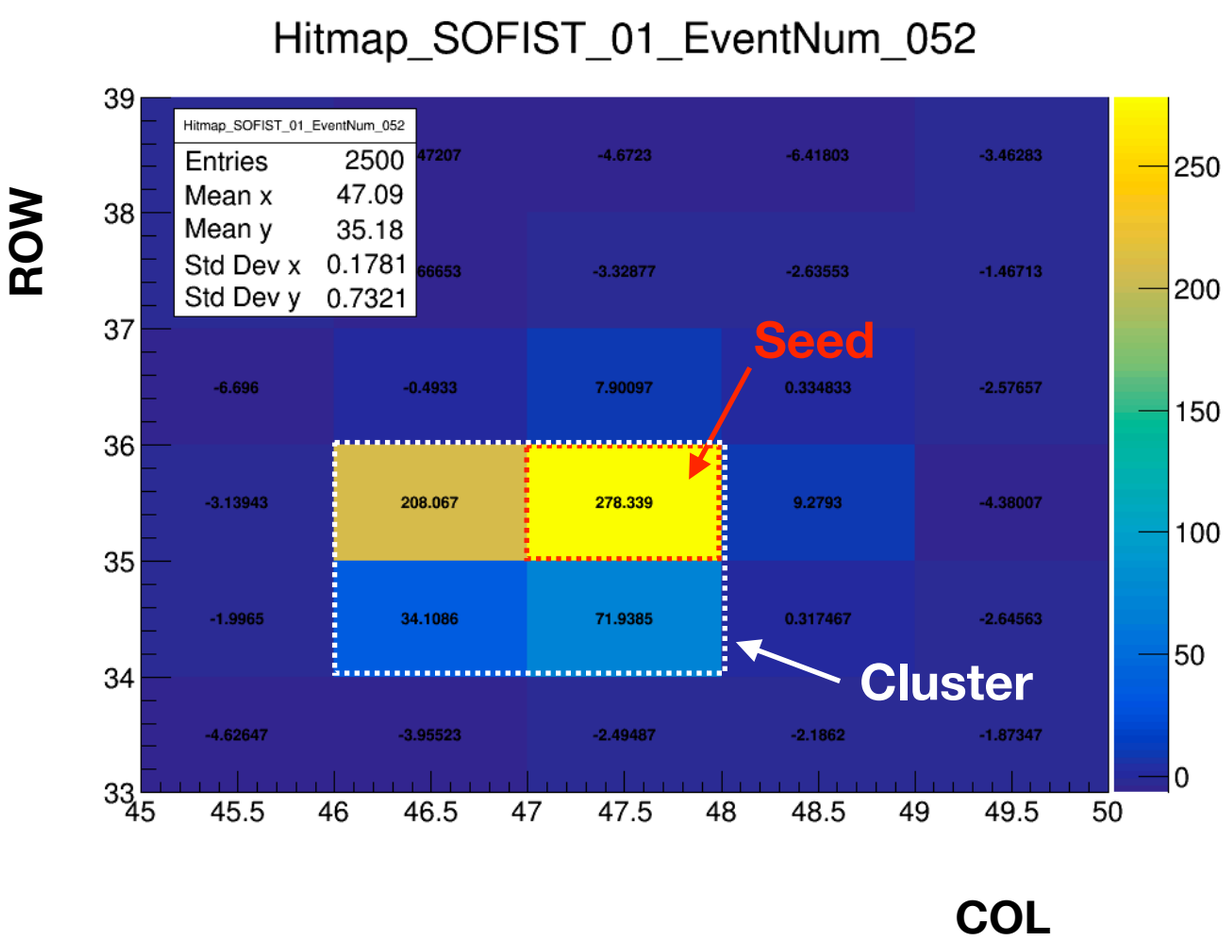
# Cluster

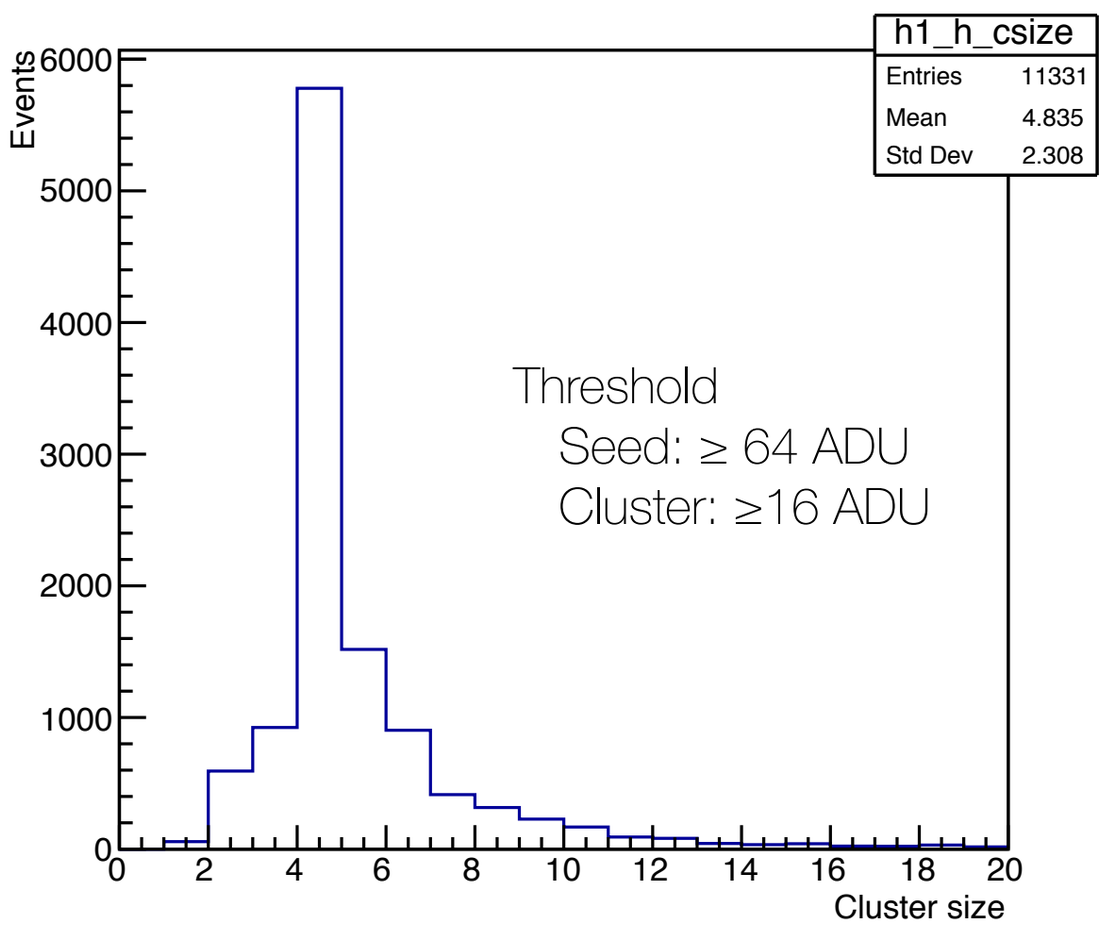
## SOFIST setup

Readout: 12 bit external ADC (SEABAS2 onboard)
Bias voltage = 130 V

## Clustering

1) find seed pixel which is ≥ 64 ADU.
2) add pixels which are ≥16 ADU to cluster.
3) check 2) for 6 × 6 pixels centered on the seed pixel.



# S/N

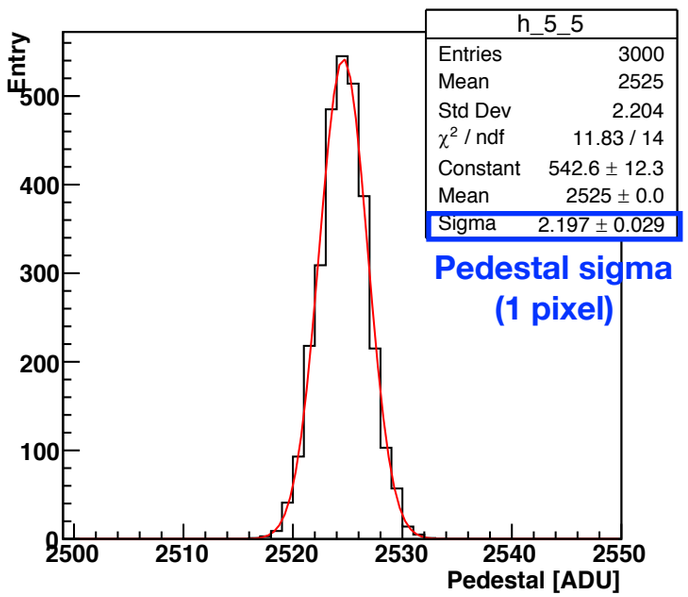
## SOFIST setup

Readout: 12 bit external ADC (SEABAS2 onboard)
Bias voltage = 130 V

## Clustering

1) find seed pixel which is ≥ 64 ADU.
2) add pixels which are ≥16 ADU to cluster.
3) check 2) for 6 × 6 pixels centered on the seed pixel.

**Pedestal (1 pixel)**

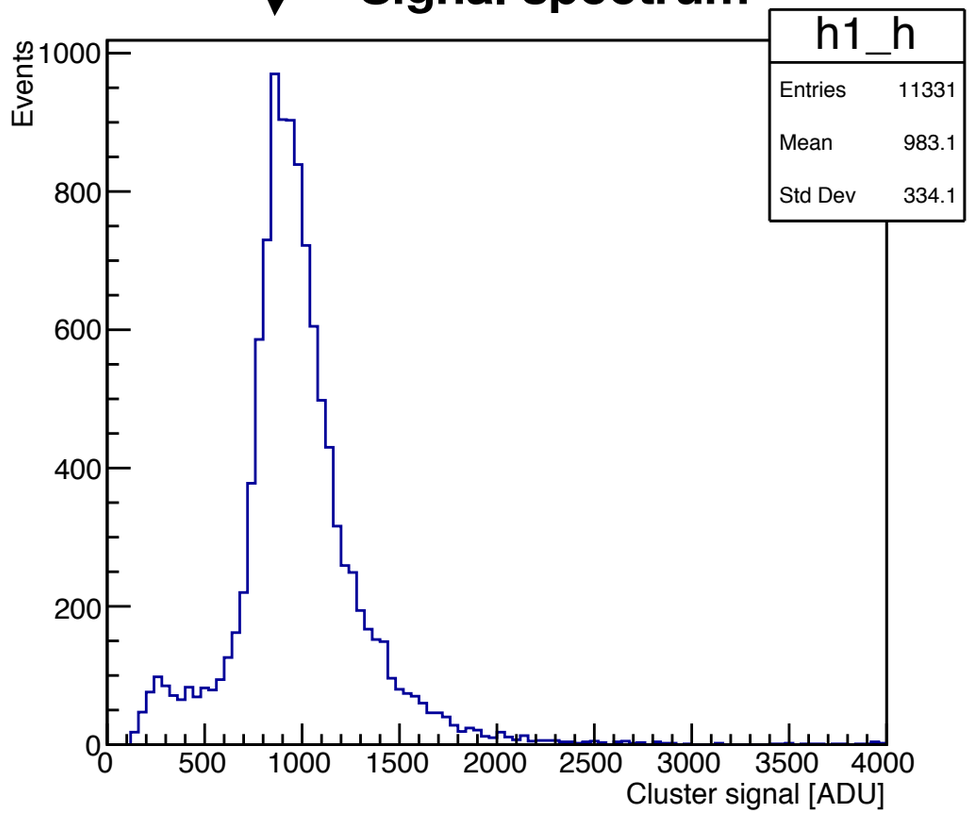



**Pedestal sigma (Noise)**
**Mean = 2.2 (All pixels)**




**Signal peak: ~800 ADU**

**Signal spectrum**




## Signal to Noise ratio

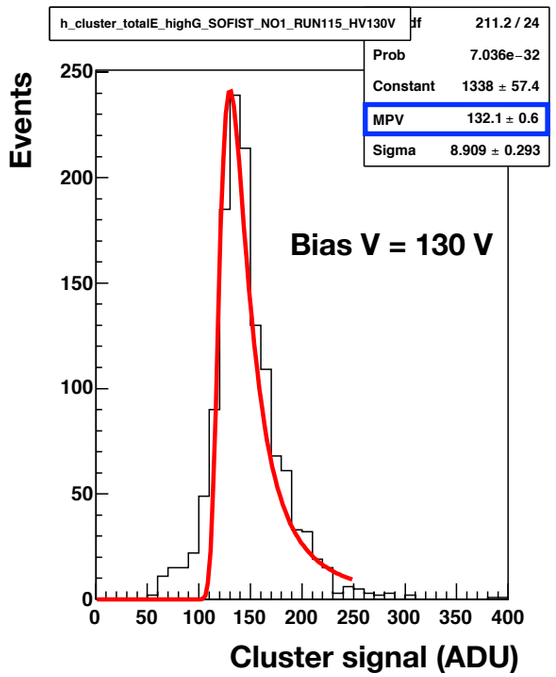
Signal peak = ~800 ADU
Pixel noise = ~2.2 ADU

→ S/N ~ 360 (Full depletion of 500 $\mu$m thickness)

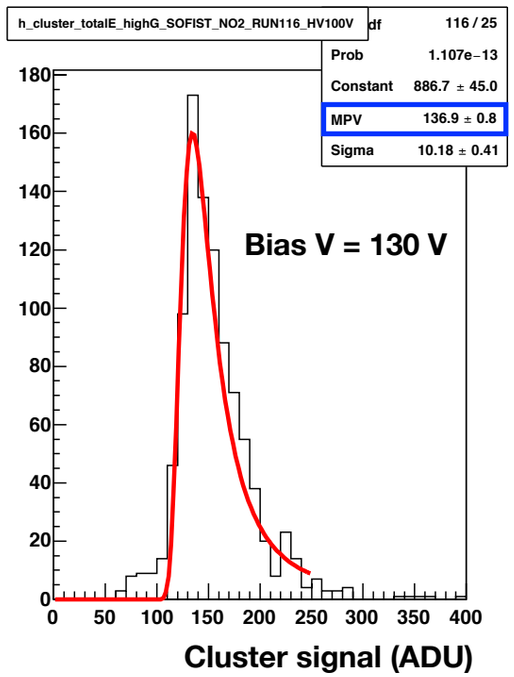
# HV Scan

**Signal peak dependence on a bias voltage.**

SOFIST #1



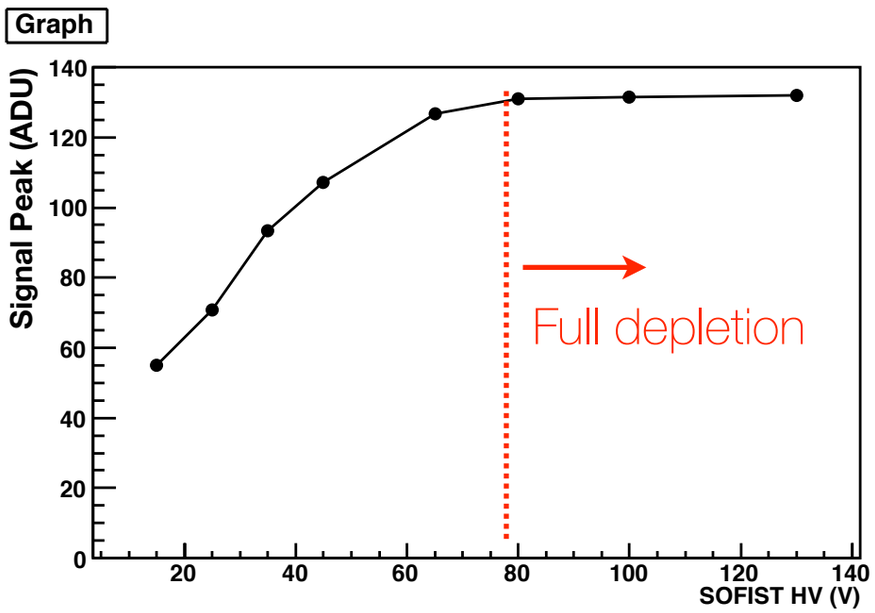

SOFIST #2

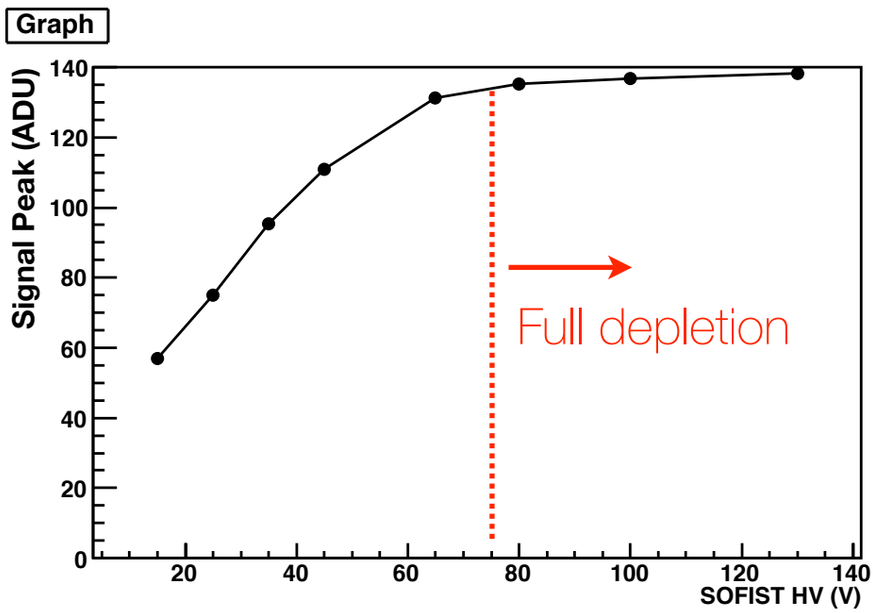



Signal spectrum fitted by Landau function.
(Readout: On chip 8 bit ADC)

→ Plot MPV as a function of the bias voltage.

Full depletion voltage is ~80 V for 500 $\mu$m.



# Tracking and Residual

**Sensor alignment (software)**

Parallel shift (*x* and *y*) and rotation (around the *z*-axis).

**Hit position reconstruction**

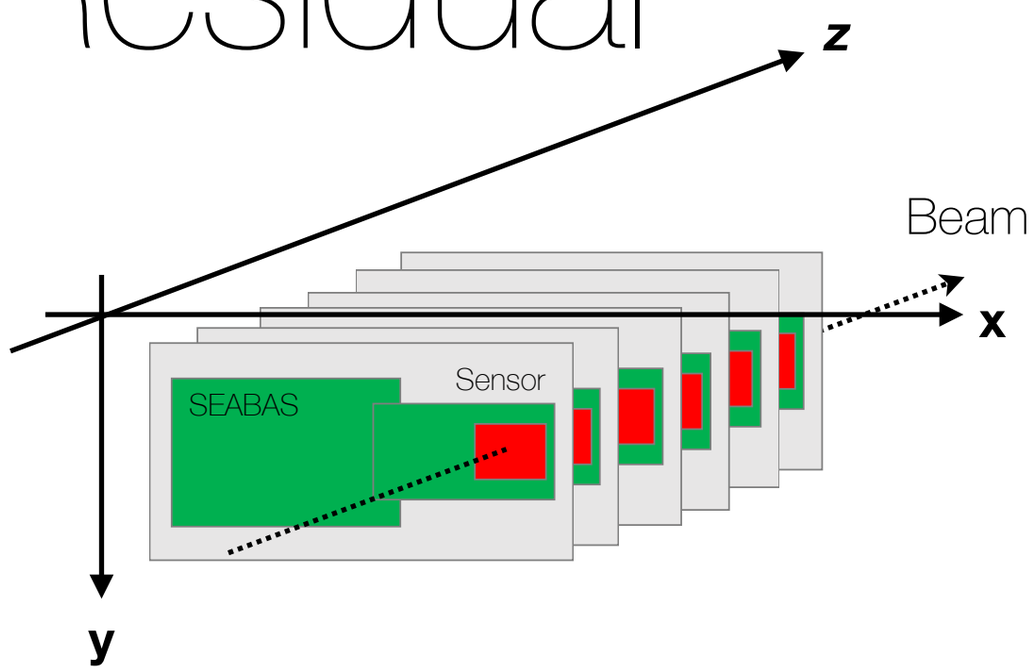
Calculate weighted center of charges (6 × 6 pixels).

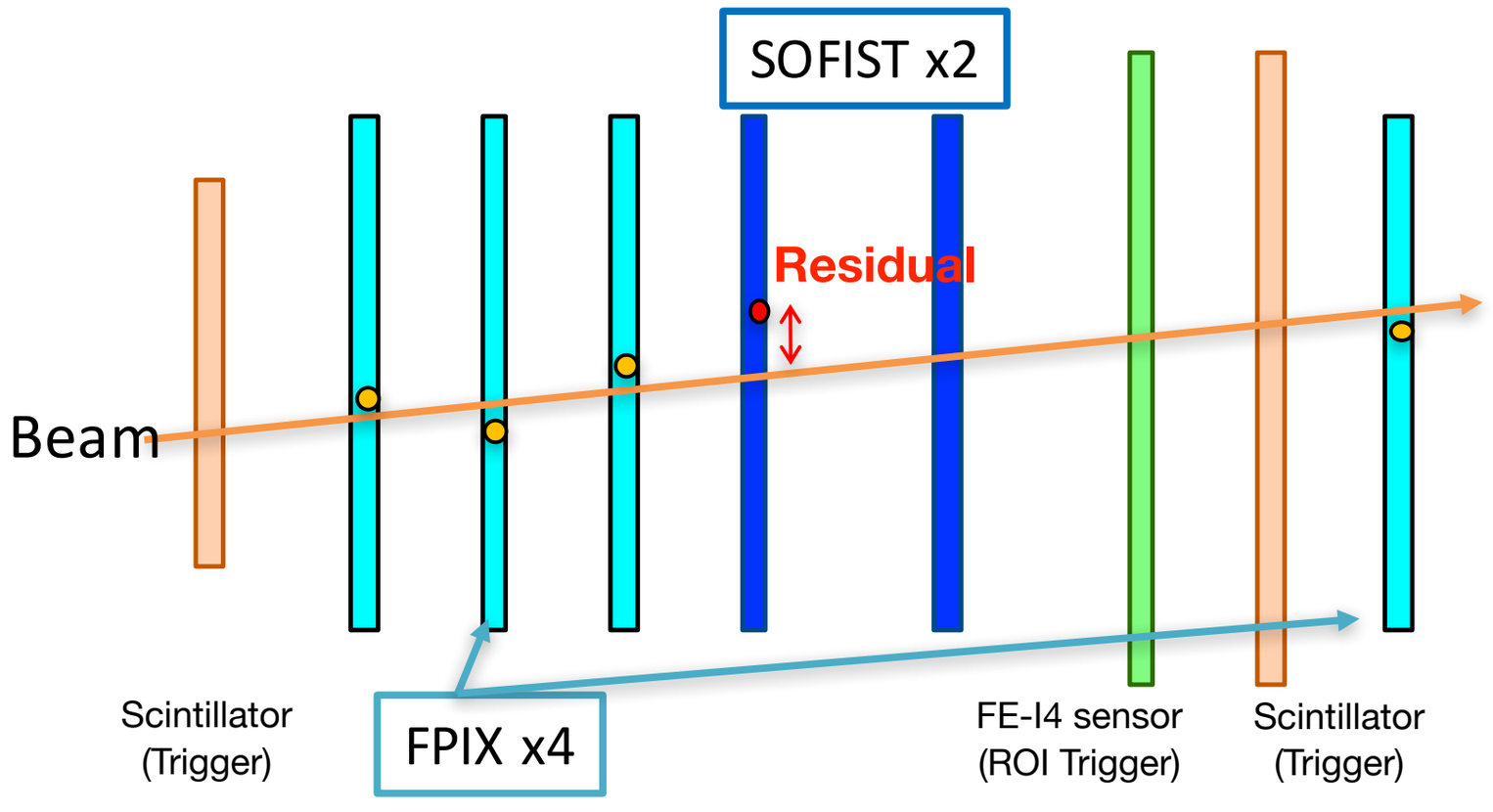
**Track reconstruction**

Find track candidates by four layers of FPIX.
The track that has the minimum chi2 is chosen
for calculating the residual.

**Residual**

Difference between reconstructed track and actual hit
on the SOFIST.

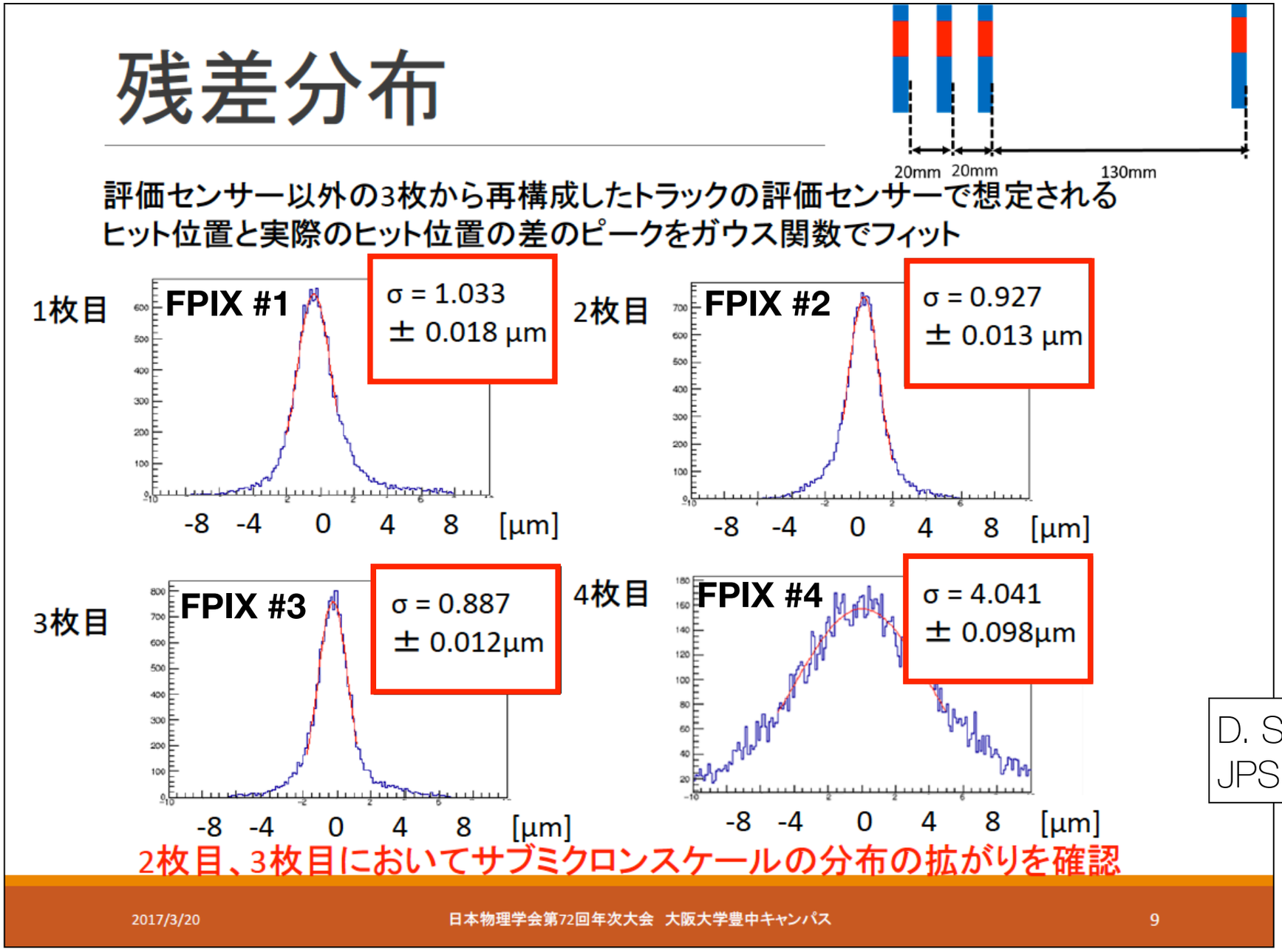


# FPIX Residual

**Tracking for FPIX**

Reconstruct track with three layers of FPIX without DUT.




D. Sekikawa (Univ. Tsukuba)
JPS 72nd annual meeting, Mar. 2017

**FPIX #2 and 3 achieved residual better than 1 *μ*m.**

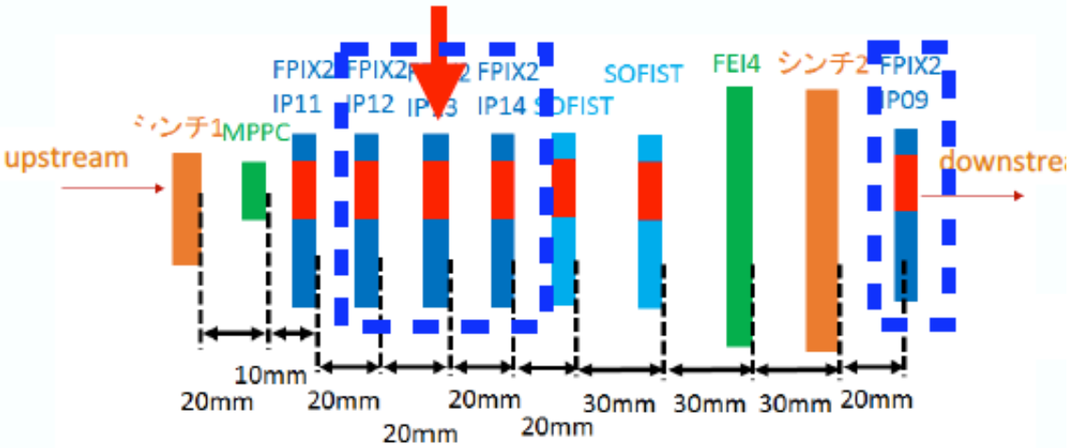
# FPIX Position Resolution

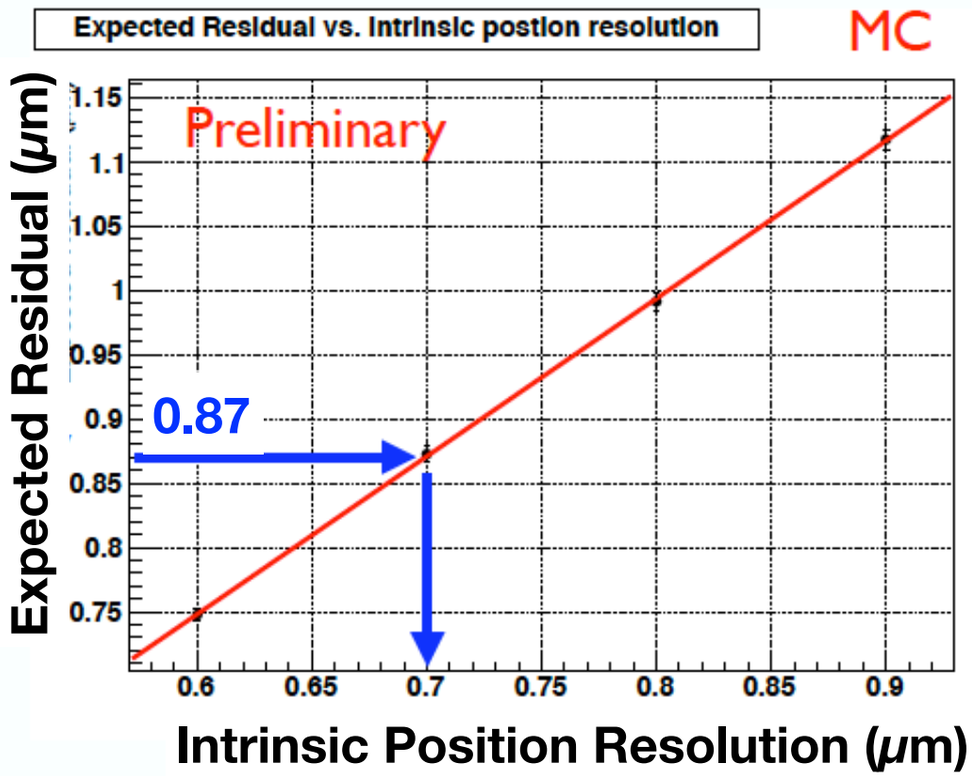
M. Togawa (KEK)
LC Vertex Detector Workshop, Ringberg
May 2nd, 2017

FPIX

## The position resolution of FPIX2 demonstrated by MC

Evaluated by center sensor




- Intrinsic position resolution is expected to be ~0.7 μm !
  - No evaluation systematic error yet
- Tracking resolution is ~0.5 μm

Sub-micron resolution was achieved !
< 1 um tracking was achieved !!

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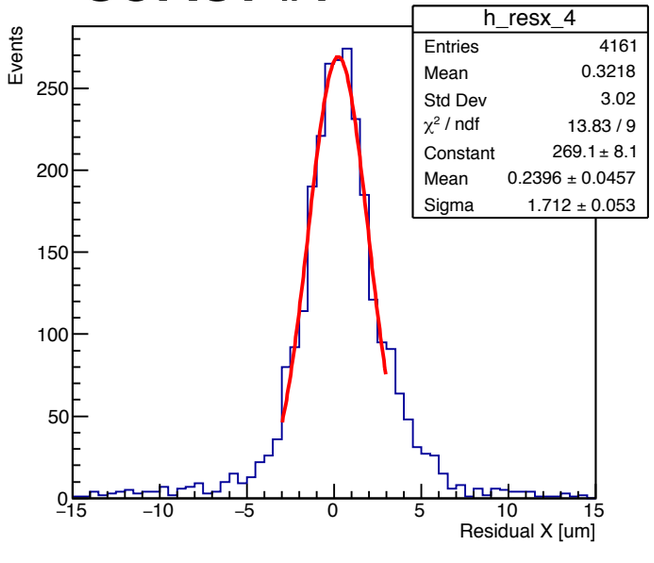
# SOFIST Residual

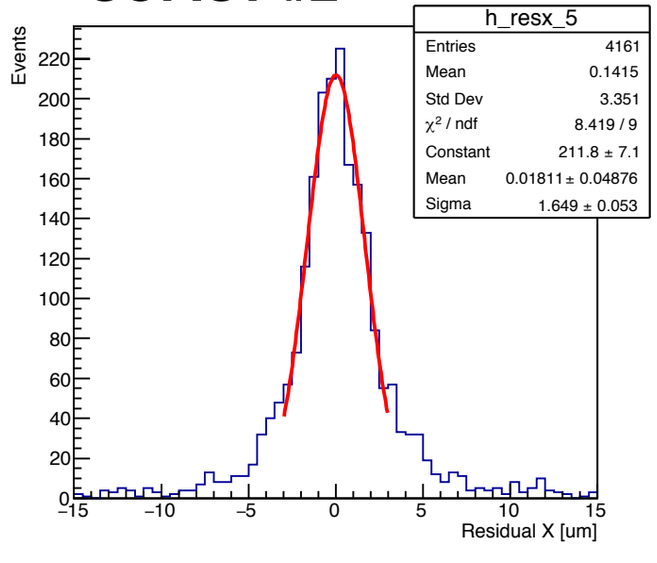
**Residual X**

**SOFIST #1**



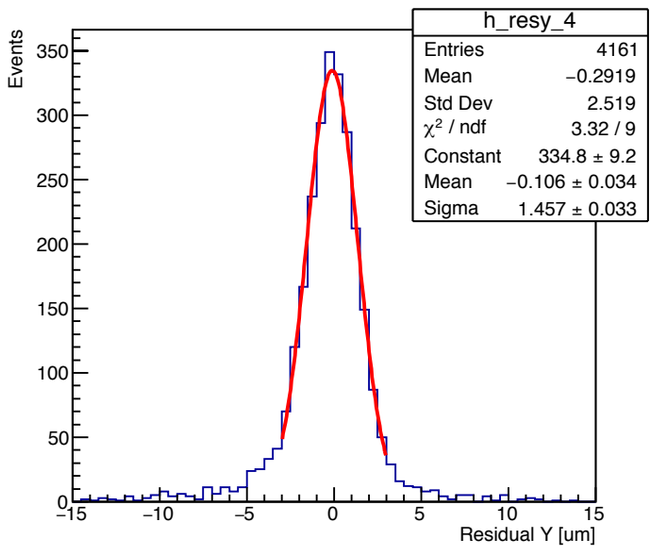

**1.65 ± 0.05 $\mu$m**

**SOFIST #2**

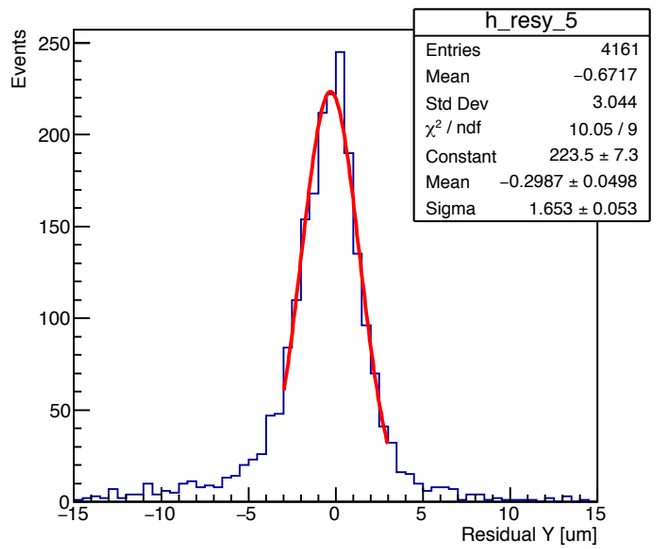



**1.71 ± 0.05 $\mu$m**

**Residual Y**




**1.46 ± 0.03 $\mu$m**



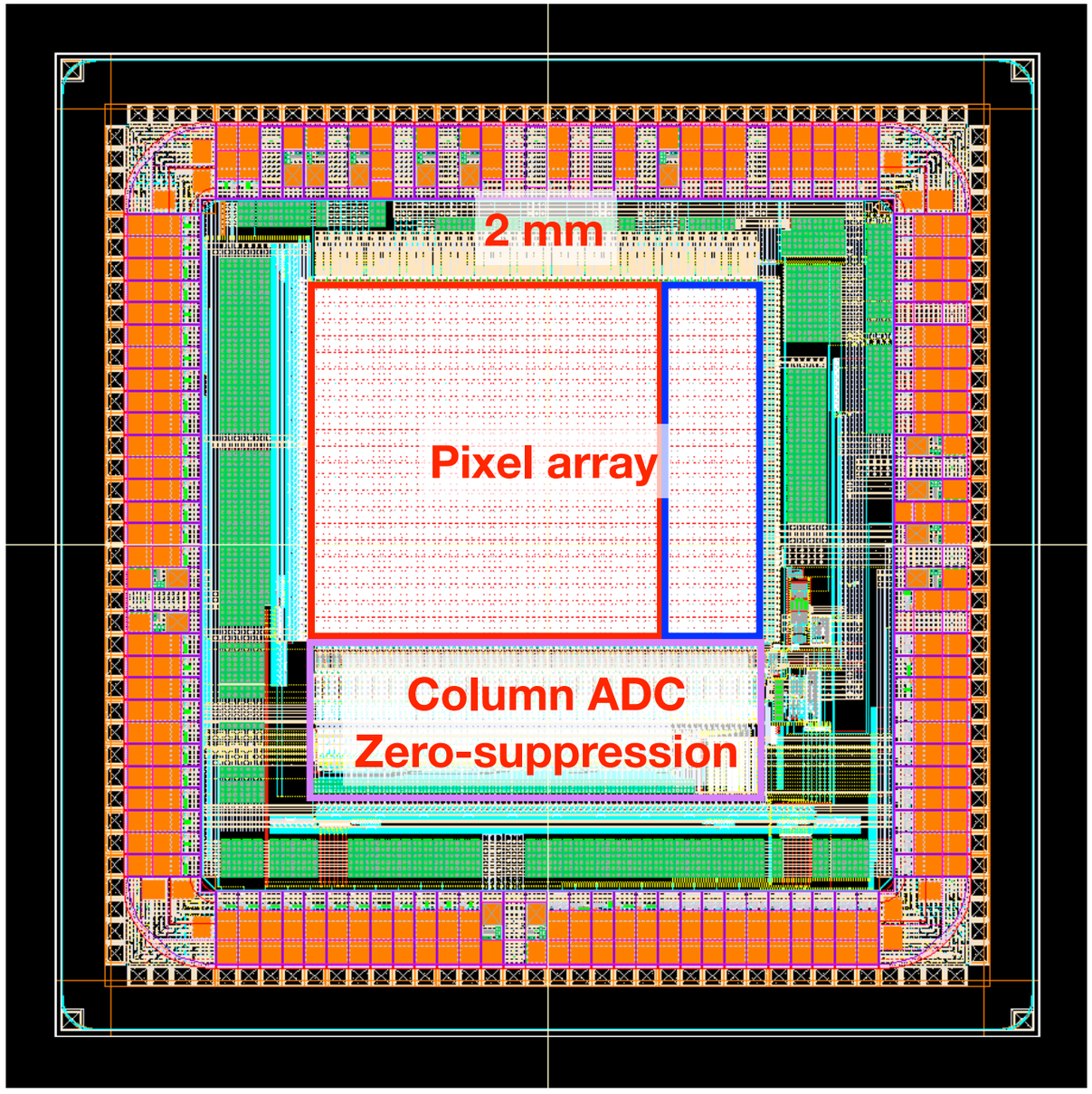

**1.65 ± 0.05 $\mu$m**

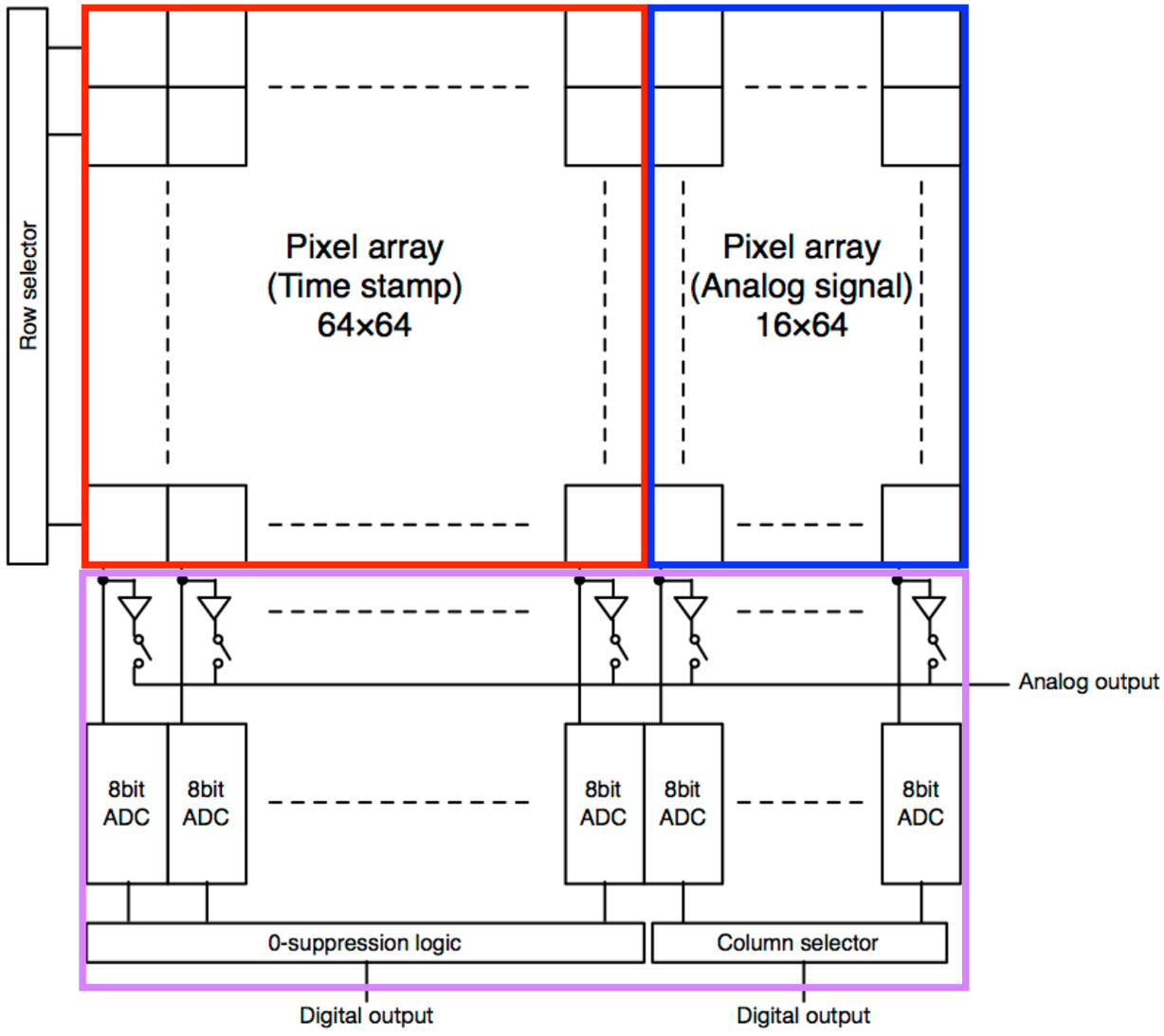
**SOFIST achieved the residual to ~1.5 $\mu$m with 20 × 20 $\mu$m$^2$ pixel.**

# SOFIST ver.2

# SOFIST ver.2

**Wafer: FZ *p*-type**




Pixel size: 25 × 25 $\mu$m$^2$
Chip size: 4.45 × 4.45 mm$^2$
Active area: 2.0 × 1.6 mm$^2$ (80 × 64 pixels)
Wafer: CZ *p*-type, Double SOI, 300 $\mu$m thickness

# SOFIST ver.2

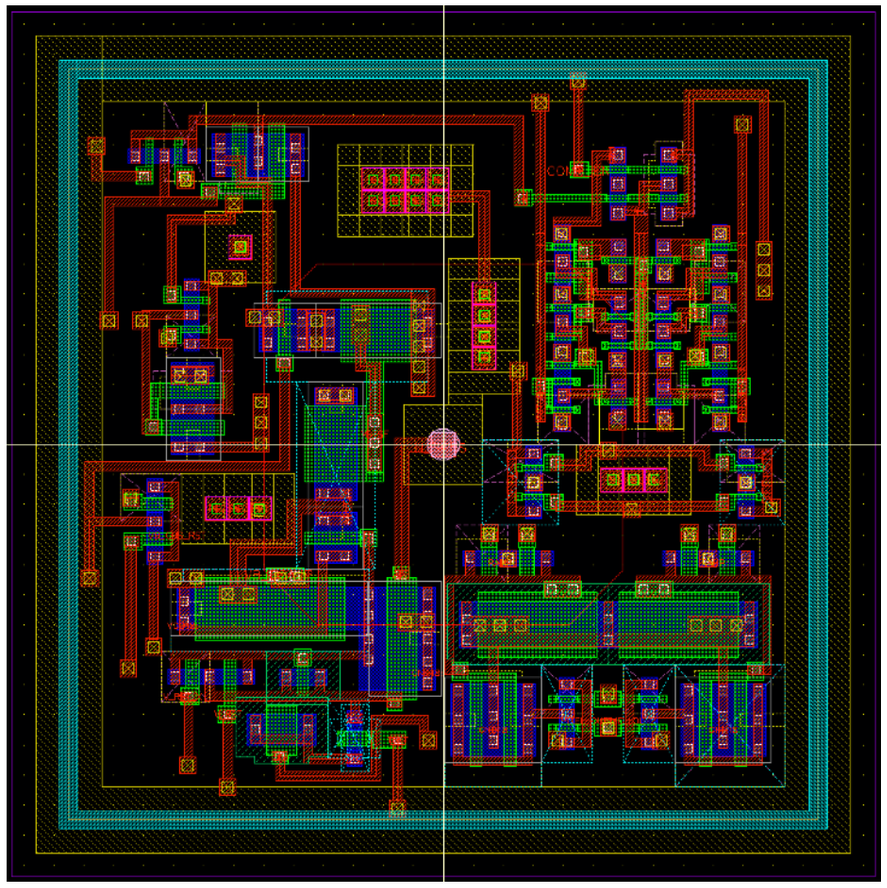
**Pixel**

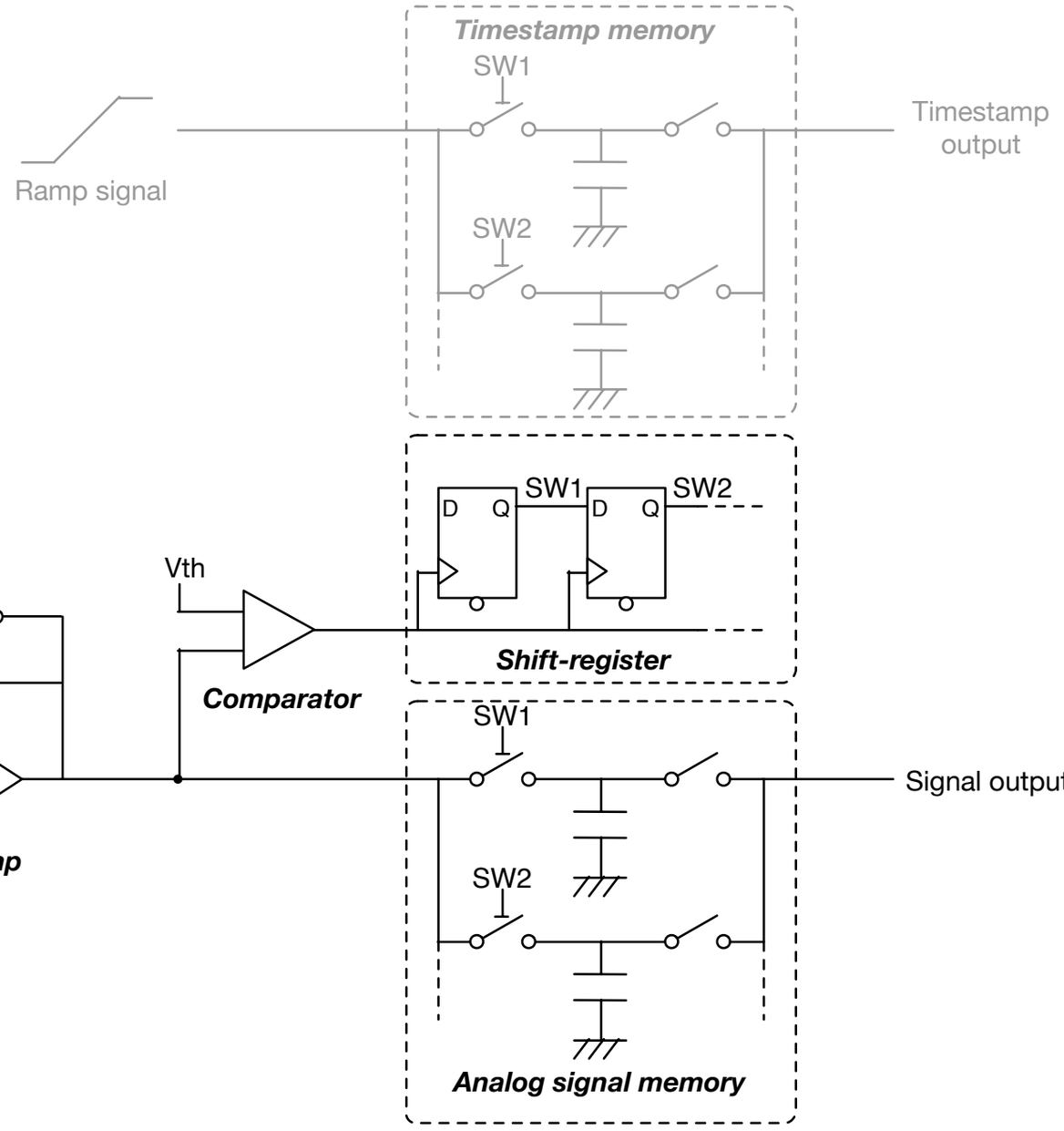
- Pre. amplifier (Charge sensitive amplifier)
- Comparator (Chopper inverter)
- Shift register
- Analog signal memories (two memories)
  or Time stamp memories (two memories)

**On chip**

8 bit column ADC
Zero-suppression logic

Pixel size: 25 × 25 $\mu m^2$






**SOFIST ver.2**
**Analog pixel**

# SOFIST ver.2

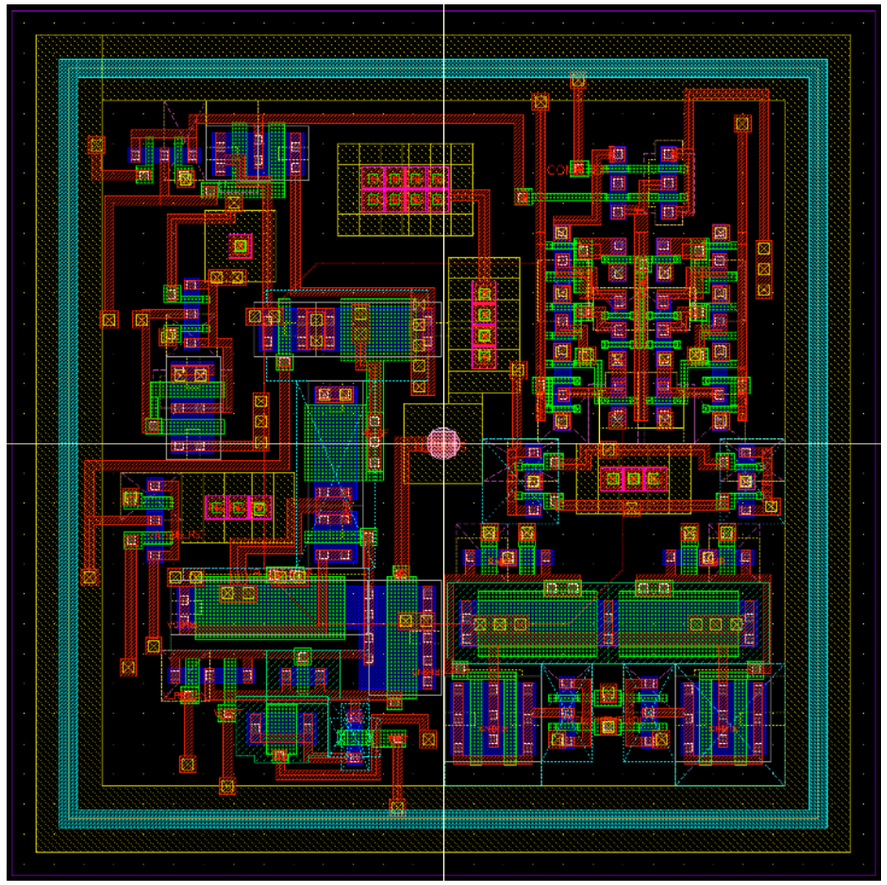
**Pixel**

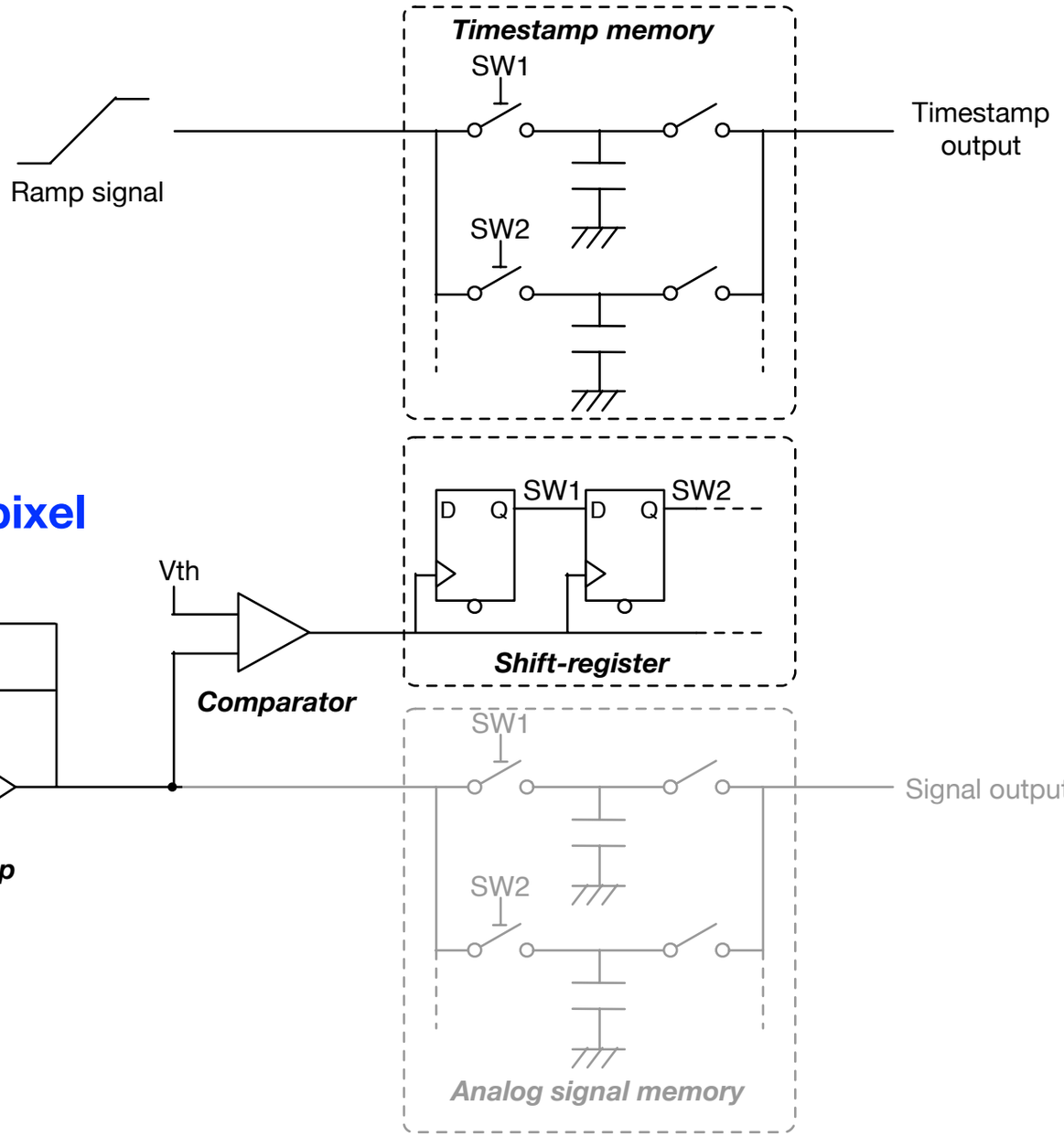
- Pre. amplifier (Charge sensitive amplifier)
- Comparator (Chopper inverter)
- Shift register
- Analog signal memories (two memories)
  or Time stamp memories (two memories)

**On chip**

8 bit column ADC
Zero-suppression logic

Pixel size: 25 × 25 $\mu m^2$



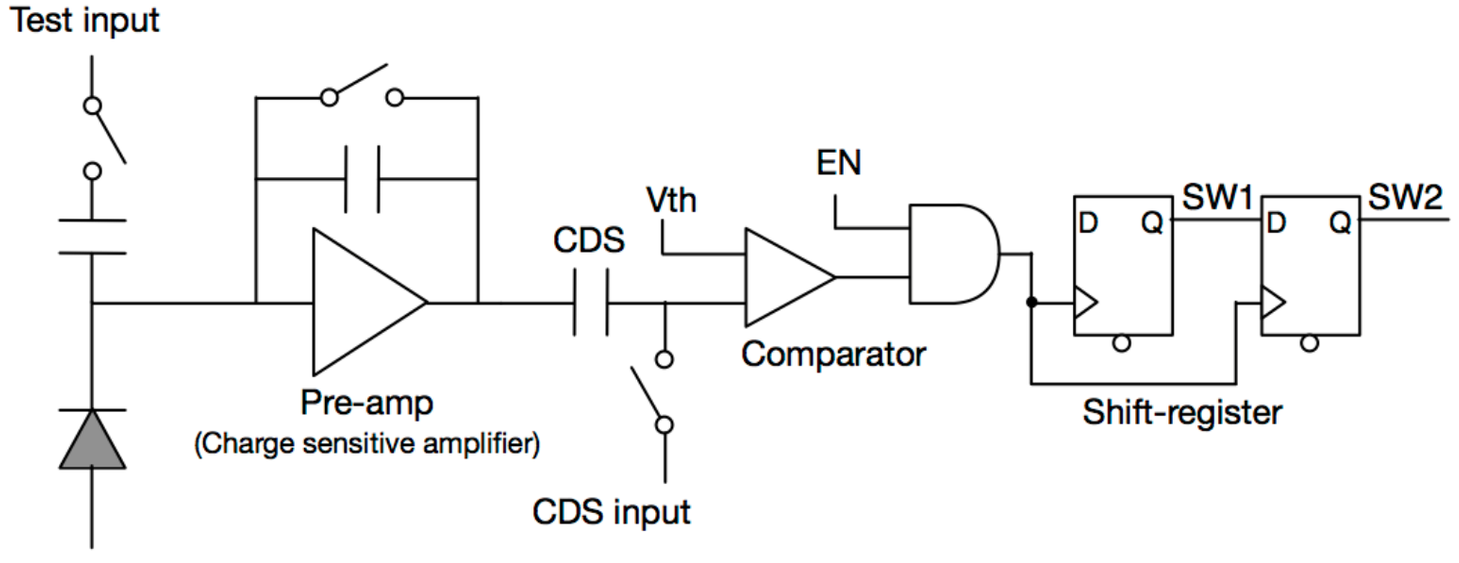


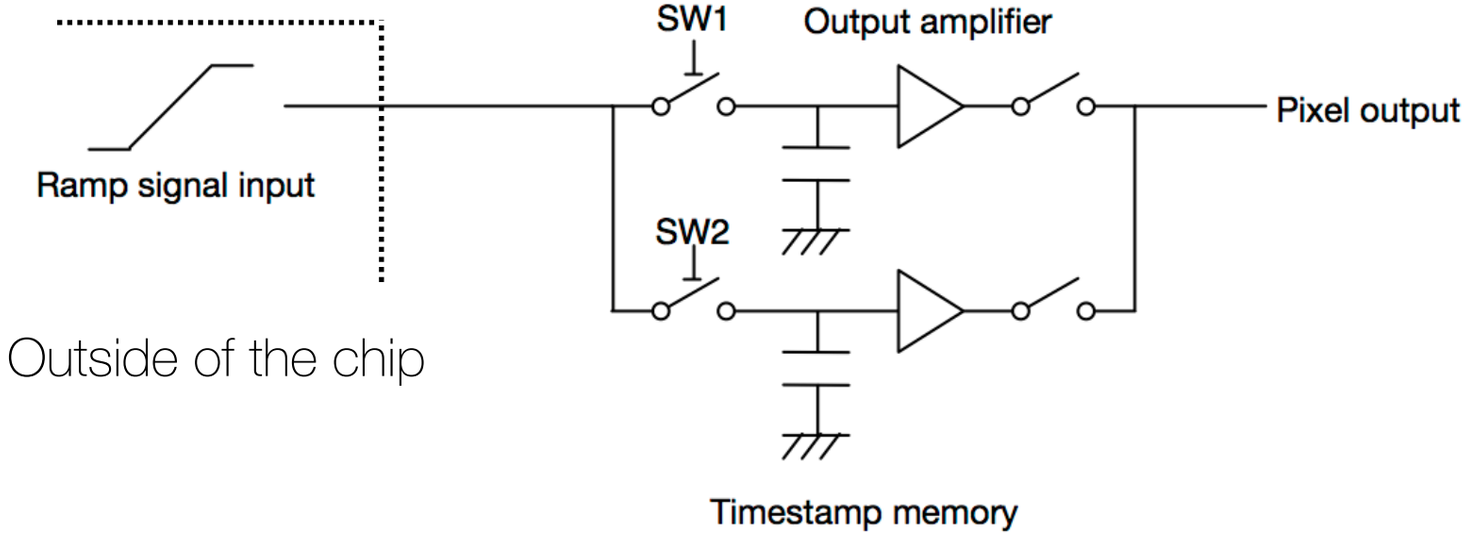

**SOFIST ver.2**
**Time stamp pixel**

# Time Stamp Pixel

Designed by S. Ono (KEK)

- Pre-amplifier
  Charge Sensitive Amp.
- Comparator
  Chopper Inverter type
- Shift register
  D-FF

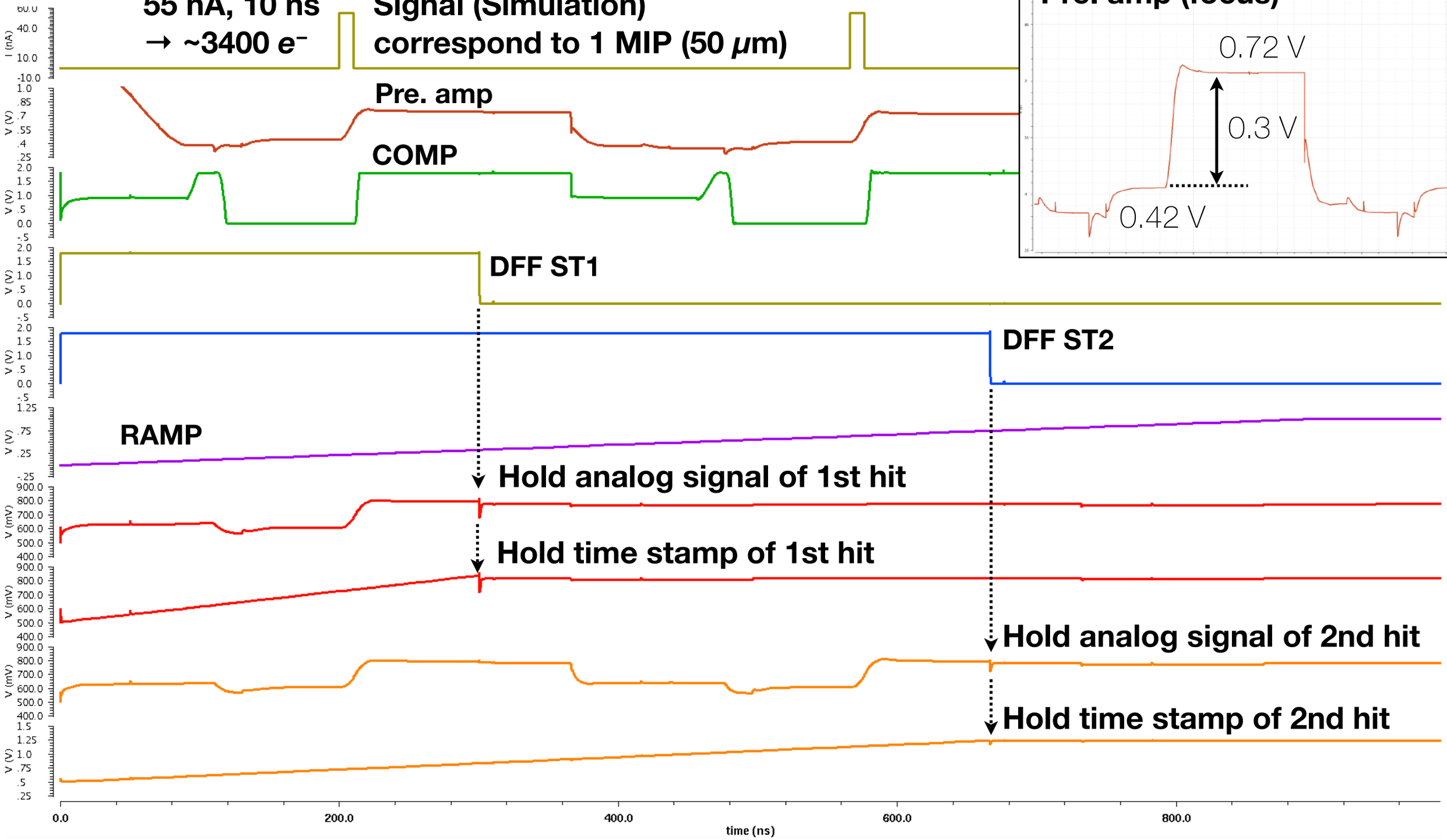



1) Input a RAMP waveform.
2) Open a store switch (ST1) when a comparator output changes to High.
3) Keep the voltage of RAMP to the time stamp memory as a time stamp.
4) in the same way for 2nd hit.

# Time Stamp and Analog Pixel

**Simulation of 1 $\mu$s transient analysis**



# SOFIST ver.3 & 4

# SOFIST ver.3

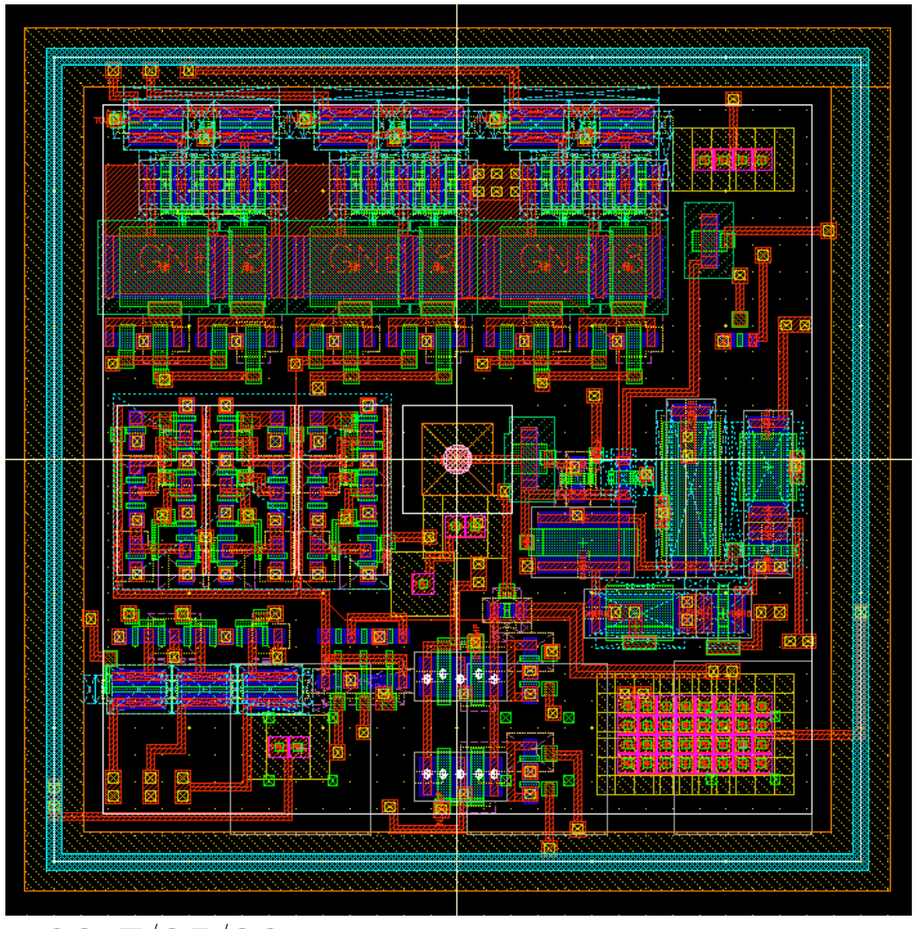
**Pixel**

- Pre. amplifier (Charge sensitive amplifier)
- Comparator (Chopper inverter)
- Shift register
- Analog signal memories (three memories)
- Time stamp memories (three memories)

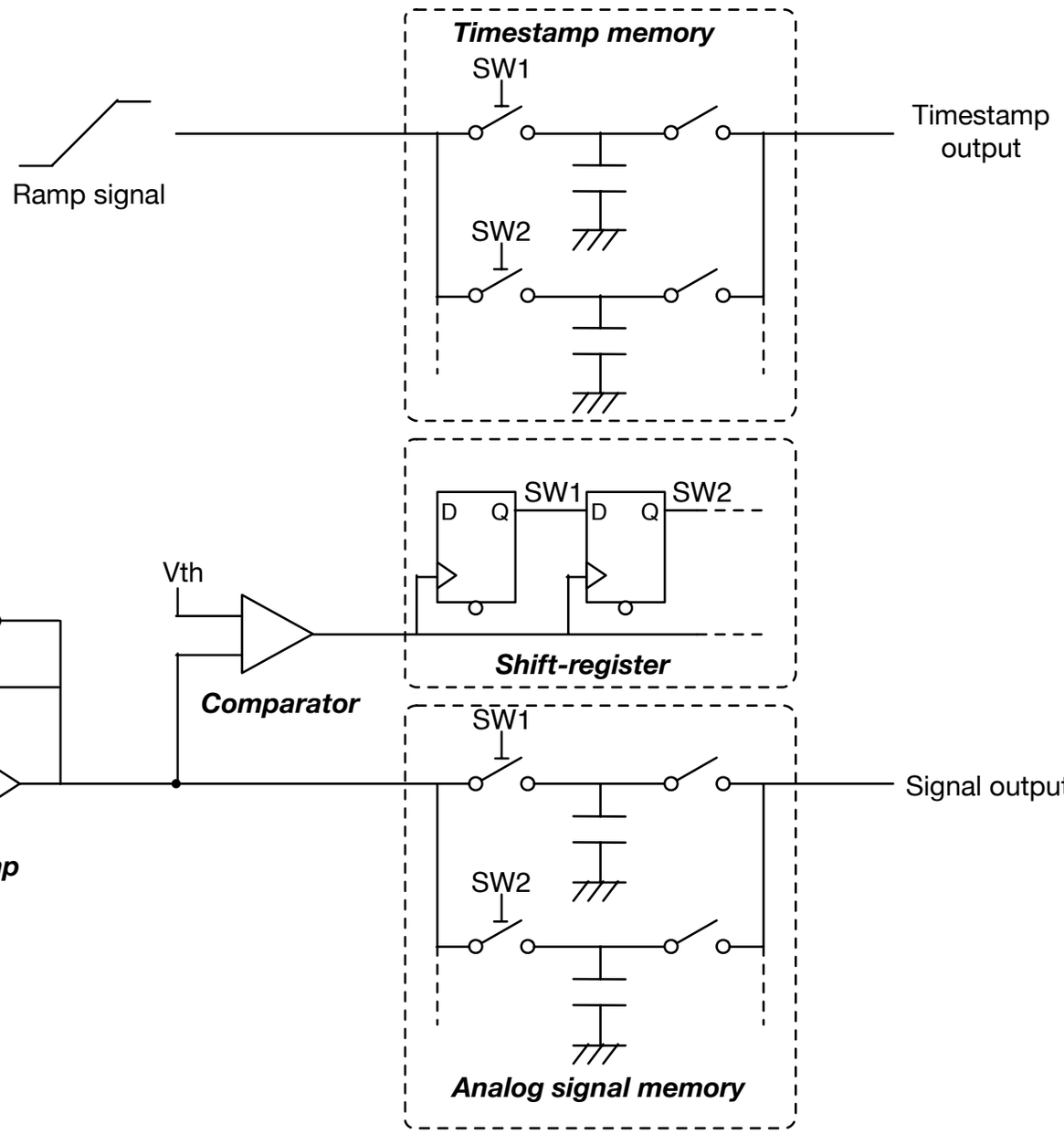
**On chip**

8 bit column ADC

Pixel size: 30 × 30 $\mu m^2$



SOFIST ver.3 is still under designed.
We are going to submit in June 2017.

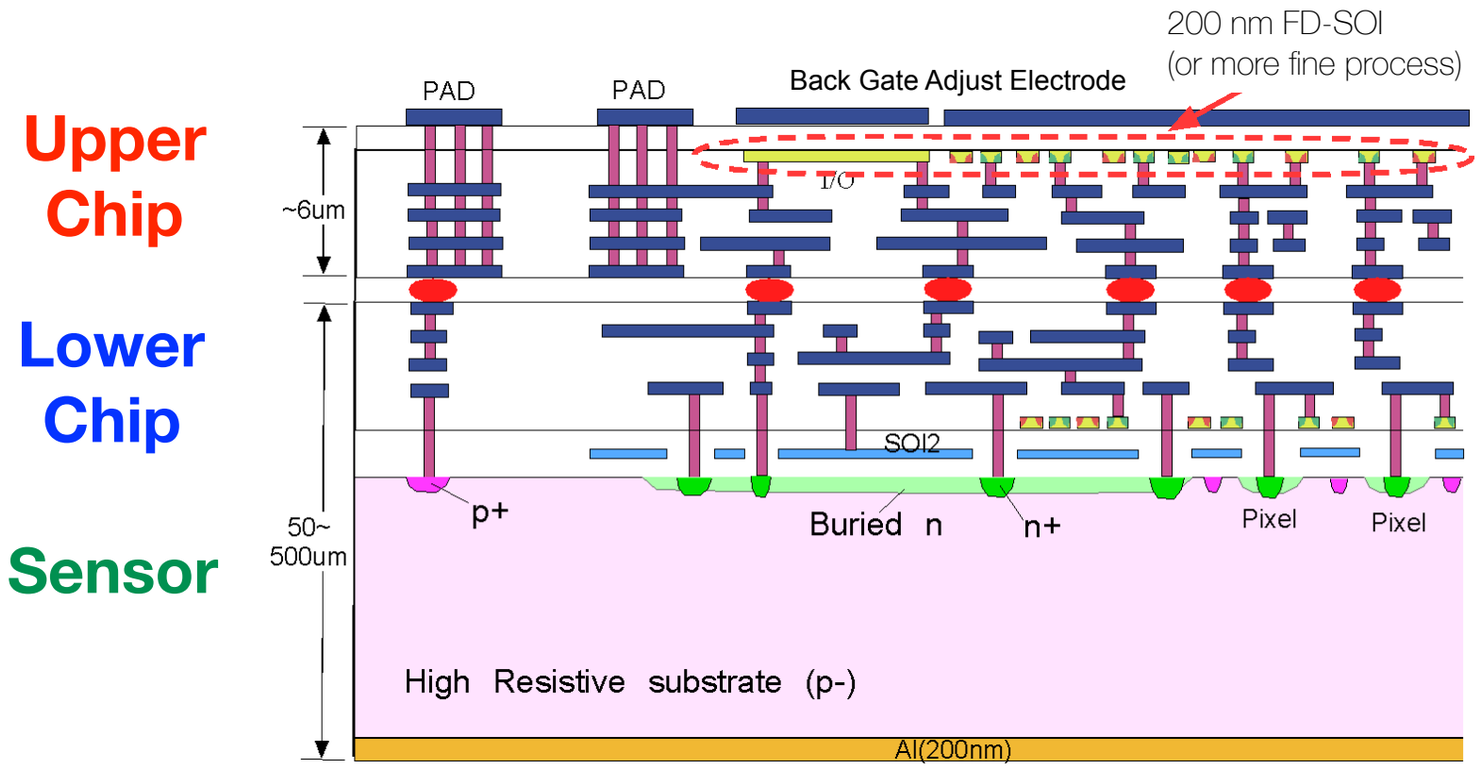


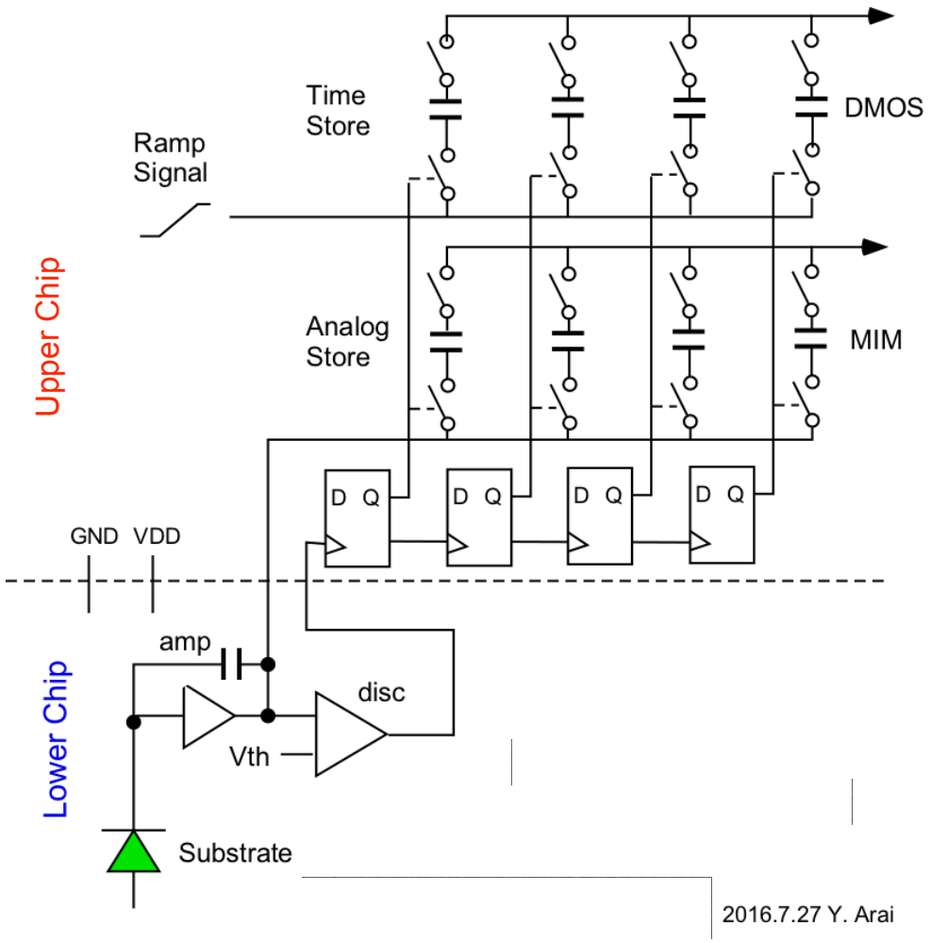

All the functions are implemented in a pixel but lager pixel size.

# SOFIST ver.4 (3D)

**3D integration of SOI sensor**

for implementation of complex circuit within 20 × 20 $\mu m^2$ pixel.




Upper chip: Digital part (D-FF, analog memories and time stamp memories up to 3 or more hits)
Lower chip: Analog part (pre.amp and comparator)

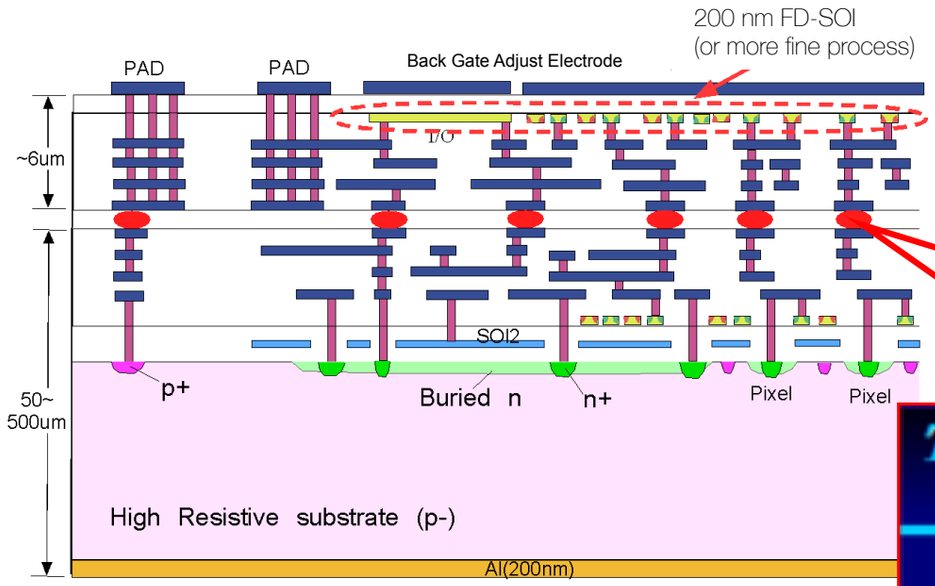
# SOFIST 3D

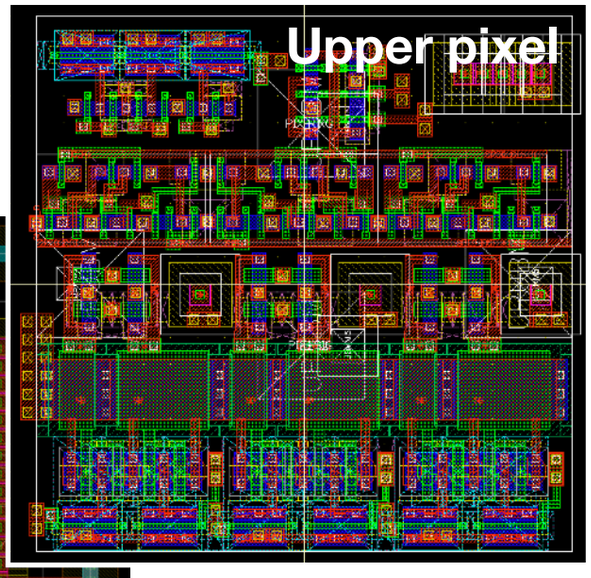
**3D integration of SOI sensor**
**→Connect the upper and lower chip by Au cone bump (2.5 *μmϕ*).**

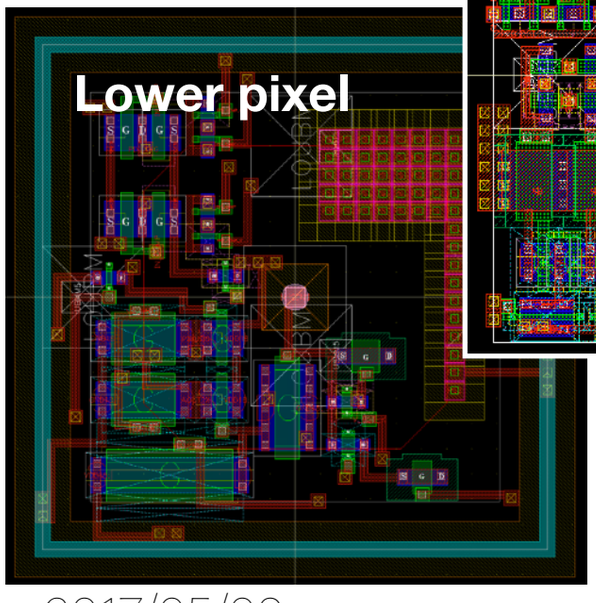
**Upper Chip**

**Lower Chip**

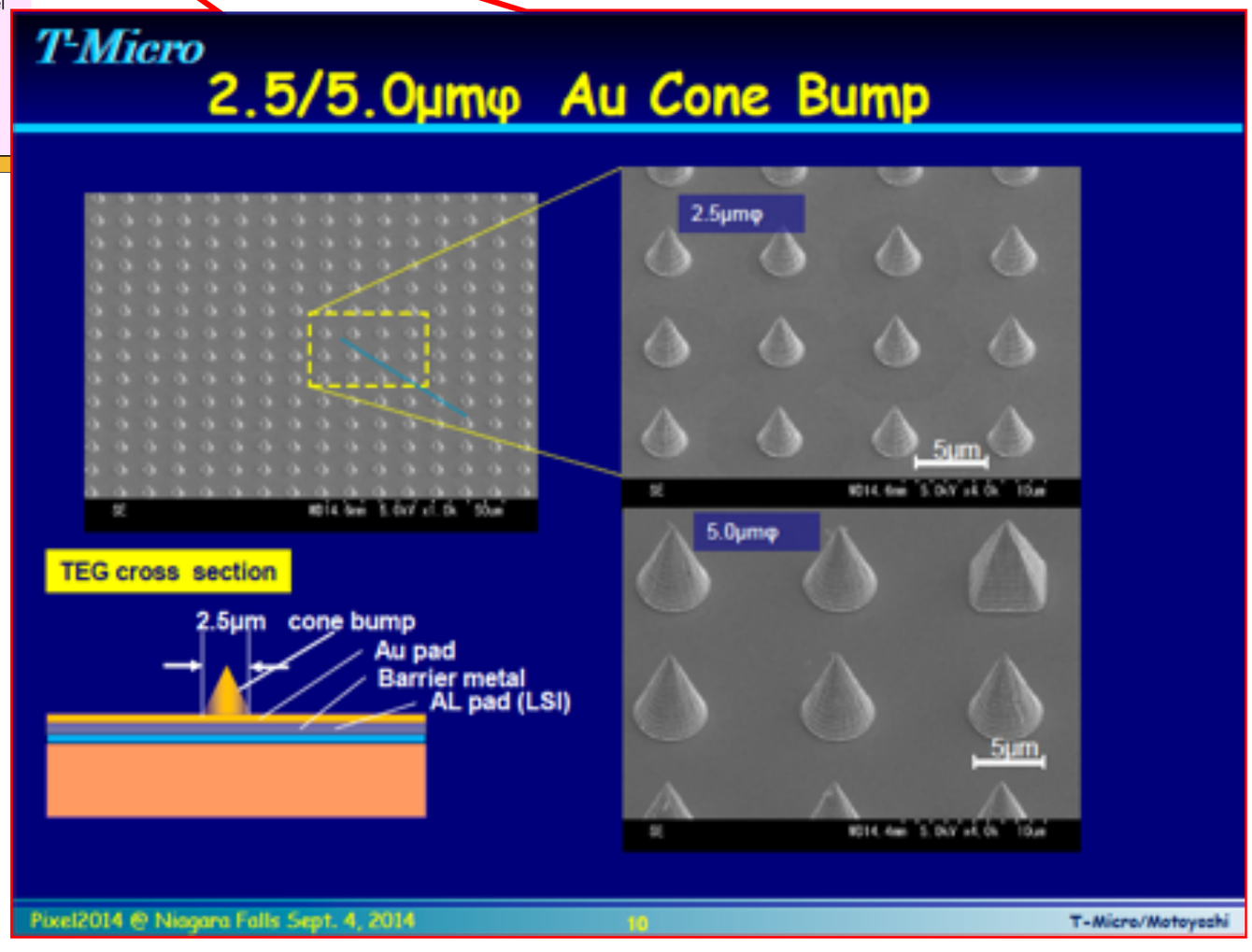
**Sensor**




**Tohoku MicroTec Co., Ltd.**
http://www.t-microtec.com



# Summary

We are designing and developing a monolithic type pixel detector with SOI technology for the ILC vertex detector (SOFIST).

**SOFIST ver.1**

We evaluated S/N and position resolution by using 120 GeV proton beam at Fermilab beam test facility in Jan. 2017.

- S/N ~360 at HV = 130 V for 500 $\mu$m thickness sensor.
- Position resolution (residual) ~1.5 $\mu$m.

**SOFIST ver.2**

Chip have already delivered to KEK in Jan. 2017, and we are preparing DAQ.

We will evaluate

- Time stamp function for multiple hit (up to two hits).
- Thinned sensor (75 $\mu$m).

**SOFIST ver.3 and 4**

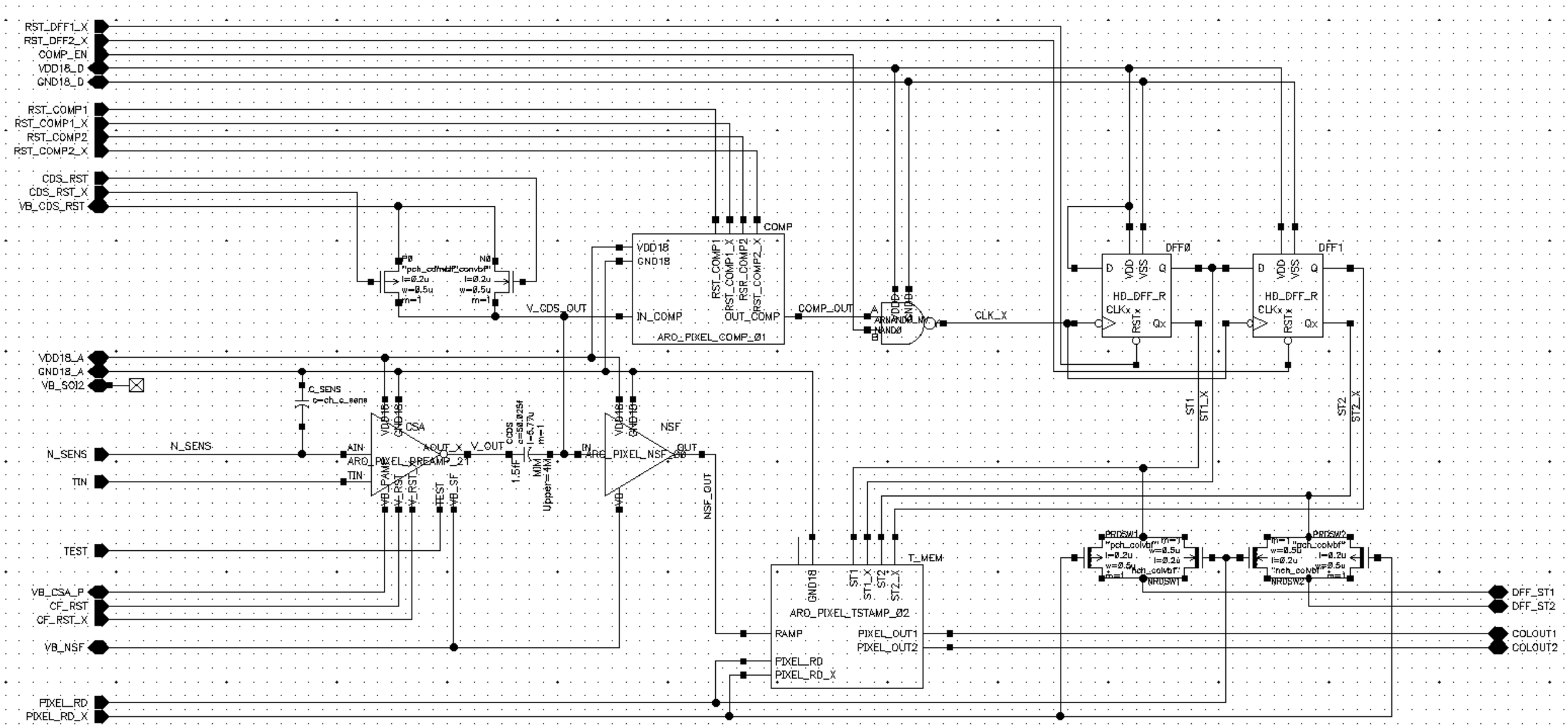
ver.3 and 4 chips are still under designing (submit in June 2017).

ver.3: all necessary functions are implemented in a single pixel but 30 × 30 $\mu m^2$ pixel size.

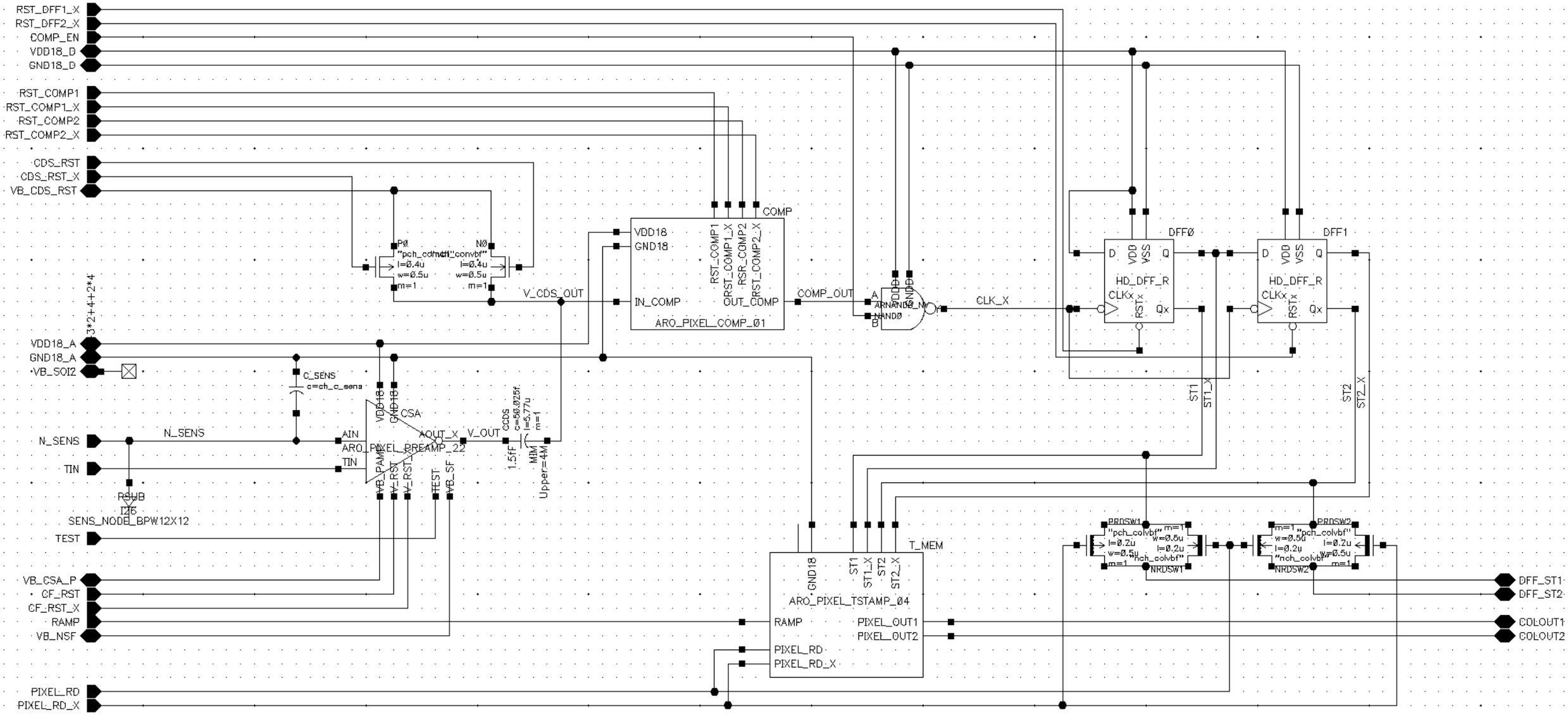
ver.4: all necessary functions are implemented in 20 × 20 $\mu m^2$ pixel with 3D integration technology (Au cone bump).

# Backup

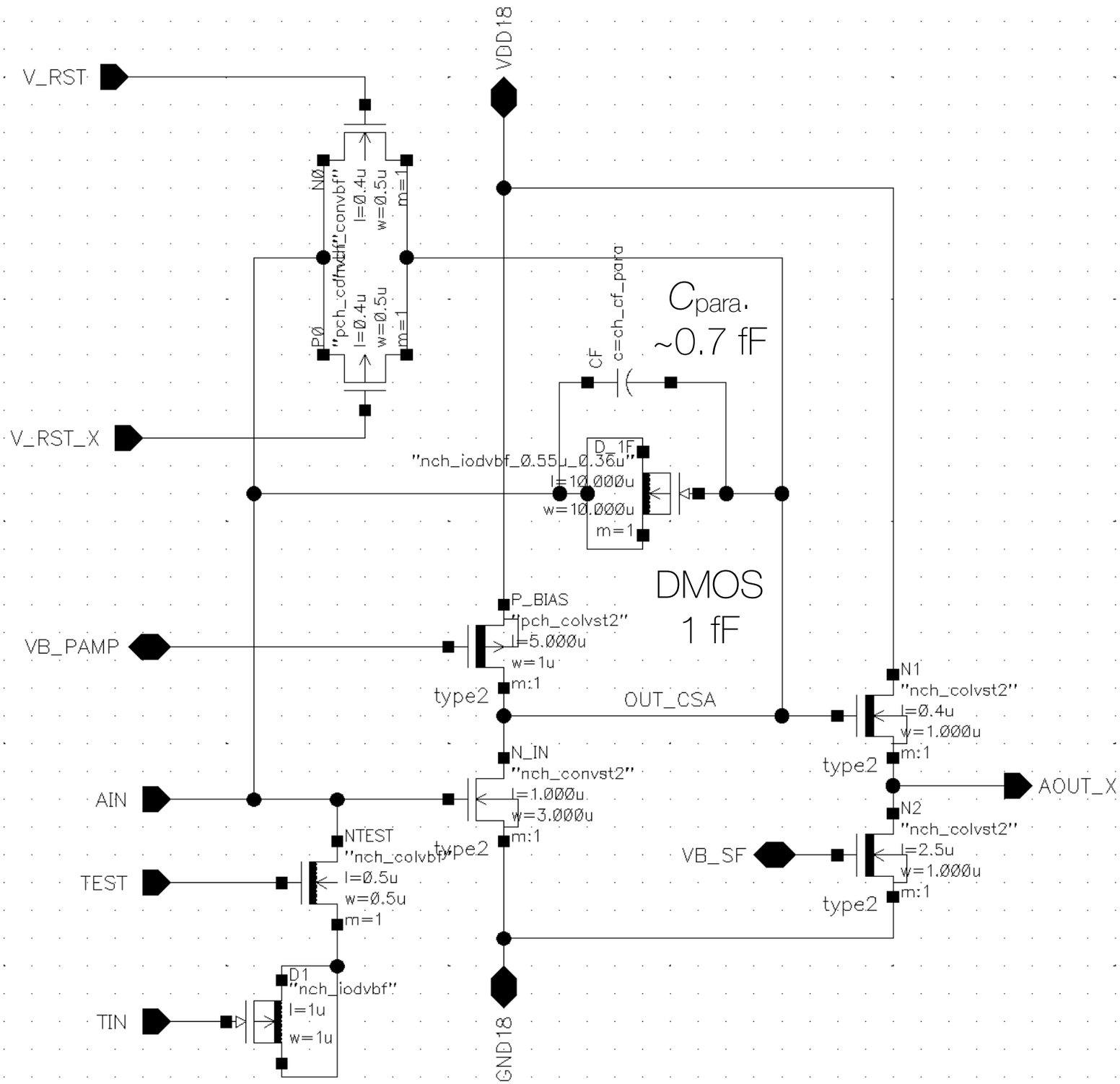
# Analog Pixel



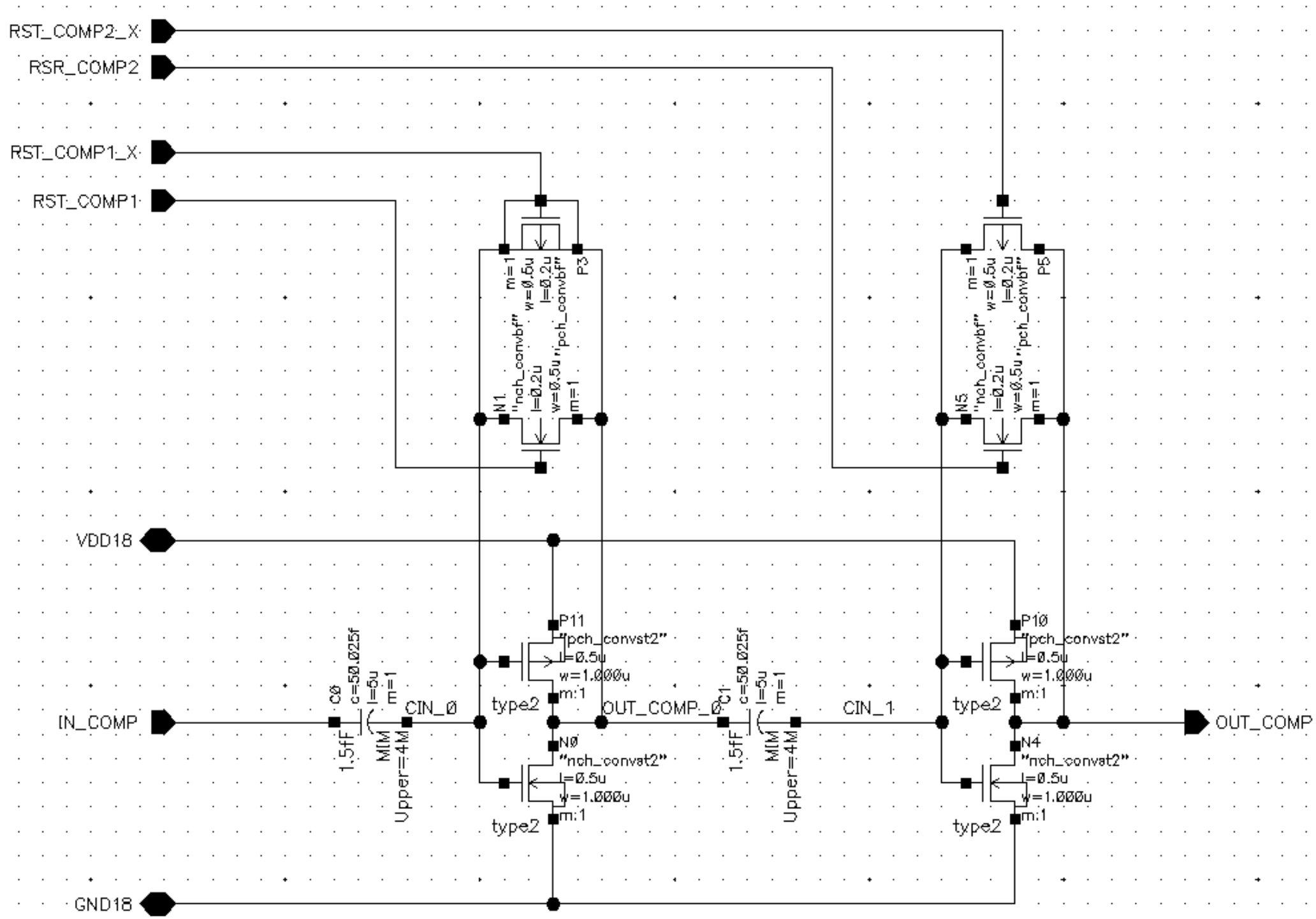
# Time Stamp Pixel



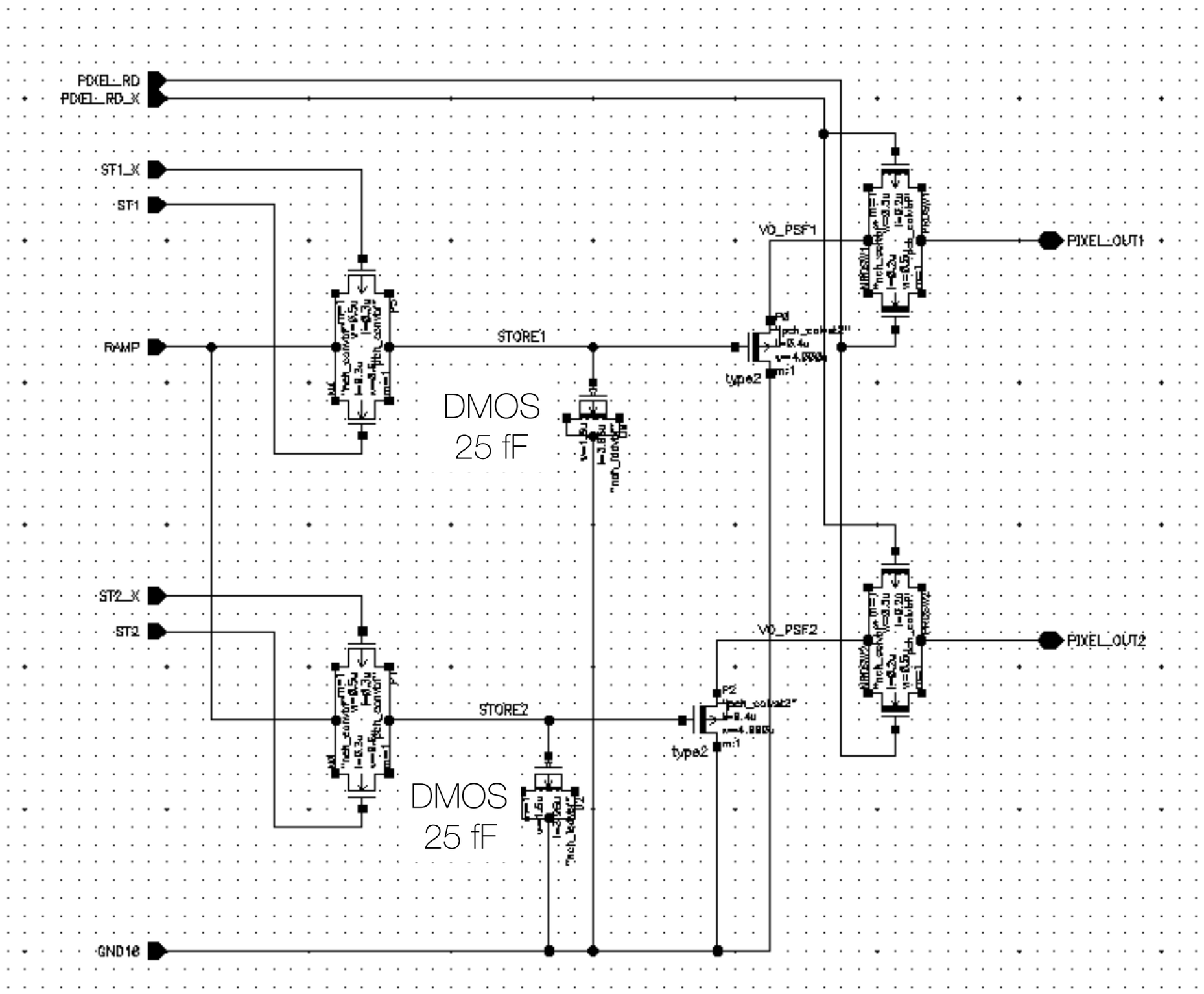
# Pre-amplifier



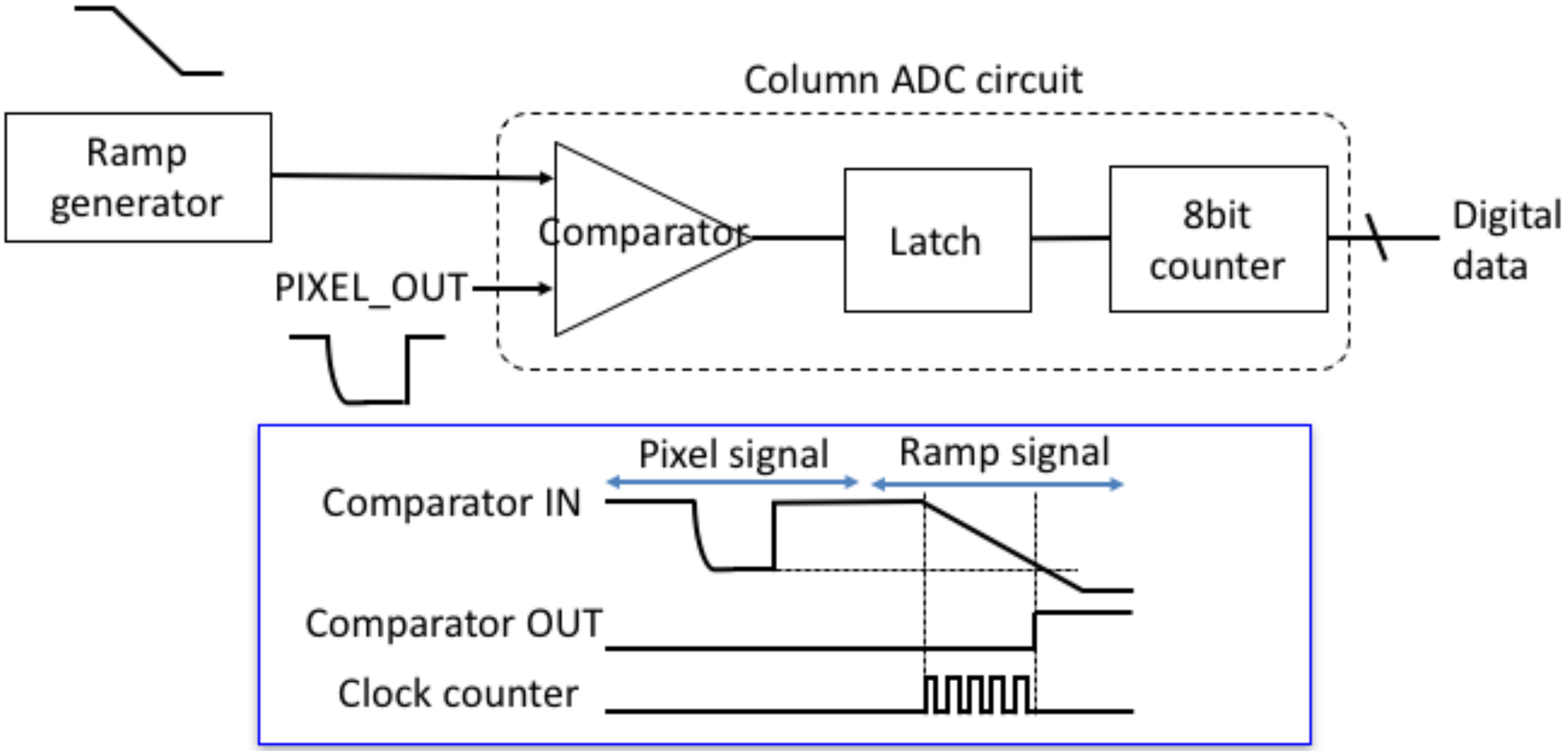
# Comparator


RST_COMP2_X
RSR_COMP2
RST_COMP1_X
RST_COMP1
VDD18
GND18
IN_COMP
OUT_COMP
CIN_Ø
CIN_1
OUT_COMP_Ø
C1
c=50.025f
l=5u
m=1
1.5fF
MIM
Upper=4M
type2
P11
"pch_convst2"
l=Ø.5u
w=1.ØØØu
m:1
NØ
"nch_convst2"
P3
P5
P1Ø
N4
N5
N1
"nch_conv6f"
l=Ø.2u
w=Ø.5u
"pch_conv6f"

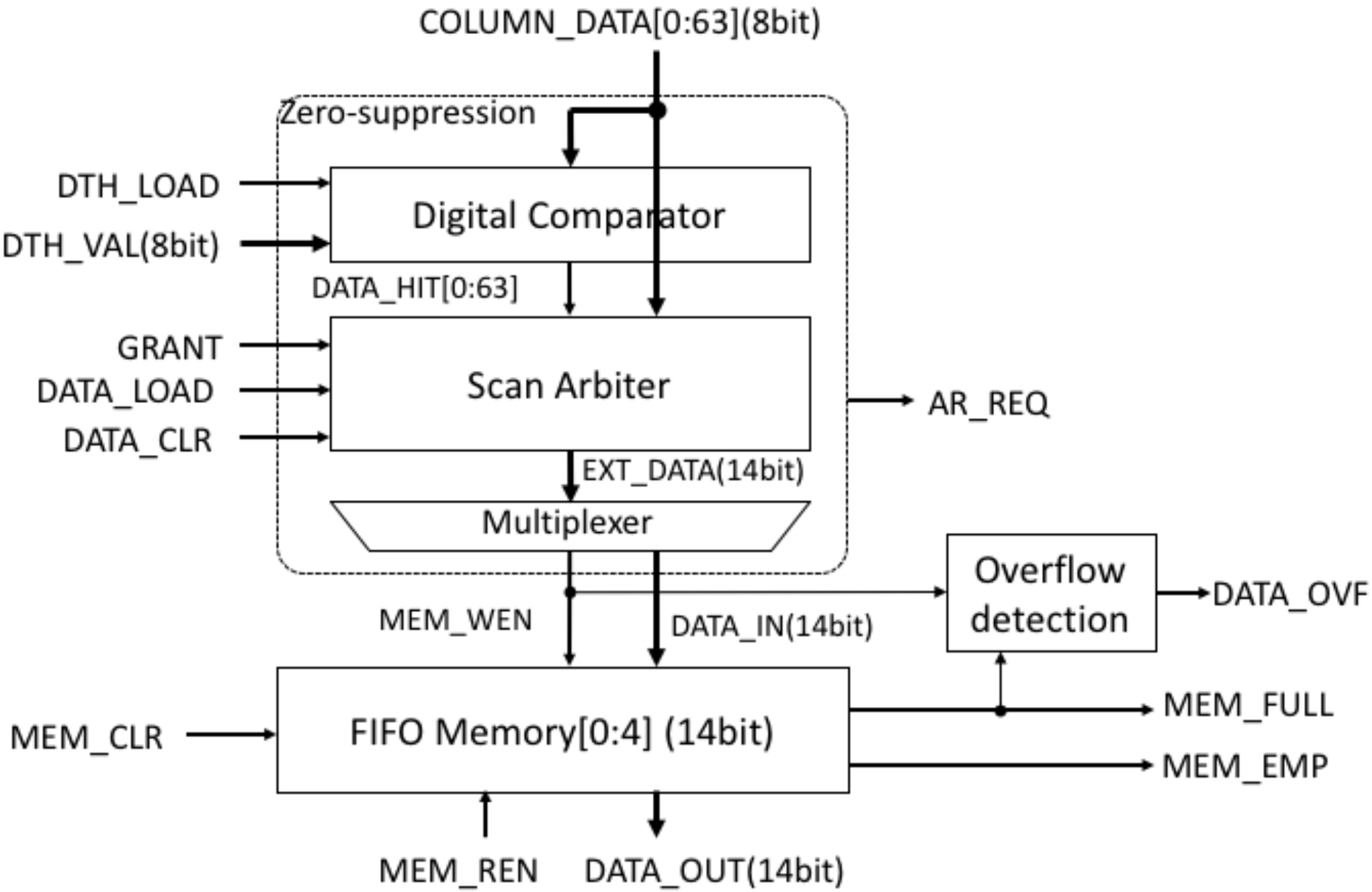
# Memory


PIXEL_RD
PIXEL_RD_X
ST1_X
ST1
RAMP
STORE1
VO_PSF1
PIXEL_OUT1
DMOS
25 fF
ST2_X
ST2
STORE2
VO_PSF2
PIXEL_OUT2
DMOS
25 fF
GND18

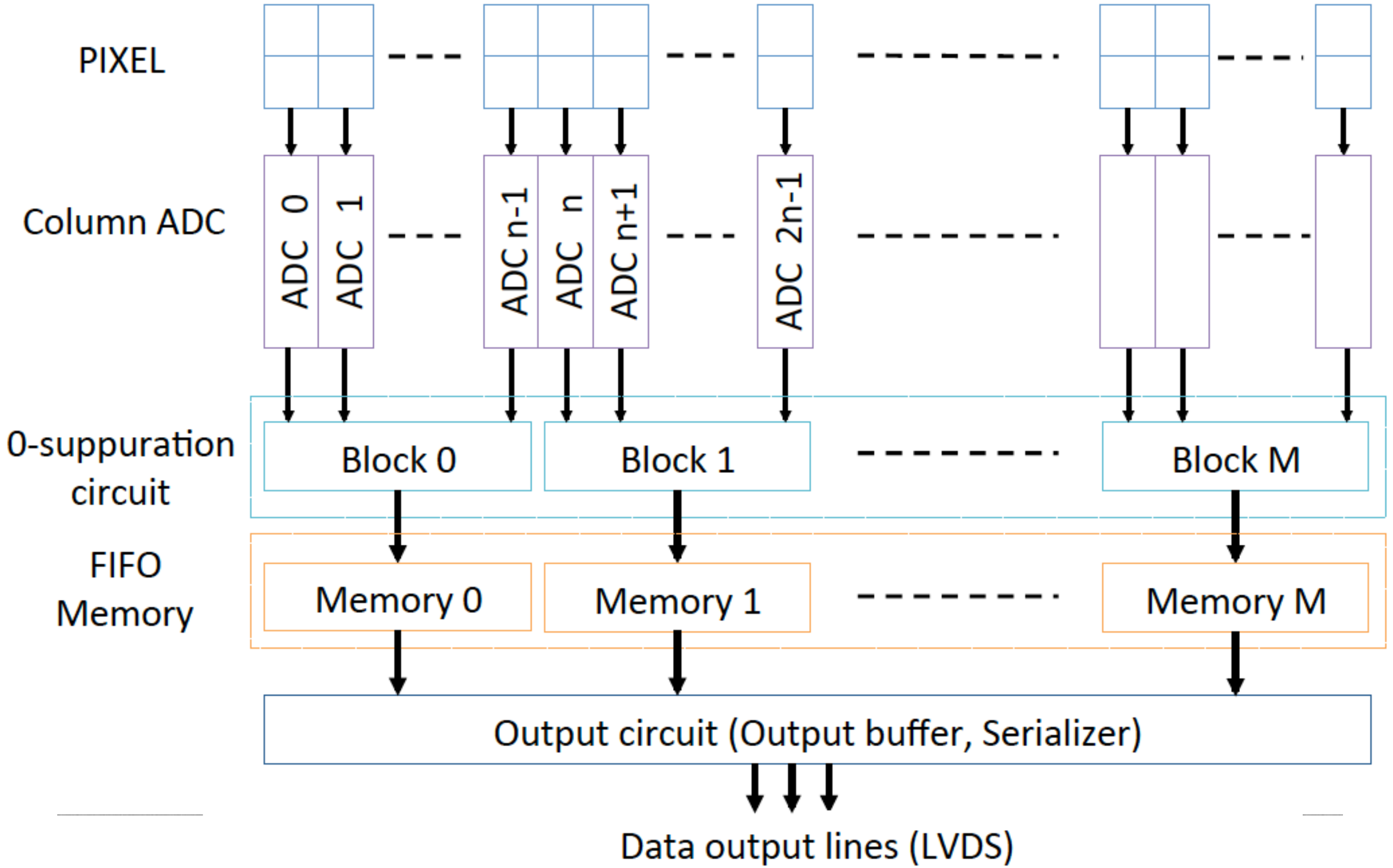
# Column ADC


Column ADC circuit
Ramp generator
PIXEL_OUT
Comparator
Latch
8bit counter
Digital data
Pixel signal
Ramp signal
Comparator IN
Comparator OUT
Clock counter

# 0-suppression Logic

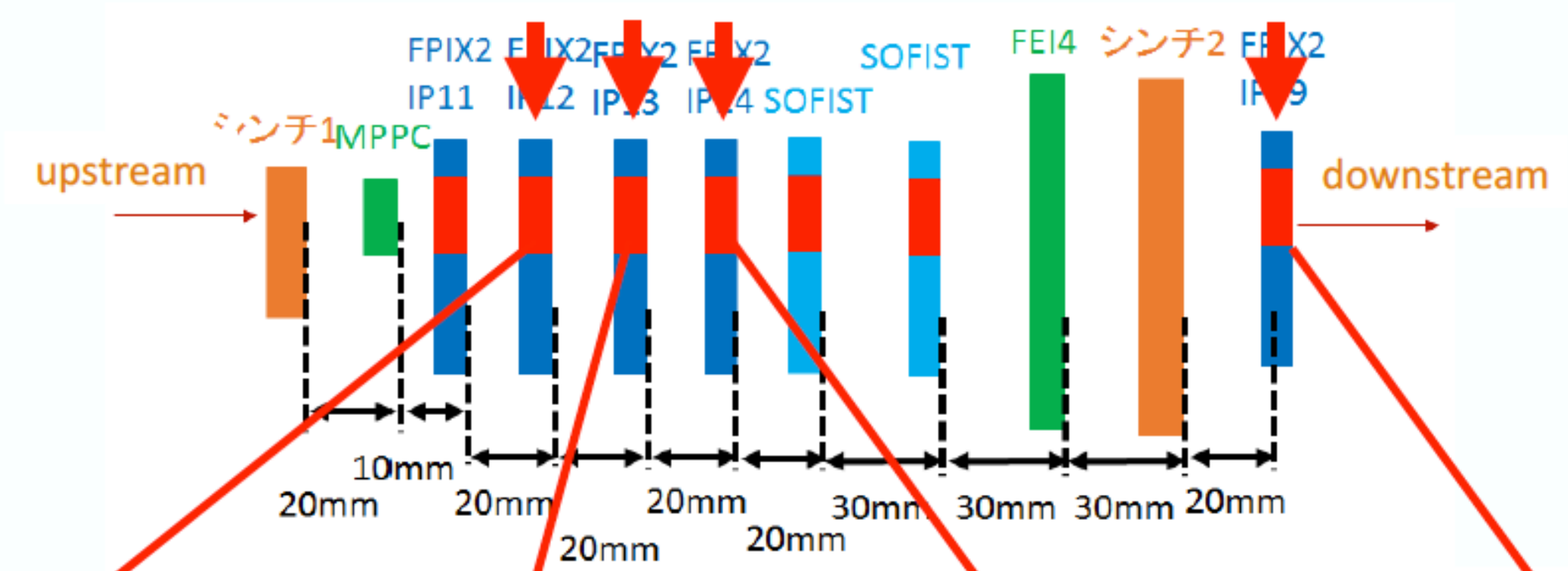


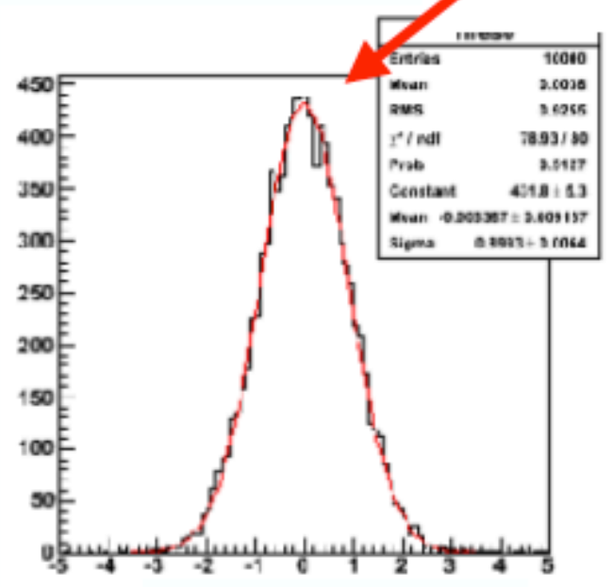
# Data Flow


PIXEL
Column ADC
ADC 0
ADC 1
ADC n-1
ADC n
ADC n+1
ADC 2n-1
0-suppuration circuit
Block 0
Block 1
Block M
FIFO Memory
Memory 0
Memory 1
Memory M
Output circuit (Output buffer, Serializer)
Data output lines (LVDS)

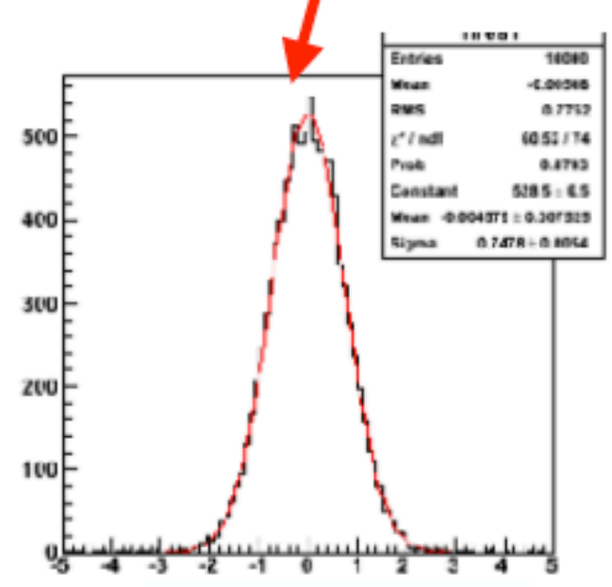
# Residual distribution by MC w/ intrinsic resolution=0.6 um

- Tracking by straight line : y = ay * z + by

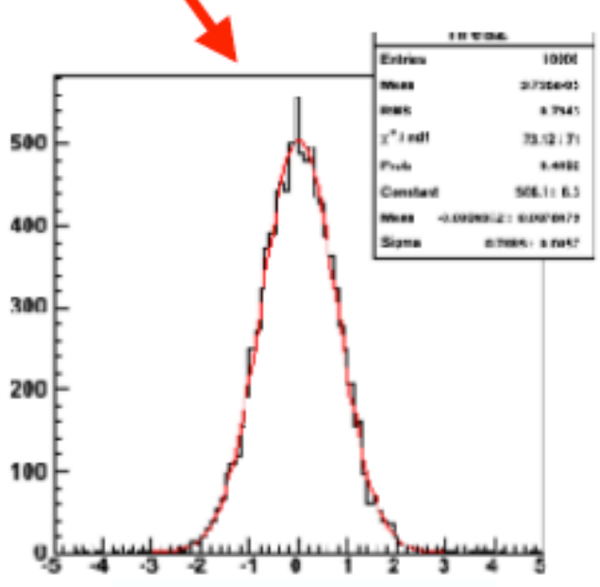


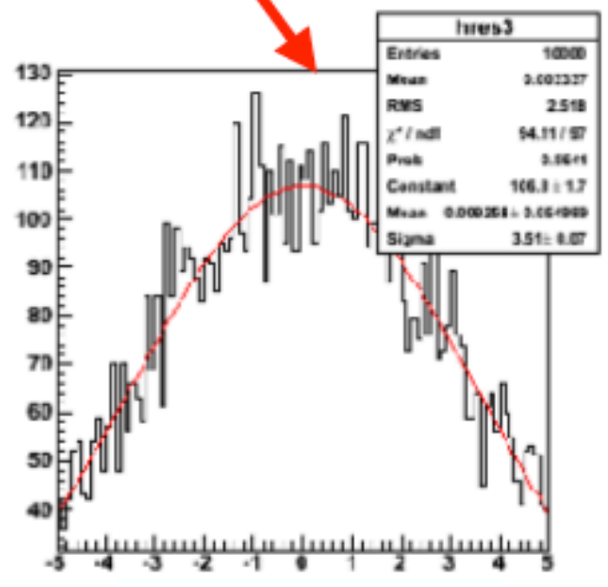
σ = 0.90 um



σ = 0.75 um



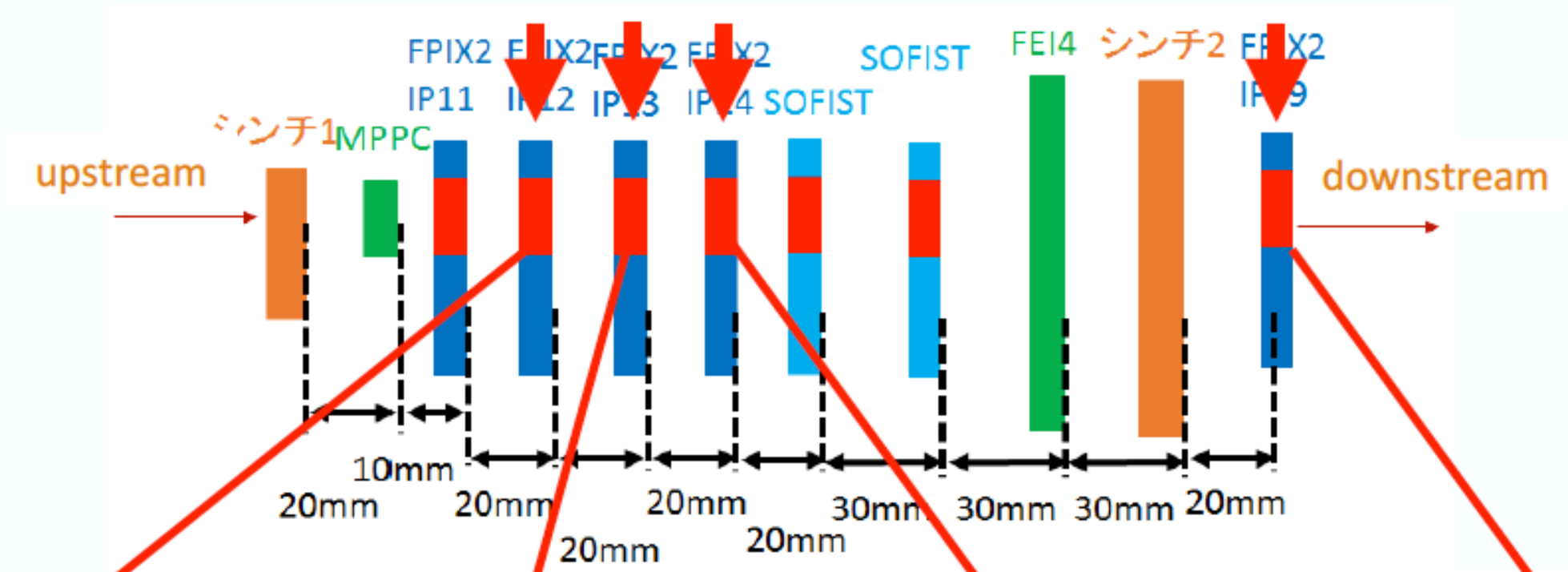
σ = 0.77 um

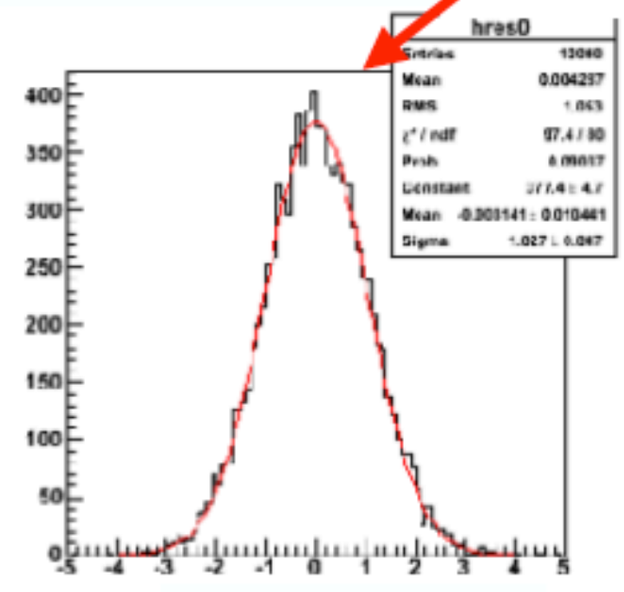


σ = 3.51 um

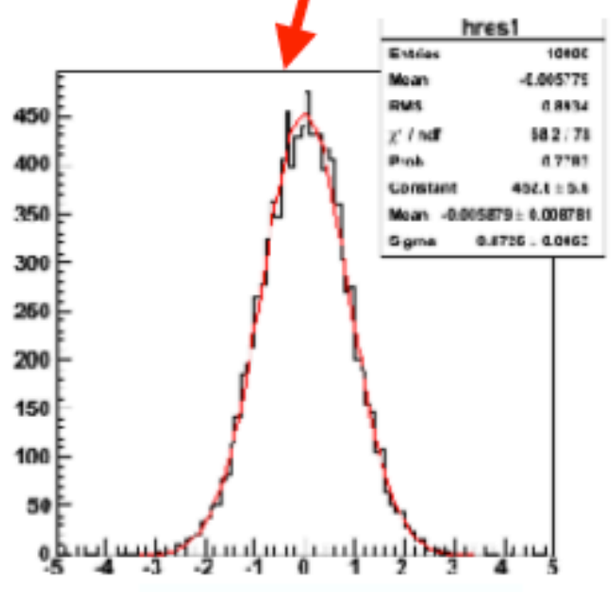
# Residual distribution by MC w/ intrinsic resolution=0.7 um

- Tracking by straight line : y = ay * z + by

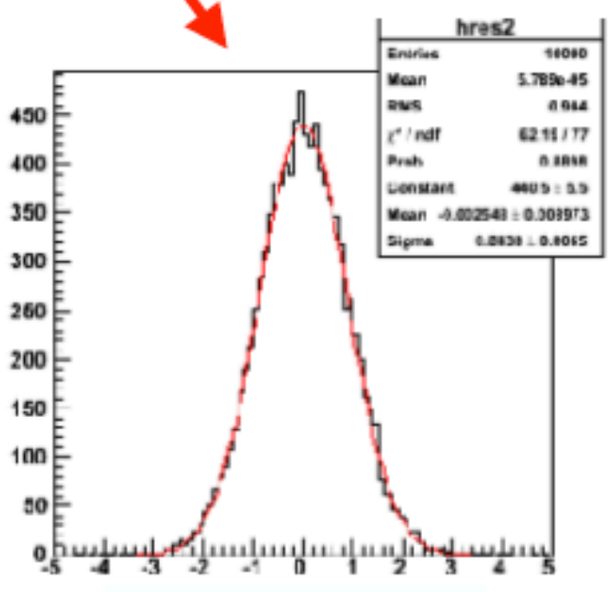


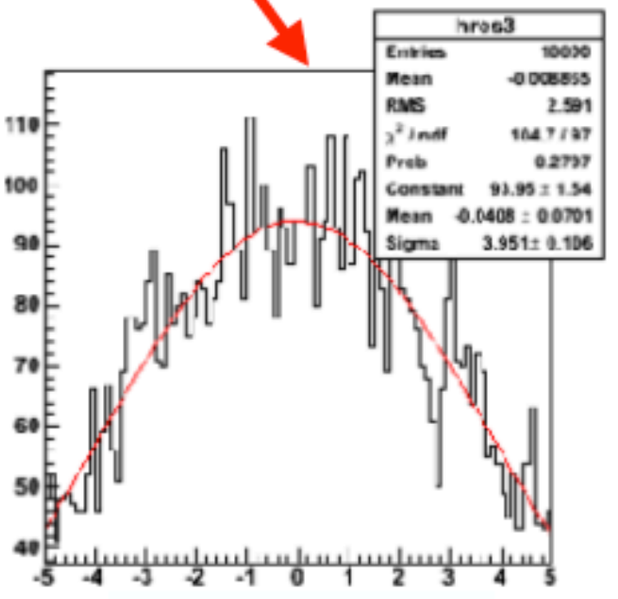

σ = 1.03 um




σ = 0.87 um



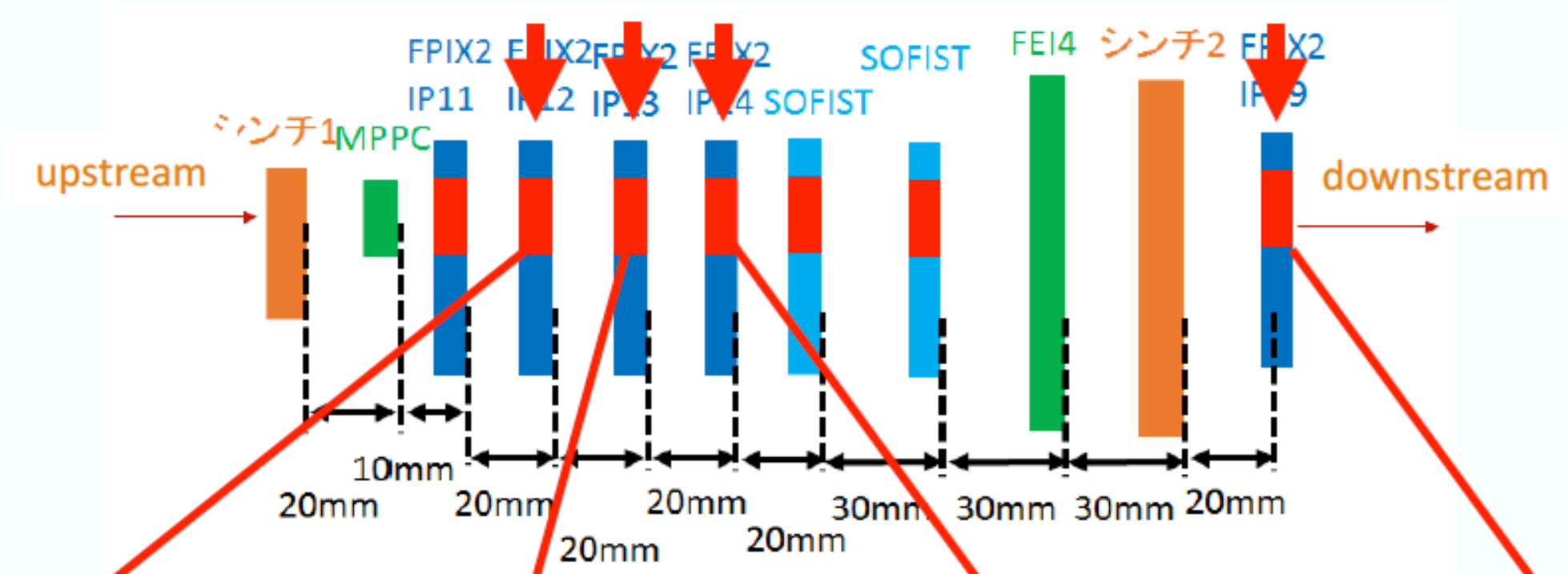

σ = 0.88 um

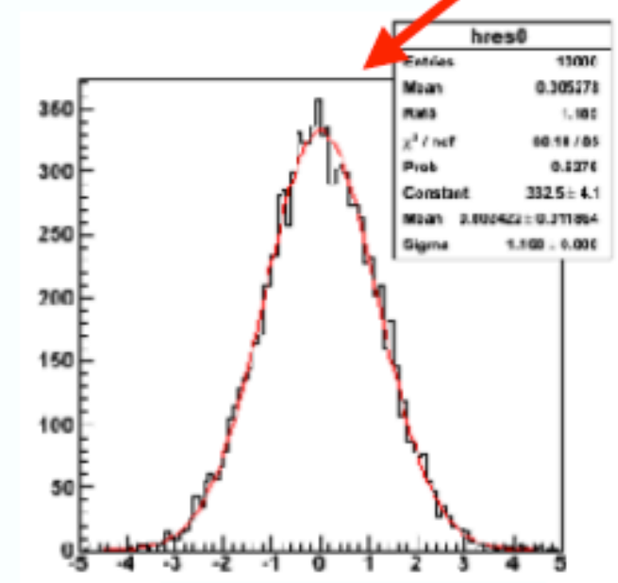



σ = 3.95 um

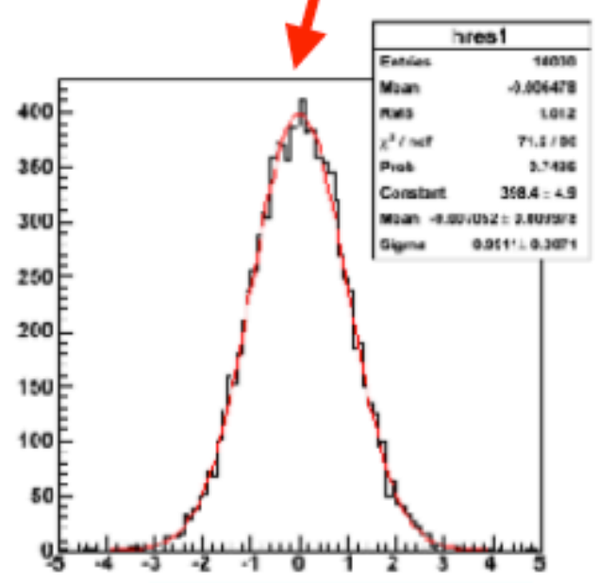
# Residual distribution by MC w/ intrinsic resolution=0.8 um

- Tracking by straight line : y = ay * z + by

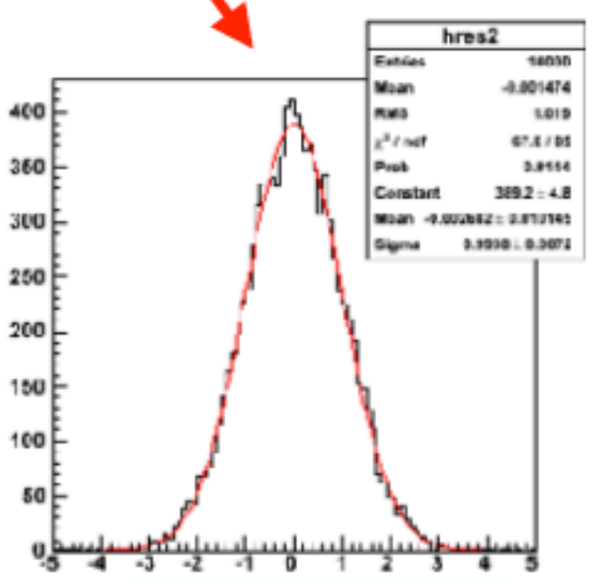


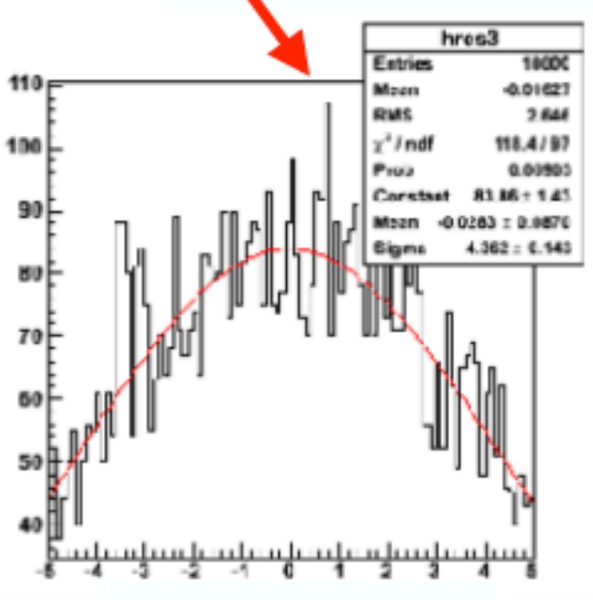

σ = 1.17 um




σ = 0.99 um




σ = 1.00 um




σ = 4.36 um