Overview of SOI Pixel Development

May 9, 2017

TYL-FJPPL Satellite Meeting@Strasbourg

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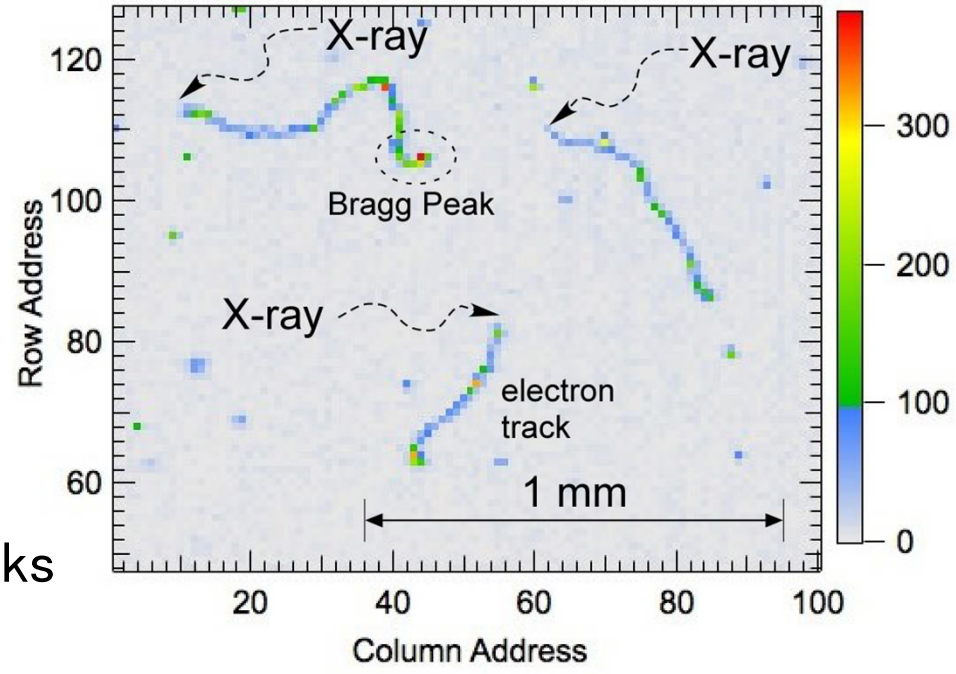
On behalf of SOIPIX collaboration

High Energy Accelerator Research Organization (KEK)
& The Okinawa Institute of Science and Technology (OIST)
yasuo.arai@kek.jp, http://rd.kek.jp/project/soi/

Outline

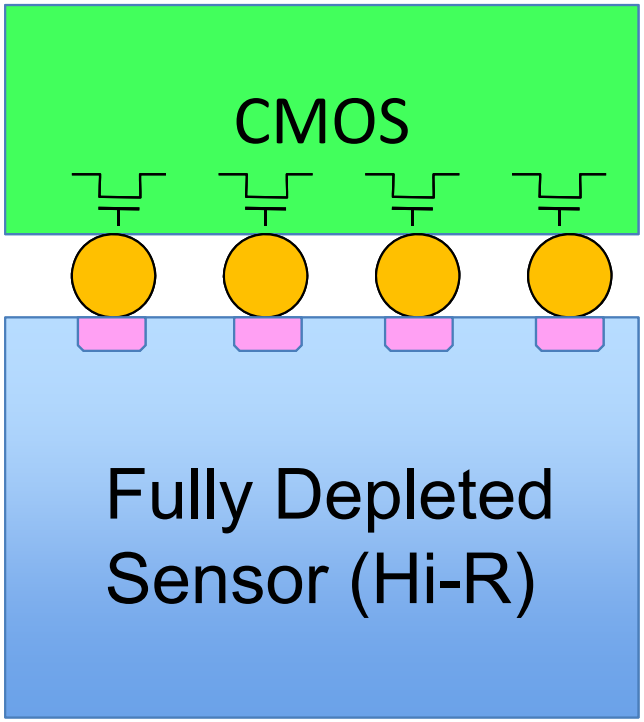
I. Introduction
II. SOI Pixel Process & Run
III. Design Examples
IV. Summary



Compton Electrons Tracks

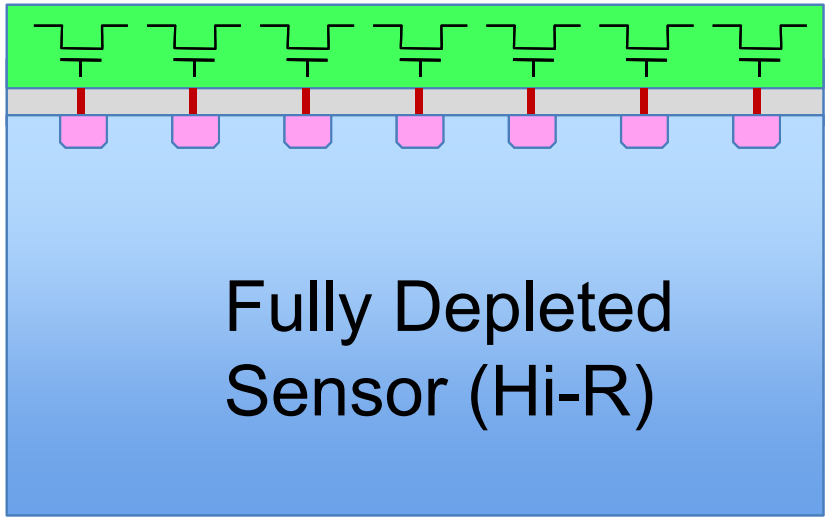
I. Introduction

Hybrid Detector



Monolithic

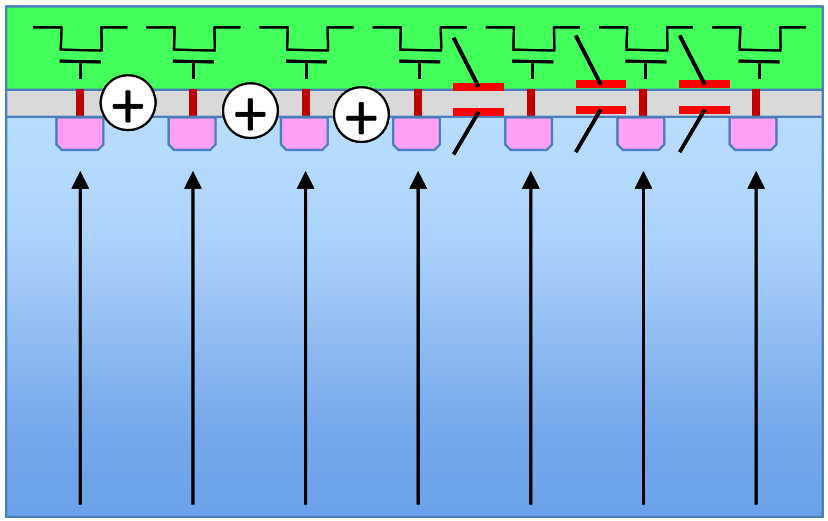
Silicon-On-Insulator (SOI)



To use SOI technology for pixel detector is already discussed in 1990(*).

(*) Jean-Pierre Colinge, 'An overview of CMOS-SOI technology and its potential use in particle detection systems', NIM A305 (1991) 615-619.

Issues in SOI Pixel



- Transistors does not work with Detector High Voltage. (Back-Gate Effect)
- Circuit signal and sense node couples. (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage. (Radiation Tolerance)

Unfortunately, in 1990s, due to immature process technology, no good high-resistivity SOI wafer etc. , many SOI sensor R&D projects were stopped.

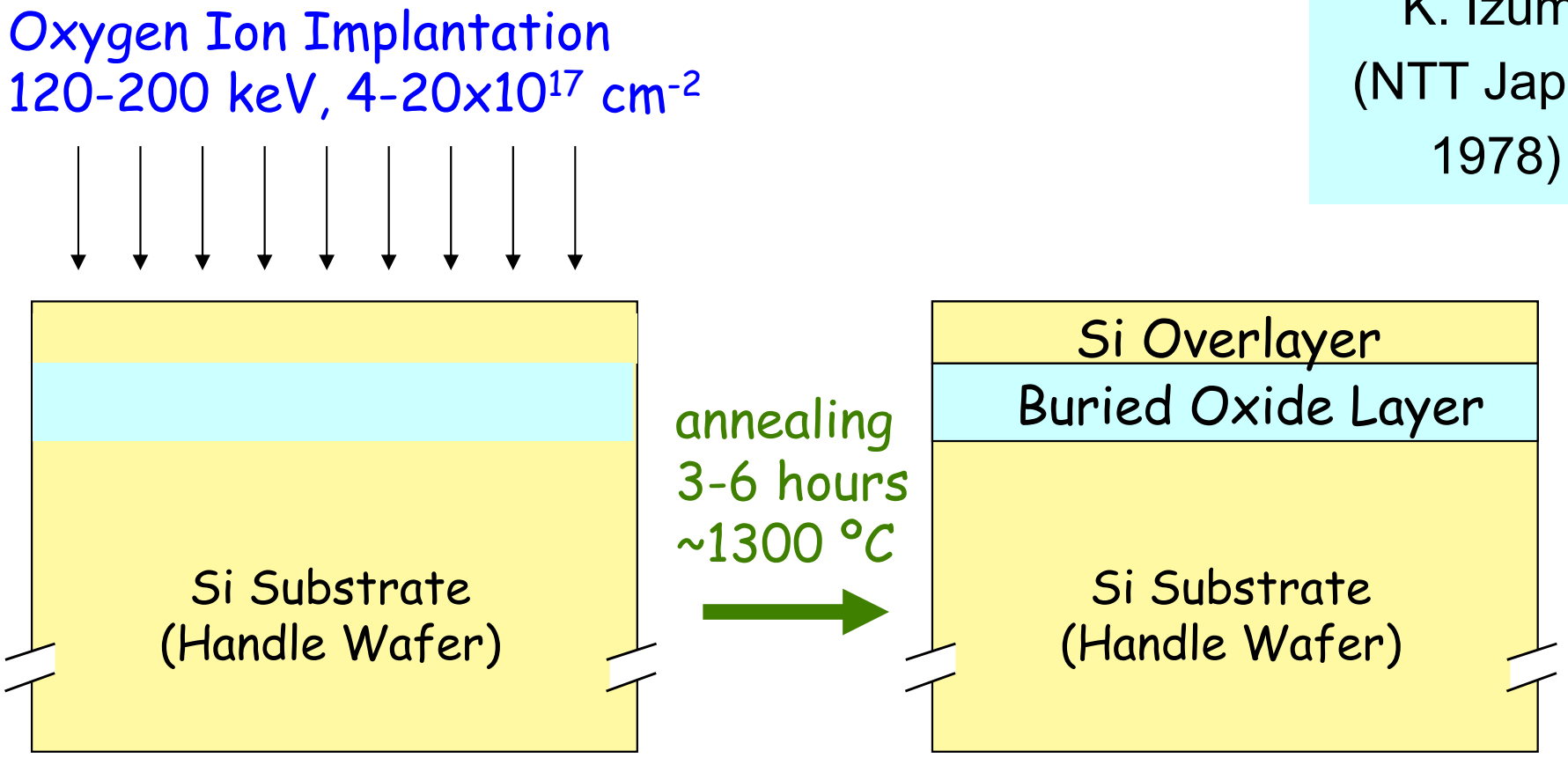
First SOI Wafer (SIMOX)

First good quality SOI wafer

SIMOX (Separation by Implanted Oxygen)

This took long implantation time of Oxygen, so the production cost was very high and applications are limited.

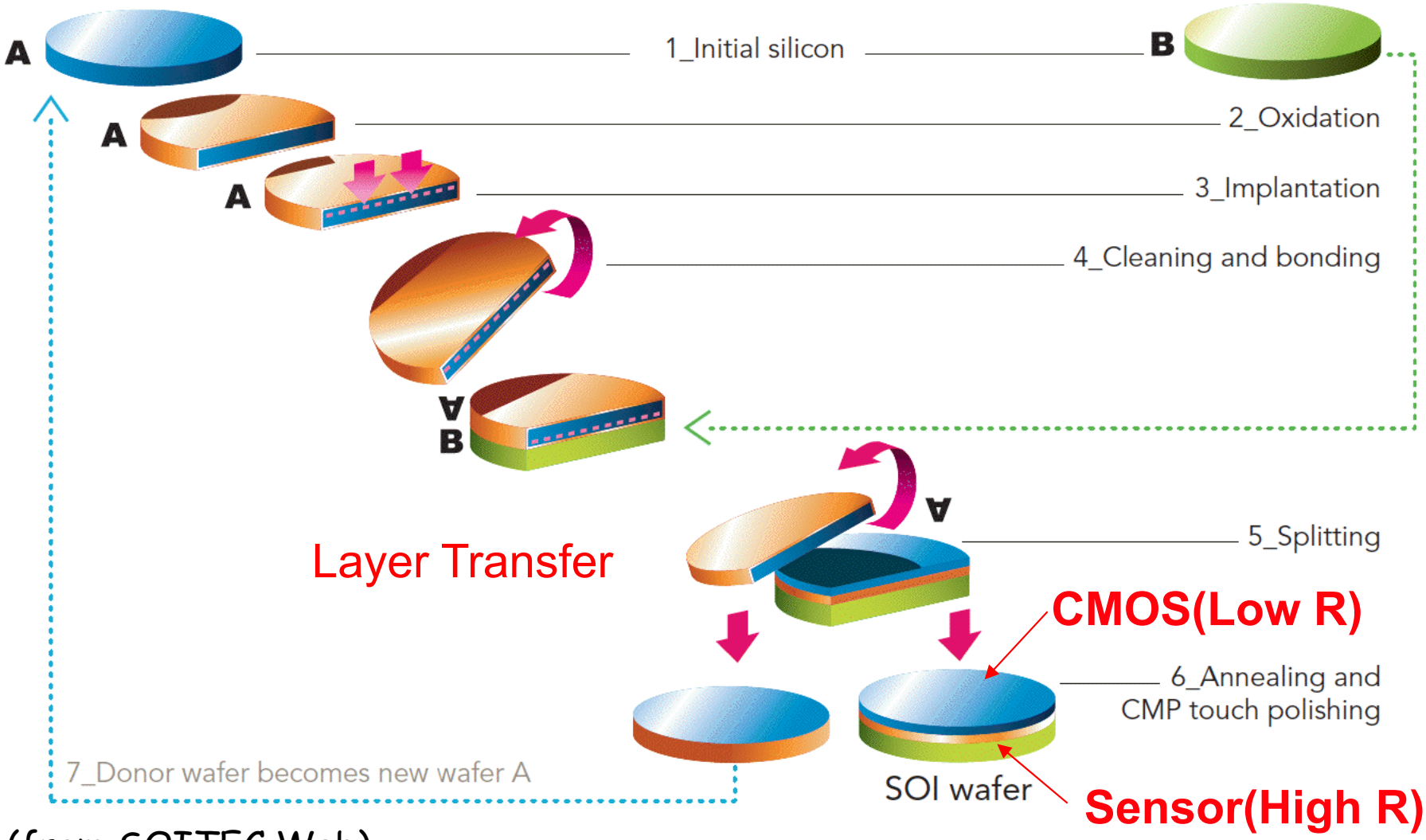
K. Izumi
(NTT Japan, 1978)



Pesent SOI Wafer (SmartCut™)

Michel. Bruel (Leti, 1991)

Become popular after 2000. soitec

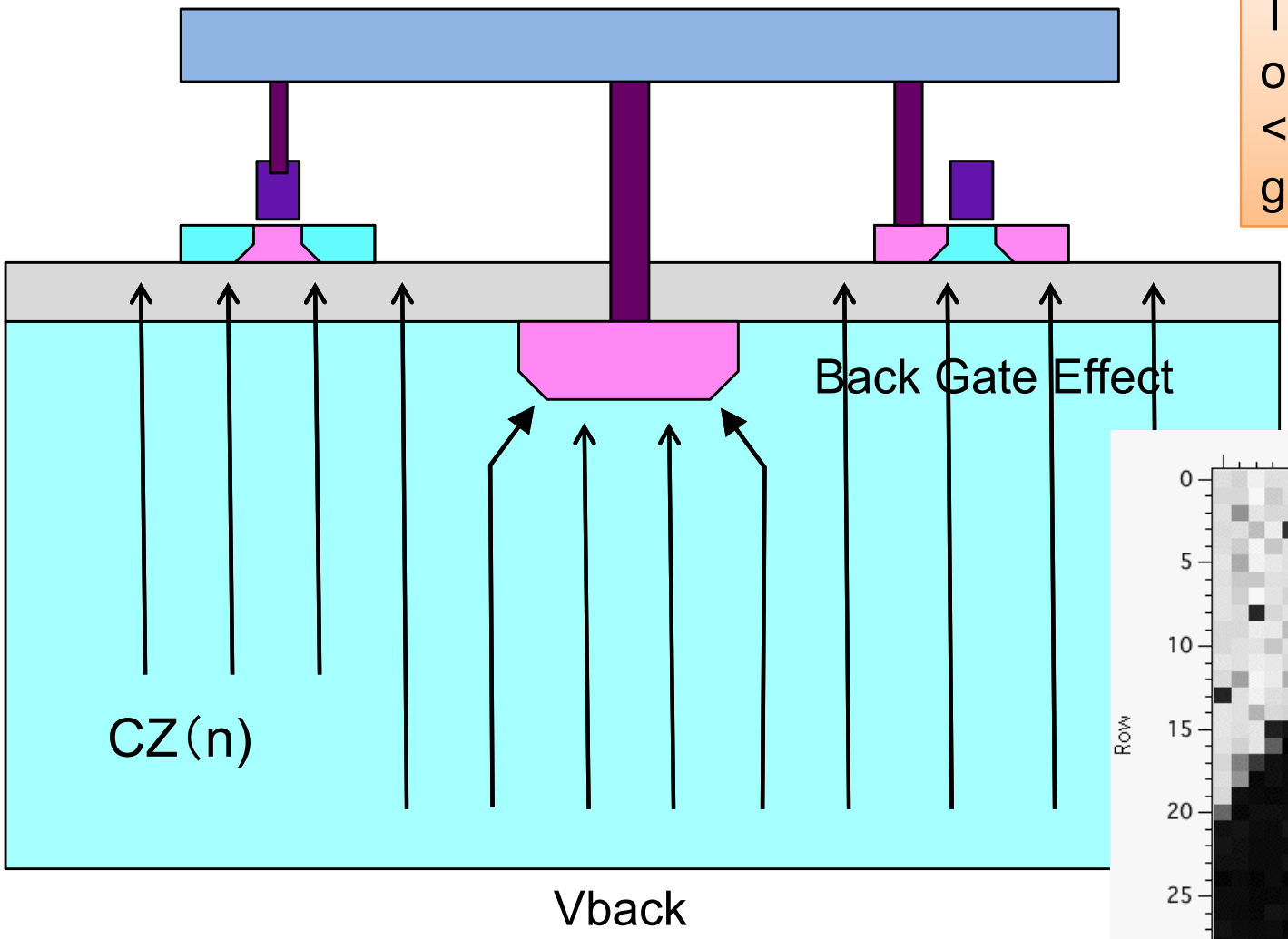


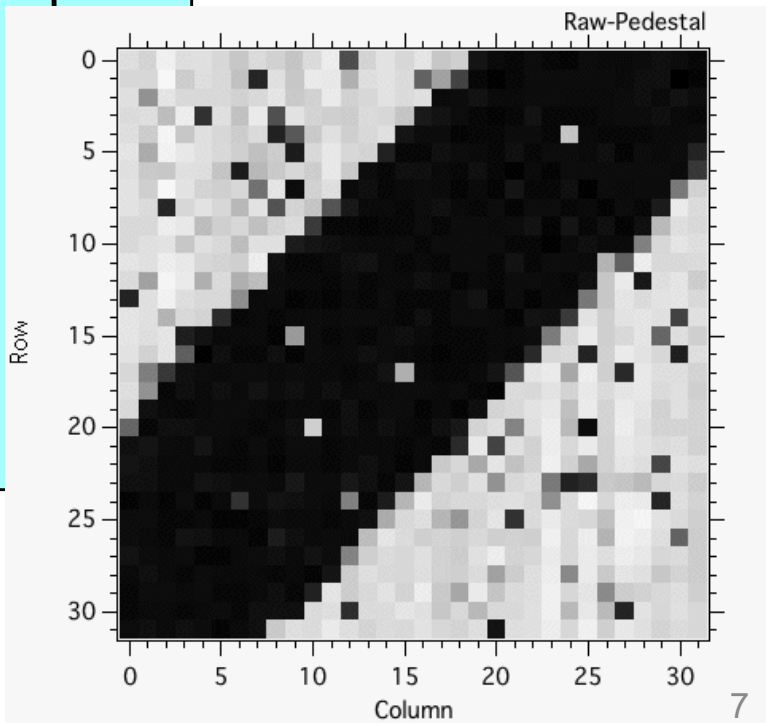
(from SOITEC Web)

First KEK SOI Pixel Detector

2006

This detector can be operated only at Vback <15V due to the back gate effect

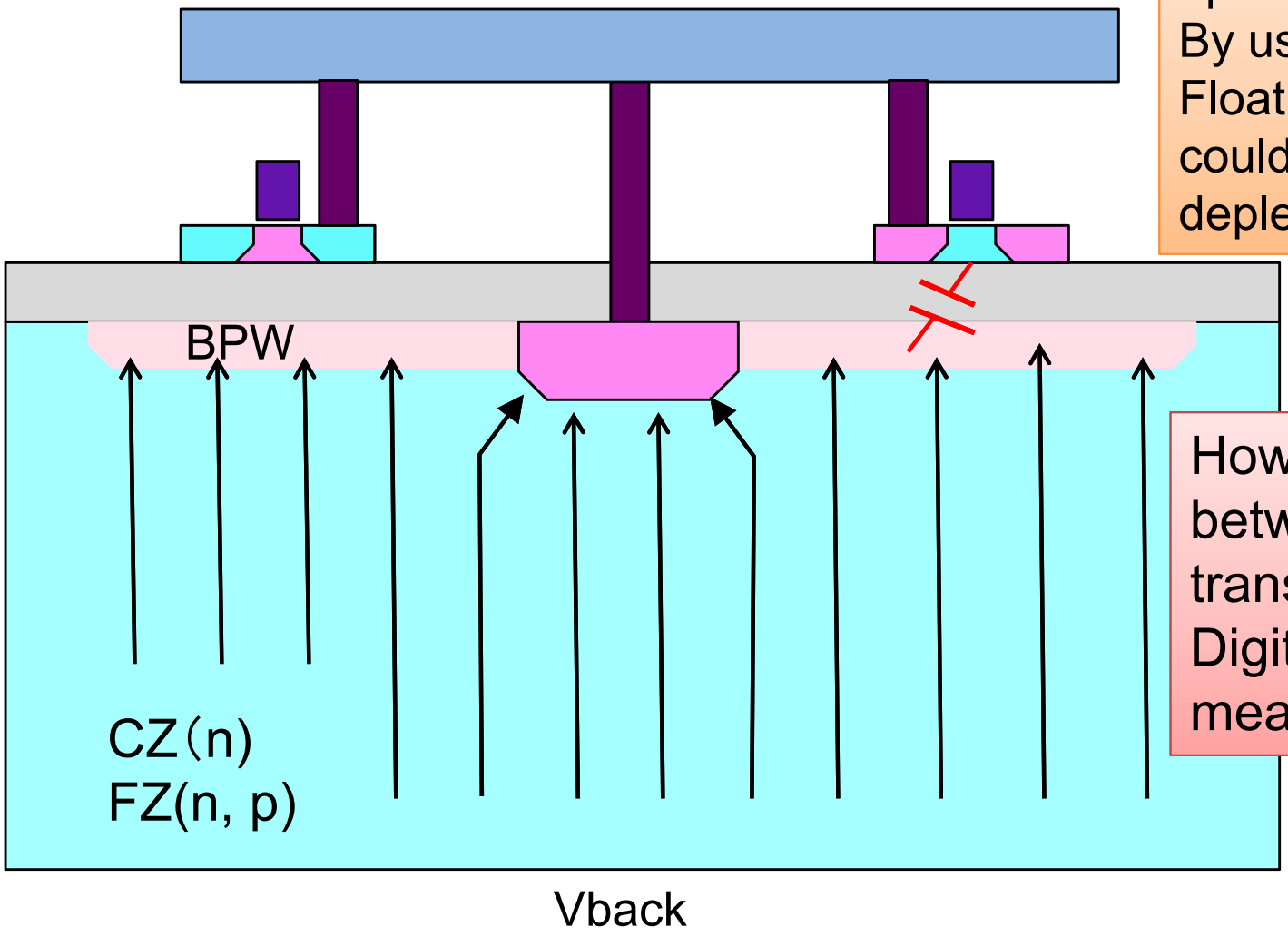




First Image (Wire)

Introduce BPW and FZ wafer

2009

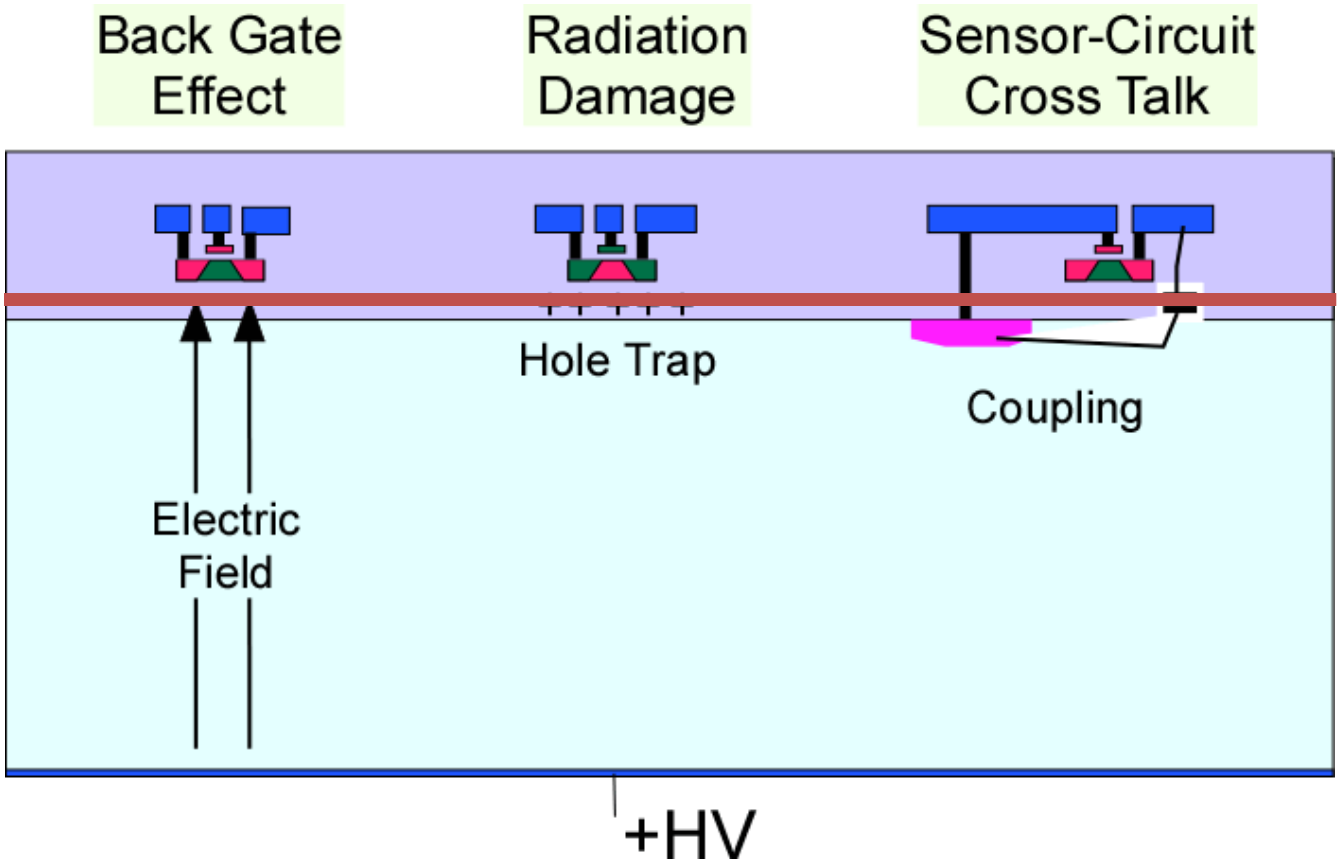


The detector can be operated above 400V . By using high-resistivity Floating Zone wafer, we could achieve thick full-depletion region.

However, capacitance between sensor and transistor is increased. Digital operation during measurement is difficult.

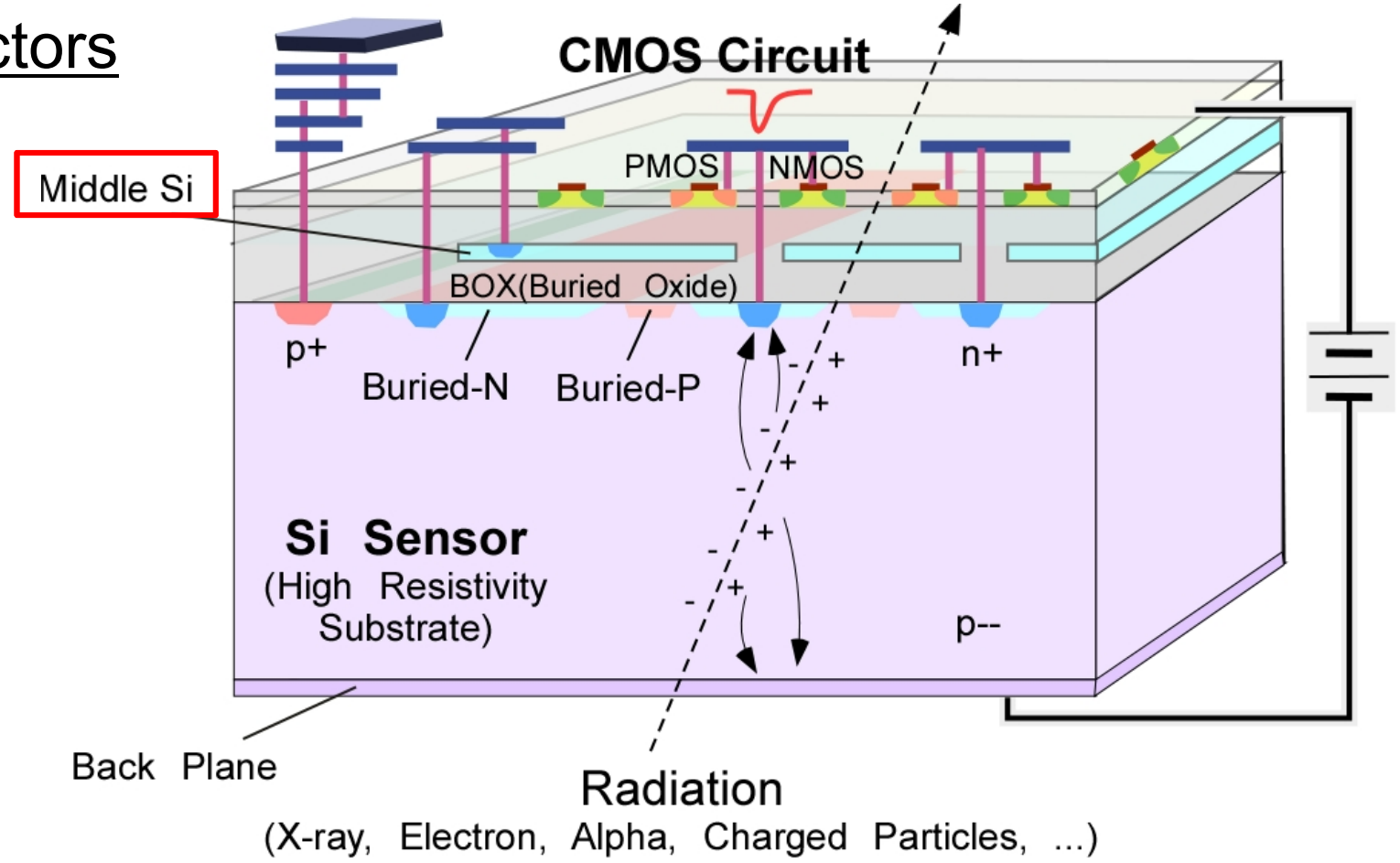
Double SOI Wafer

2014



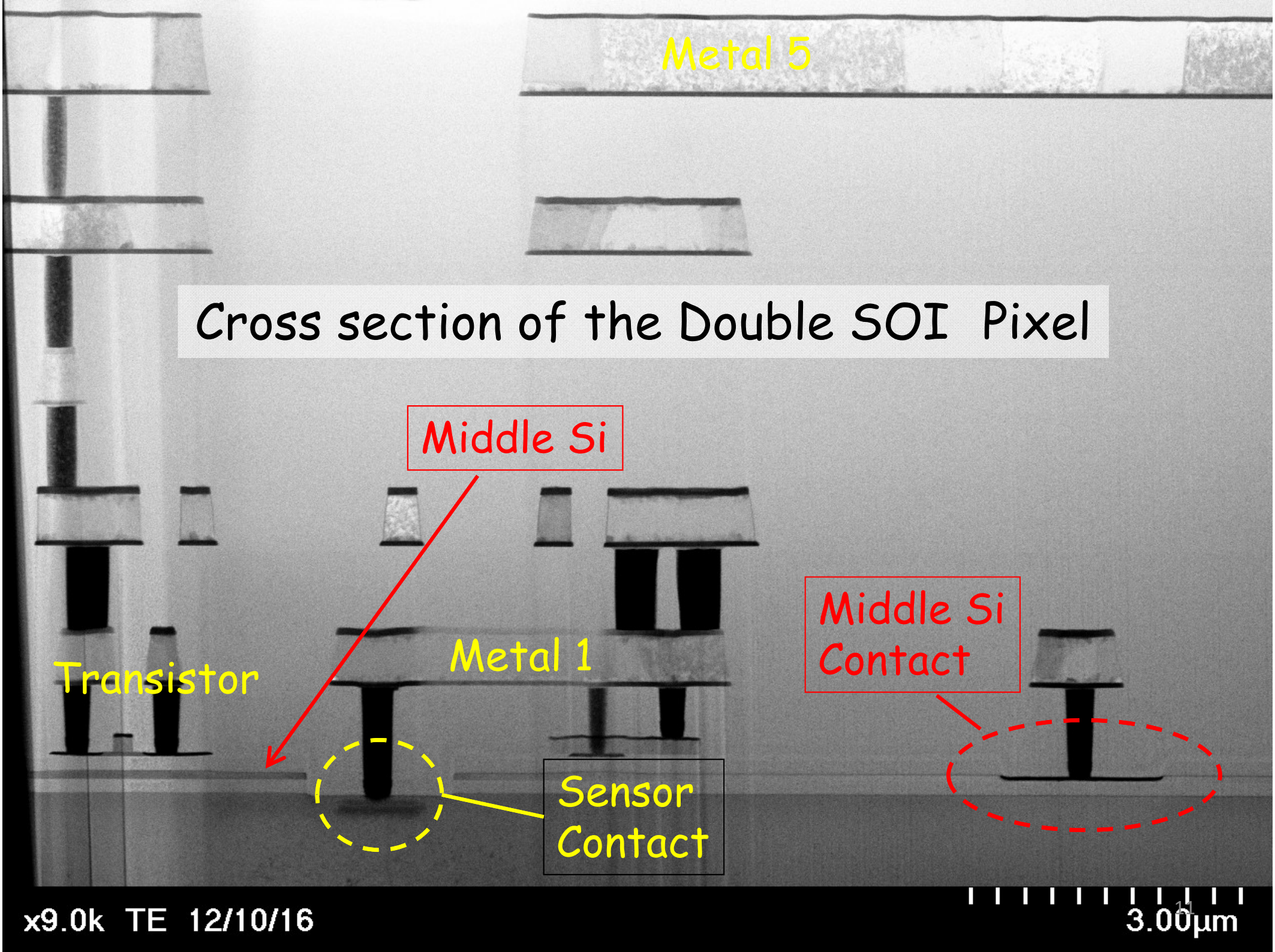
Additional conductive layer under the transistors solved all issues

SOIPIX Detectors (Double)



Double SOI Detector

- Middle Si layer shields coupling between sensor and circuit.
- It also compensate E-field generated by radiation trapped hole.
- Good for Complex function and Counting-type sensor.
- Can be used in High radiation environment.

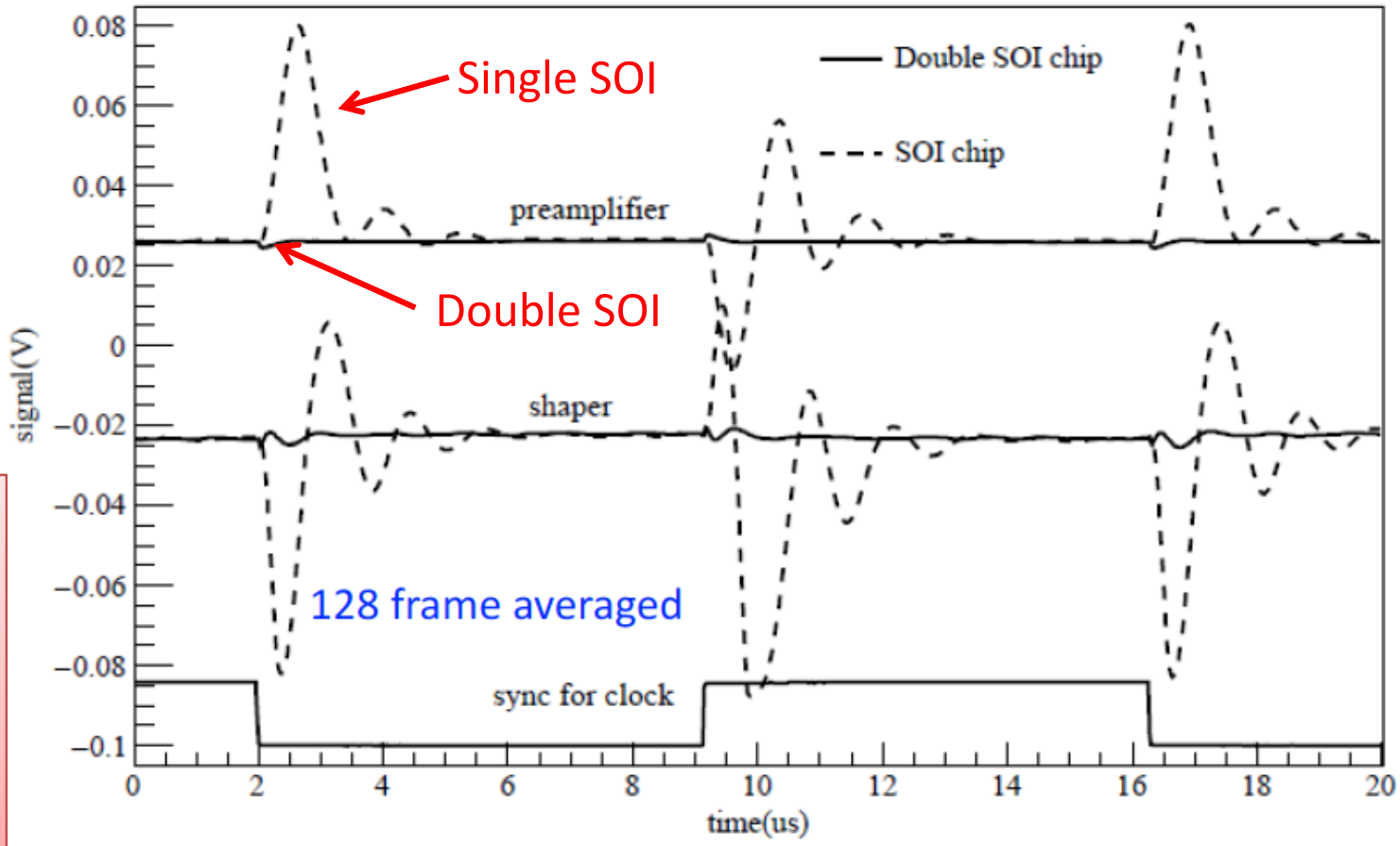

Metal 5
Cross section of the Double SOI Pixel
Middle Si
Transistor
Metal 1
Middle Si
Contact
Sensor
Contact
x9.0k TE 12/10/16
3.00µm

Specifications of Double SOI wafers

Layer	D-1	D-2	D-3 (next run)
Company	SOITEC	Shinetsu	Shinetsu
SOI1	p-type 88 nm, < 10 Ω •cm	p-type 88 nm, < 10 Ω •cm	p-type 88 nm, < 10 Ω •cm
BOX1	145 nm	145 nm	145 nm
SOI2	p-type 88 nm, < 10 Ω •cm	n-type 150 nm, < 10 Ω •cm	n-type 150 nm, 3-5 Ω •cm
BOX2	145 nm	145 nm	145 nm
Substrate	n-type Cz, 725um, ~700 Ω •cm	p-type Low Ox Cz, 725um, > 1.0 k Ω •cm	p-type FZ, 725um, > 5.0 k Ω •cm

Effect of Double SOI

Cross Talk from Clock line



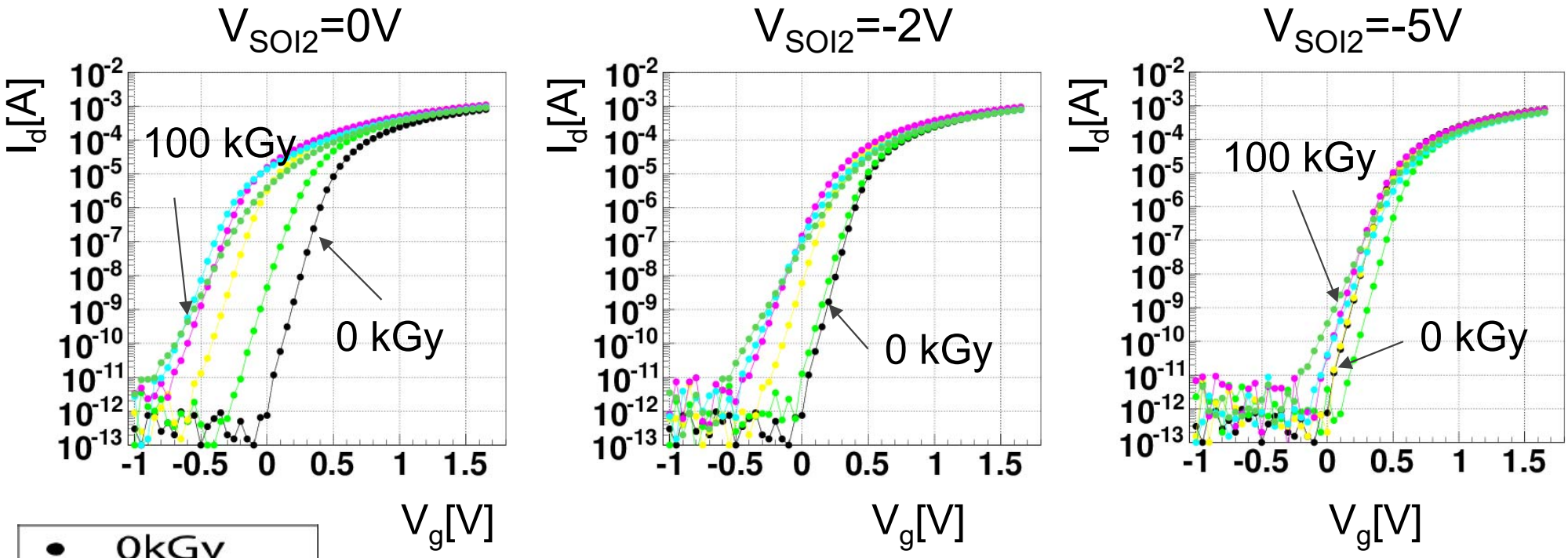
(by Lu Yunpeng (IHEP))

Shield:
Cross Talk between Circuit and Sensor is reduced to 1/20.

Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS



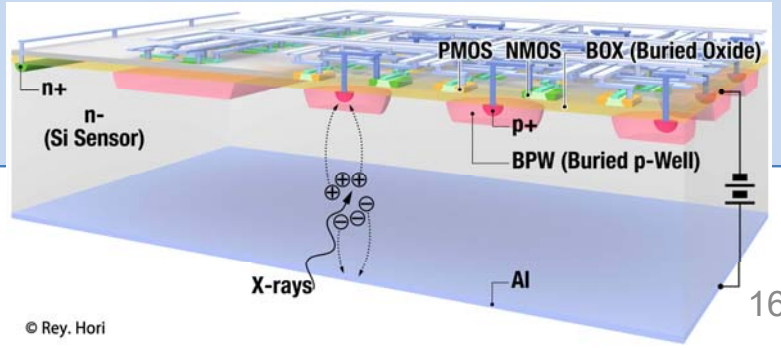
By setting Middle Si potential (Vsoi2) to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

(by U. of Tsukuba)

II. SOI Pixel Process & Run

Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only.
  → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.

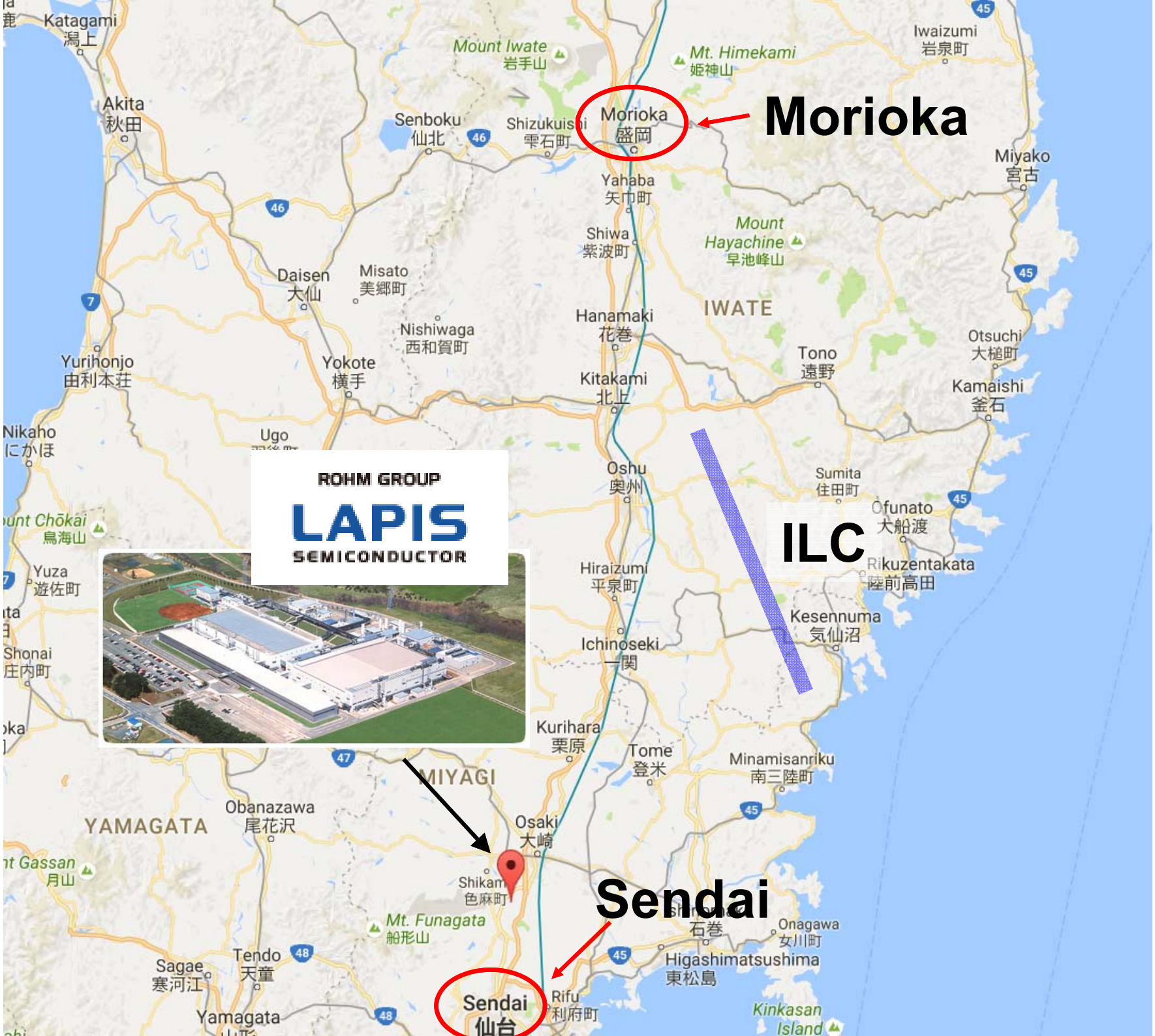


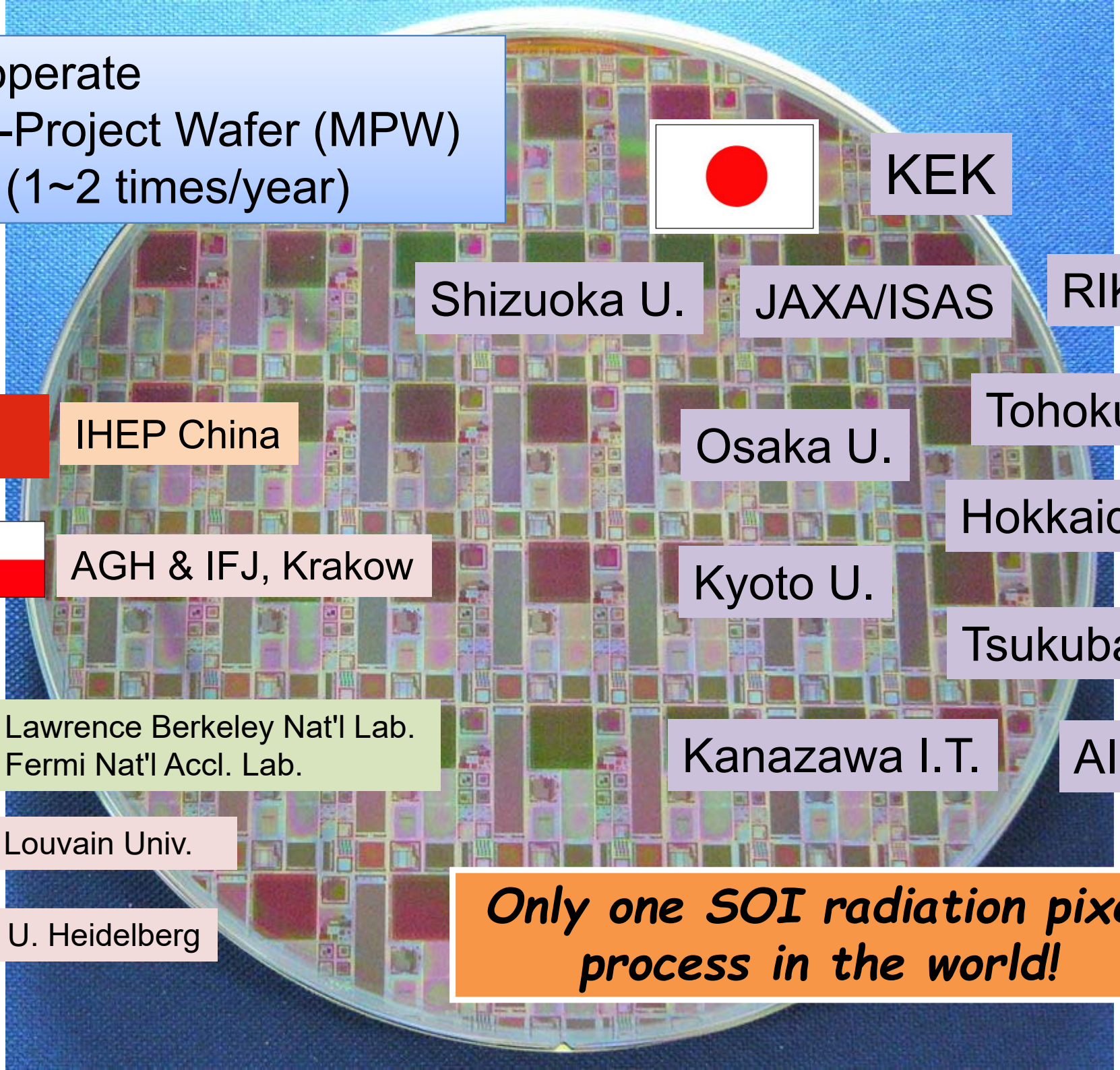
Lapis Semi.(*) 0.2 μm FD-SOI Pixel Process

→ Kurachi's Talk

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer (single)	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

(*) Former OKI Semiconductor Co. Ltd.


Morioka
ILC
Sendai
ROHM GROUP
LAPIS
SEMICONDUCTOR
Katagami
潟上
Akita
秋田
Mount Iwate
岩手山
Mt. Himekami
姫神山
Iwaizumi
岩泉町
Senboku
仙北
Shizukuishi
雫石町
Morioka
盛岡
Miyako
宮古
Yahaba
矢巾町
Shiwa
紫波町
Mount Hayachine
早池峰山
Daisen
大仙
Misato
美郷町
IWATE
Hanamaki
花巻
Nishiwaga
西和賀町
Yurihonjo
由利本荘
Yokote
横手
Tono
遠野
Otsuchi
大槌町
Kamaishi
釜石
Kitakami
北上
Nikaho
にかほ
Ugo
Oshu
奥州
Sumita
住田町
Ofunato
大船渡
Rikuzentakata
陸前高田
Hiraizumi
平泉町
Kesennuma
気仙沼
Ichinoseki
一関
Yuza
遊佐町
Shonai
庄内町
Kurihara
栗原
Tome
登米
Minamisanriku
南三陸町
MIYAGI
YAMAGATA
Obanazawa
尾花沢
Osaki
大崎
Shikama
色麻町
Mt. Funagata
船形山
Ishinomaki
石巻
Onagawa
女川町
Higashimatsushima
東松島
Tendo
天童
Sagae
寒河江
Yamagata
Sendai
仙台
Rifu
利府町
Kinkasan Island



We operate
Multi-Project Wafer (MPW)
run. (1~2 times/year)

KEK

Shizuoka U.

JAXA/ISAS

RIKEN

IHEP China

Tohoku U.

Osaka U.

Hokkaido U.

AGH & IFJ, Krakow

Kyoto U.

Tsukuba U.

Lawrence Berkeley Nat'l Lab.
Fermi Nat'l Accl. Lab.

Kanazawa I.T.

AIST

Louvain Univ.

U. Heidelberg

Only one SOI radiation pixel process in the world!

MPW Run Web Page

PDK

- Mar. 22, 2017: New SOI SemiTOOLS of which license is extended to Mar. 31, 2018 are released. NEW!
  *LAPIS_Semi_TOOLS61_ ... .gz (for IC6.1)
  *LAPIS_Semi_TOOLS_Se ... IC5.1)).
  (You can check the expirati ...
- Mar. 22, 2017: Bit assignment of 20 bit fuse is corrected. (manual, gds). If you want to trace wafer number and your chip location within wafer please put this fuse pattern on your chip in vertical direction. NEW!
- Apr. 25, 2016 : PDK Rel. 0510_ic61 (Contents, Rel Note, PDK Rel 0510, Documents) NEW!
  (SPICE parameter of nch/pch core normal-vt st2 is updated, OF(GDS#64) is added to technology file, document for new fuse layout (20 bits) is added)
- Sep. 12, 2014 : Contact Tree (p.8) is updated (020SOI_022Wiring_forK ...
- Sep. 10, 2014 : 1/f model parameters are updated. Please replace relevant files in 02_soi020_kek_LAPIS_Semi_ic61/SIM_PARAM/hspice/Cor directory with this.

PDK is provided by Lapis

Other Documents

- July 17, 2015 : Implantation Layer summary.
- Sep. 12, 2014 : Design Note on the N and P-substrate common design.
- Dec. 17, 2013 : Design Note of the double-SOI (v.1).
- June 5. 2013 : SPICE Simulation Parameters (QSD-11523, Rev. 11)
- June 3, 2013 : Hot Carrier Reliability Standard (QSD-11041, Rev. 4)(English)
- Aug. 5, 2011 : Summary of Implantation Condition (V1.0 confidential!)
- June 1, 2010 : Electro Migration Standard (QSD-10606, v. 3)(Japanese, English)(recommendation)
- Jan. 29, 2010 : Guideline for Dummy Metal Prohibit Area (Japanese, English)
- July 7, 2009 : Summary Report on Sensor Diode and BPW layer (09HAC-1259_ES2Y0-001JA with English Translation)
- Jan. 26, 2009 : Calibre CCI RC extraction User's Guide (pdf(Japanese, English), Quantus command template, Star command template))

(*1) --- Not relevant to ordinary users

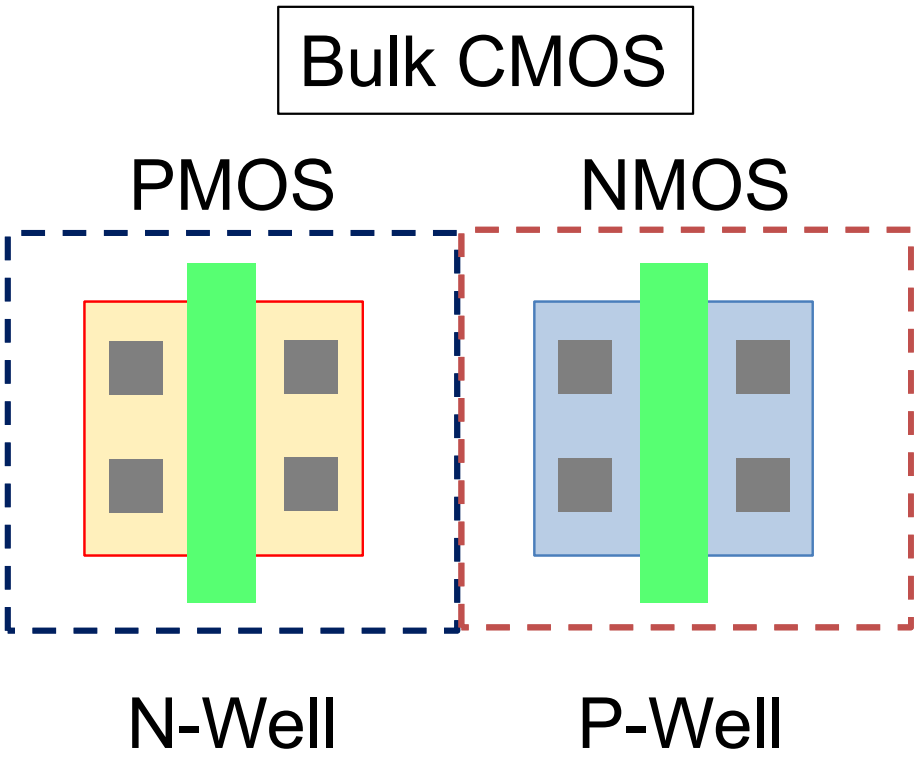
CAD Tools:
- Cadence Virtuoso
- Mentor Calibre (DRC, LVS, PEX)
- Synopsys HSPICE

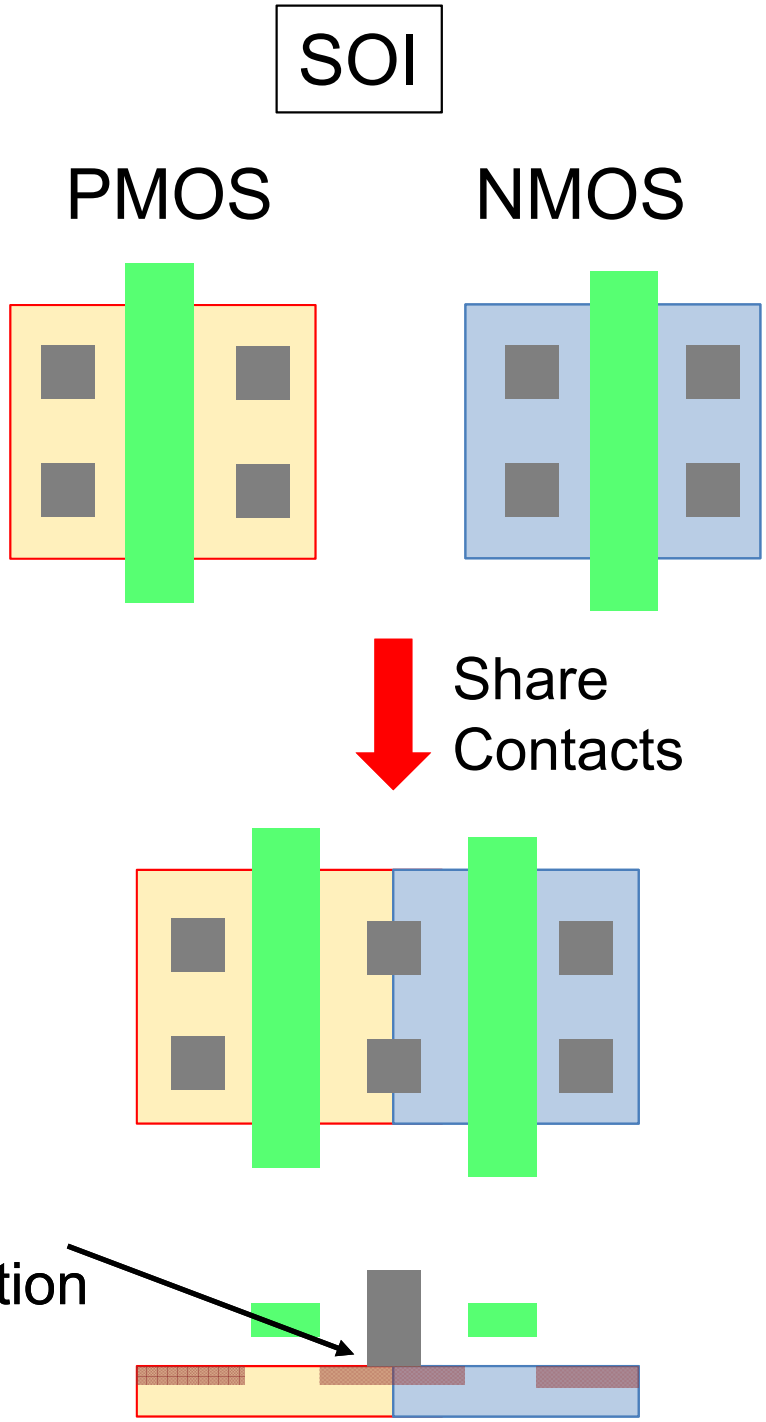
Libraries
- Simple I/O Library
- Free User Libraries
- No Digital Library

SPICE

- Feb. 10, 2017 : Modech SPICE models for the increased LDD. NEW!
- June 14, 2016 : SPICE model of core diode written by A-R-Tec.
- June 25, 2012 : SPICE rev.8 readme.txt (English), readme_core_st_lv_e.txt (English)
- June 30, 2009 : How to specify Body-Tie, Source-Tie, and Body-Floating Tr parameters in SPICE (pdf)
- June 23, 2009 : Diode model of dio_ppn_io is only supported (Layout & I-V curve)

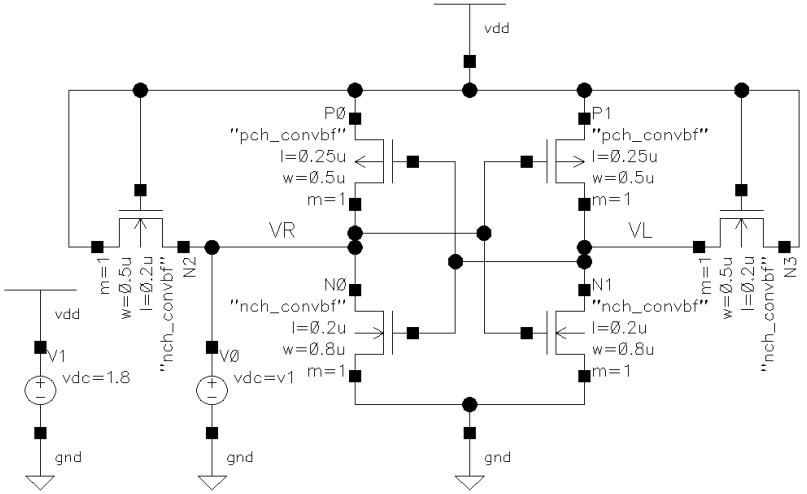
Layout Shrink（Active Merge)

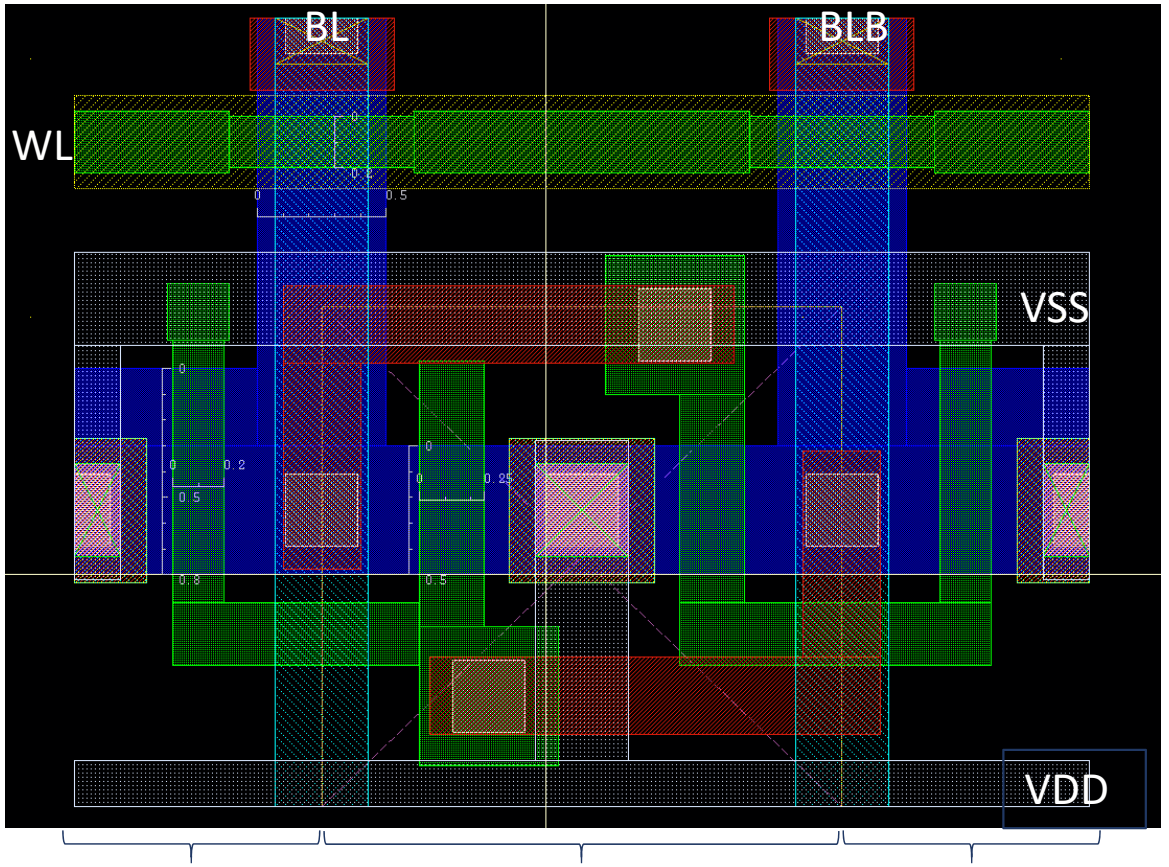




In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

Single Port SRAM Bit Cell



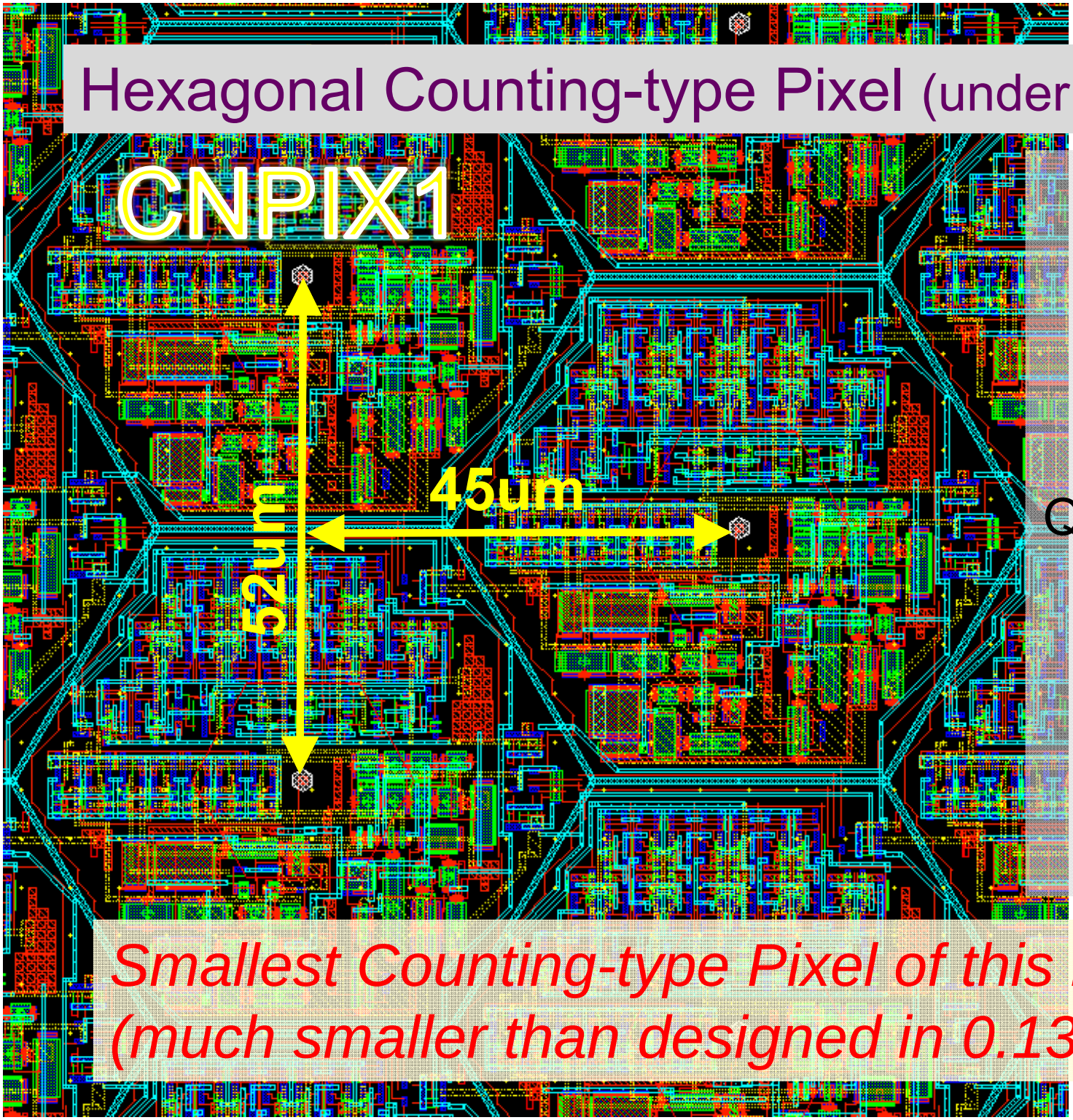


Only 1 Active region

Nch Pch Nch

Cell Size : 3.94µm X 3.06µm = 12.06µm²

Hexagonal Counting-type Pixel (under development)



Charge Amp
+
Shaper
+
Discriminator
+
Q Share Handling
+
19bit Counter
+
7bit register

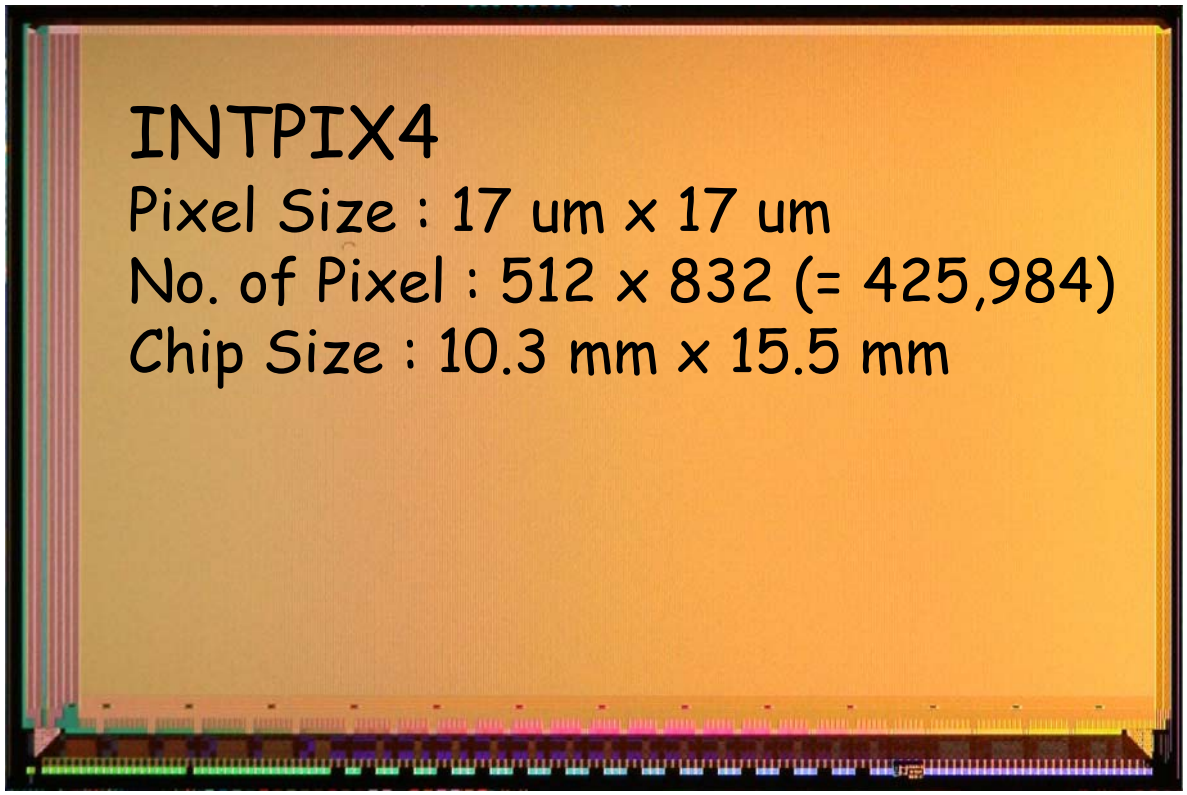
(in 2,340 um^2)

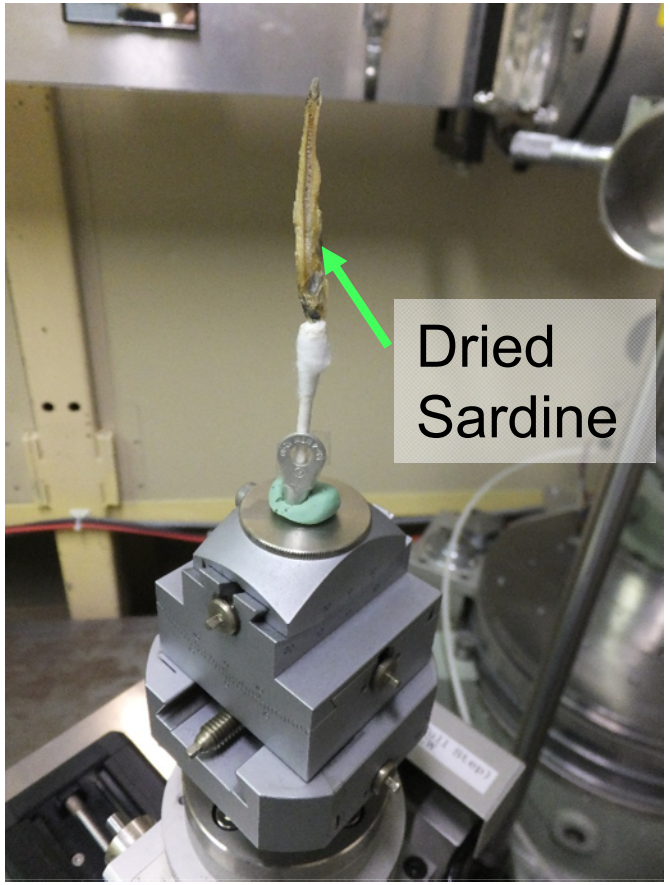
Smallest Counting-type Pixel of this kind.
(much smaller than designed in 0.13um process)

III. Design Examples

Integration type detector & 3D CT

→ Miyoshi's Talk





- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V、Integration Time : 1ms、ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0~180° at every 1 degree.

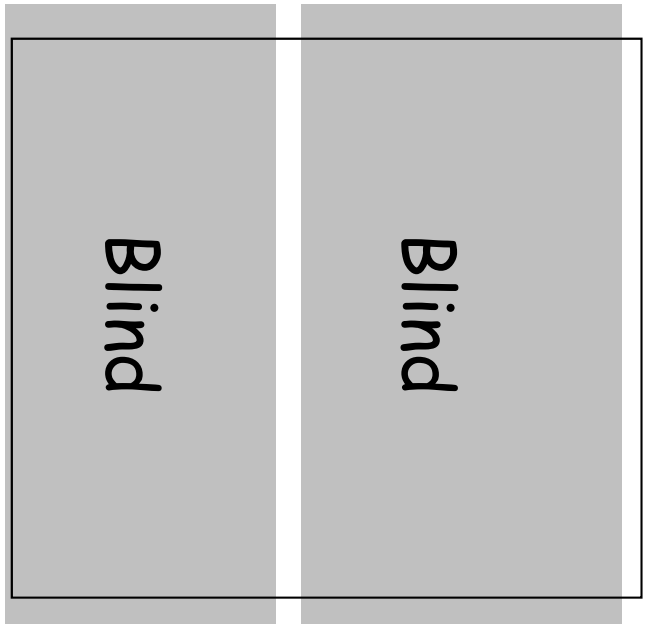
(by R. Nishimura, K. Hirano (KEK)

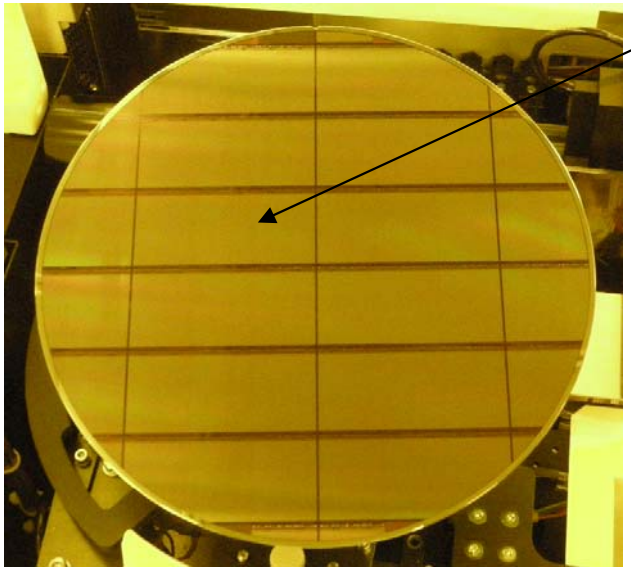
INTPIX4: Computed Tomography with Syncrotron X-ray

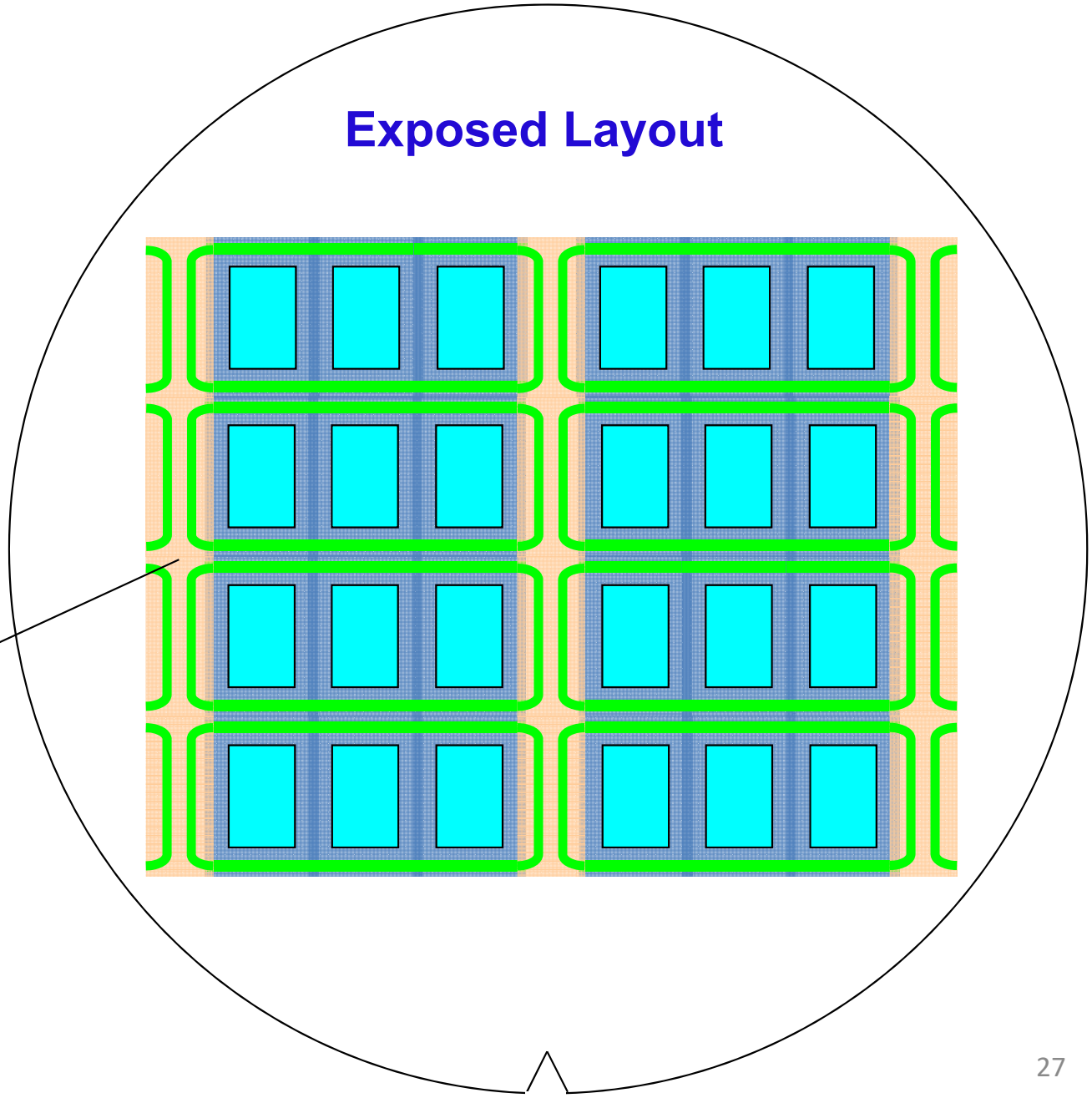
(by R. Nishimura, K. Hirano (KEK)

Stitching Exposure for Large Sensor

Mask Layout



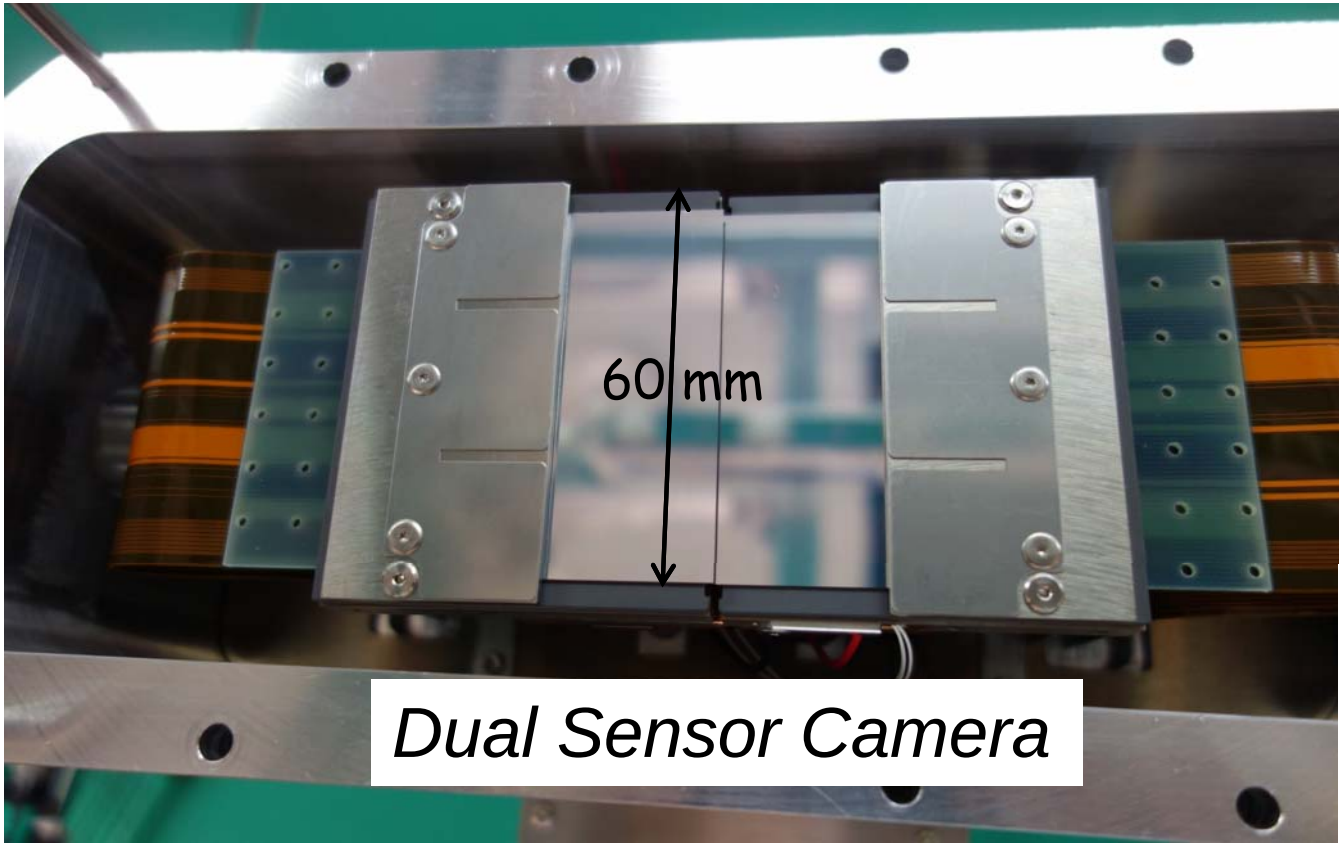




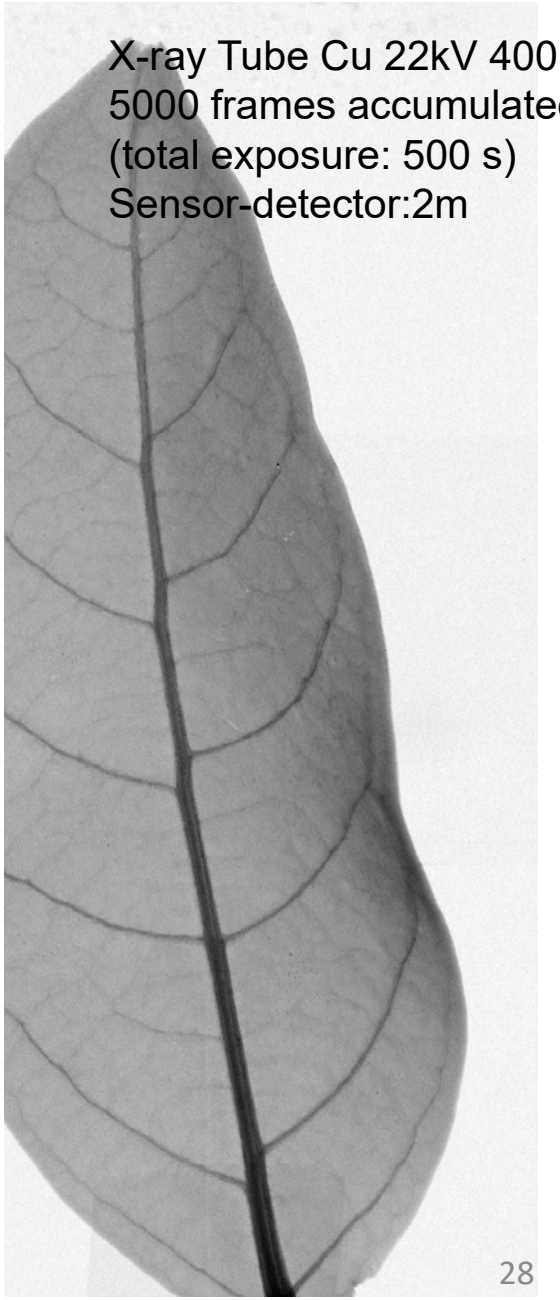
SOI Photon-Imaging Array Sensor (*SOPHIAS*) *for* X-ray Free Electron Laser (XFEL) SACLA

Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.



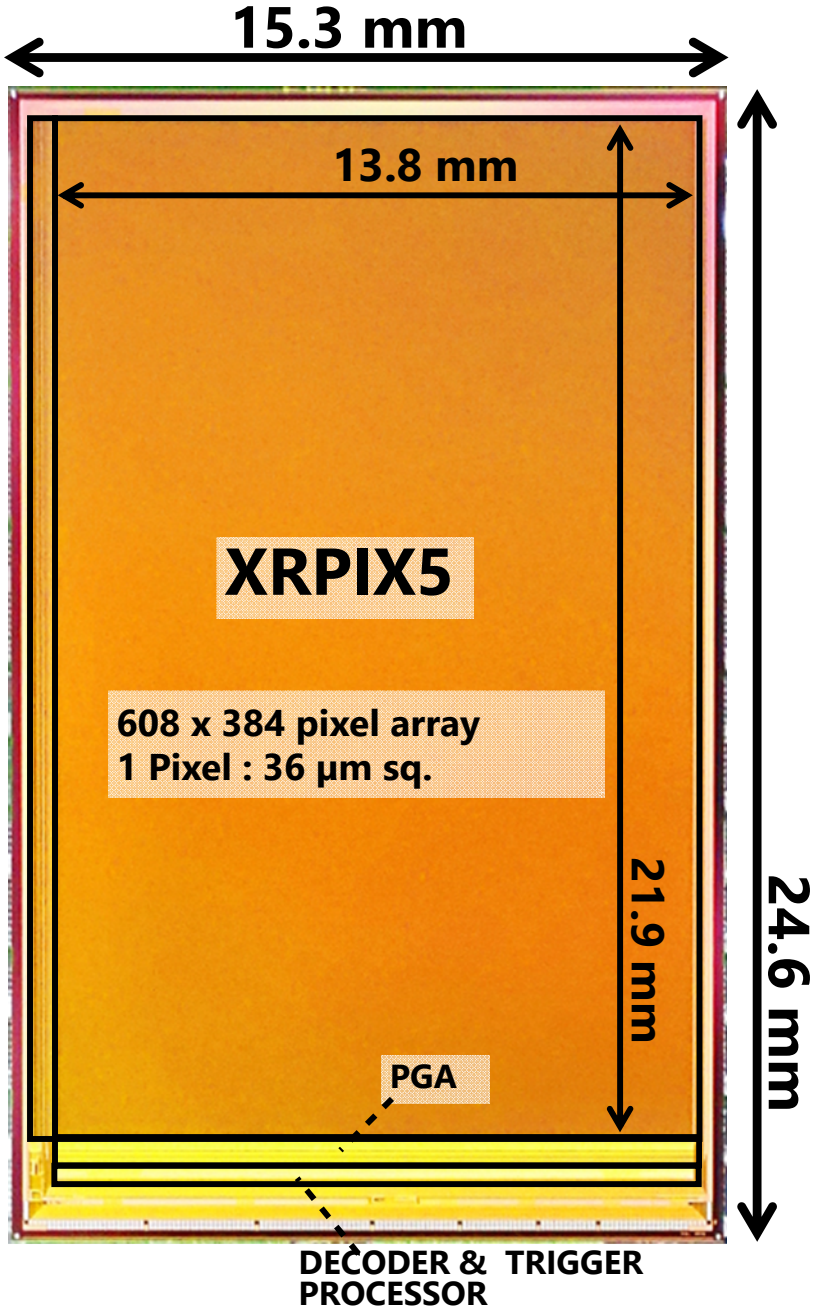
Dual Sensor Camera



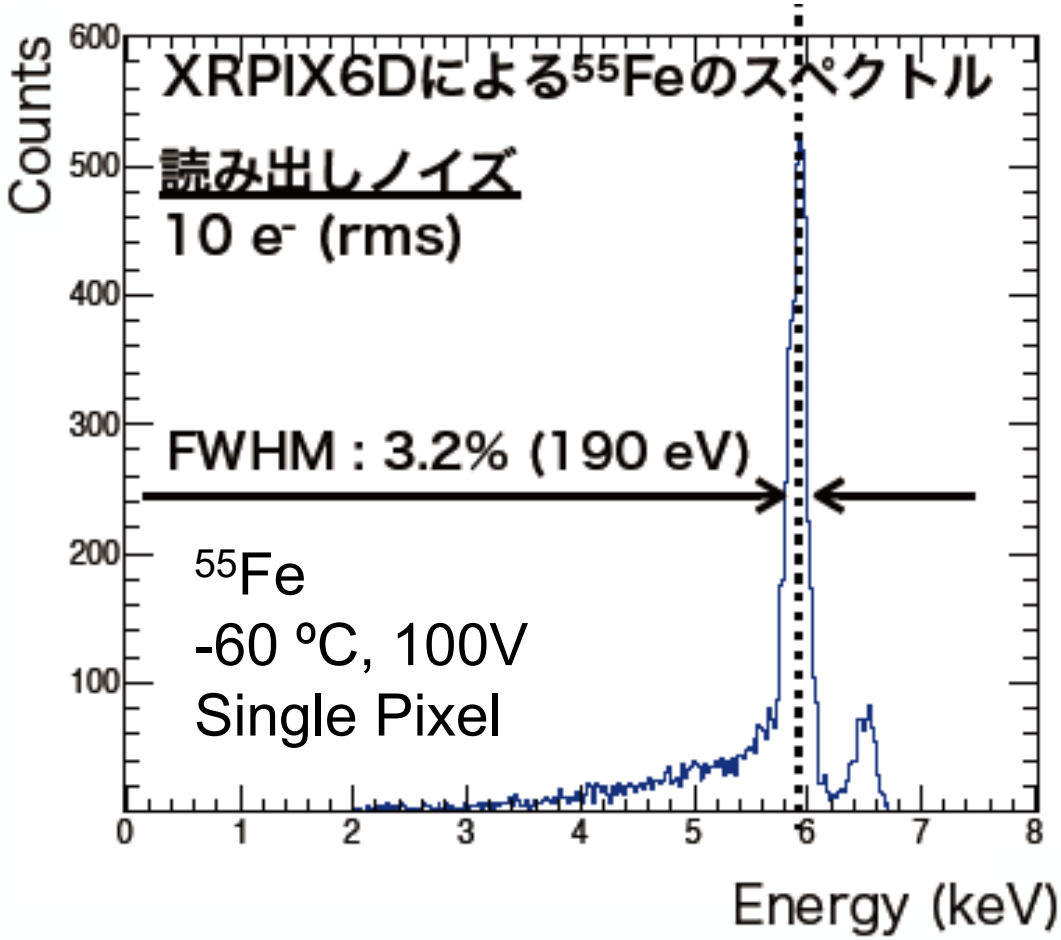
X-ray Tube Cu 22kV 400uA
5000 frames accumulated
(total exposure: 500 s)
Sensor-detector:2m

XRPIX: Event Driven X-ray Astronomy Detector

→ Tsuru's Talk



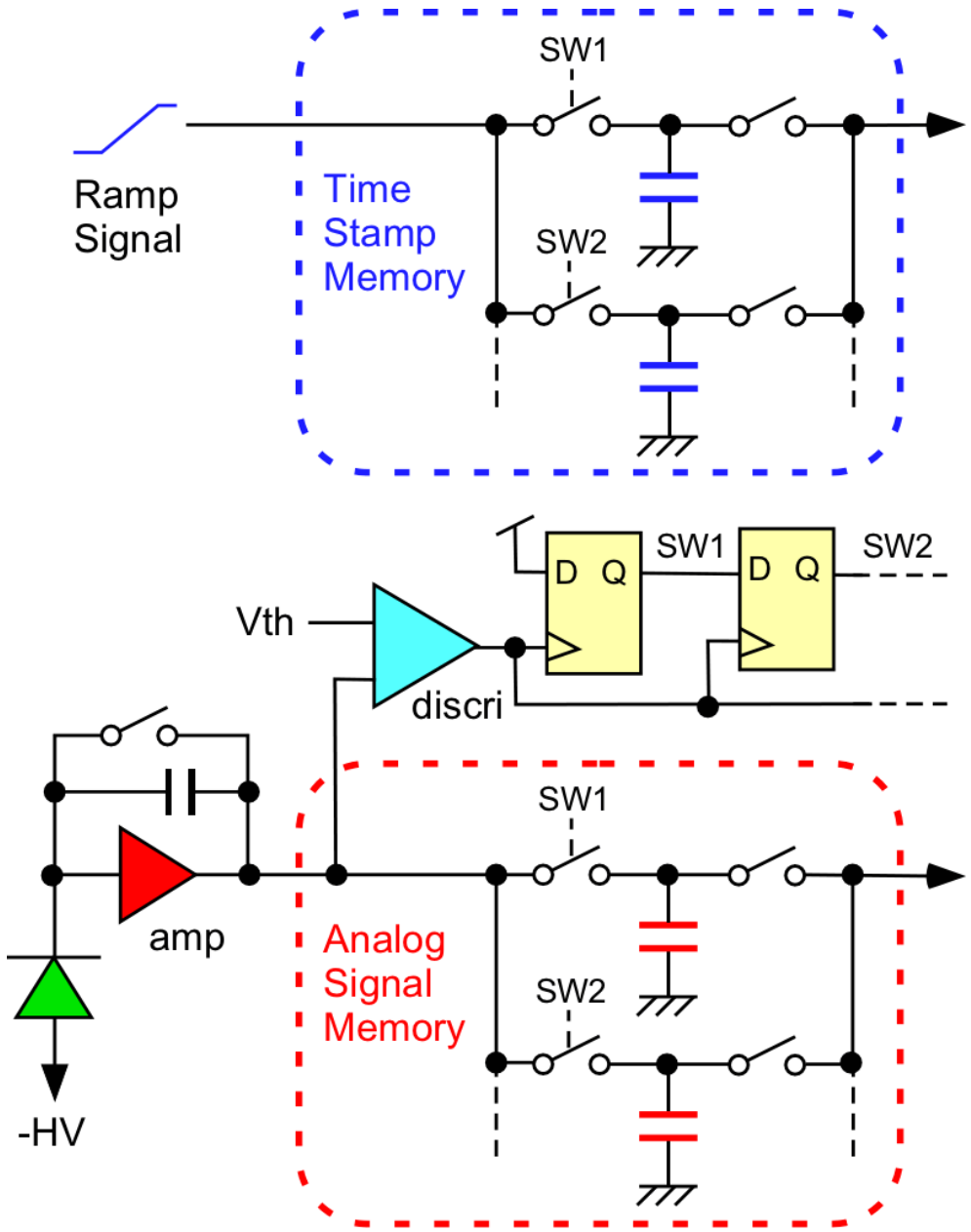
- Chip size : 24.6 mm x 15.3 mm
- Pixel size : 36 μm sq.
- # of pixel : 608 x 384 (= ~233k)
- Thickness of sensor layer : 310 μm (CZ wafer)
  500 μm (FZ wafer)



ILC Vertex Detector R&D : SOFIST

(SOI sensor for Fine measurement of Space & Time)

→ Yamada's Talk



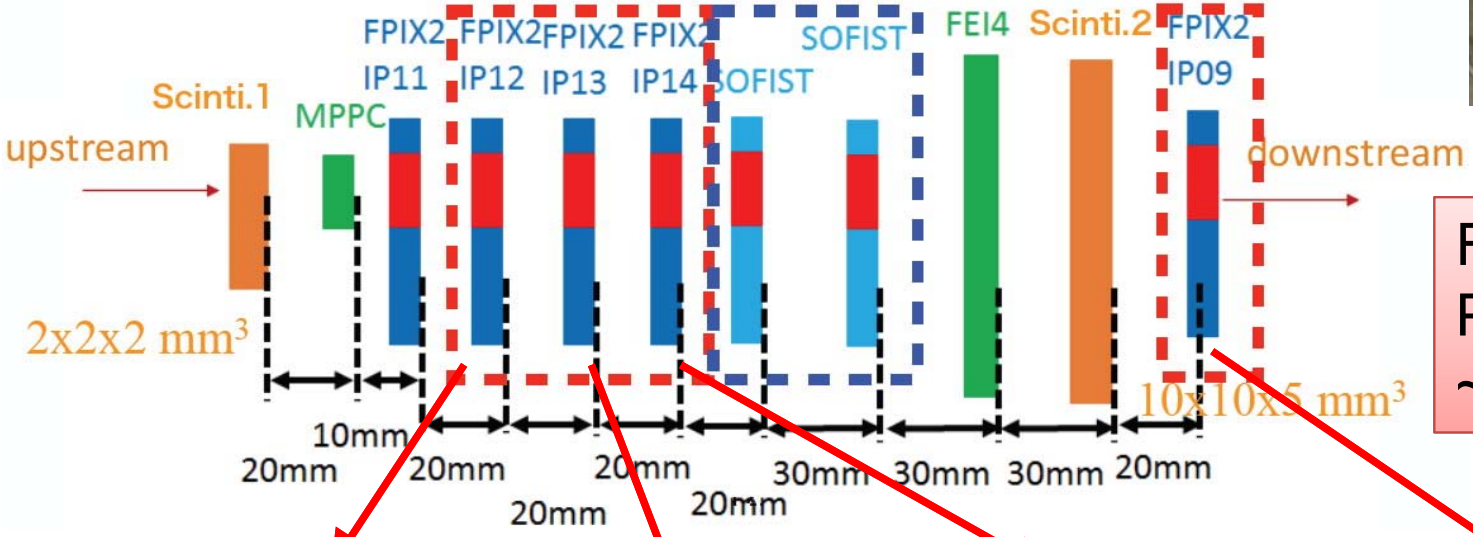
Test Chip Spec.

- Chip size: 2.9 × 2.9 mm2
- Substrate (FZ n-type, 2 kΩ•cm)
- Pixel size: 20~25 μm
- No. of Pixel: 50 × 50 pixels
- Gain: 32 mV/ke- (@Cf=5fF)
- Analog signal memories: 2 for signal or 2 for time
- Column-ADC: 8 bit
- Zero Suppression Logic

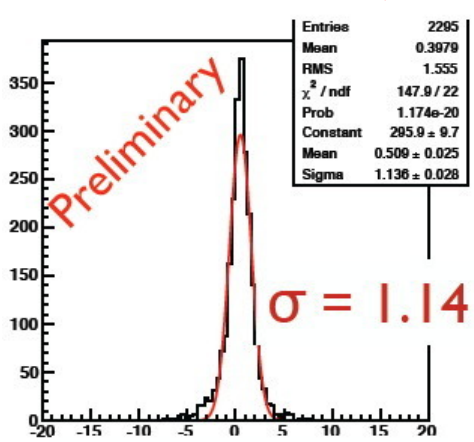
R&D for 3D integration is also progressing.

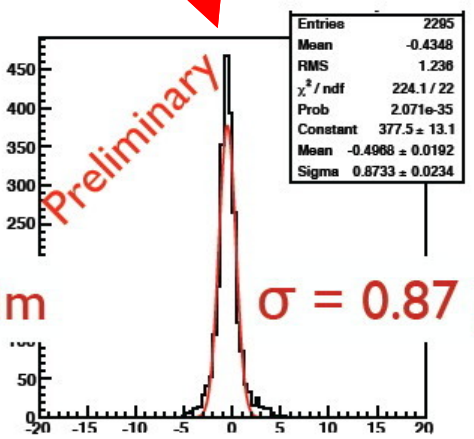
120GeV/c Proton Beam test at FNAL

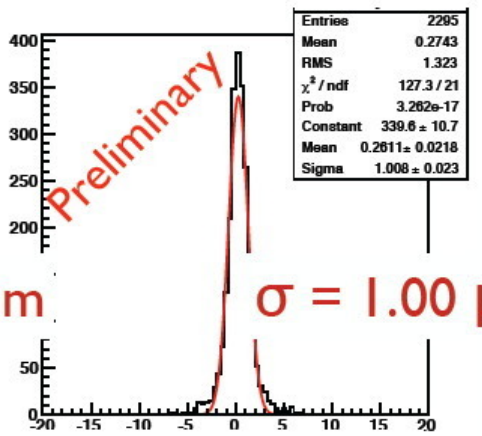
FPIX2 (8 μm pixel) x 4
SOFIST_v1 (20 μm pixel) x 2

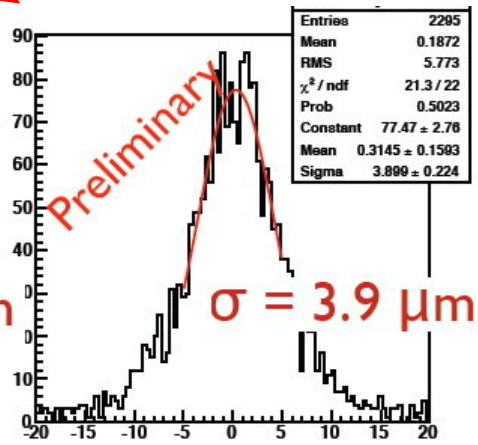


FPIX2
Position Resolution
~0.7 μm



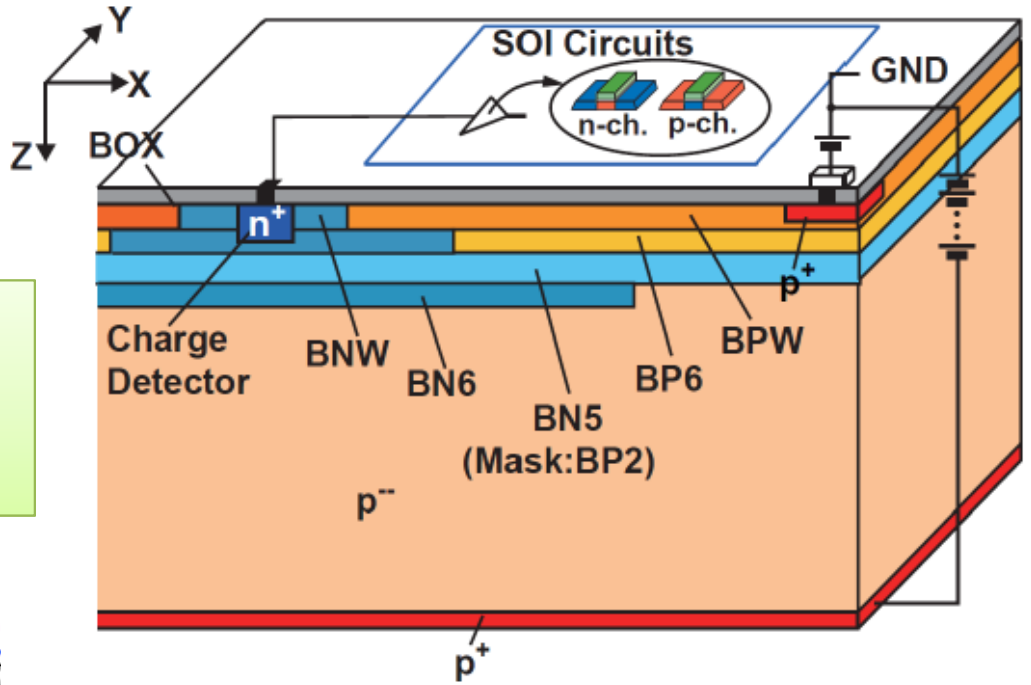


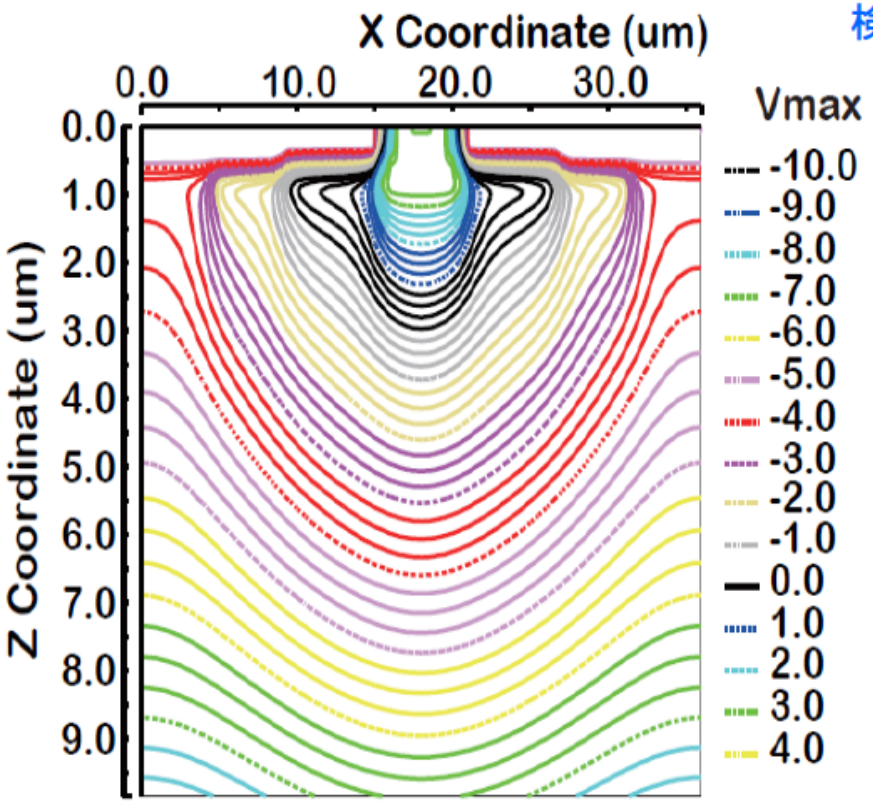


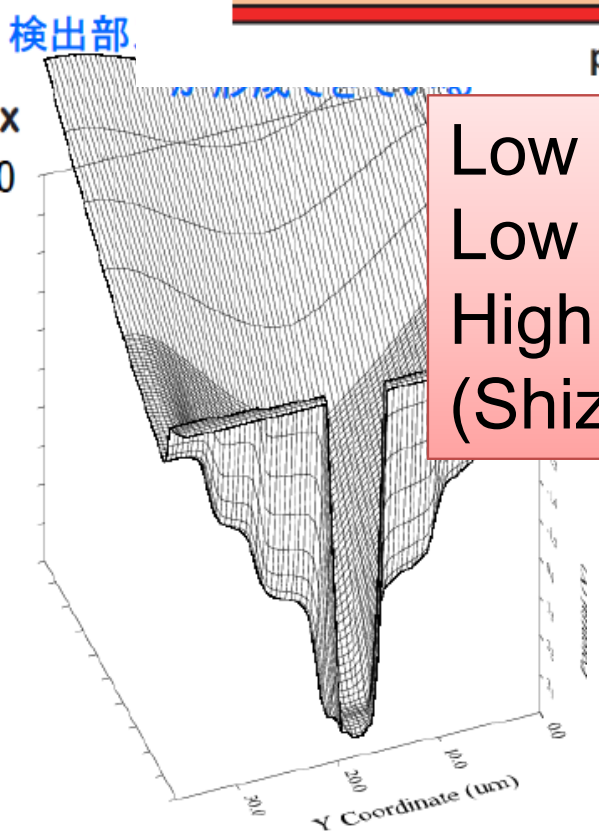


R&D on Backside Surface Pinning Pixel

Our SOI Pixel process is very flexible!
→ 5 Buried layers







Low Sense node Cap.
Low Leak current
High Gain
(Shizuoka Univ.)

IV. Summary

- SOI pixel technology becomes mature. Back-gate and sensor-circuit coupling issues are solved by introducing double SOI wafer.
- Radiation tolerance is improved to more than 10 Mrad by biasing middle Si of the Double SOI.
- NMOS-PMOS active merge reduces layout size very much. This is almost equivalent to go to finer process while keeping analog voltage of 0.2um process (1.8V/3.3V).
- Many kinds of SOI X-ray detectors are developed (or under development) so far.
- With the collaboration of IPHC group and the SOIPIX group, I expect large synergy will be borne.

1st International Worksop on SOI Detector (SOIPIX2015) @Sendai, June 3-6, 2015


11th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking detectors (HSTD11)
in conjunction with
2nd Workshop on SOI Pixel Detector (SOIPIX2017)
OIST, Okinawa, Japan, Dec. 11-15, 2017.
TOPICS:
Simulations
Technologies
Pixel and Strip Sensors
Radiation Tolerant Materials
ASICs
Large Scale Applications
Applications in Biology, Astrophysics, Medical, ...
New Ideas and Future Applications
SOI Detectors
KEY DATES:
Abstract submission: 10 July - 28 Aug.
Registration: 10 July – 20 Nov.
https://indico.cern.ch/event/577879/
For further information – email: hstd@ml.post.kek.jp
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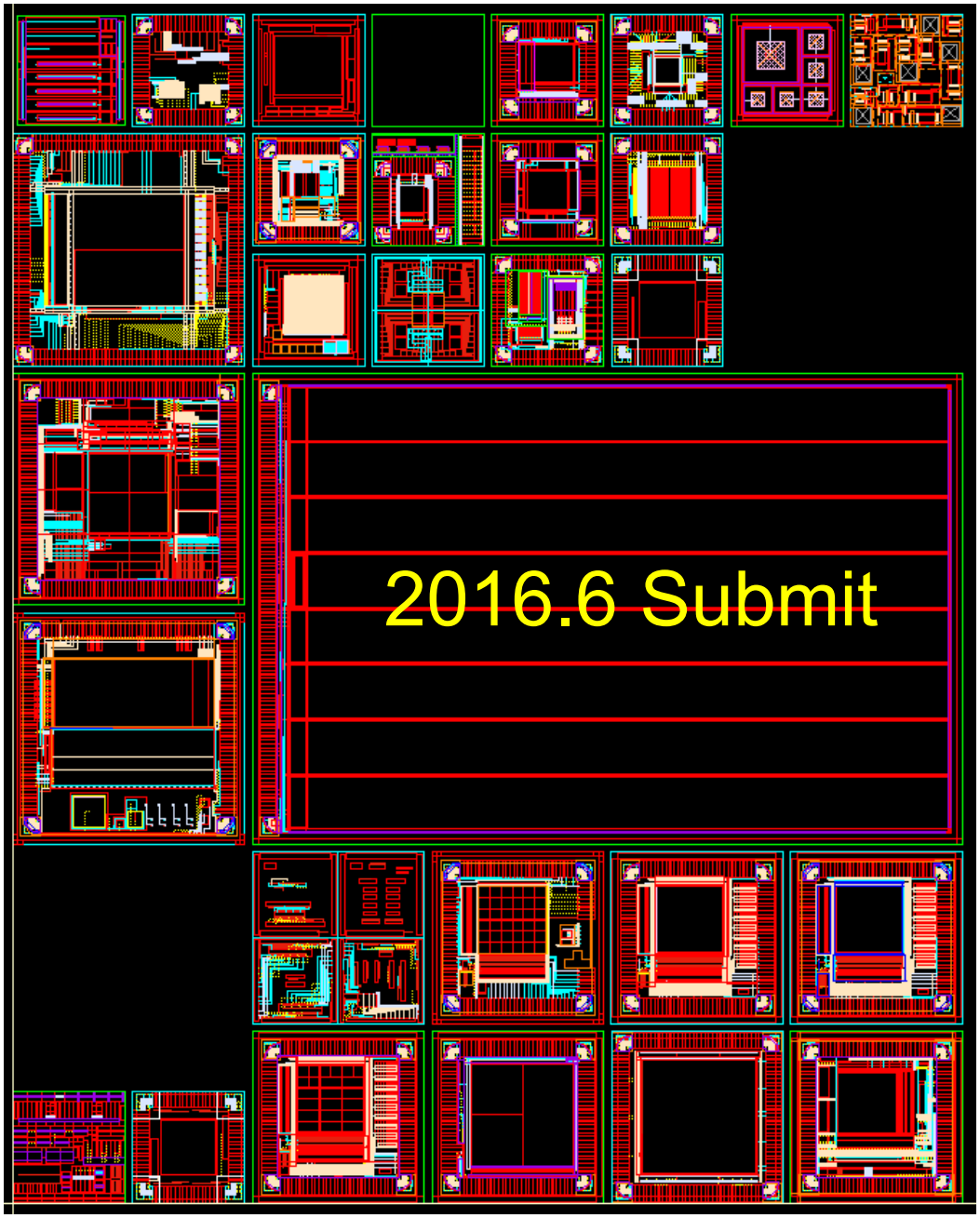
Thank You!



Backup