SOIPIX
Silicon-On-Insulator Pixel Detector Project

Integration-type SOI pixel sensor

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(High Energy Accelerator Research Organization, KEK)

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IPHC, Strasbourg, France

Outline

Development history

Developed SOI sensors
- -DIPIX (column ADC study)
- FPIX(1,1b, 2,3)
- INTPIXh2 (radiation tolerance study)
- INTPIX4-8

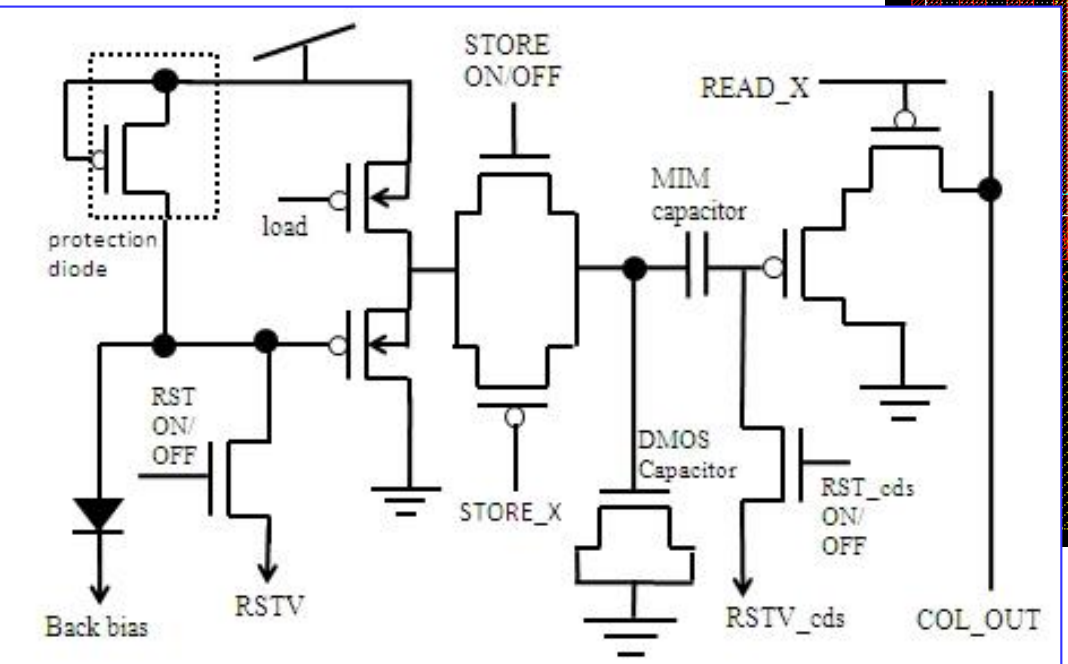
DAQ system (current and future plan)

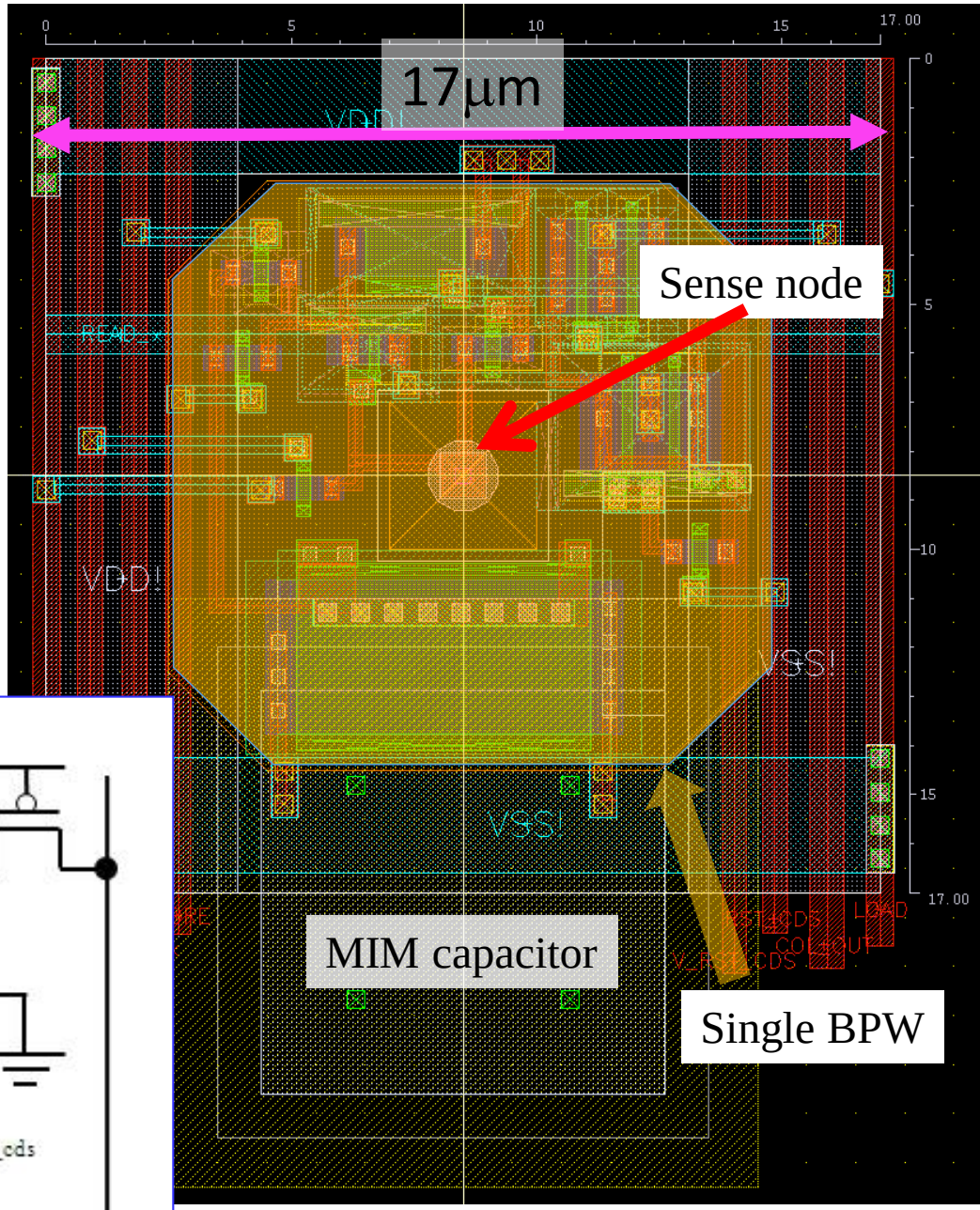
Summary & Future prospects

Features of integration-type SOI pixel sensors

Simple pixel circuit
Small pixel size
- w./o. storage capacitor > 8um
- w. storage capacitor > 12um

Good for basic evaluation tests

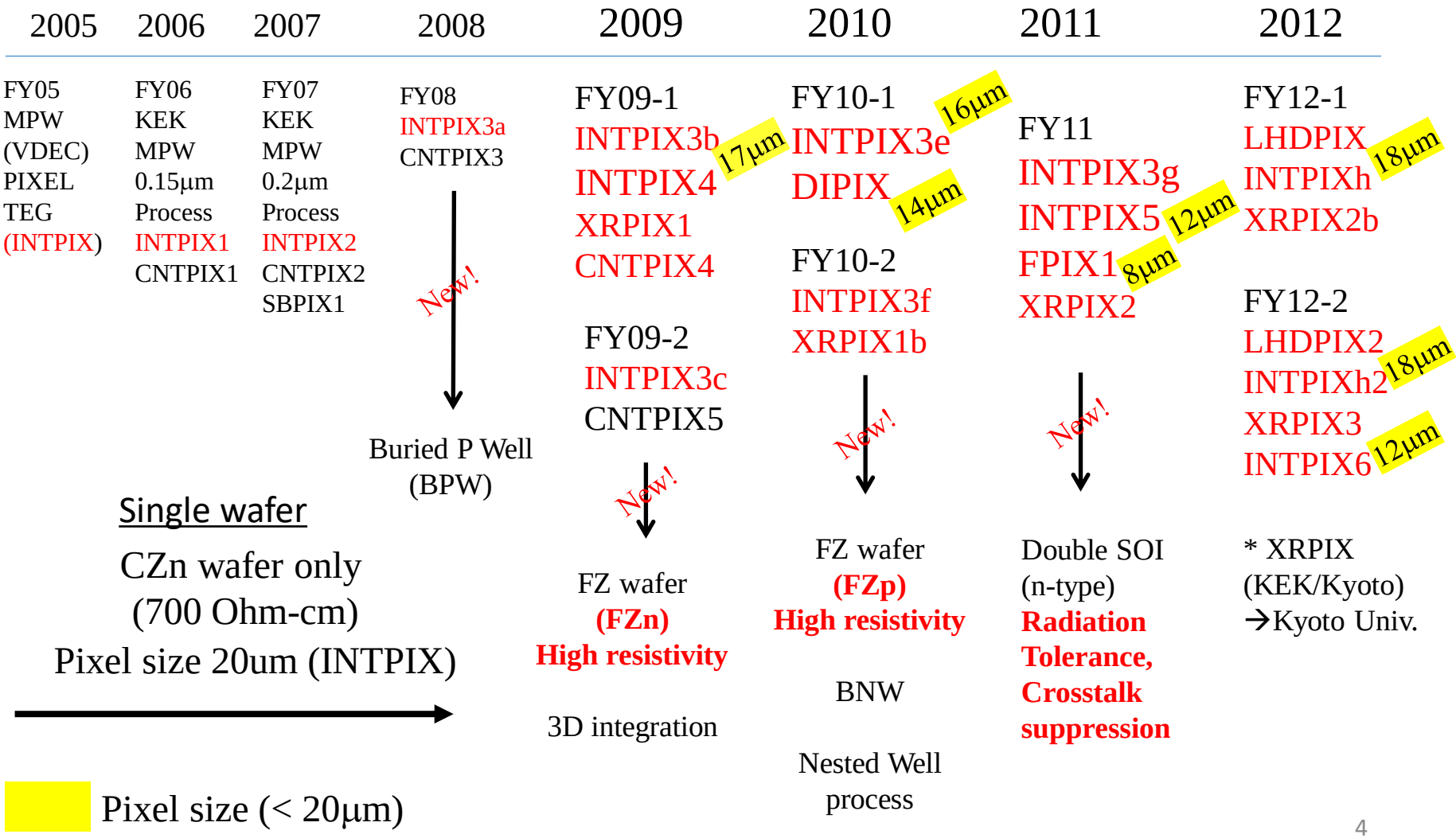




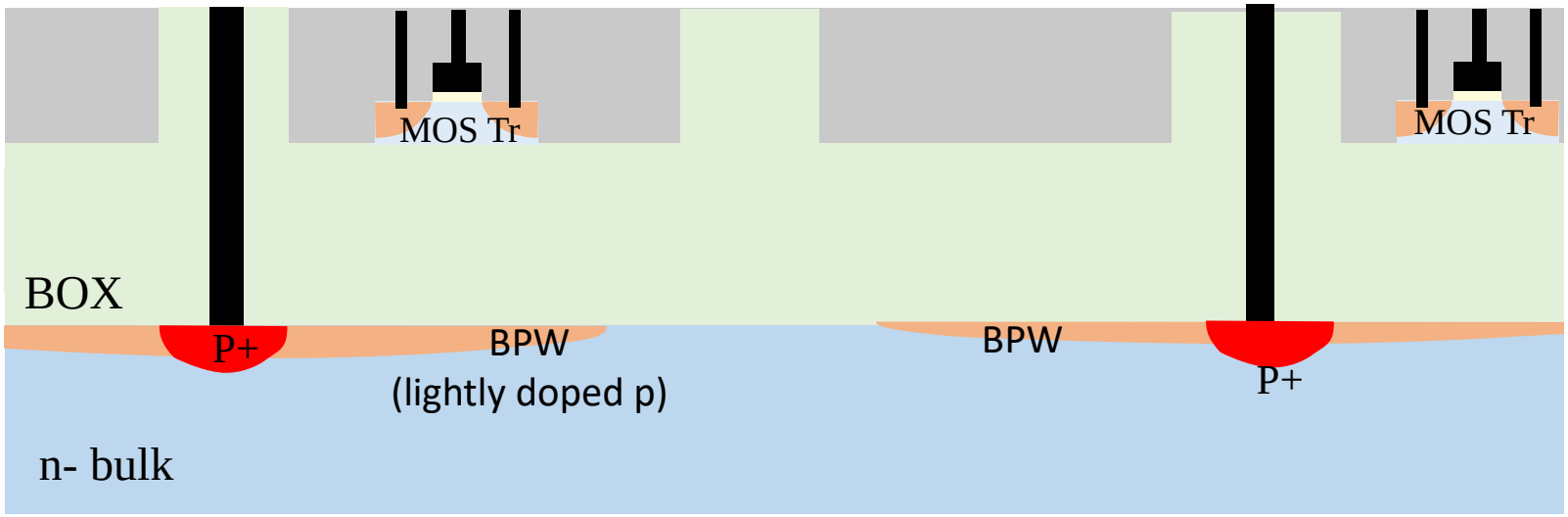
INTPIX4 (2009)

Development history (1)

KEK pixel sensors （red：integration）
Integration-type, counting-type, binary, etc.



Buried-P Well process (2009-)

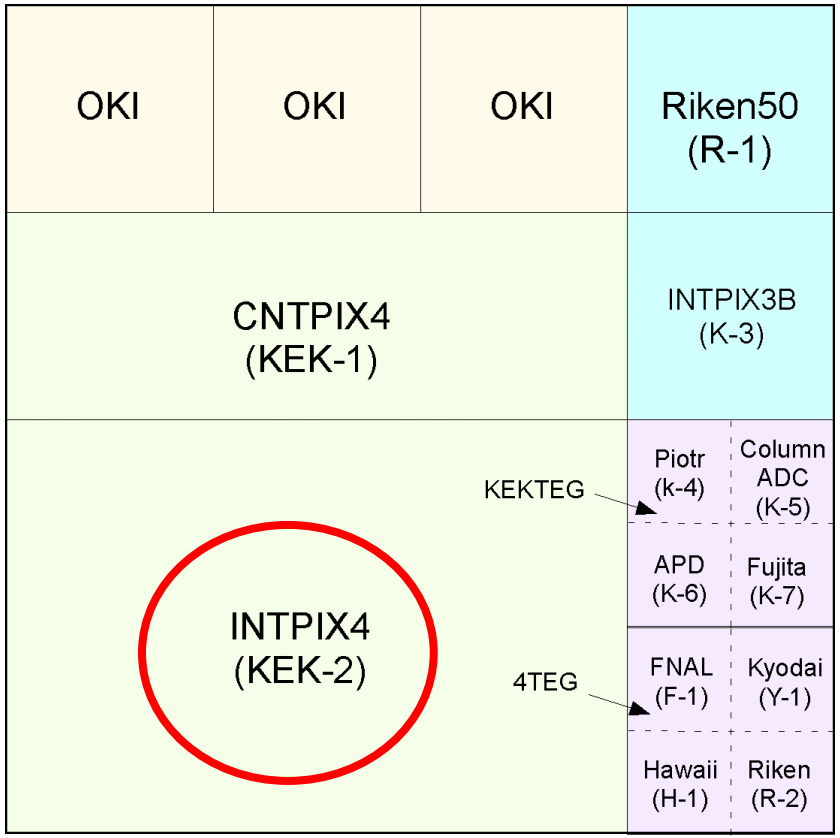


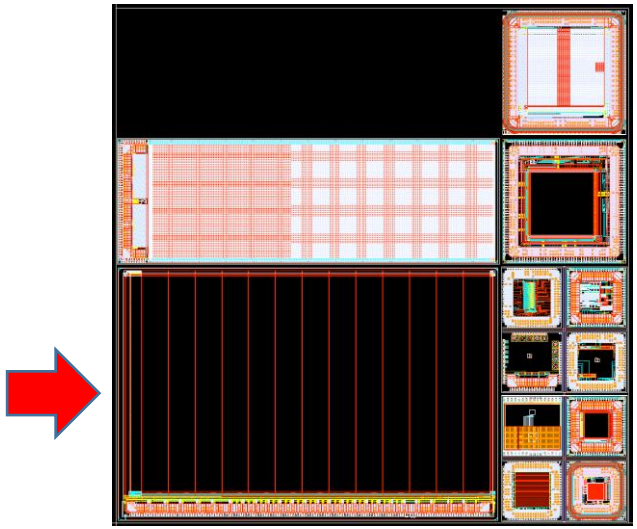
Side view of Pixels

Shield the back gate effect
(~2V: visible light detection → ~100 V: X-ray detection)

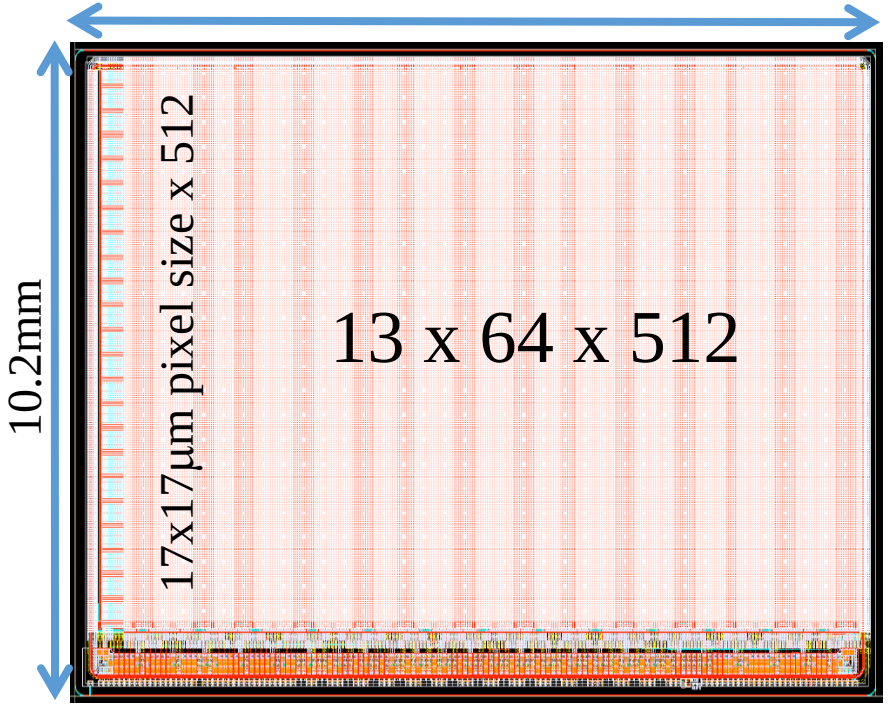
FY09-1 MPW run (2009)

20.4mm x 20.4mm





15.3mm



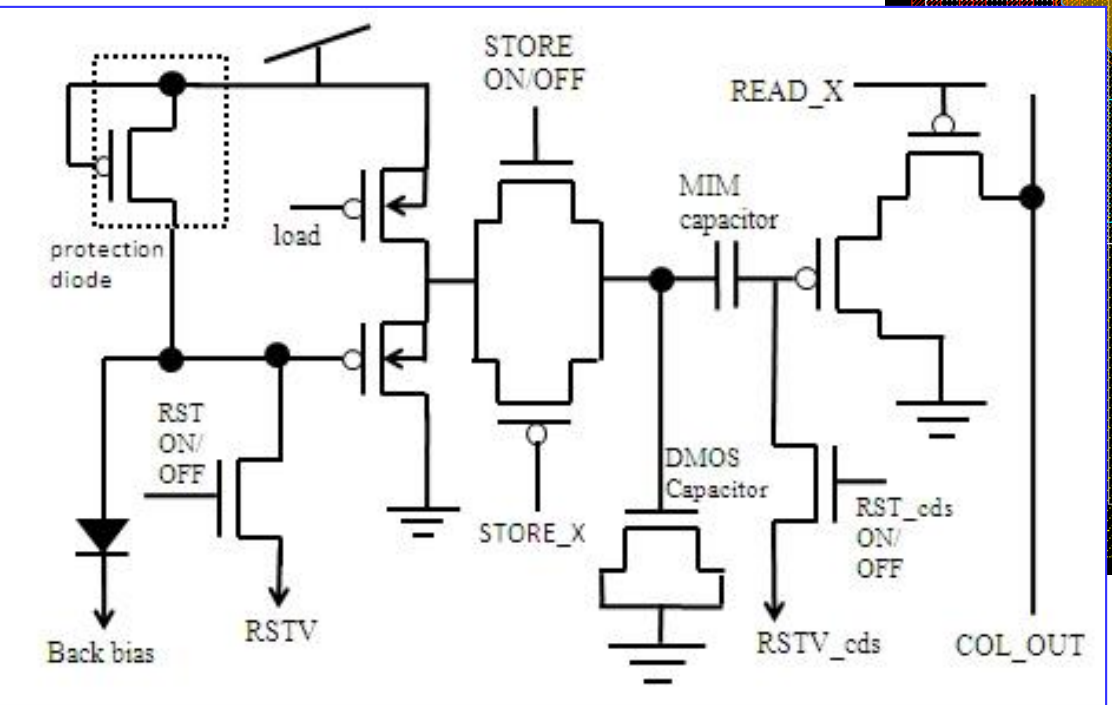
13 analog out

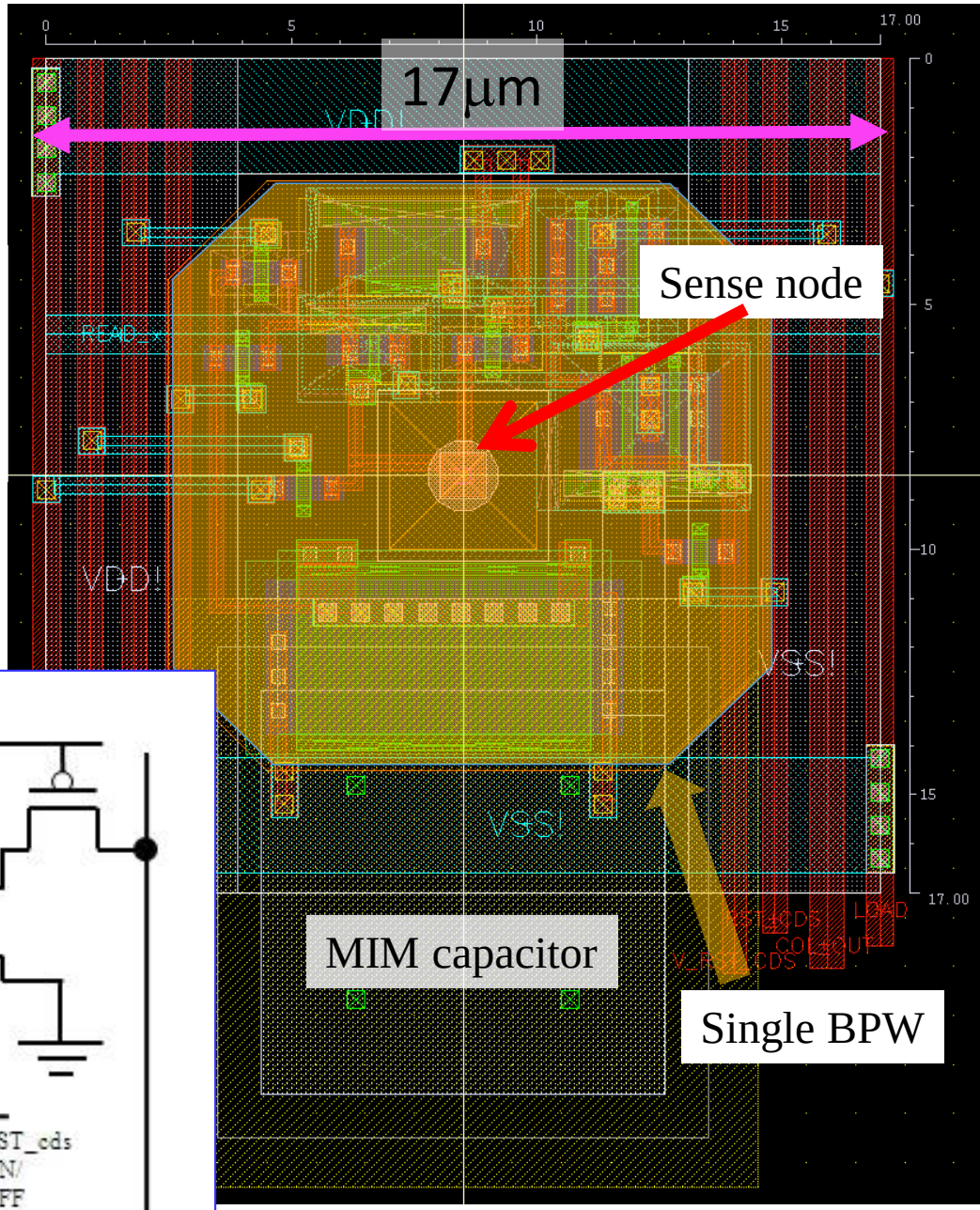
INTPIX4

Pixel Layout

- Pixel size 17 x 17 µm
- Circuit is based on PMOS
- Single BPW inside

Pixel circuit with CDS





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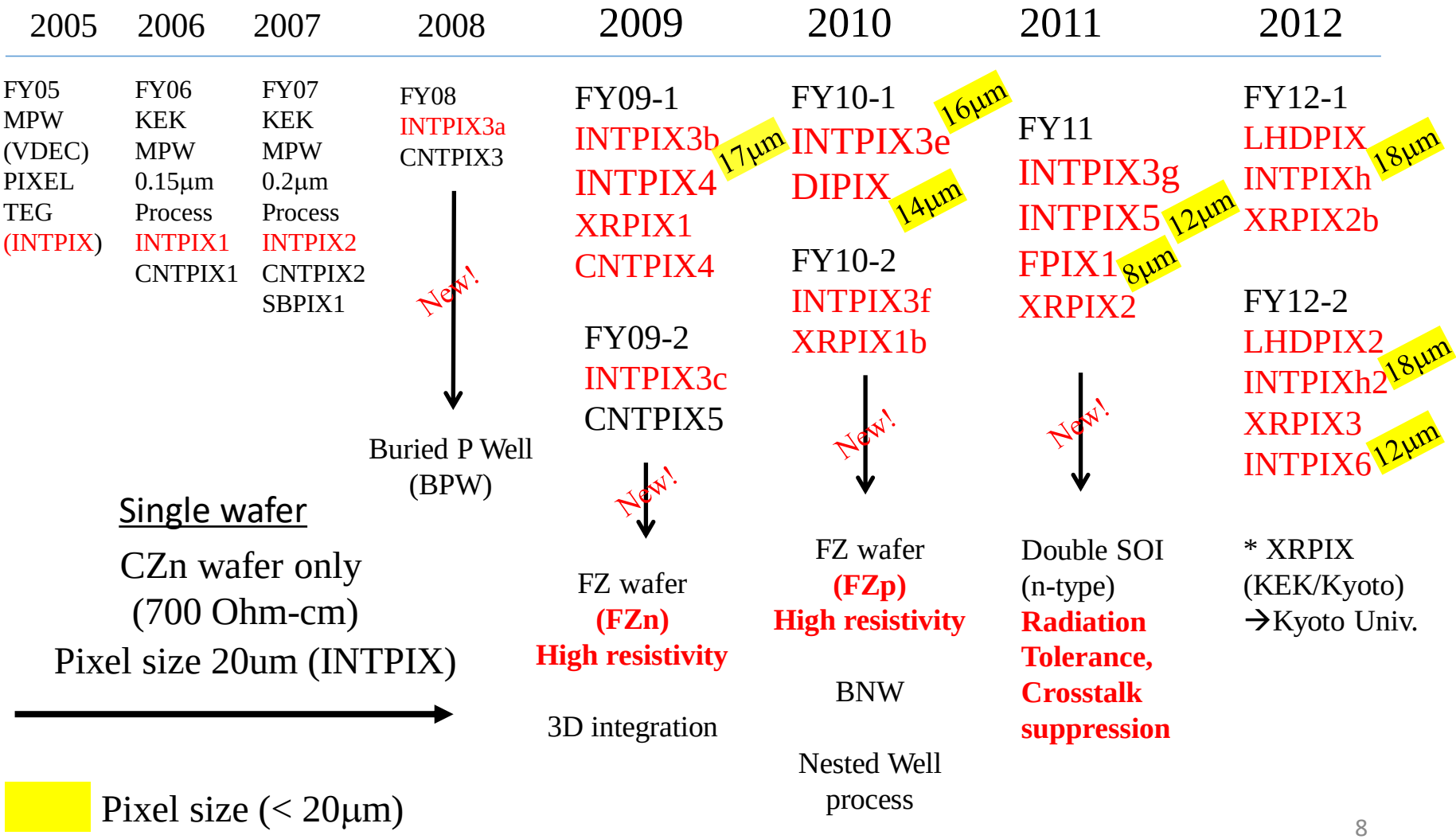
Integration-type, counting-type, binary, etc.



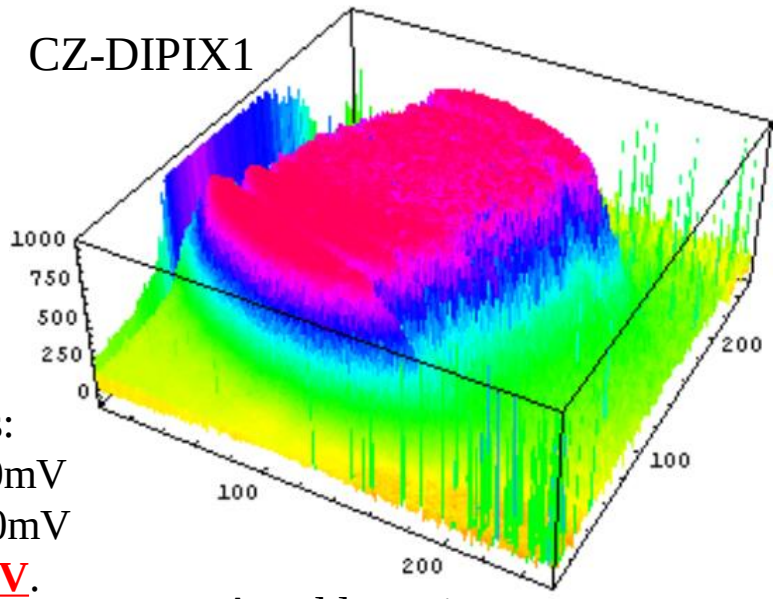
Digital output test (DIPIX)

General purpose test chip

P. Kapusta (Krakow)

DIPIX analog output → Column ADC (10bit)

CZ-DIPIX1



A red laser image

Operational condition

I_{RG}=0.67uA, I_{RGSF}=5.2uA, ADC_CLK=50MHz

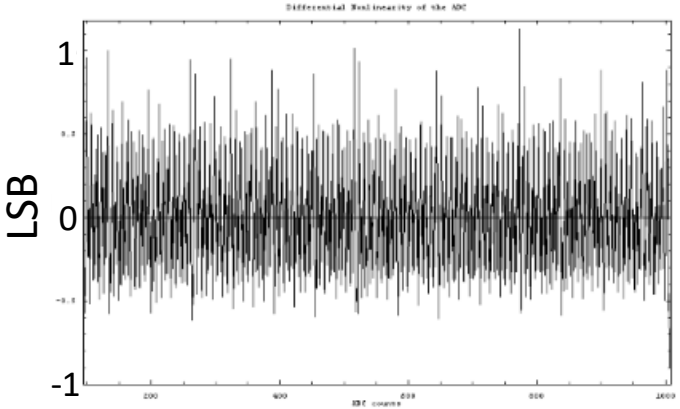
Conversion time 30 us for 50MHz clock
@1.8V limit (core supply),
Ramping capacitance 9.9 pF, and
Ramping current 0.67uA

Parameters:
V_{RSTN}=750mV
V_{IPIX}=1800mV
VDET=50V.

Linearity

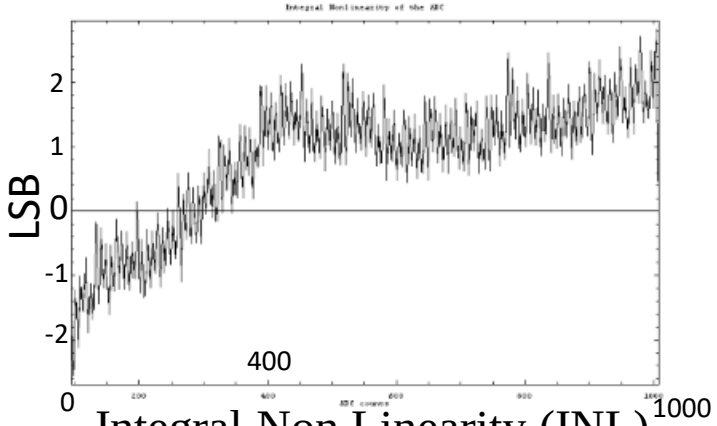
Input signal 720-1780mV(~1V) : ADC 94-1008(10bit).

DNL: -0.95 LSB to 1.13 LSB



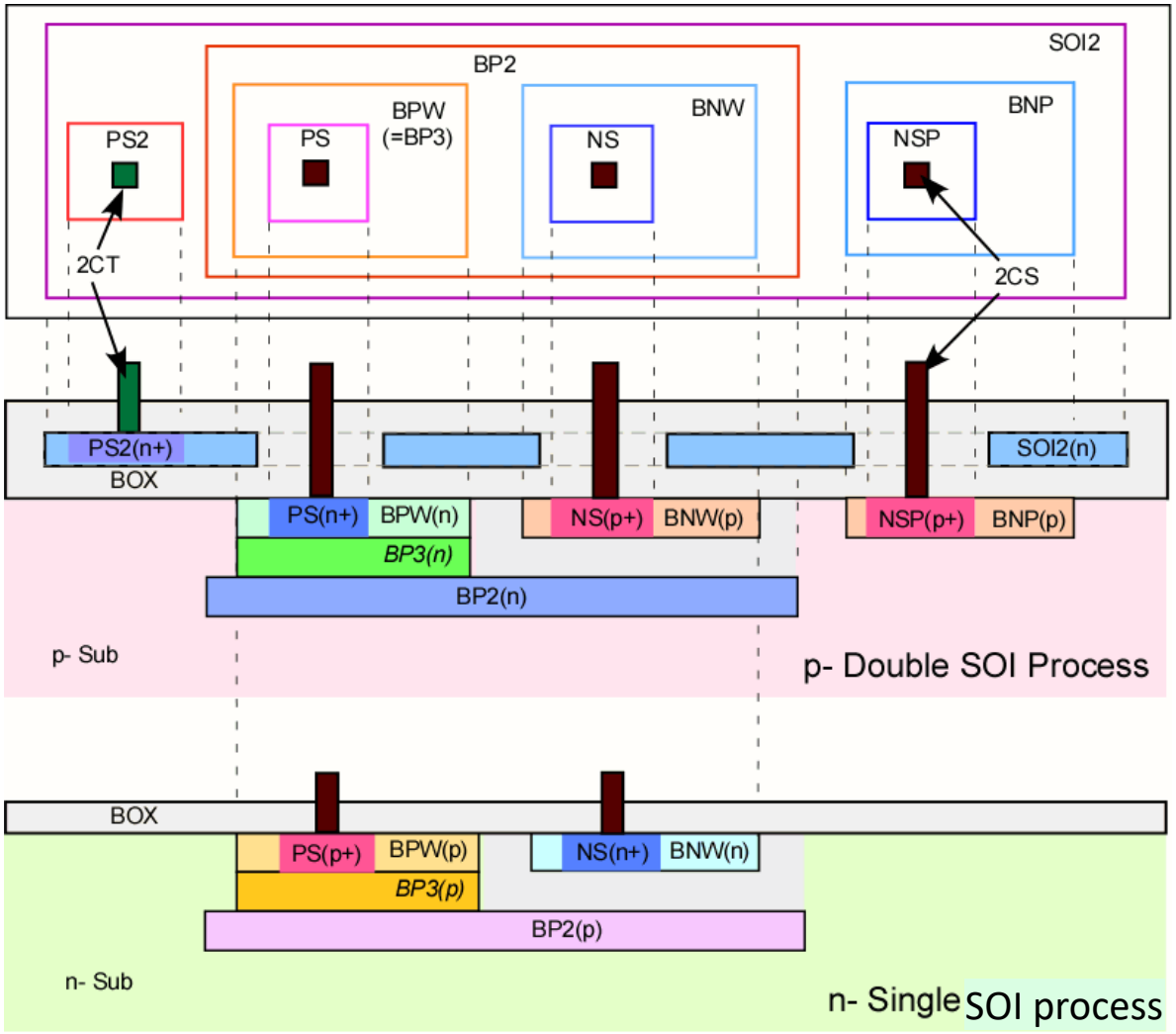
Differential Non Linearity (DNL)

INL: -2.6 LSB to 2.8 LSB

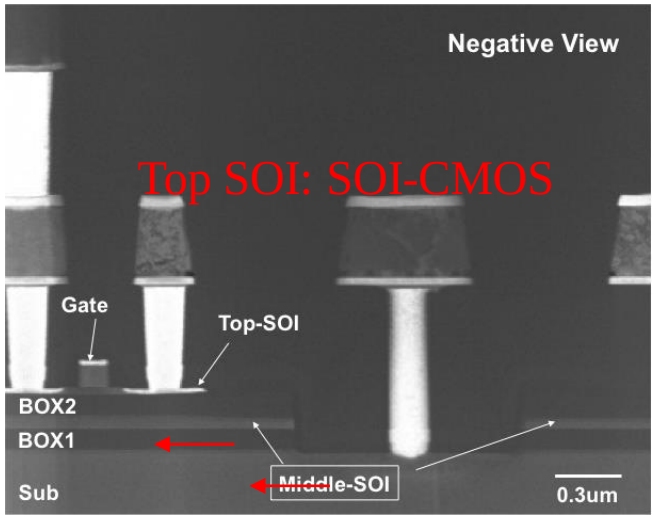


Integral Non Linearity (INL)

Various Implantation Options in Sensor part and Double SOI



Double SOI (DSOI)
STEM image



Middle SOI:
Additional shield layer

p/n various doping density

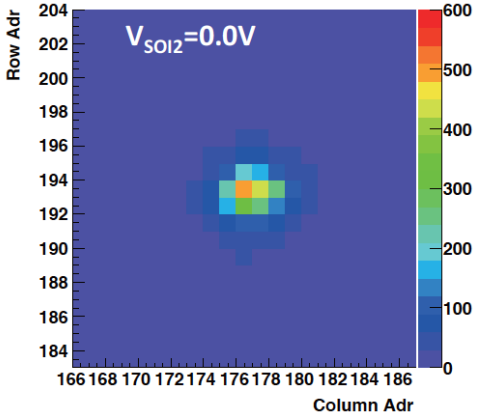
Shield the back-gate effect / optimize charge collection efficiency

Nested-well process

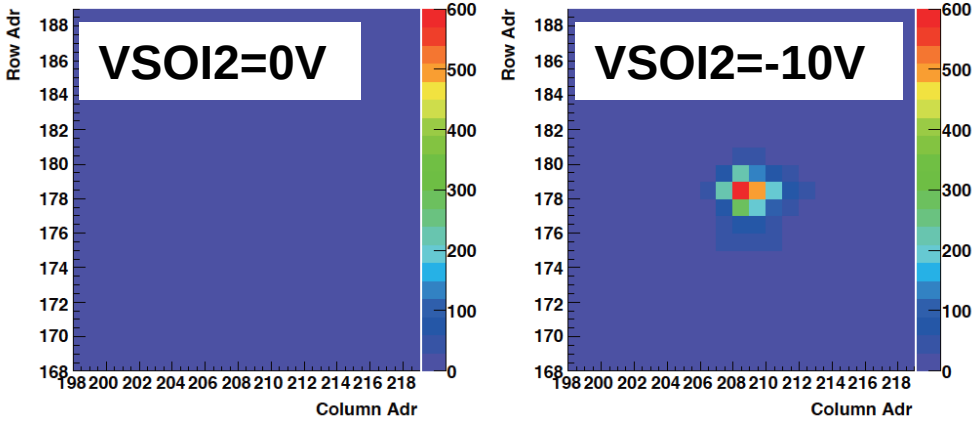
N-type Double SOI pixel sensor (INTPIXh2)

Sensor test

Pre-irrad

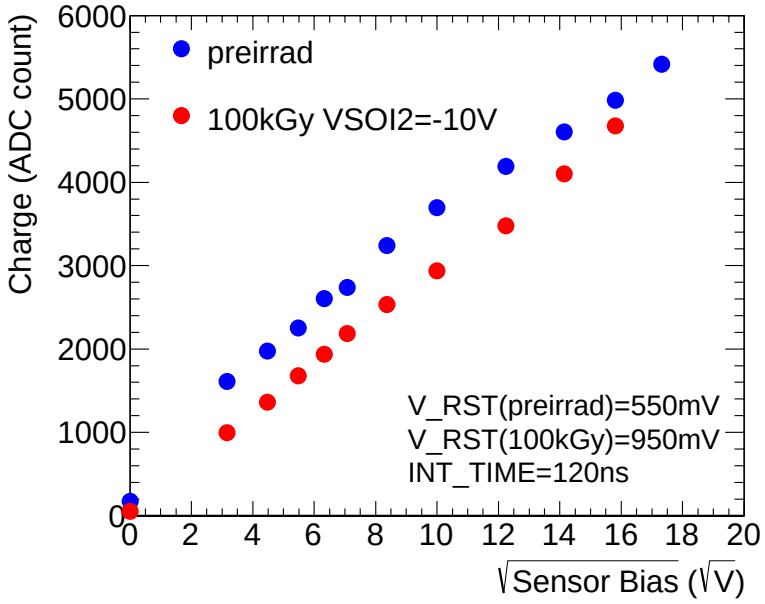


Response to infrared laser of 1064 nm wavelength and 10 ns pulse duration.



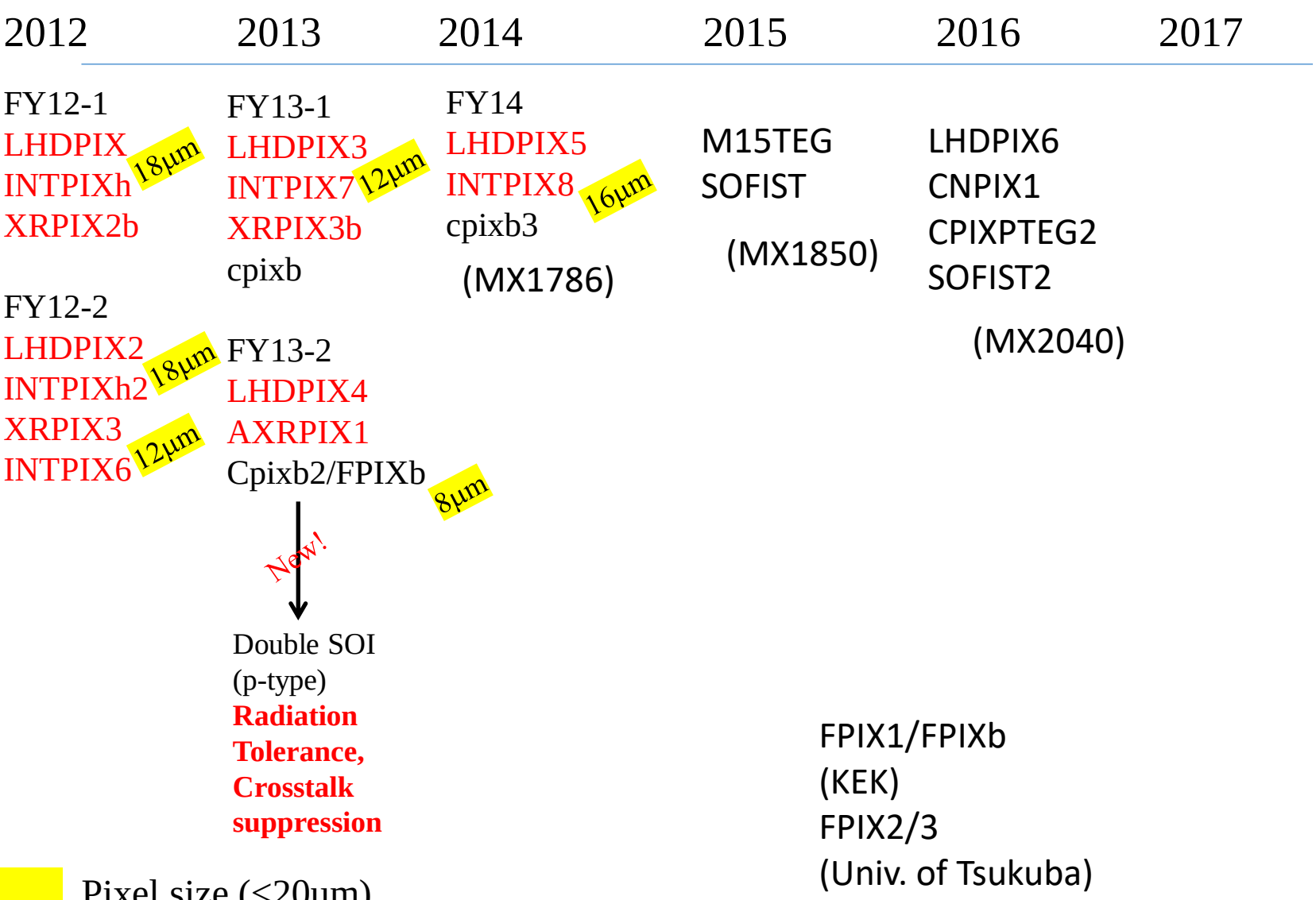
The pixel images after 100 kGy (10Mrad) could not obtain but recovered with VSOI2=-10V.

The average ADC count as function of the square root of the bias voltage for sensor.
➔Obtained similar linearity and sensitivity to pre-irradiation with VSOI2=-10 V .



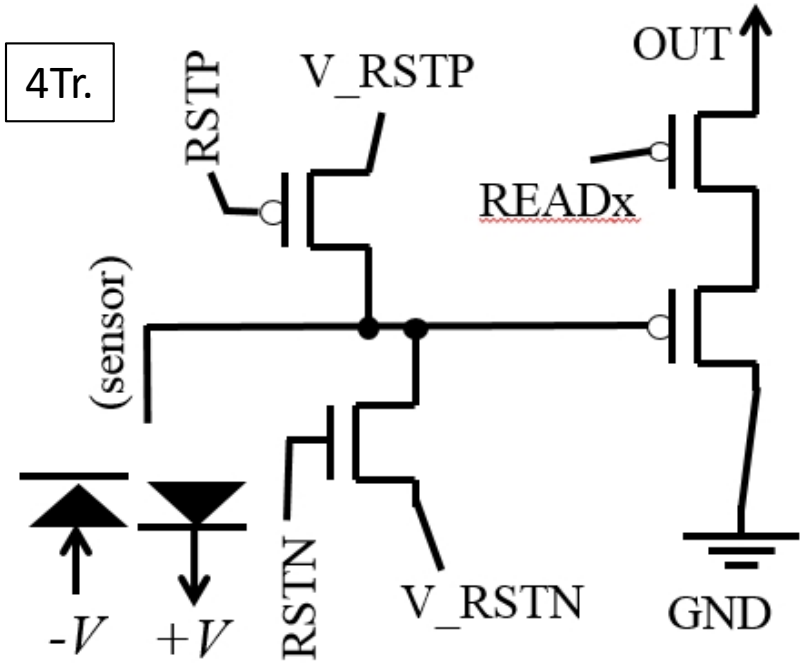
S. Honda et al., TIPP2014, 2-6 June 2014, Amsterdam

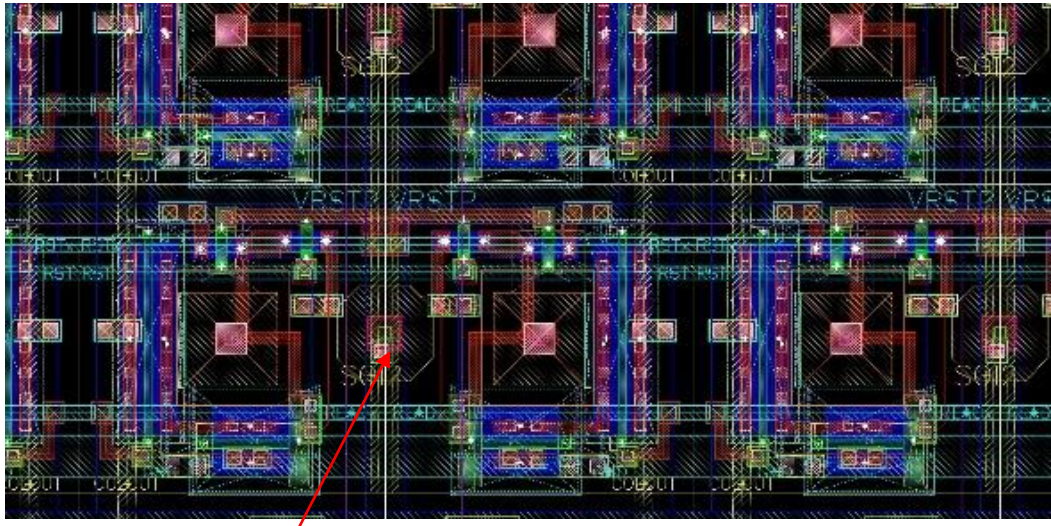
Development history (2)



SOI Pixel sensor (8 μm pixel)

fpixb (MX1711): pixel size 8 um x 512 x 192 pixels



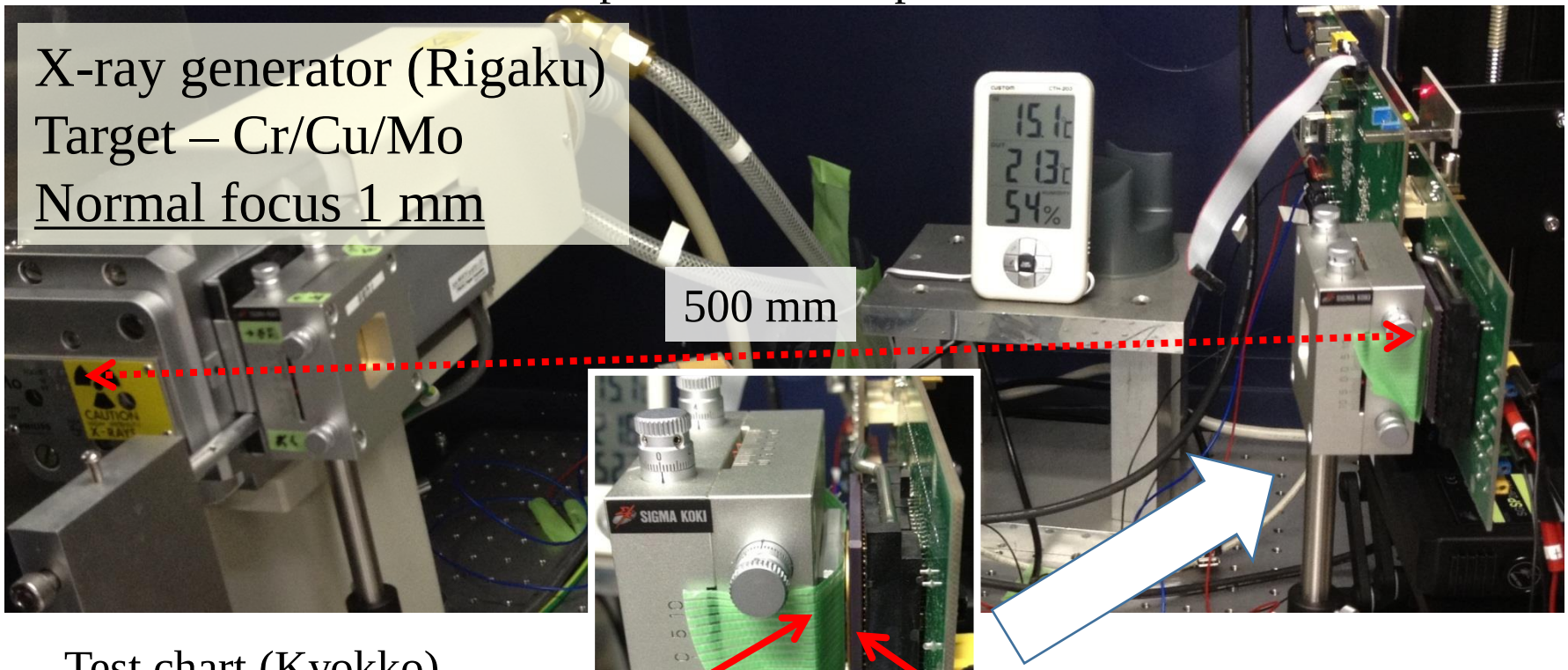


PS2 contact for middle SOI between pixels

No storage capacitor
Not good at synchronous measurement
Good at asynchronous measurement

Spatial resolution study

Experimental Setup

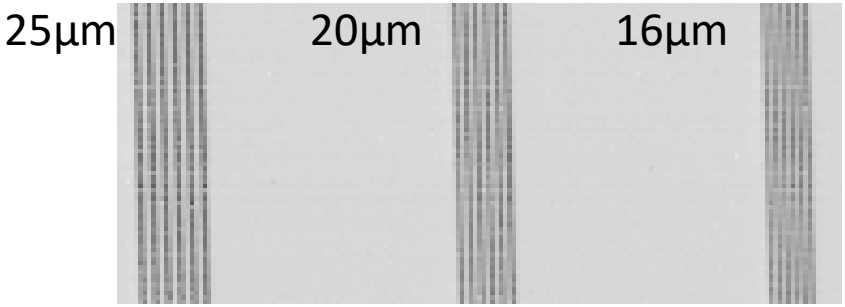


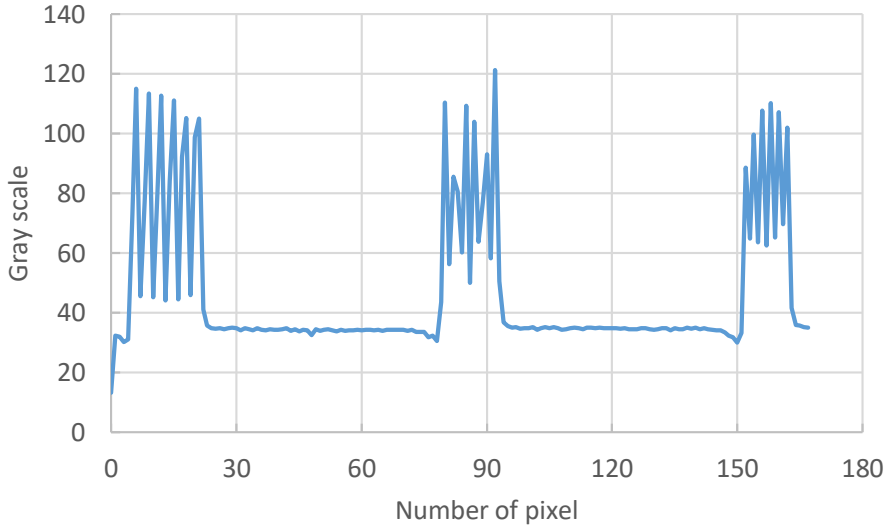
- Test chart (Kyokko)
  Pb 30 μm
  < 20 LP/mm
- Micro chart (JIMA)
  Au 1 μm
  3-50 μm slits
- X-ray Imaging demonstration

Spatial resolution

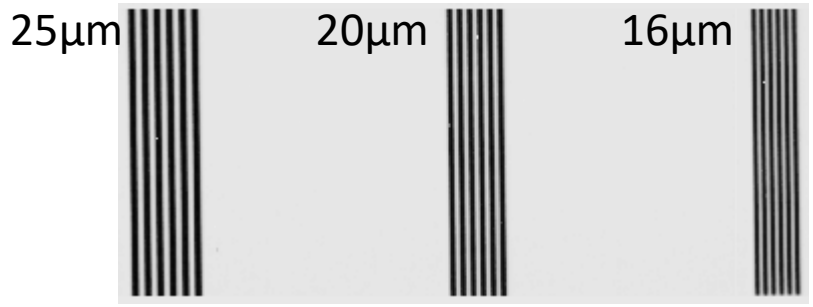
X-ray test chart + X-ray tube

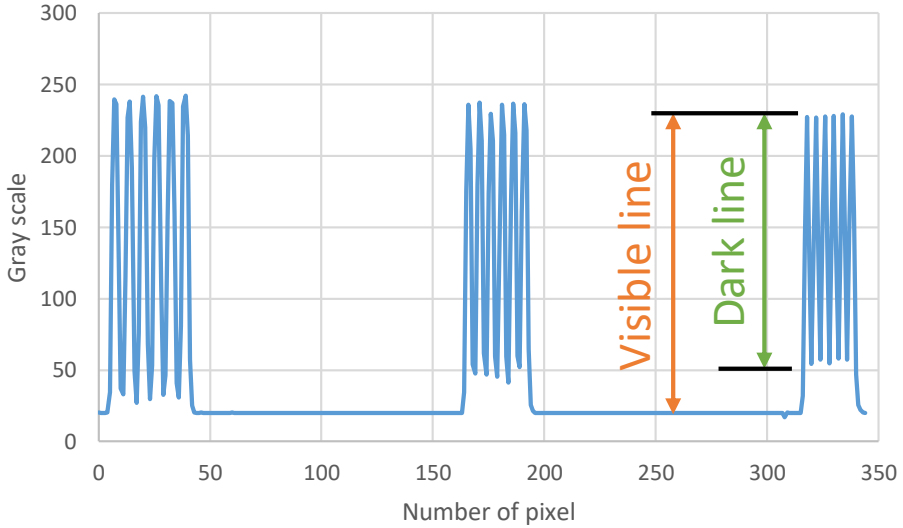
2009 NFZ-INTPIX4 17um pixel





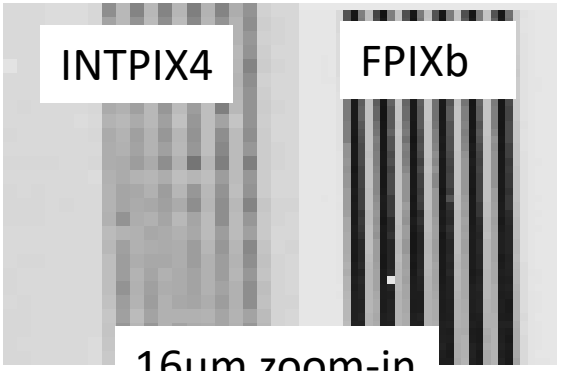
2014 NFZ-FPIXb 8um pixel





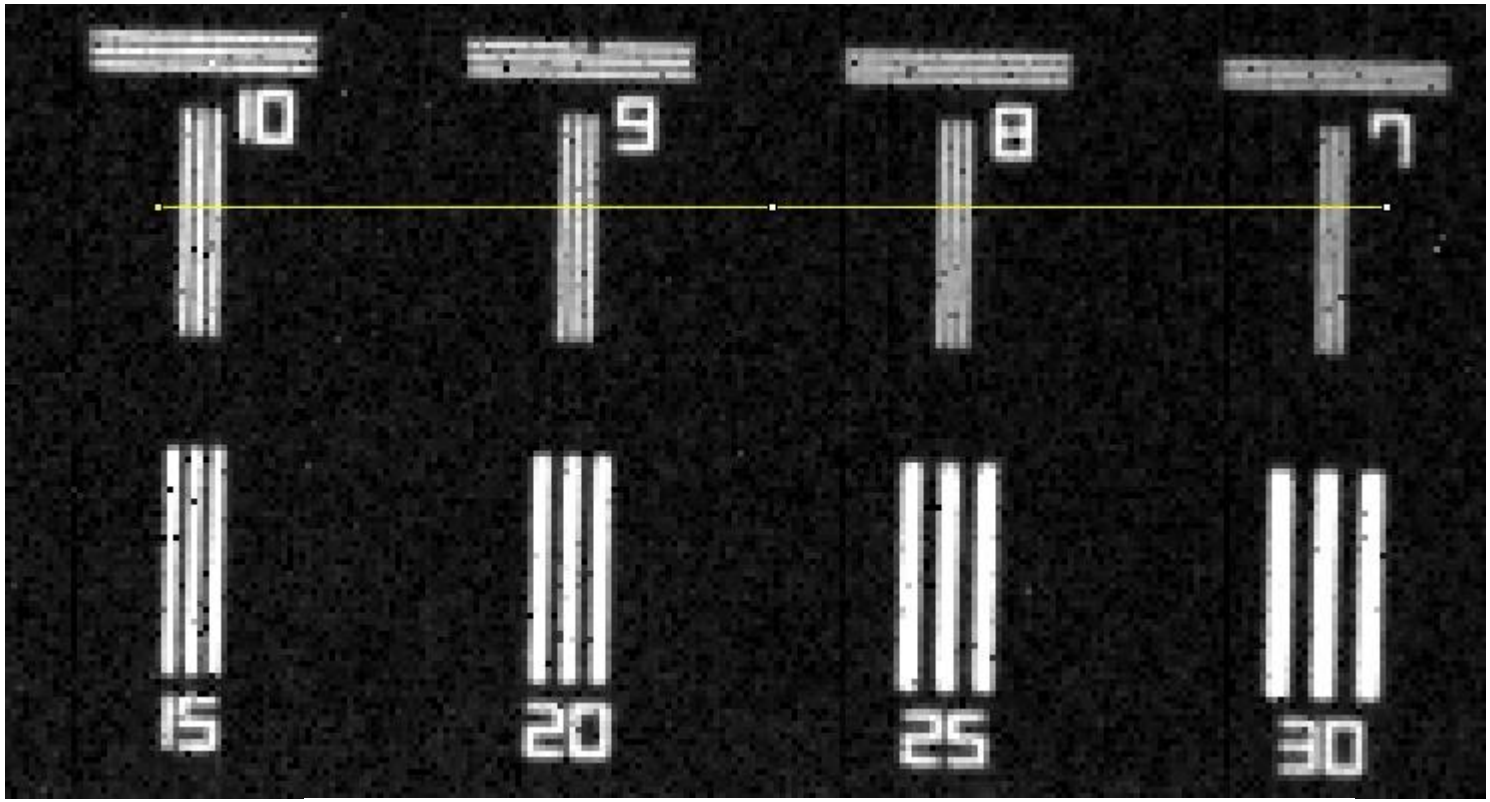
- Cu 8keV、20kV、2mA、front illumination, bias 100V
- Ratio 16μm slit: Dark line / visible line

INTPIX4(17μm)：0.57、FPIXb(8μm)：0.83

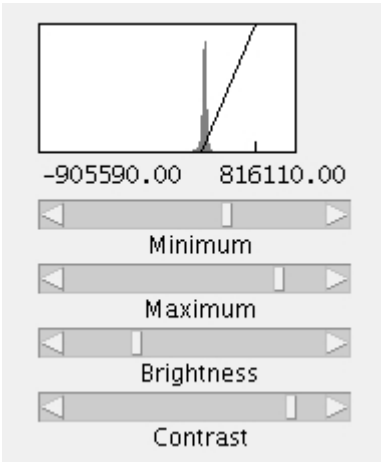


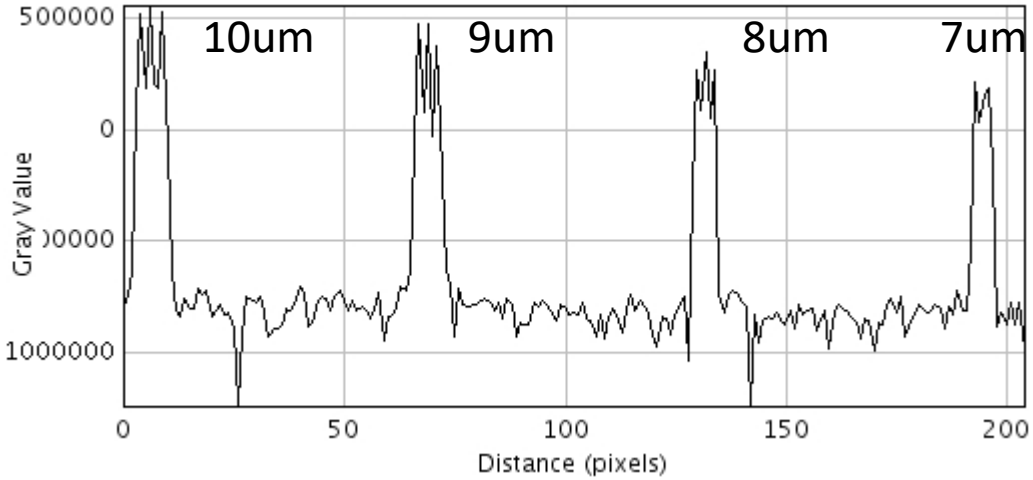
JIMA X-ray test chart image

2015/8/13



grayscale
Invert





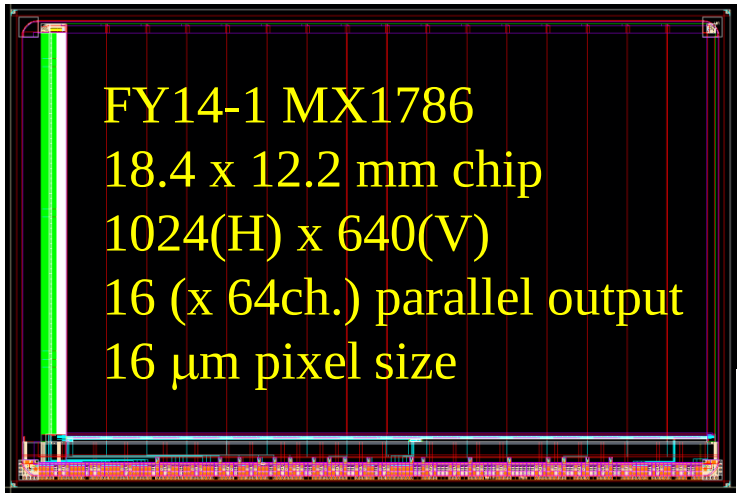
1d histogram

8um --- 3 slits

INTPIX4-8

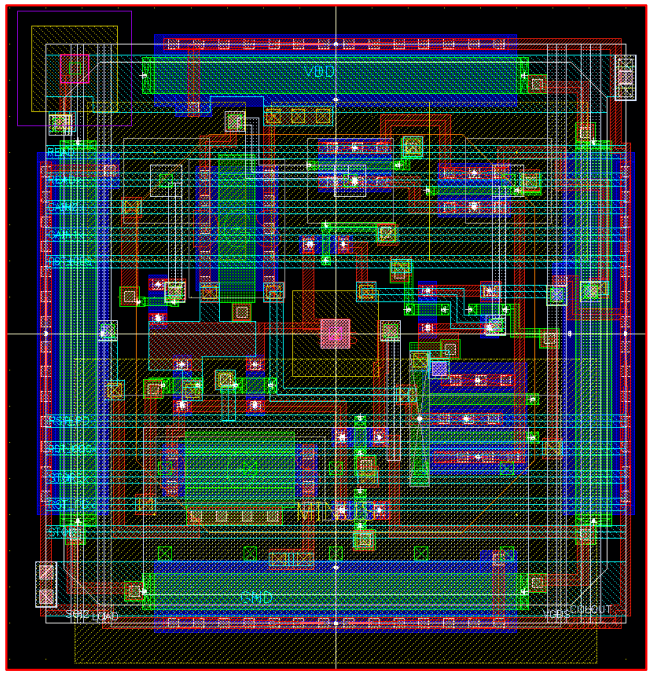
	INTPIX4	INTPIX5	INTPIX6	INTPIX7	INTPIX8
Process	MX1350	MX1501	MX1594	MX1655	MX1786
Pixel size	17 um sq	12 um sq	12 um sq	12 um sq	16 um sq
# of pix.	512 x 832 (425,984 pix)	896 x 1408 (1,261,568)	896 x 1408 (1,261,568)	1408 x 1408(1,982,464)	640 x 1024 (655,360)
Chip size	10.2 x 15.4mm2	12.2 x 18.4 mm2	12.2 x 18.4 mm2	18.4 x 18.4 mm2	12.2 x 18.4 mm2
Sensitive area	8.7 x 14.1mm2	10.7 x 16.9 mm2	10.7 x 16.9 mm2	16.9 x 16.9 mm2	10.9 x 17.4
Global Shutter	yes	yes	yes	yes	yes
Rolling Shutter	no	yes	yes	yes	yes
Frontend Amp	PMOS Source Follower	PMOS Source Follower	PMOS Source Follower	PMOS Source Follower	PMOS Charge Amp
CDS	In Pixel CDS	Column CDS	Column CDS	In Pixel CDS	In Pixel CDS
Sensor gain	~14uV/e-	~2.5/15 uV/e-	~2.5/15 uV/e-	~16 uV/e-	~12/18/36/80 uV/e-
Gain Sw	no	yes(1bit)	yes(1bit)	no	yes(2bit)
# of output	1or13	1or11	1or11	1or11	1or16
Wafer type	n-type	n-type	INTPIX6n(n、n-DSOI) INTPIX6p(p)	N,p, p-DSOI	N,p,p-dsoi

Integration-type sensor - INTPIX8 (FY14-1)

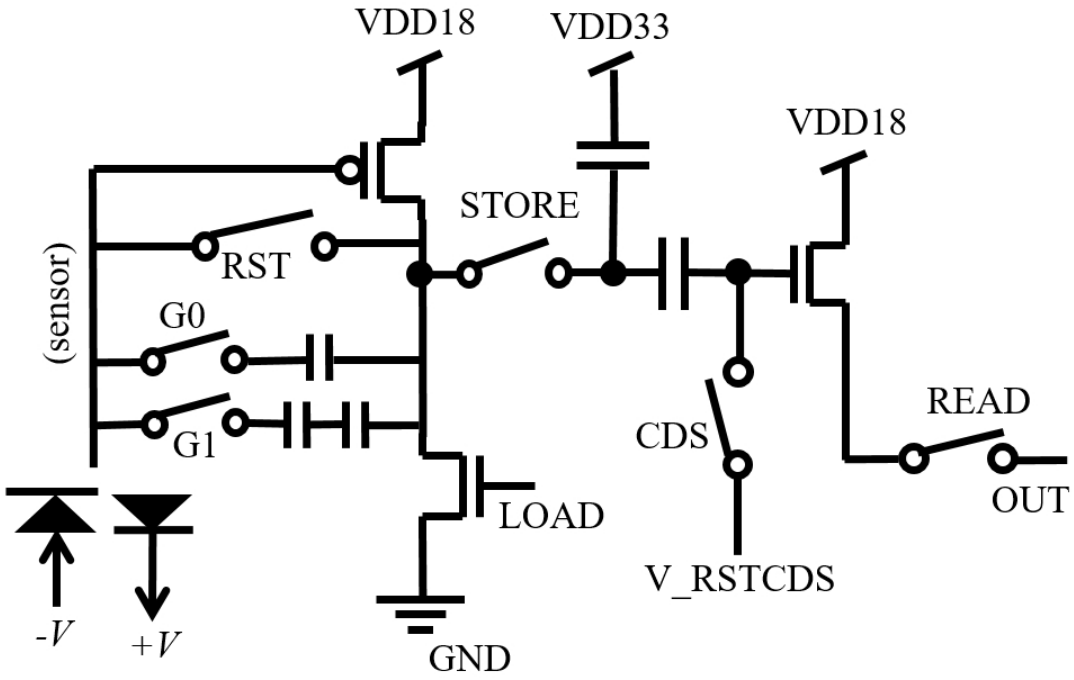


Double SOI (Cz-p) 300 μm
Single SOI (FZ-p) 500 μm

Low gain mode G0,G1 off
High gain mode G0,G1 on

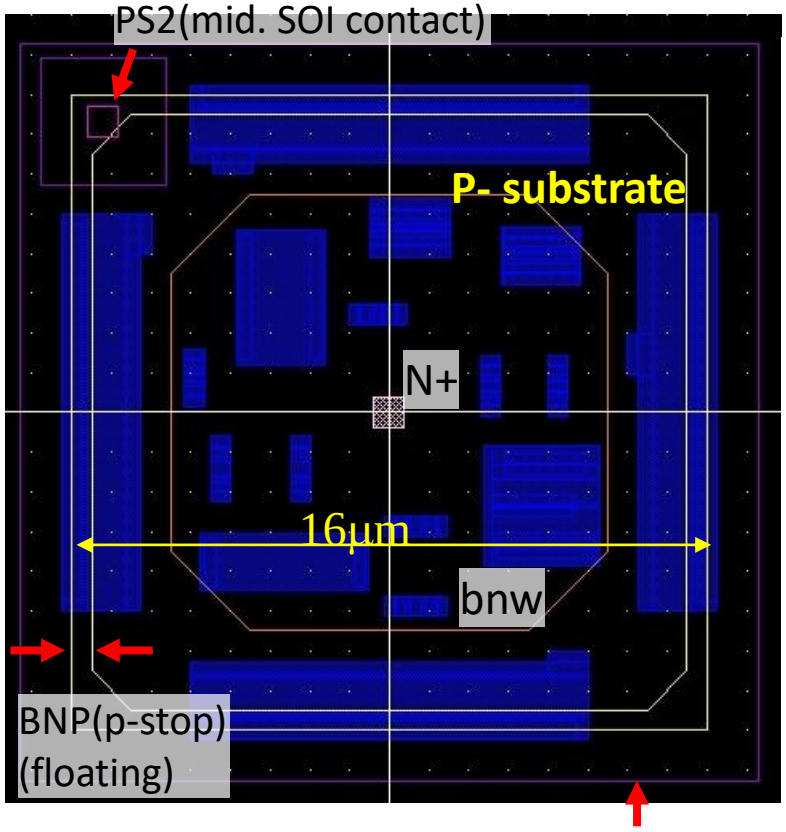


Pixel layout 16 μm x 16 μm

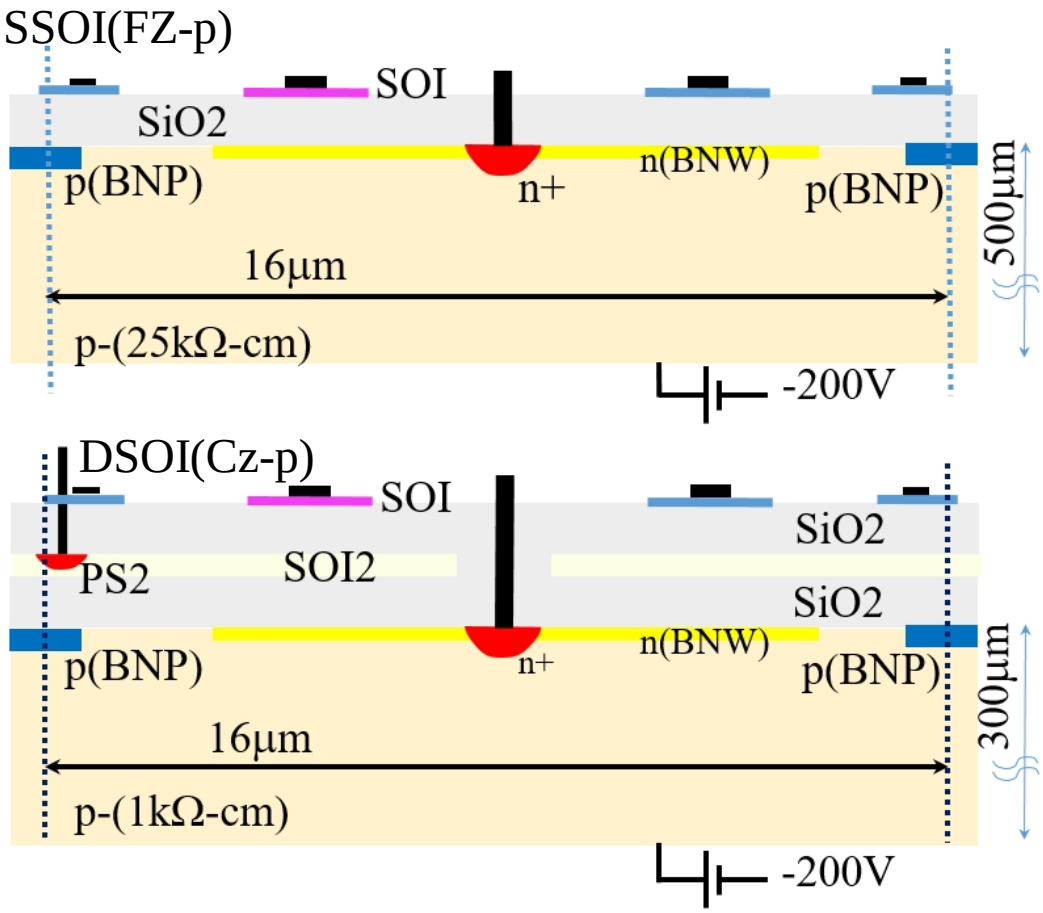


Pixel circuit

Integration-type p-type SSOI/DSOI sensor - INTPIX8 (FY14-1)



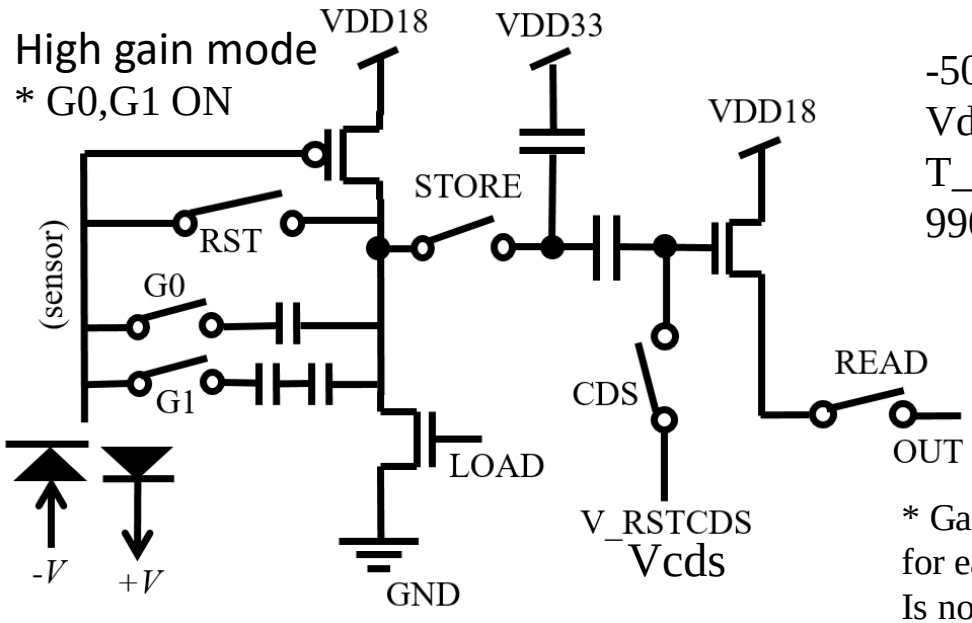
Top view



Side view

Am-241 spectra by p-type SSOI/DSOI INTPIX8

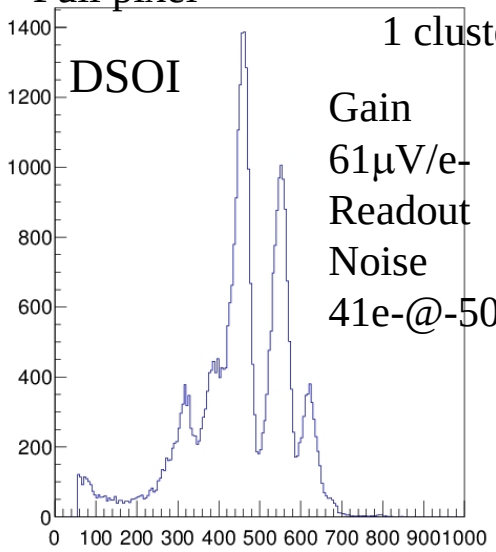
High gain mode
* G0,G1 ON

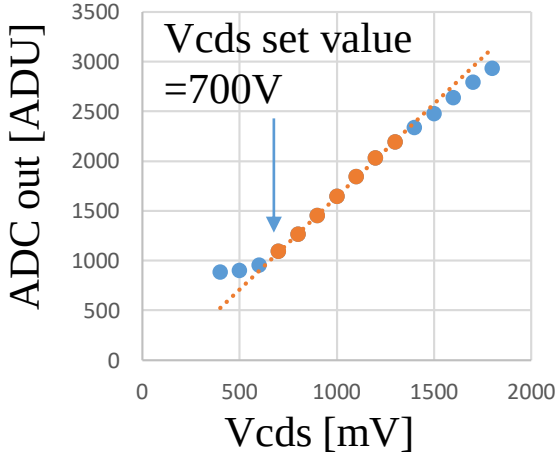


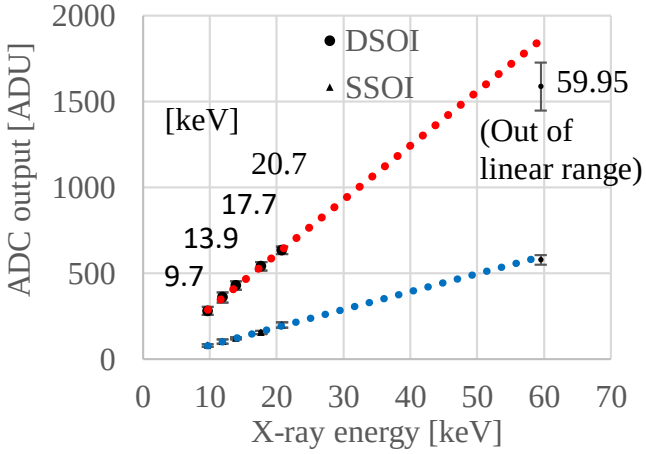
-50deg.C
Vdet=-200V
T_integ=0.5ms
9900 frames

* Gain correction
for each pixel
Is not done

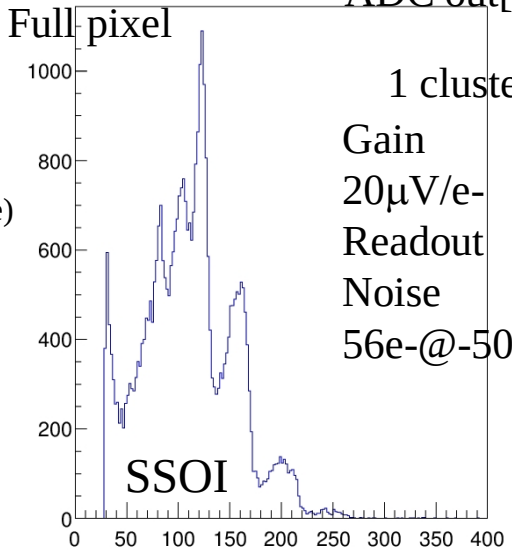
Full pixel





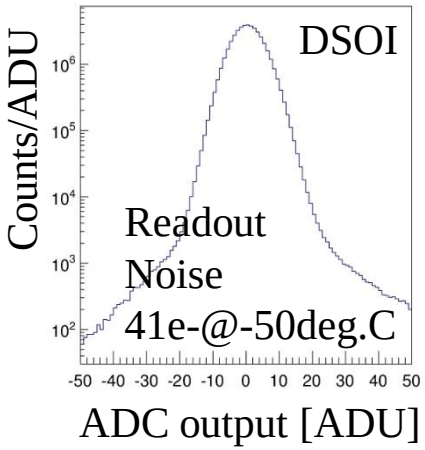


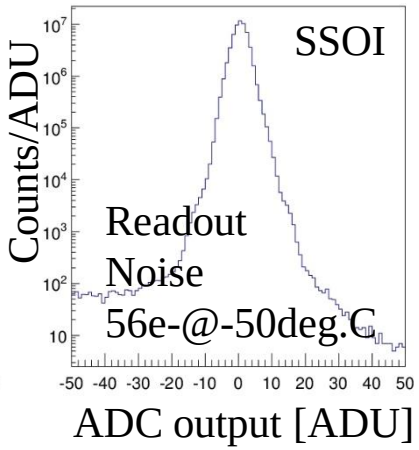
Full pixel



* IIN1=10mA, IIN2=7mA, IINABUF=36mA

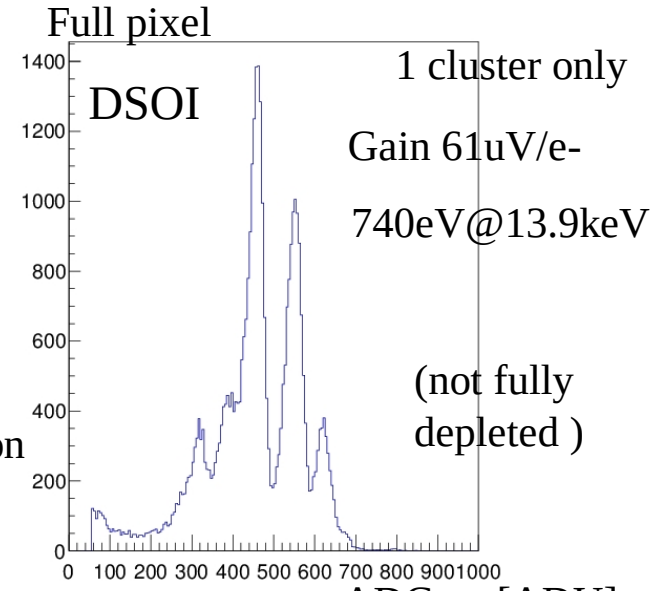
Am-241 spectrum by p-type SSOI/DSOI INTPIX8

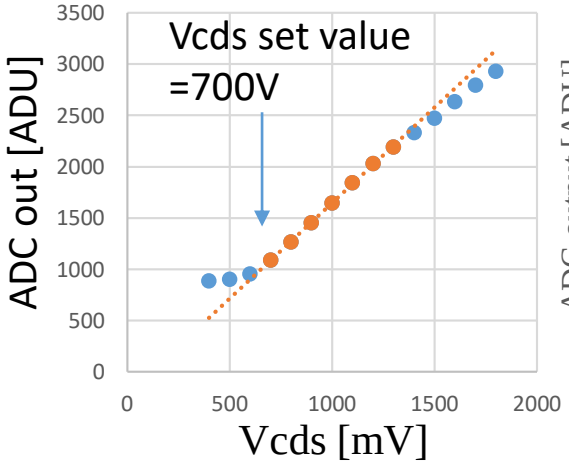


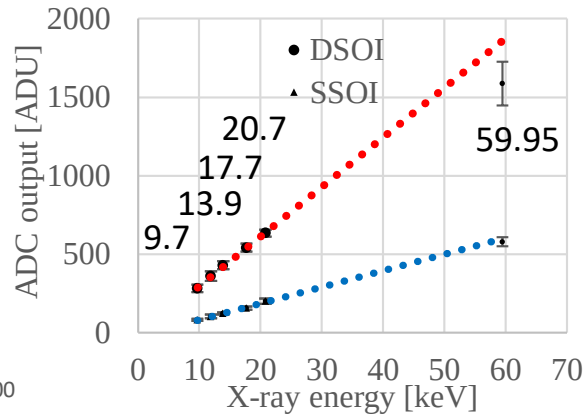


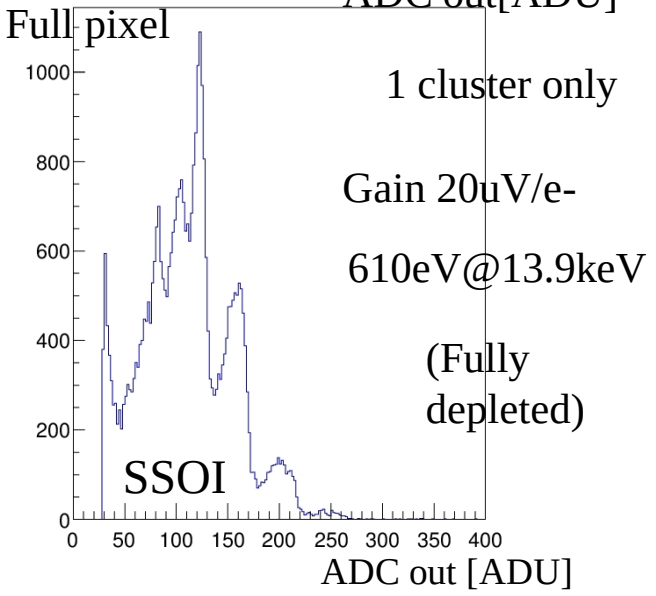
-50deg.C
Vdet=-200V
T_integ=0.5ms
9900 frames

* Gain correction
for each pixel
Is not done



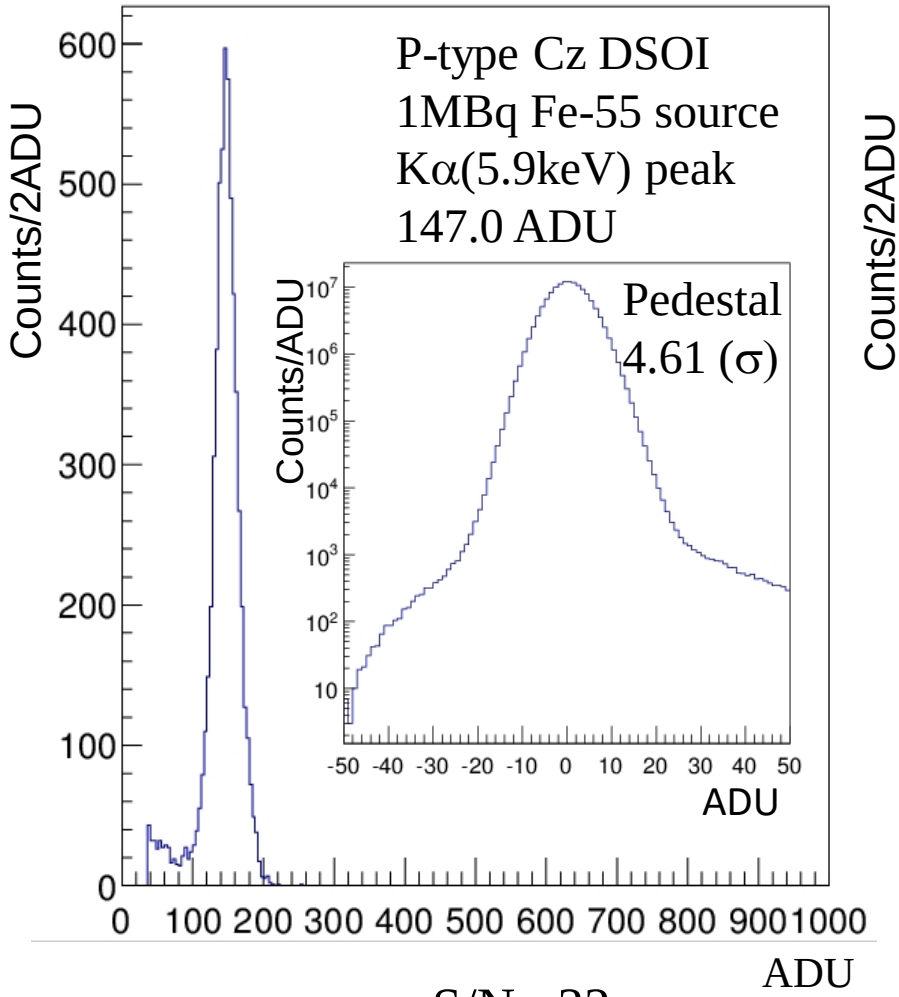




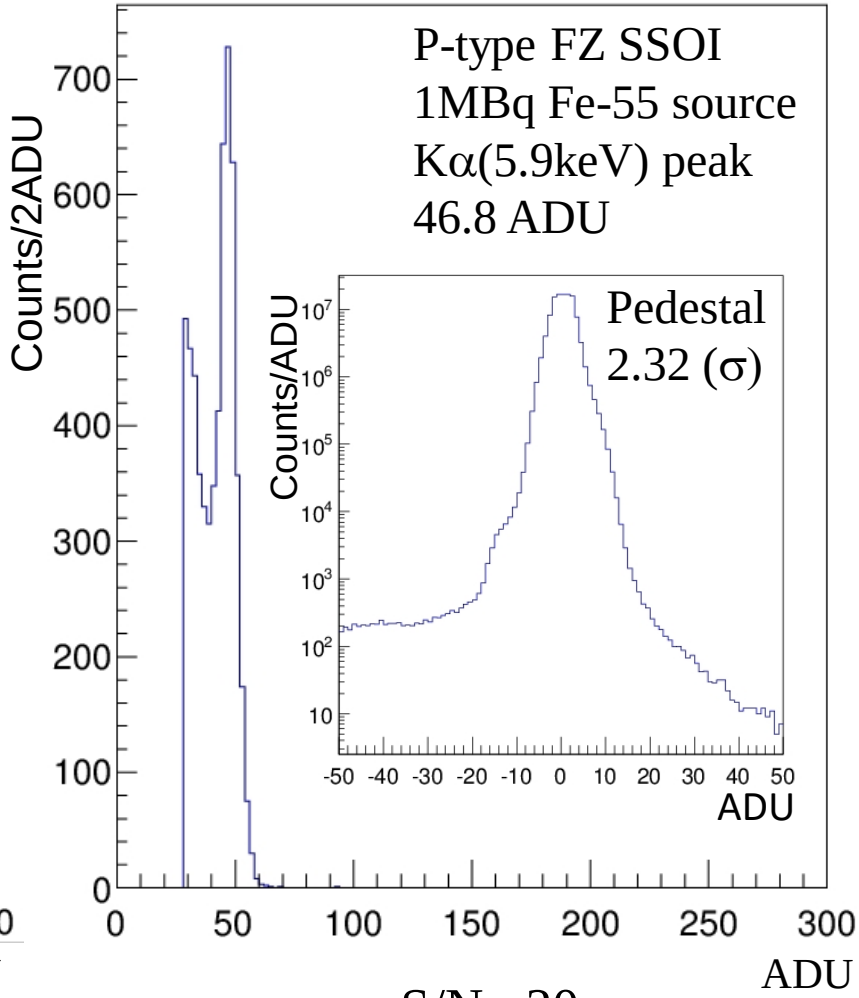


* IIN1=10mA, IIN2=7mA, IINABUF=36mA

Fe-55 spectra with high gain mode



S/N ~32

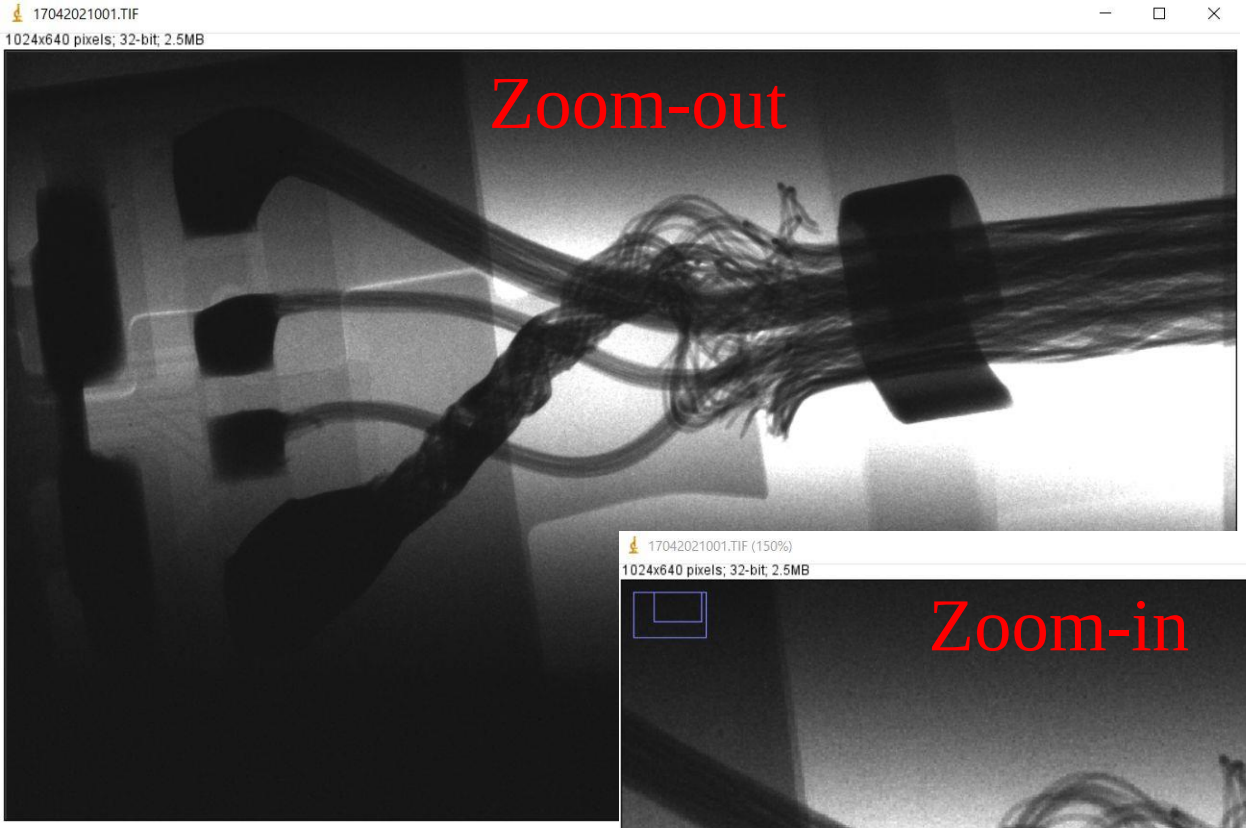


S/N ~20

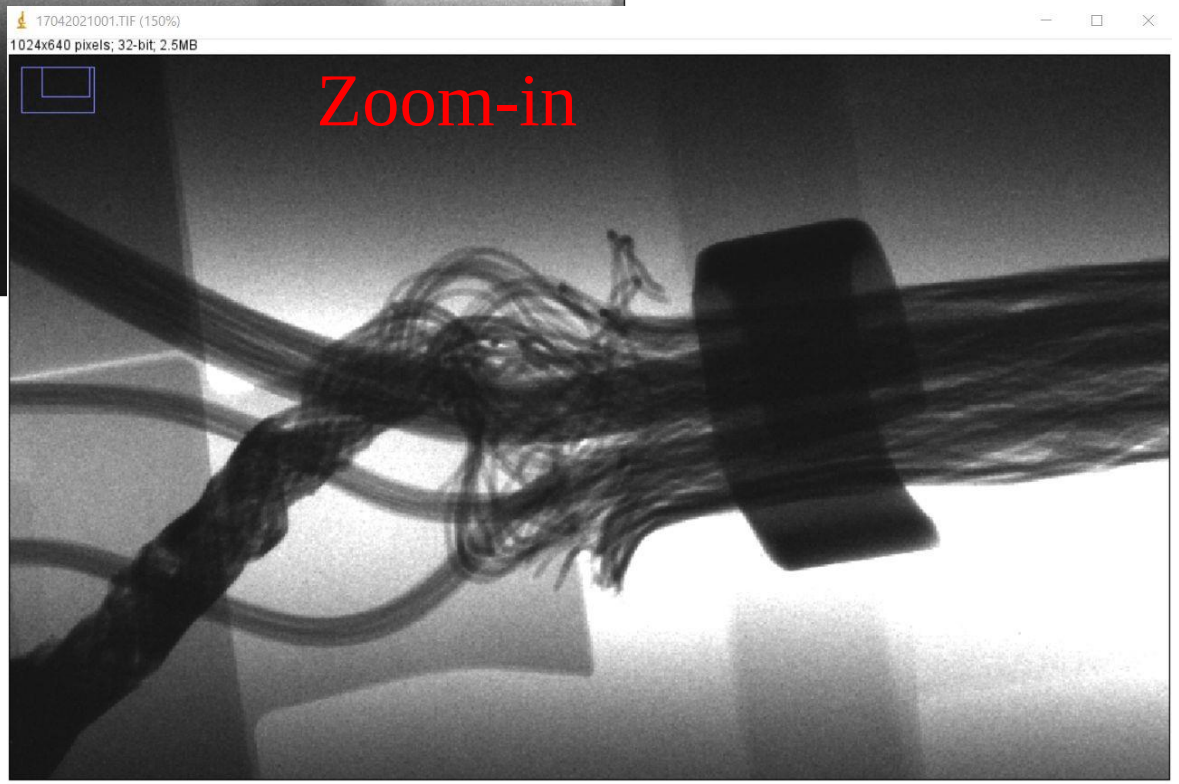
Tinteg.=0.5ms,Vsensor=-200V, -50deg.C

Demonstration of X-ray imaging

Preliminary
Confidential

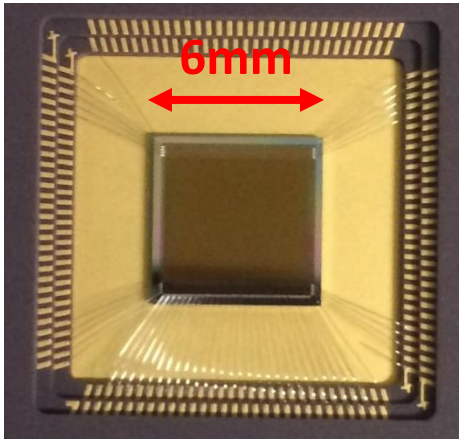


INTPIX8
Low gain mode
40 keV Monochro. X-ray
1ms x 500 frame
KEK PF-AR NE-7A
Beam size 40mm(H) x 4mm(V)

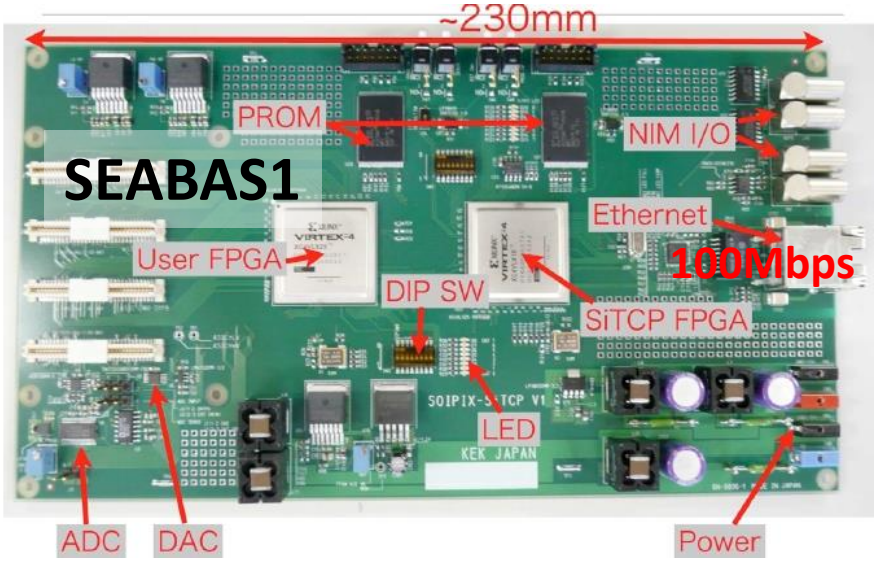


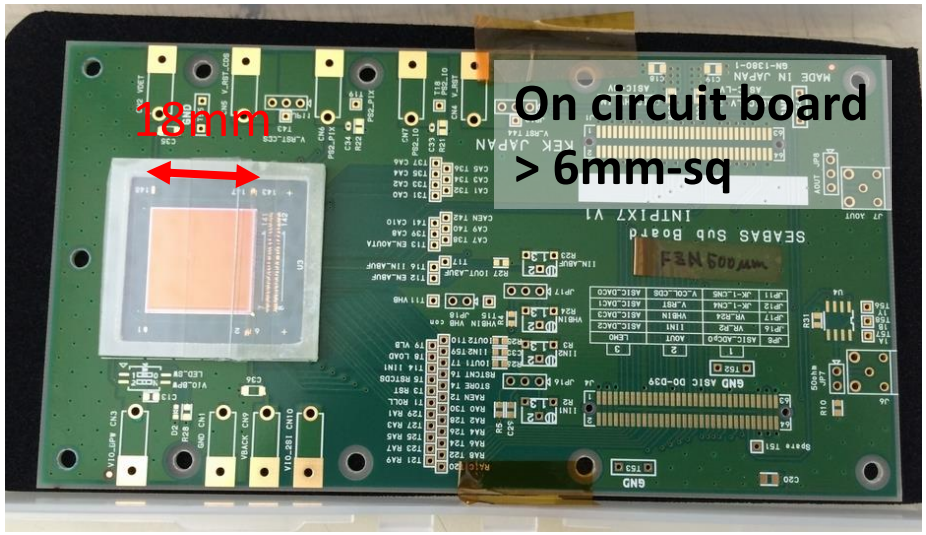
A well-known cable

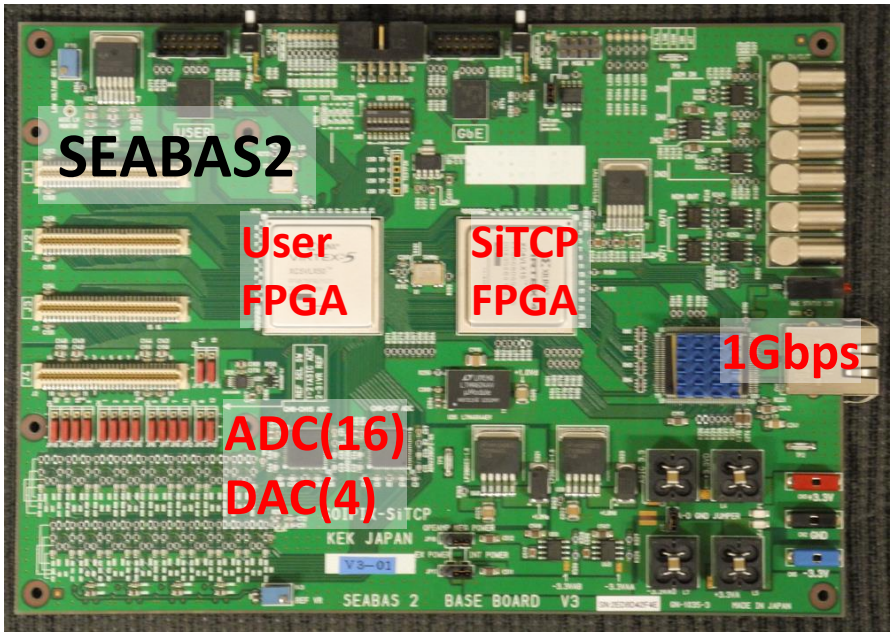
Sensor test and DAQ system



A package socket is mounted on a sub circuit board







DAQ system in the future

Existing DAQ system

SEABAS1 Vertex4

SEABAS2 Virtex4/5

~7,200 slices, BlockRAM ~2,160Kb

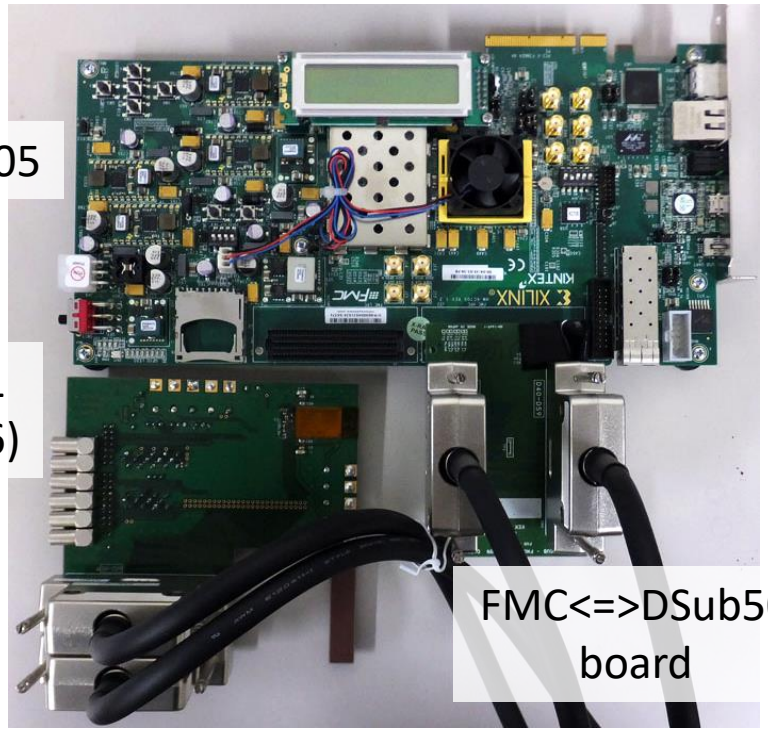
No DDR

Xilinx KC705 board (2017-)

- FPGA (Kintex-7)
- 50,950 slice, 16,020 Kb BlockRAM
- DDR3 memory
- Gb Ethernet, light fiber

KC705

CNPIX1
(FY2016)



CNPIX1-1kHz(1.7Gbps~)

SEABAS3 with Kintex-7 & DDR3 memory & 10 Gbps? (~2018?)

Summary & Future prospect

Integration-type pixel sensor with single/double SOI wafer
w./o. storage capacitor --- FPIX series: pixel size > 8 um
w. storage capacitor --- INTPIX series and more: pixel size > 12um
New counting type pixel sensor with double SOI wafer will be developed

Future prospect

Small pixel less than 8um? → active marge, 3D chip…

Optimization/modification of storage capacitor
1.5fF/um2 → larger capacitance per um2

Readout board upgrade (go to 10 Gbps?)

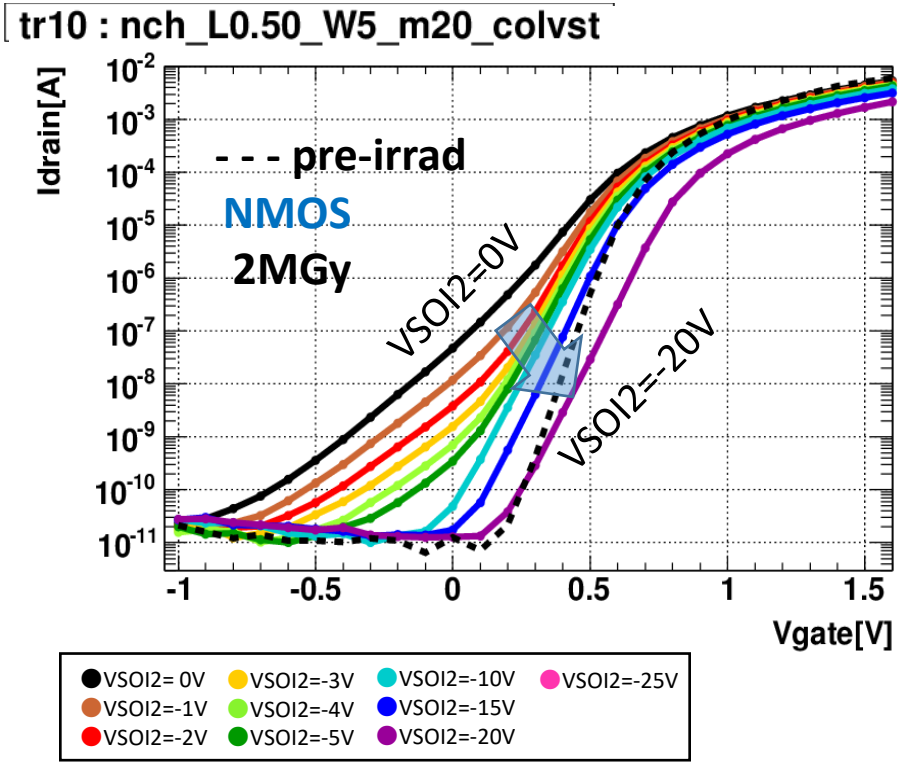
Integration-type pixel sensor with column ADC (DIPIX2?)

High resistivity p-type double SOI integration-type pixel sensor (INTPIX8)

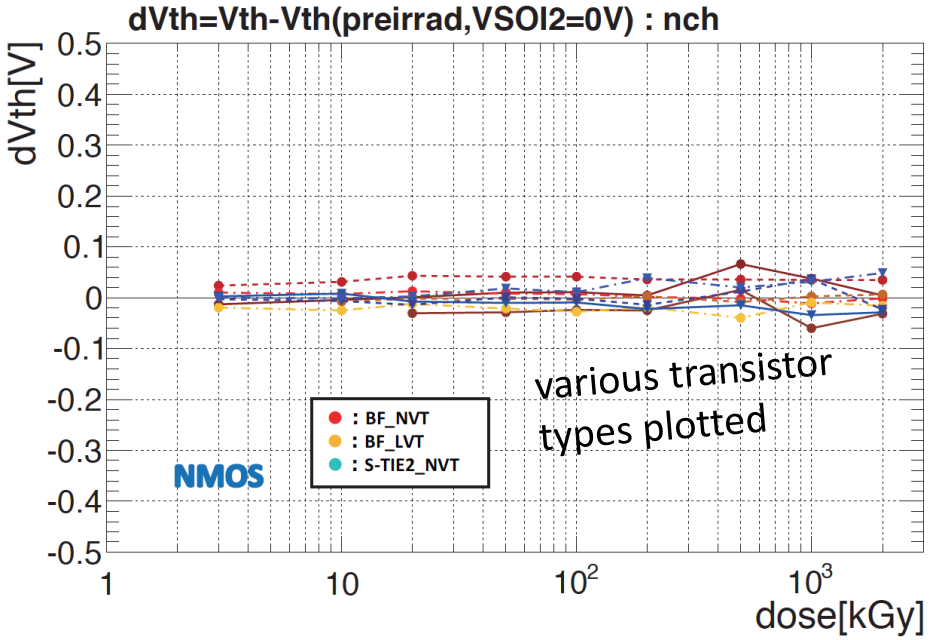
supplement

FET threshold shifts and compensation in DSOI

IV curves of an NMOS (2MGy irradiated) with Changing VDSOI2



Residual of Vth shifts of various FET types (FETs grouped into 3 in VSOI2 setting)



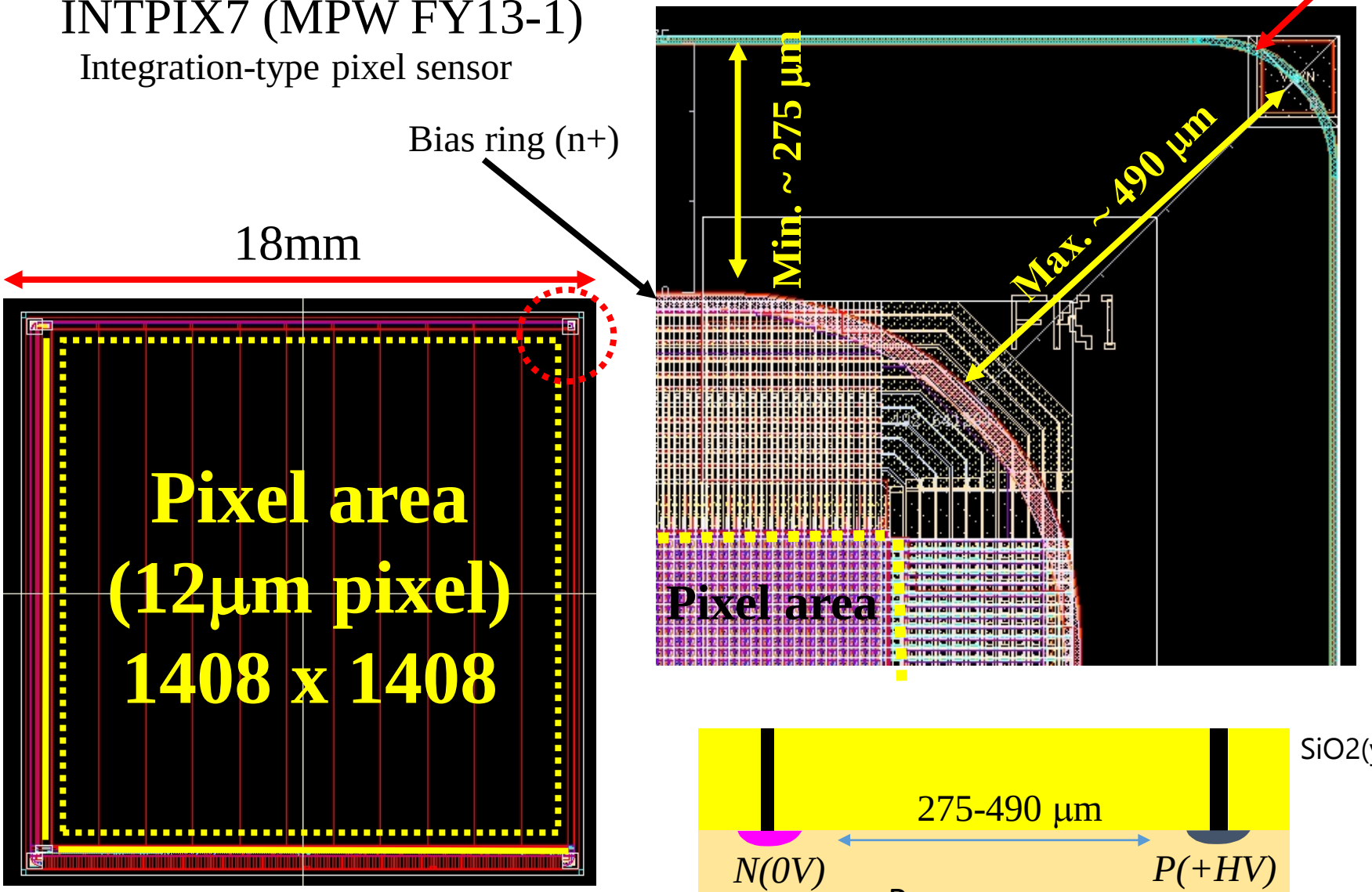
S. Honda et al., “Total Ionization Damage Compensations in Double Silicon-on-Insulator Pixel Sensors”, PoS (TIPP2014)039.

K. Hara et al., ”Initial Characteristics and Radiation Damage Compensation of Double Silicon-on-Insulator Pixel Device,”, PoS(VERTEX2014)033.

An example of Sensor layout

INTPIX7 (MPW FY13-1)

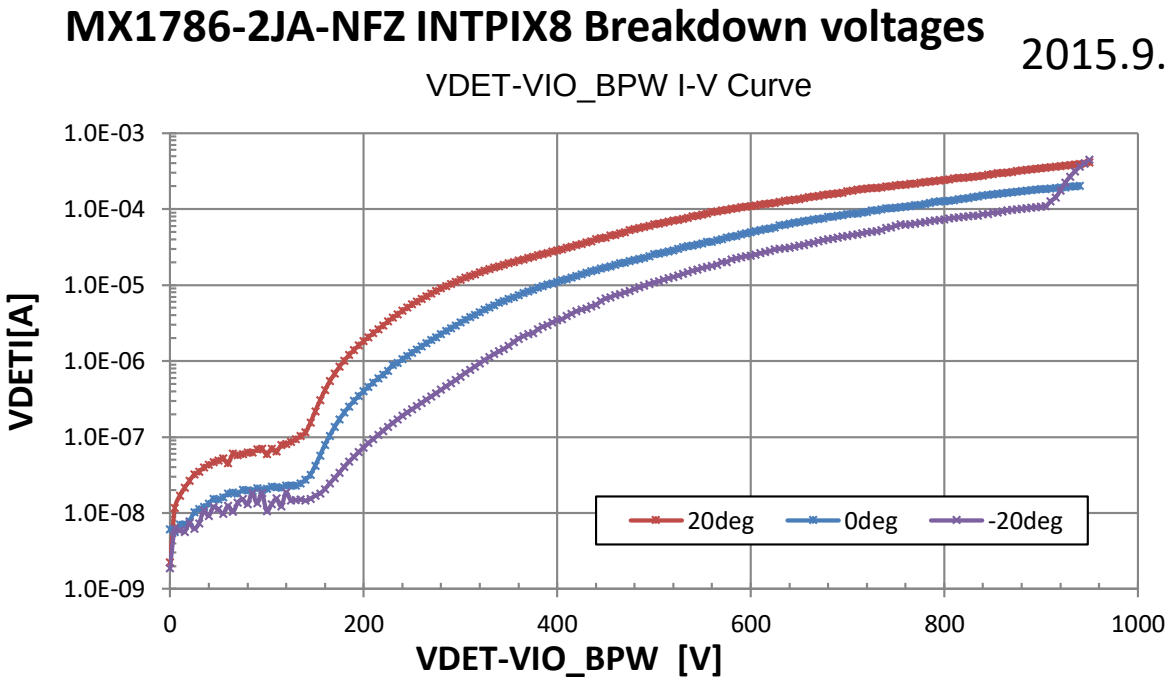
Integration-type pixel sensor



Breakdown voltage ~ 600 (Max.)

Enge of the chip (side view)

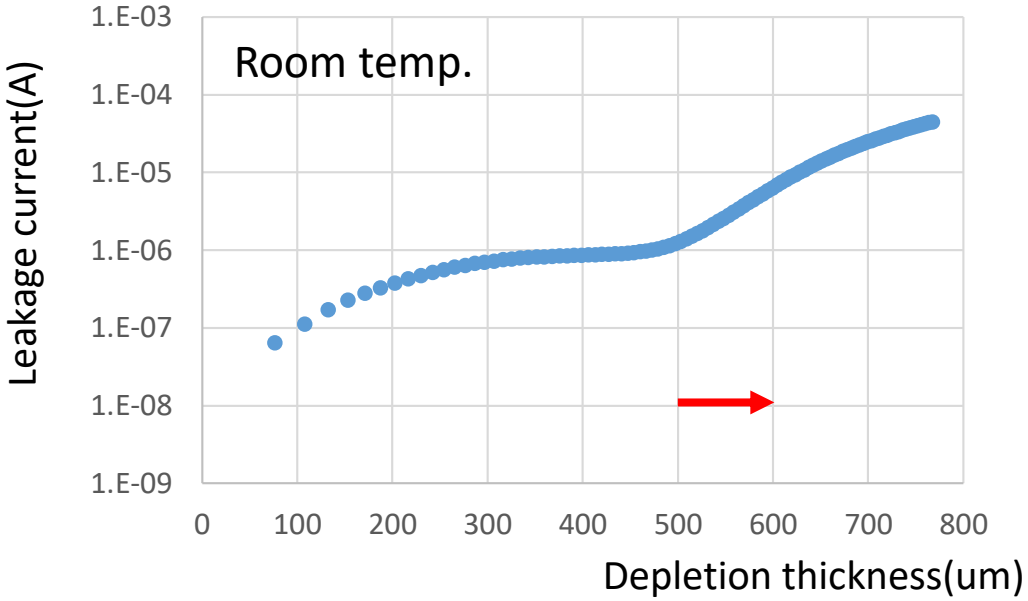
Maximum (?) breakdown voltages



Operation voltage is typically less than 400V
After high voltage more than 900V, the sensor got non-recoverable damage.
Therefore we don't repeat this study yet.

I-V curve vs depletion thickness

NFZ-INTPIX8
5 kOhm cm
Sensor thickness 500 um
Curve slope changes at over-depletion point



P-type DSOI INTPIX8
1kOhm cm
Sensor thickness 300 um

Breakdown voltage
~ -450V
Not fully depleted