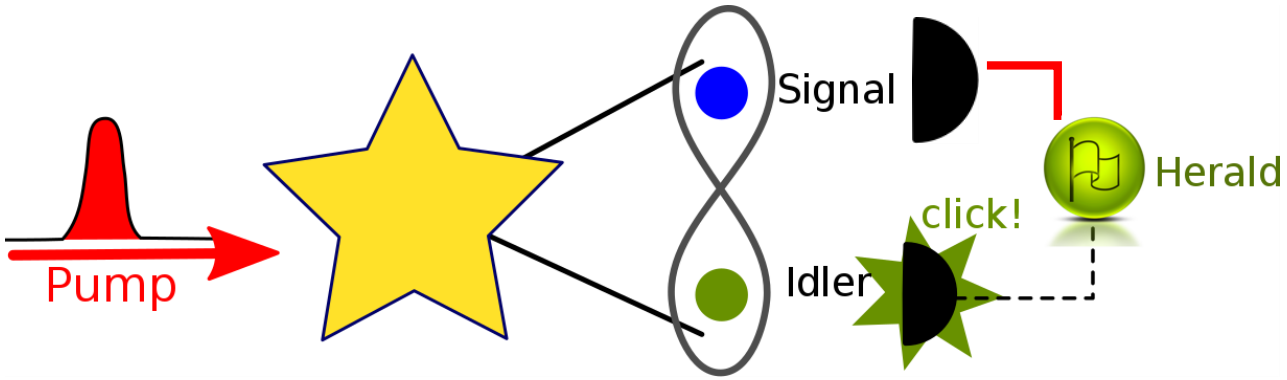
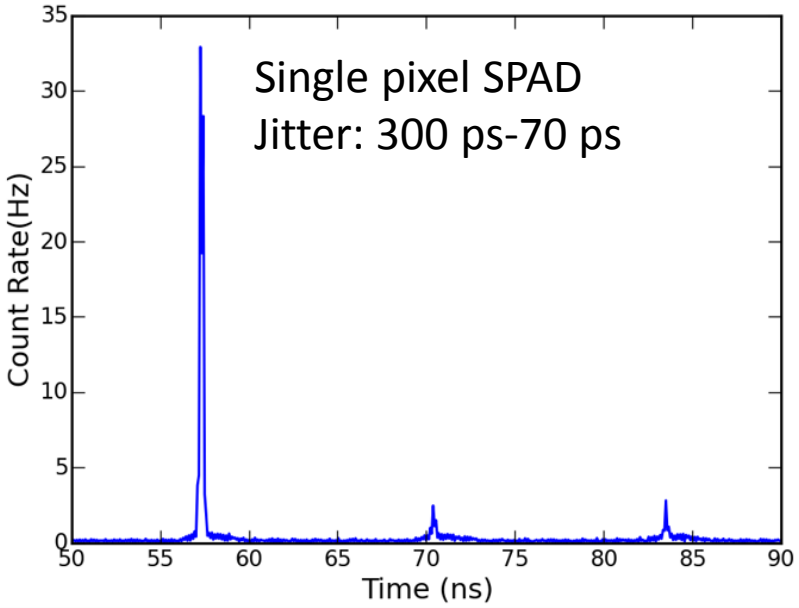
Institut de Physique de Nice

Time measurements in quantum optic

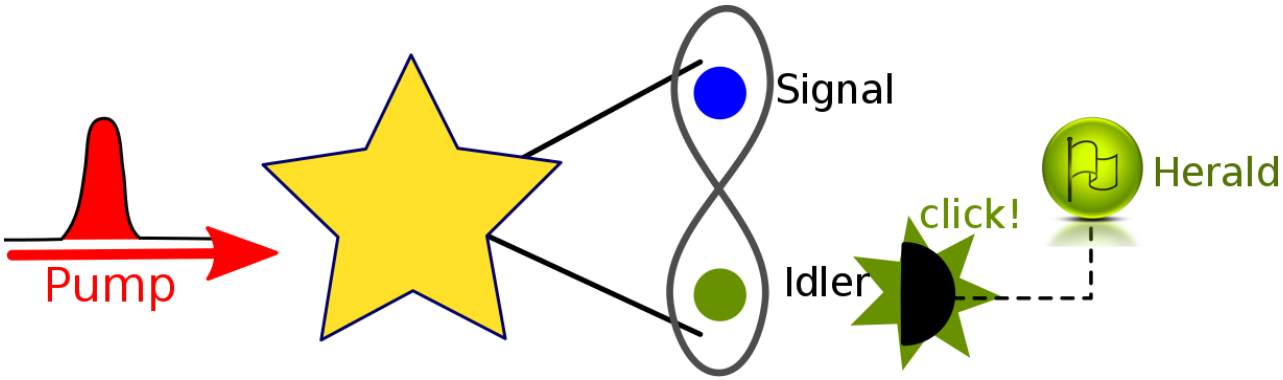
Table ronde TDCs
17/05/2017

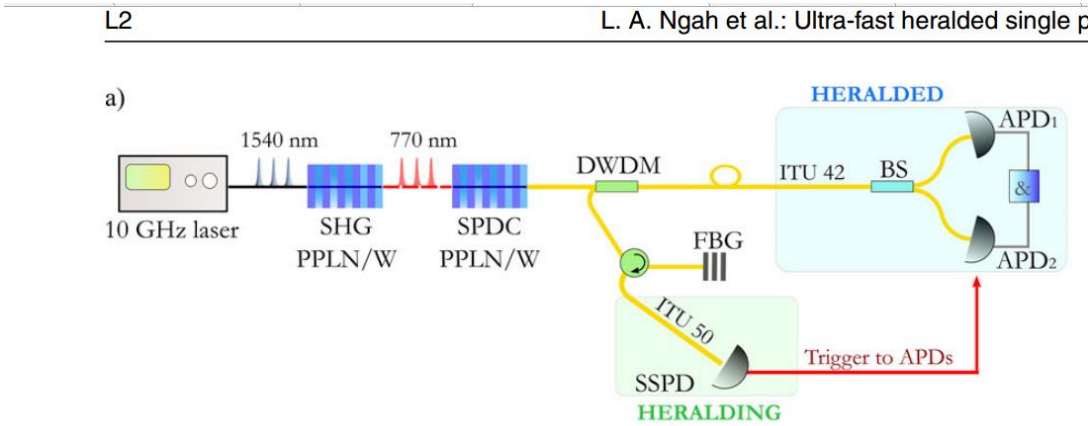
Resolution



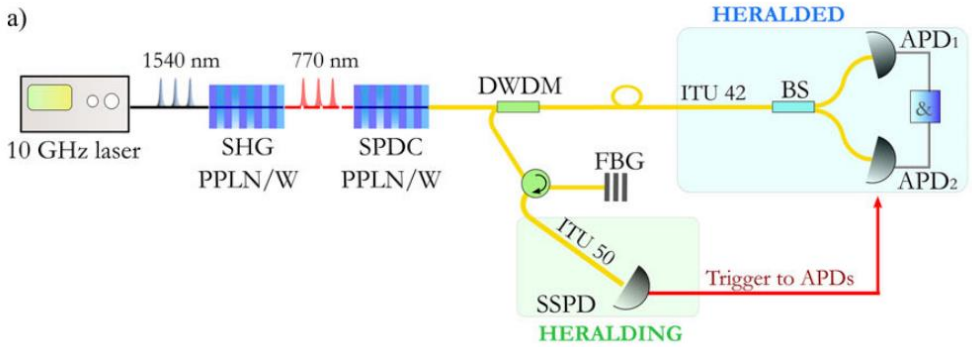


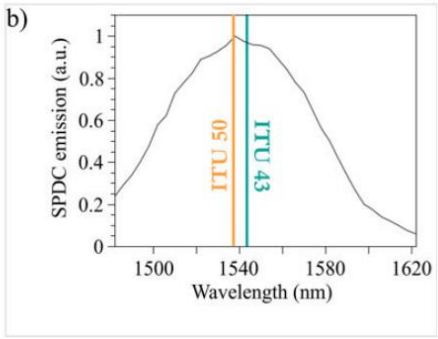
Channel count rate

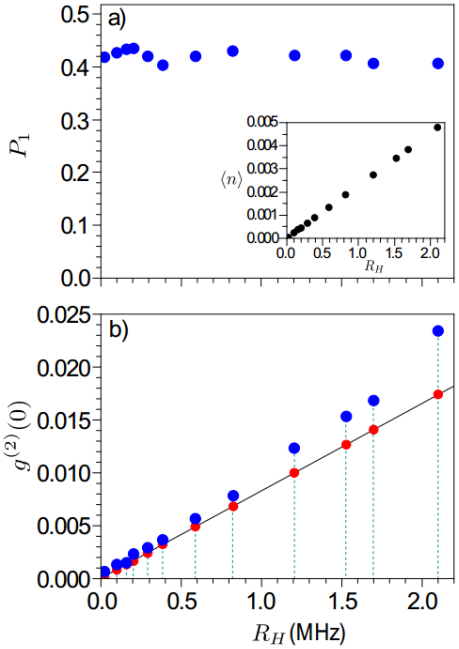


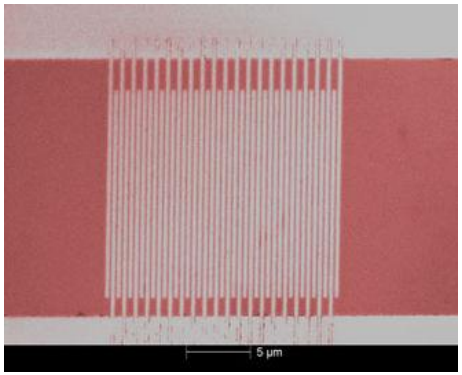


Channel count rate & modularity









15 MHz-> 100 MHz

What we are looking for..

	PicoQuant300	ID801	
Resolution	12 ps	81 ps	30 ps-50 ps
Number of Channel	2	8	16
Max count rate (channel)	5 MHz	10 MHz	>15 MHz (100 MHz ??)
Output	USB2.0 Time tagging	USB2.0 Time tagging	Time tagging Triple-Four coincidence Programmable Logic
			FPGA

How?

A 19.6 ps, FPGA-Based TDC With Multiple Channels for Open Source Applications

Matthew W. Fishburn, *Student Member, IEEE*, L. Harmen Menninga, Claudio Favi, and Edoardo Charbon, *Senior Member, IEEE*

***Abstract*—This work presents a multi-channel, time-to-digital converter (TDC) based on a field-programmable gate array (FPGA). A thorough characterization of the TDC, based on a Xilinx Virtex-6 FPGA, is presented and several performance parameters are described, including distortions due to the FPGA architecture, temperature effects, intra-chip position variation, and chip-to-chip variation. An optimized TDC exhibits 10 ps LSB duration, an integral non-linearity range of 3.86 LSB, and an**

different FPGA platforms—implemented systems are portable. Compared to full-custom chips, FPGAs have advantages in flexibility and development time. FPGAs are designed for parallelism, which makes them applicable for multi-channel and high throughput systems. However, FPGA-based TDCs are limited by the FPGA's pre-defined structure.

An open source initiative to apply FPGA-based systems in