DE LA RECHERCHE À L'INDUSTRIE

cea

TDC multicanal pour mesure du temps d'arrivée.

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Irfu

Institute of Research into the
Fundamental Laws of the Universe

SEDI

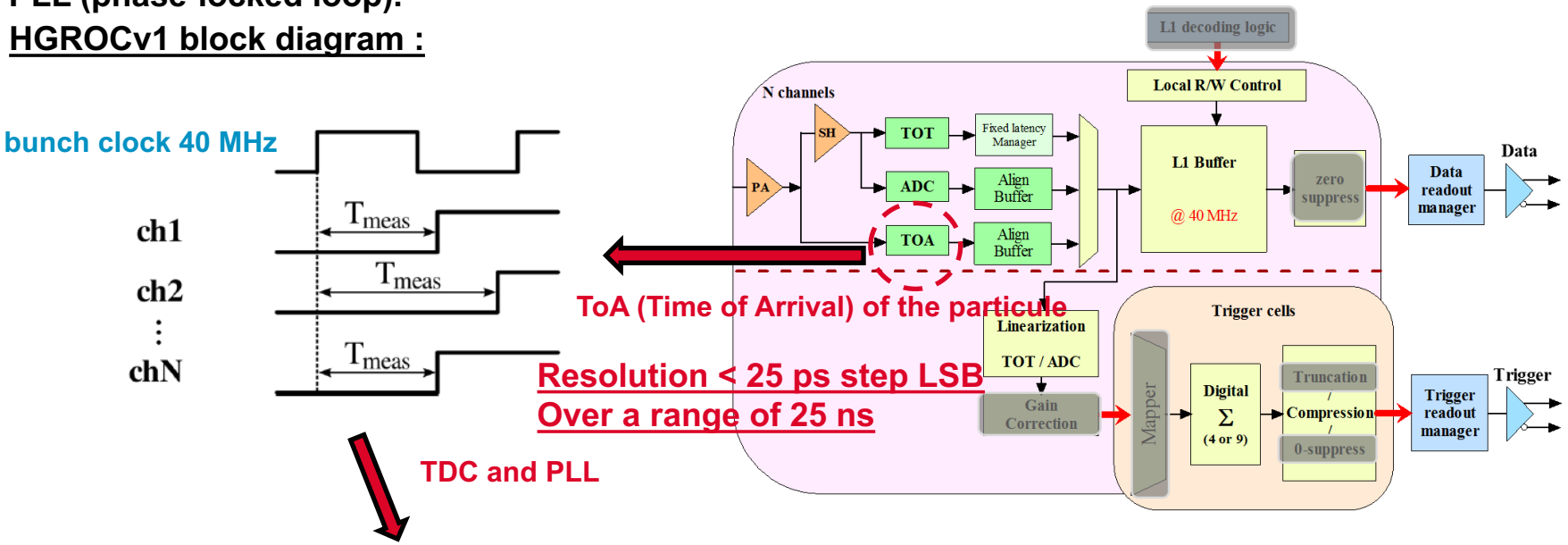
Time Of Arrival pour HGCAL

Type(s) de TDC(s) réalisé(s)	Pulse train amplifier
Type d'intégration: ASIC ou FPGA	ASIC
ASIC dédié TDC ou TDC intégré dans ASIC front-end	TDC intégré dans ASIC front-end
Nombre de voie(s)	32 (64 ou 72 visés)
Technologie (pour les ASICs)	TSMC 130nm
Gamme dynamique en temps	1,6 µs
Résolution temporelle - Pas de quantification: simulés et mesurés	11 bits, LSB=12.5 ps Simulé.
Taux de comptage / temps mort individuel	40MHz (11 bits)
Consommation par voie	2mW. Ne consomme qu'en cas d'événement
Type de discriminateur utilisé, (selon) jitter, walk	

CONTEXTE

Collaboration between **OMEGA and IRFU** in end 2016 resulted in IRFU's involvement in the design of a **fast multi-channel TDC (time to digital converter) for the ToA (Time of Arrival) and its associated PLL (phase-locked loop).**

HGROCv1 block diagram :



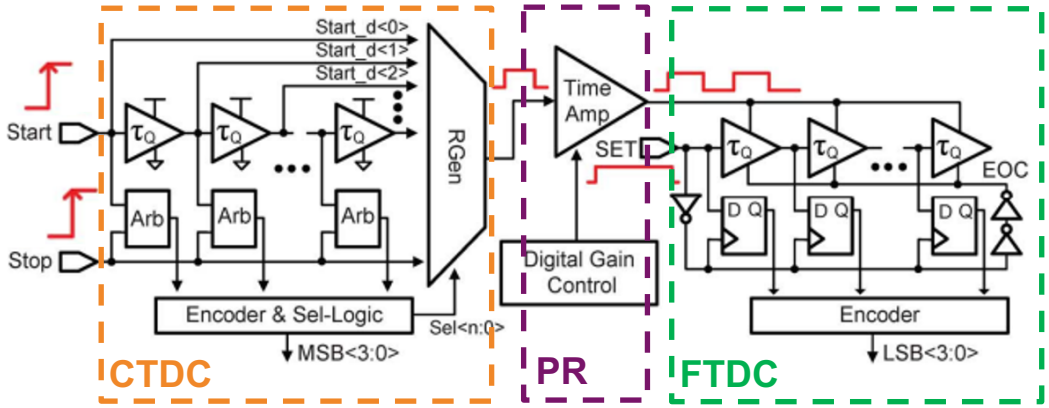
TDC (time to digital converter) for **ToA** of large-scale systems with many channels:
Measure the “relative" phase of an event with respect to the input bunch clock at 40 MHz.

PLL (phase-locked loop) will provide an internal clock in the chip with multiples frequencies, less noisy and in phase with the external bunch clock in order to have a more precise **time to digital conversion**.

TDC specifications	
Resolution	< 25 ps step LSB
Bits	10 bits (over 25 ns)
Conversion rate	> 40 MHz (bunch clock)
Power consumption	< 2 mW / channel
Area	Small for multichannel
Technology	TSMC 130 nm
Temperature	-30 °C

CHOICE OF TDC ARCHITECTURE OPTIMIZED FOR FE HGCAL

New "Two-step" architecture incorporating a **pulse train amplifier** designed and tested by [KwangSeok Kim] in 2013 :



How it works ? : Kim publication

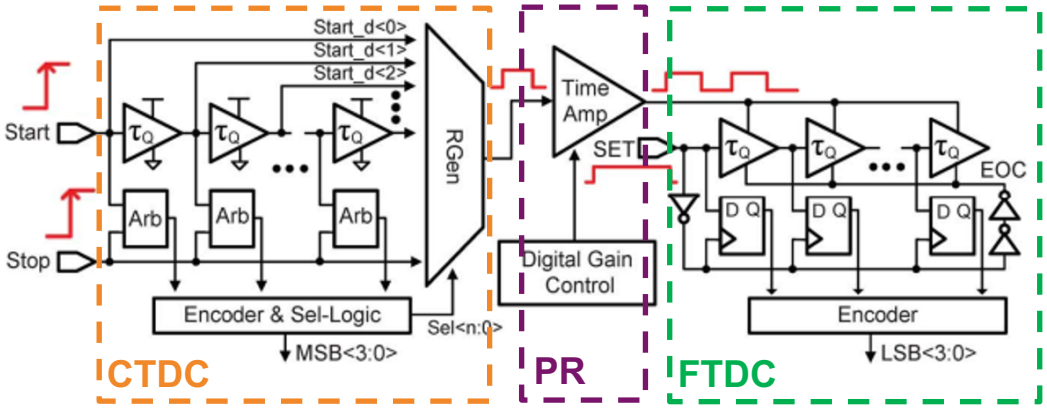
- **1st conversion step** called **Coarse TDC (CTDC)** ➔ classical **DLL (Delay-locked loop) line** (4 most significant bits) according to a START bit and STOP bit.
- **The stop signal is flashed** and the residue of this conversion between the last DLLs of the CTDC need to be interpolated by using a **Pulse Replicator (PR)**.
- This residual pulse train is sent to a **residue integrator called Fine TDC (FTDC)** based on a **DLL** line (3 LSBs)

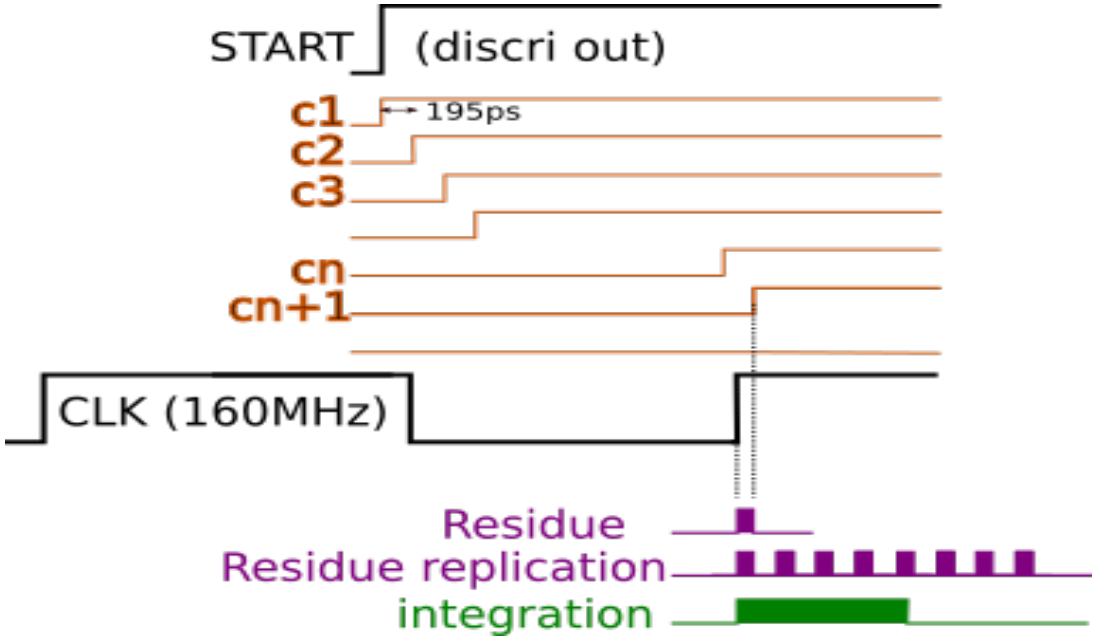
Advantages : high speed conversion and low power consumption
Weaknesses : not controlled in terms of process, mismatch, temperature ...

Improvments in our chip :
- Increase the time range by **adding a counter**
- keep performance under **temperature and process variations**

CHOICE OF TDC ARCHITECTURE OPTIMIZED FOR FE HGCAL

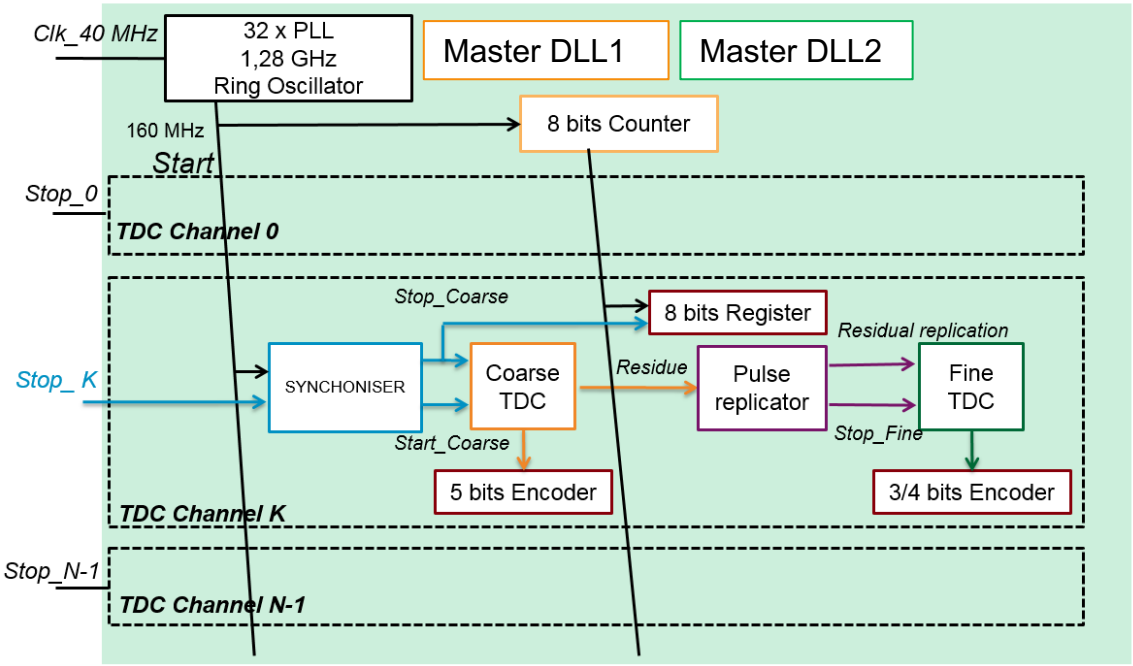
New "Two-step" architecture incorporating a **pulse train amplifier** designed and tested by [KwangSeok Kim] in 2013 :





MULTI-CHANNEL TDC ARCHITECTURE FOR THE TOA

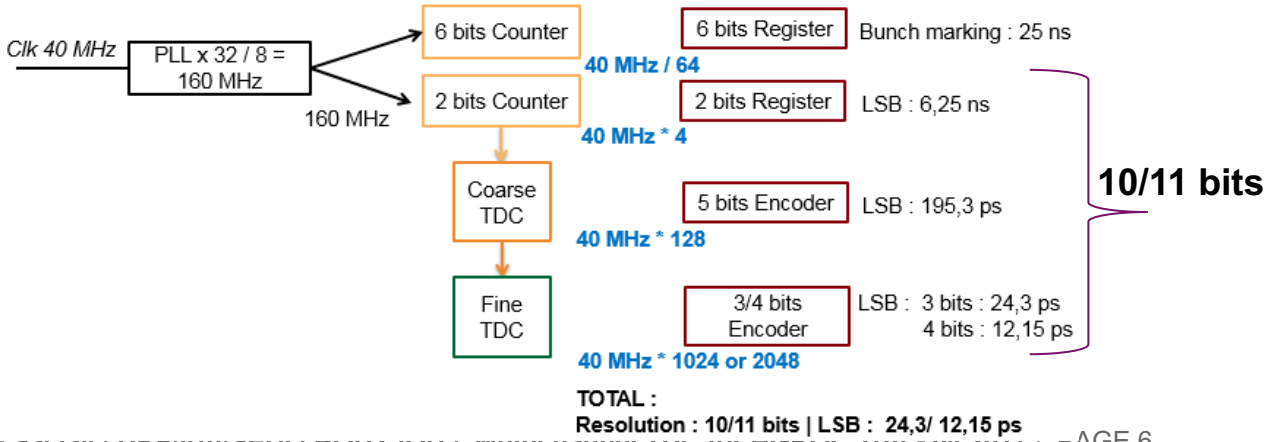
Multi-channel TDC architecture :



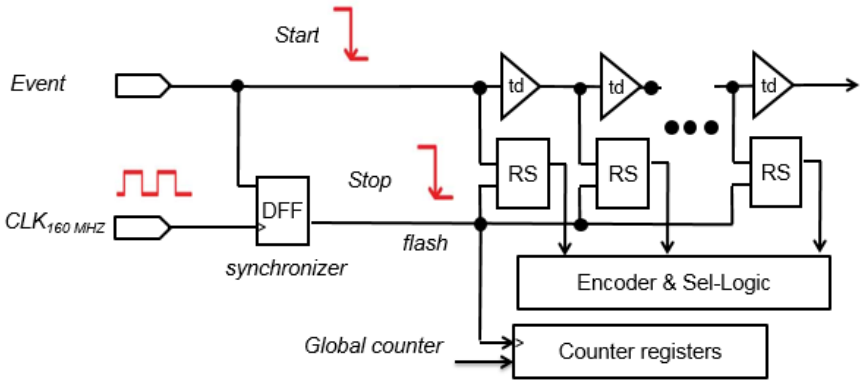
TDC resolution is increased by a counter
➔ the 2 most significant bits of the TDC are now obtained by an 8-bit **counter** operating at the CTDC frequency which is also a multiple of the 40 MHz bunch clock.

- 2 LSB bits for TDC MSBs
- 6 other bits for bunch marking.

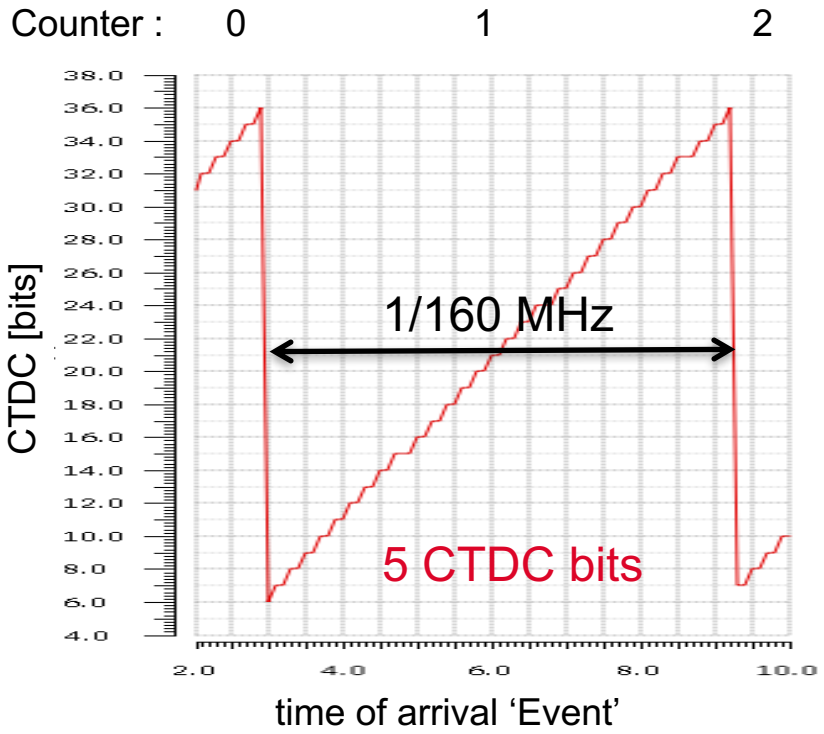
CTDC clock provided by internal PLL.



Clock synchronizer and CTDC :



Synchronizer + delay-line CTDC



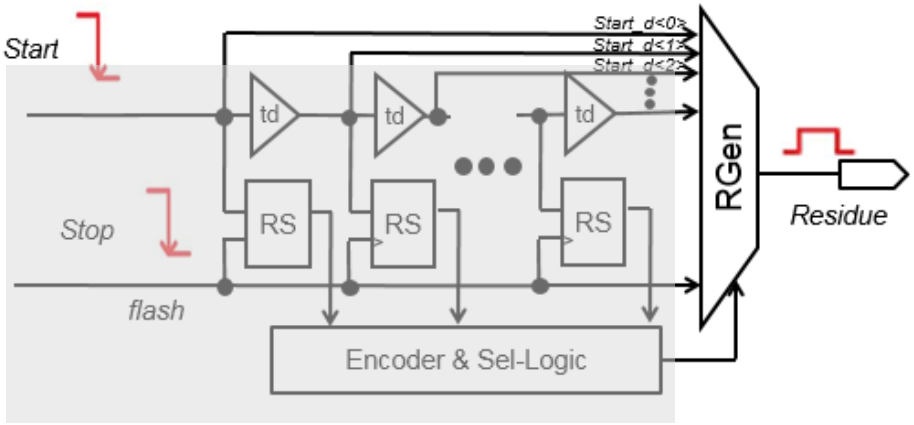
CTDC ENCODER CODE evolution for different time of arrival START_TDC between 2 and 10 ns and for CLK_PLL = 160 MHz

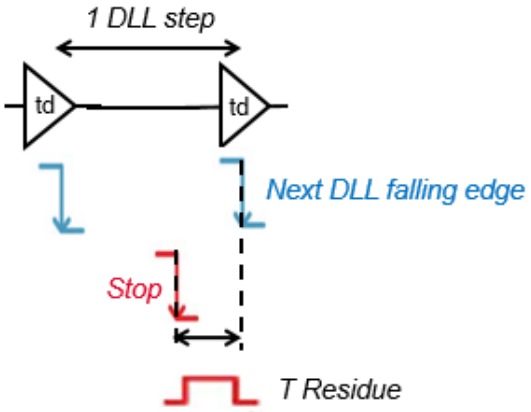
Warning : in this figure there is not enough simulated point to get a realistic estimation of the DNL and INL

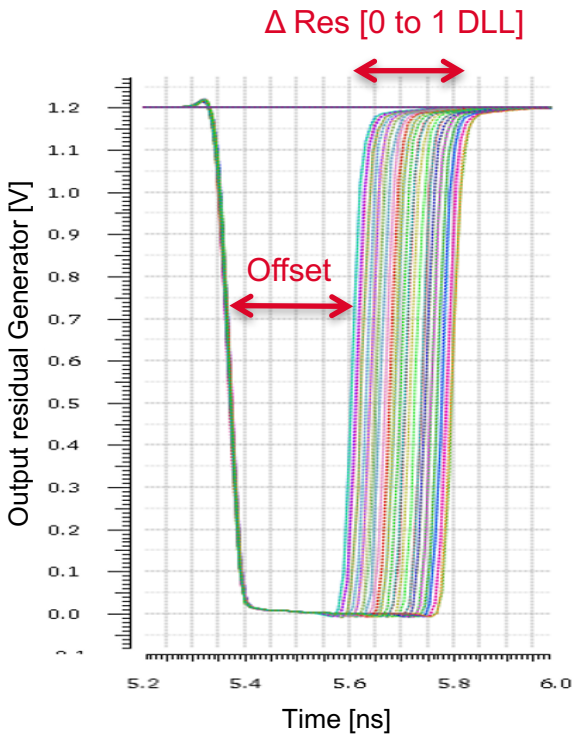
Power consumption only when an event arrives
CLK=160MHz (T=6.25ns)
Profondeur=32
LSB=6.25/32=195ps.

RESIDUE EXTRACTION

CTDC and Residue extraction :

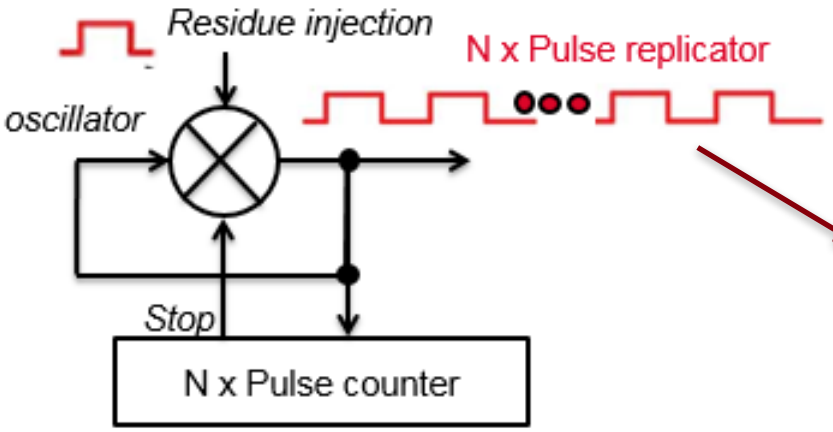


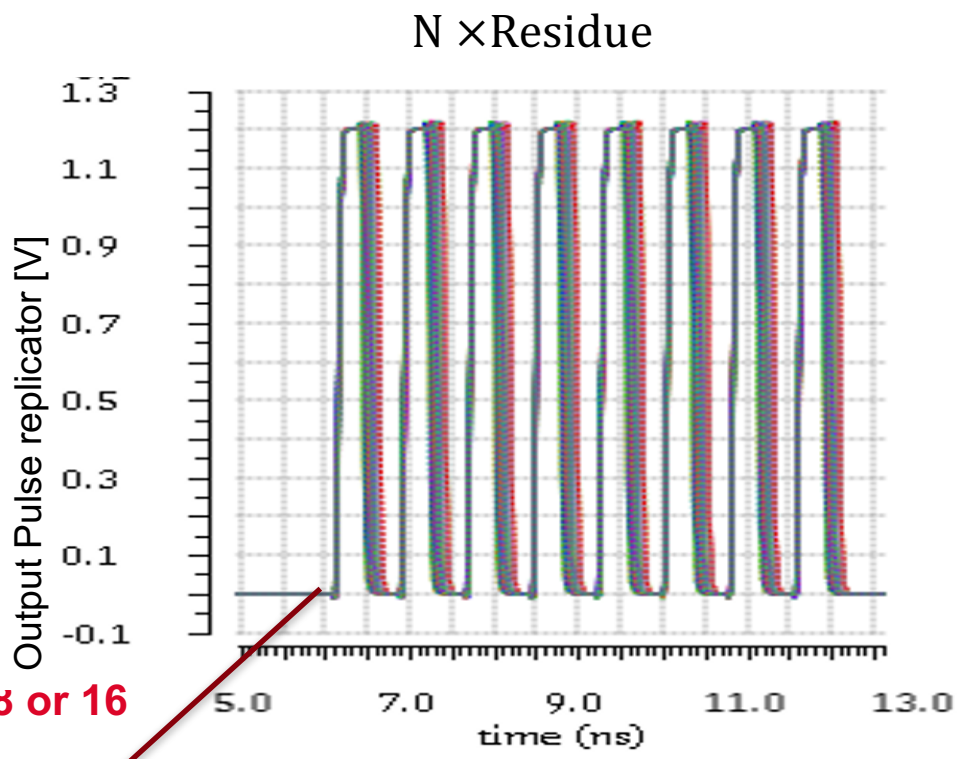




PULSE REPLICATOR

Pulse replicator :





Residue replication by 4, 8 or 16 (programmable)

Copy frequency : 1,37 GHz

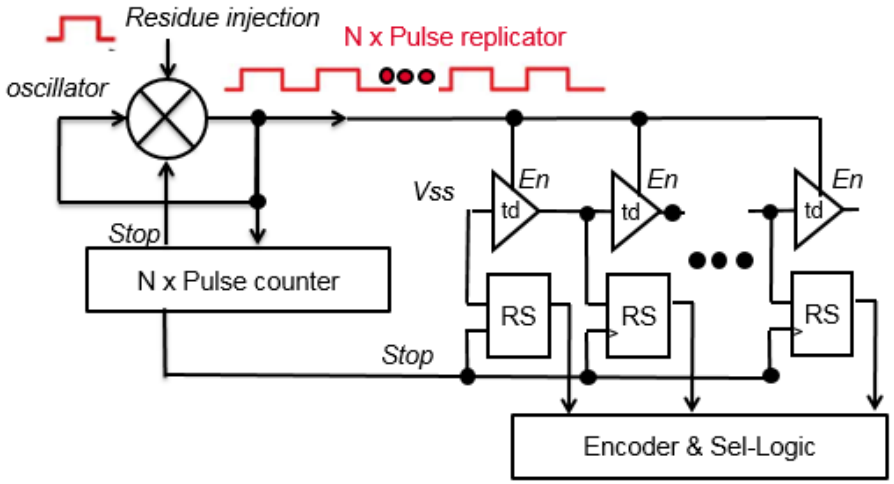
Total multiplication time :

Gain x 8 : 6 ns

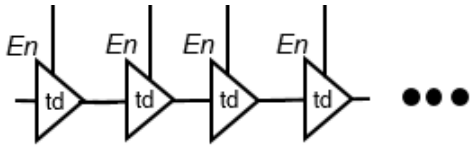
Gain x 16 : 12 ns

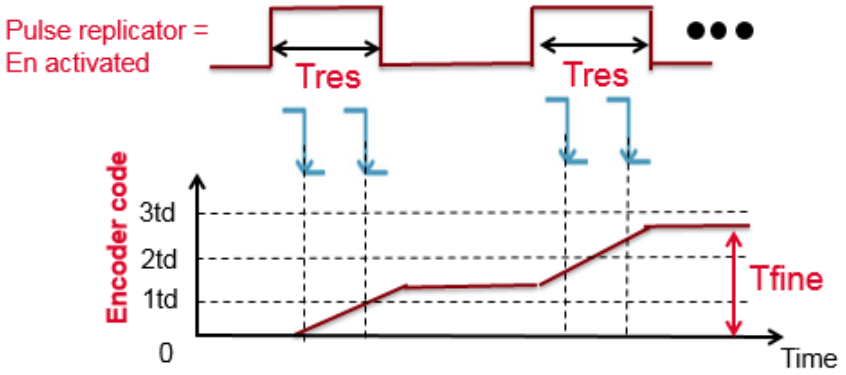
FTDC : RESIDUE INTEGRATOR

Residue integrator :

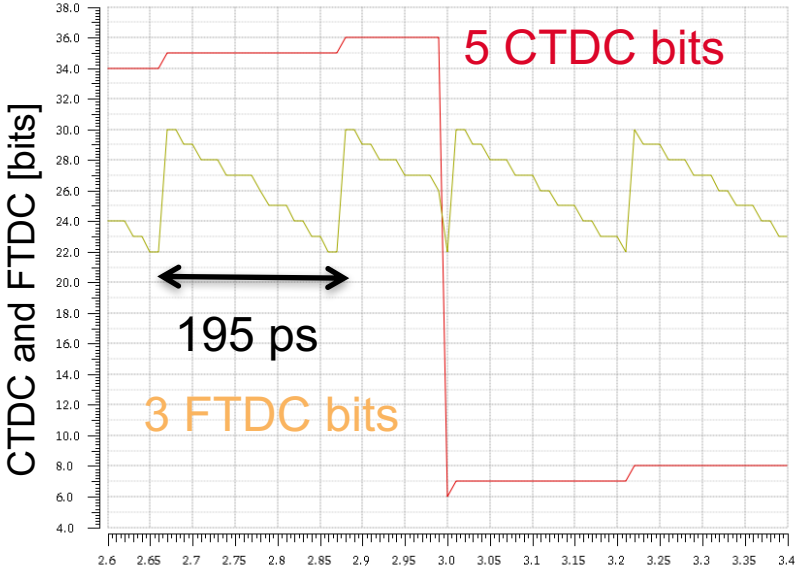


Pulse replicator + delay-line FTDC





Counter : 0 1



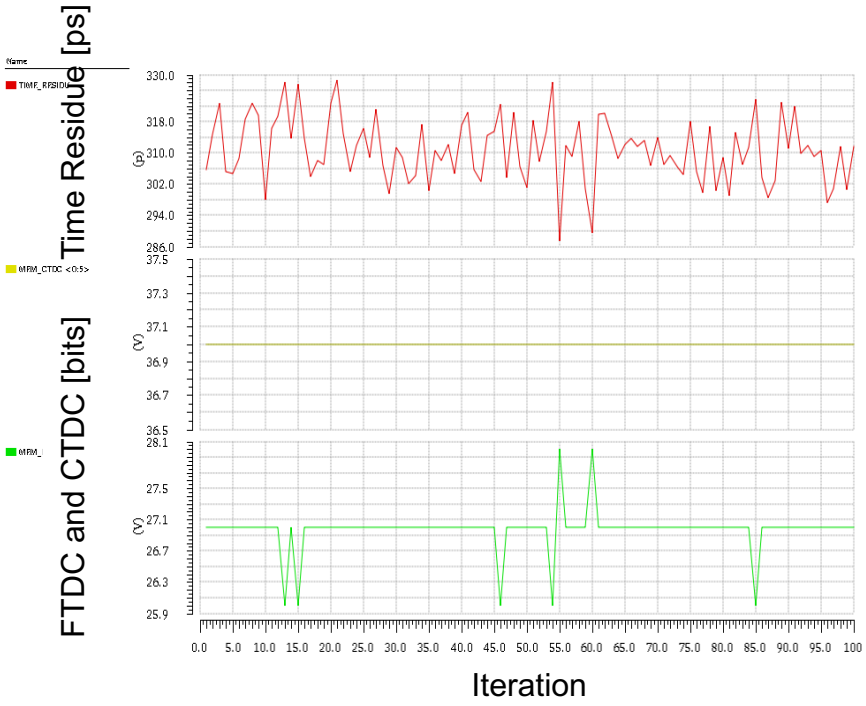
CTDC and FTDC ENCODER CODE evolution for different time of arrival Event between 2,6 and 3,4 ns and for CLK_PLL = 160 MHz

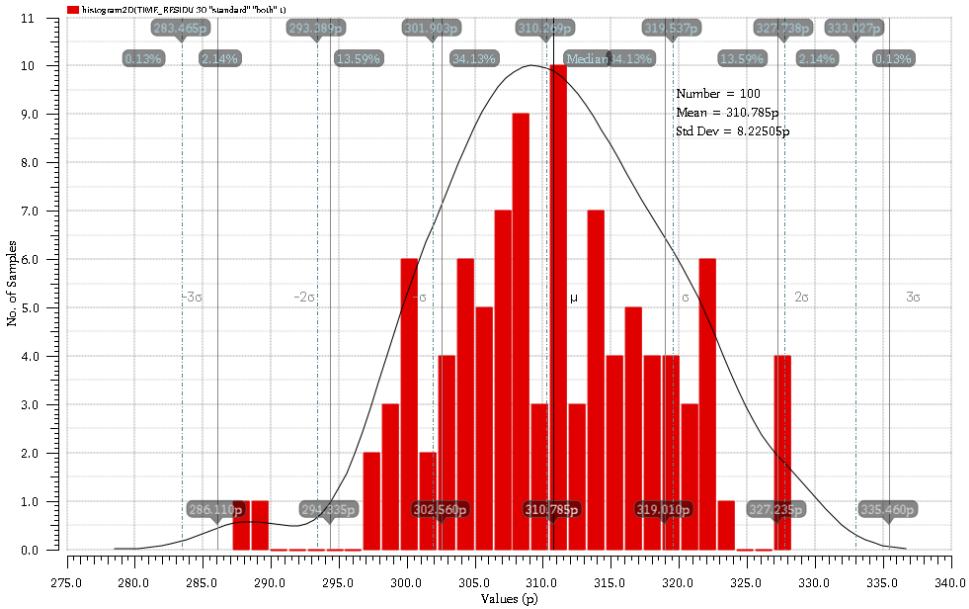
Warning : in this figure there is not enough simulated point to get a realistic estimation of the DNL and INL

$$FTDC = N.residue$$

TIME DOMAIN NOISE SIMULATION

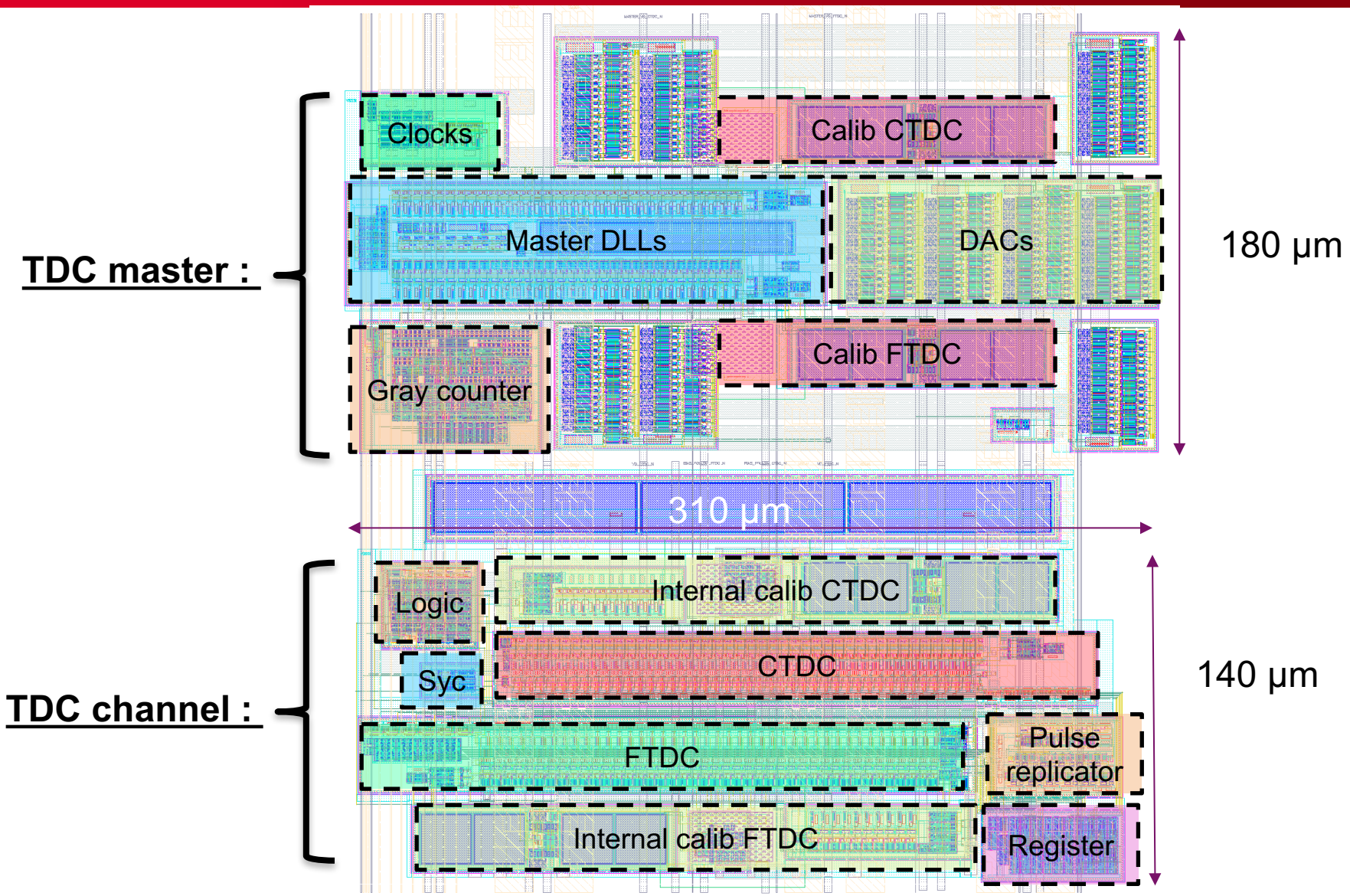
CTDC residue NOISE histogram x10 Scale with START_TDC 2,85 ns and with PLL = 160 MHz
Extracted with perfect input clock





Std Dev : 8,22/10 = 822 fs

LAYOUT


TDC master :
Clocks
Calib CTDC
Master DLLs
DACs
Gray counter
Calib FTDC
180 µm
310 µm
TDC channel :
Logic
Internal calib CTDC
Syc
CTDC
FTDC
Pulse replicator
Internal calib FTDC
Register
140 µm

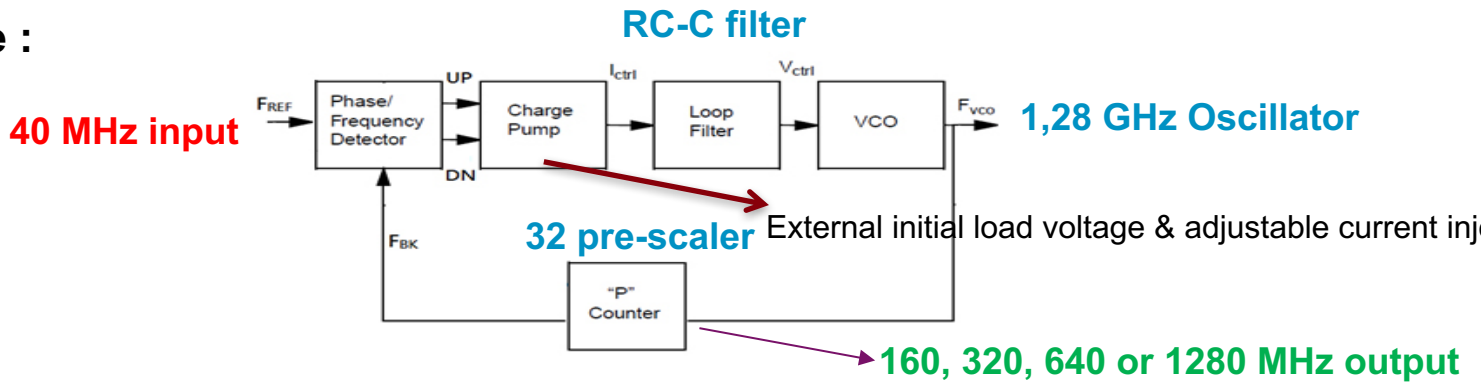
CONCLUSION

Time Of Arrival pour HGCAL	
Type(s) de TDC(s) réalisé(s)	Pulse train amplifier
Type d'intégration: ASIC ou FPGA	ASIC
ASIC dédié TDC ou TDC intégré dans ASIC front-end	TDC intégré dans ASIC front-end
Nombre de voie(s)	32 (64 ou 72 visés)
Technologie (pour les ASICs)	TSMC 130nm
Gamme dynamique en temps	1,6 µs
Résolution temporelle - Pas de quantification: simulés et mesurés	11 bits, LSB=12.5 ps Simulé.
Taux de comptage / temps mort individuel	40MHz (11 bits)
Consommation par voie	2mW. Ne consomme qu'en cas d'événement
Type de discriminateur utilisé, (selon) jitter, walk	

Soumission en juin 2017.
=> Rendez vous aux journées VLSI 2018 pour des résultats de mesure.

PLL ARCHITECTURE

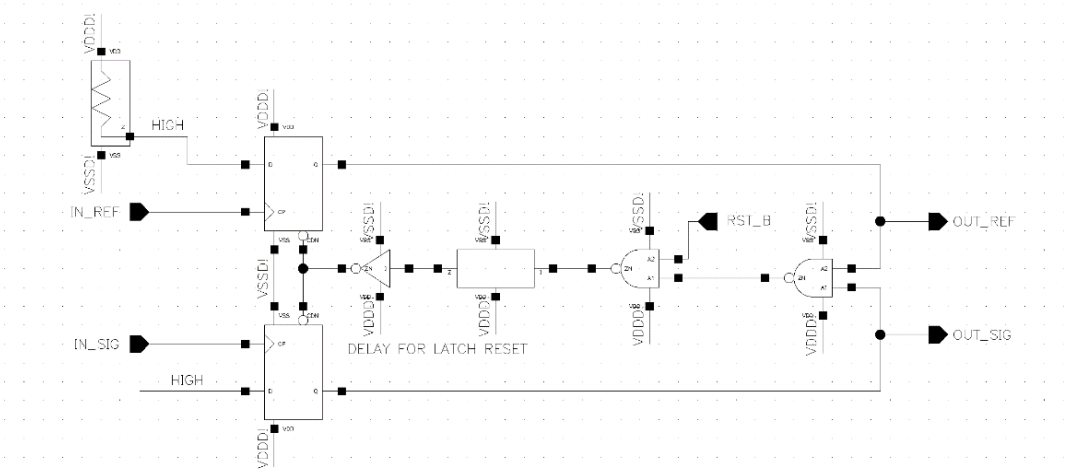
Architecture :



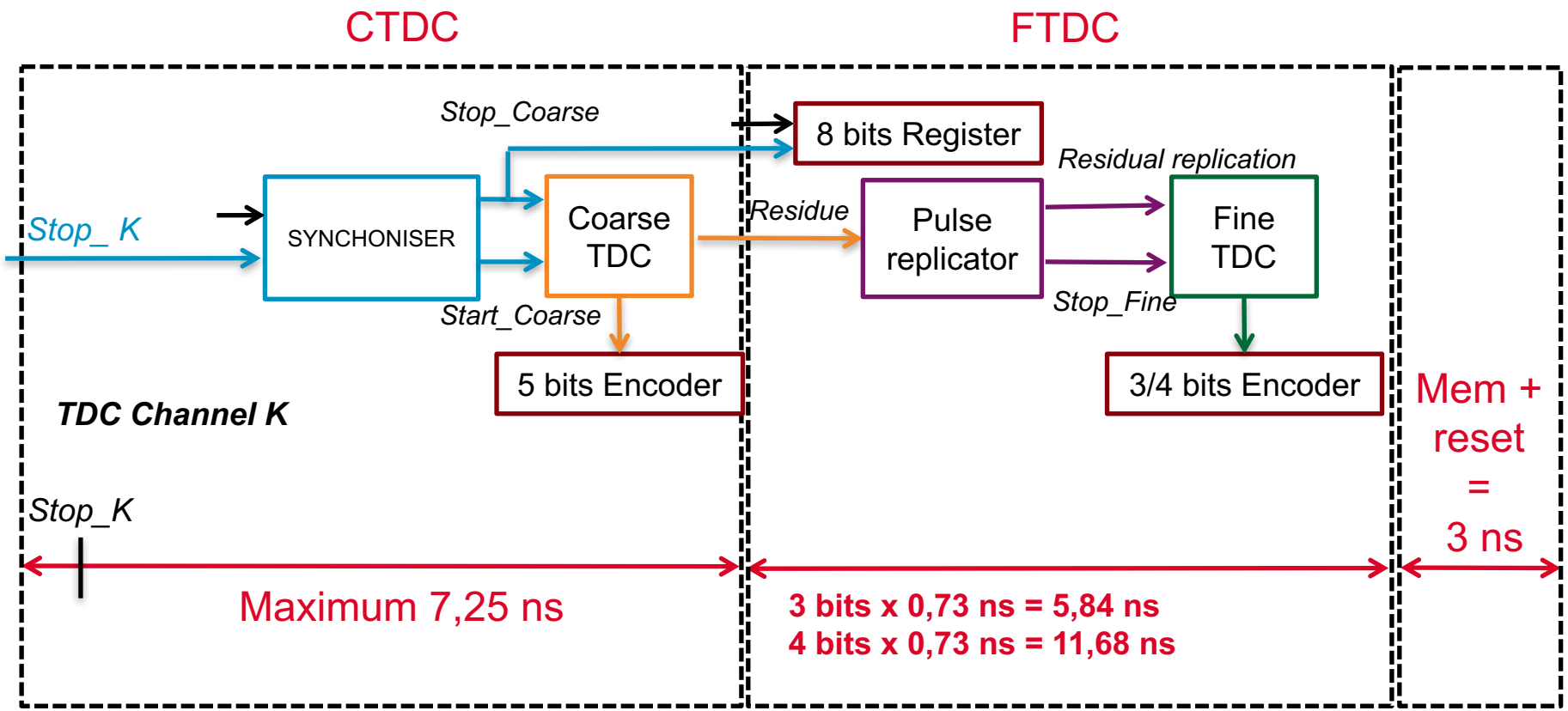
- **Multiplier** : Generate 160 MHz from 40 MHz (have an 1.28 GHz output frequency for output)
- **Internal clock in phase** with external 40 MHz (phase detector)
- **Cleaner** : Reduce the jitter of the external 40 MHz (estimated at 25 ps) in order to have a cleanest possible internal clock and less than the quantification noise of the TDC < 3.52 ps

Minimum and maximum lock frequencies : **21 to 47,6 MHz (BW : 20 MHz)**

Phase detector :



TIME BUDGET



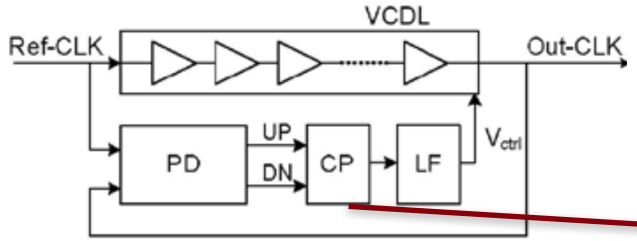
Maximum conversion time :

10 bits TDC = 16 ns

11 bits TDC = 22 ns

TEMPERATURE AND PROCESS VARIATIONS

Internal DLL channel calibration :



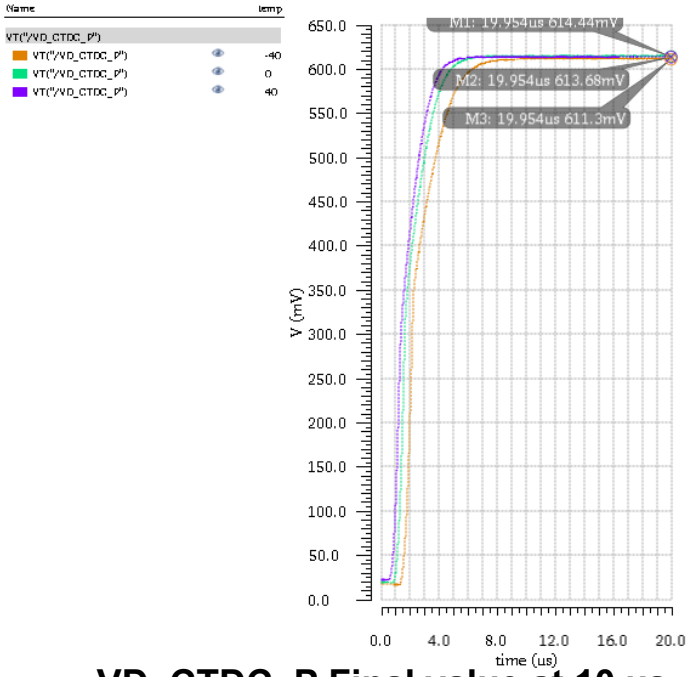
CTDC (Coarse TDC) and FTDC (Fine TDC) ➔ **Internal servo-controlled DLL**

To have the **same DLL time response** according to the temperature and process variations

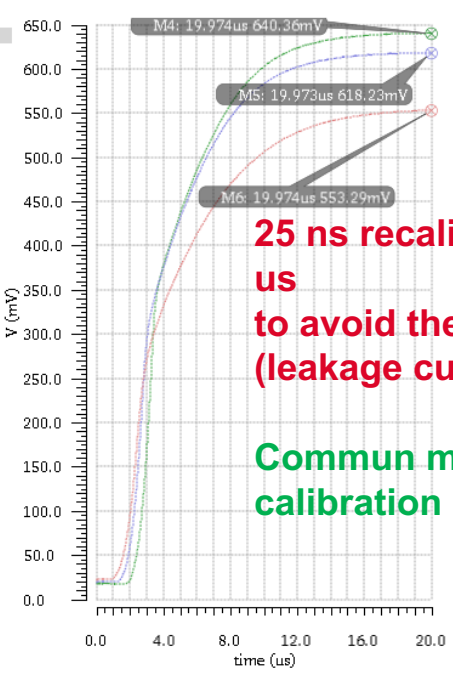
External initial load voltage & adjustable current injection

Initial lock DLL Calibration phase :

VD_CTDC_P & VD_FTDC_P internal calibration init to 0 V with VD_CTDC_N = 1,2 V and VD_FTDC_N = 1,2 V and VBIAS_N = 400 mV at -40, 0 and 40 °C [internal buffer]



VD_CTDC_P Final value at 10 µs



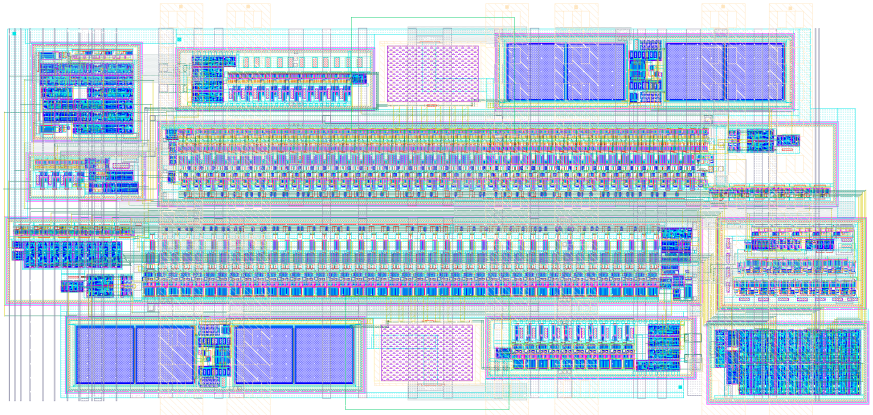
VD_FTDC_P Final value > 20 µs

25 ns recalibration every 100 us
to avoid the voltage node discharge (leakage current)

Commun master DLL for continuous calibration (mismatch?)

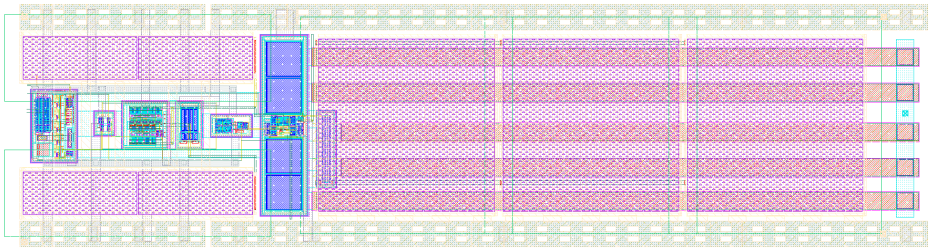
LAYOUT AND SIMULATION RESULTS

TDC layout :



Area = 140 µm x 310 µm
Triple wells under analog and digital

PLL layout :



Area = 515 µm x 141 µm
Triple wells under analog and digital

TDC	Simulation R&D TDC
Resolution	24.4 / 12.2 ps
Bits	10 / 11 bits (over 25 ns)
Rms noise	≈ 1 ps rms
Conversion rate	10 bits TDC = 62,5 MHz 11 bits TDC = 45,6 MHz
Linearity	To be done
Power consumption	During the conversion 2,18 mW [static and dynamic] or 40 µW [static]
Calibration	Internal
Area	250 µm x 160 µm
Technology	TSMC 130 nm
Temperature	-40 and 40 °C

PLL	Simulation R&D PLL
Input frequency	40 MHz (Bunch clock)
Output frequecy	MAX : 1.28 GHz Output of intermediate frequencies : (640, 320, 160 MHz)
Jitter	Jitter cleaner = 2.2 ps rms Cleaner 94 % (for 25 ps input jitter)
Power consumption	1.91 mW
Area	515 µm x 141 µm
Technology	TSMC 130 nm
Temperature	-40 and 40 °C

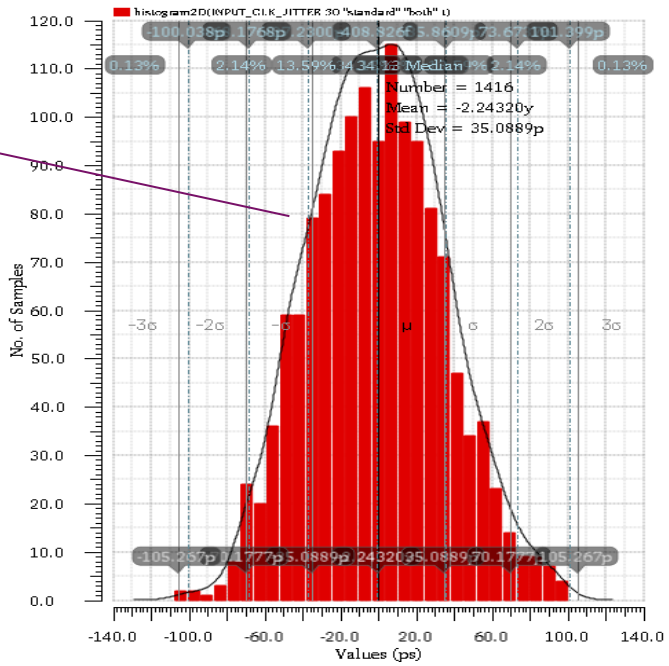
PLL TRANSIENT JITTER

Transient noise jitter injection with Cadence jitter source [extracted, buffer] @ 27 °C :

1400 periods :

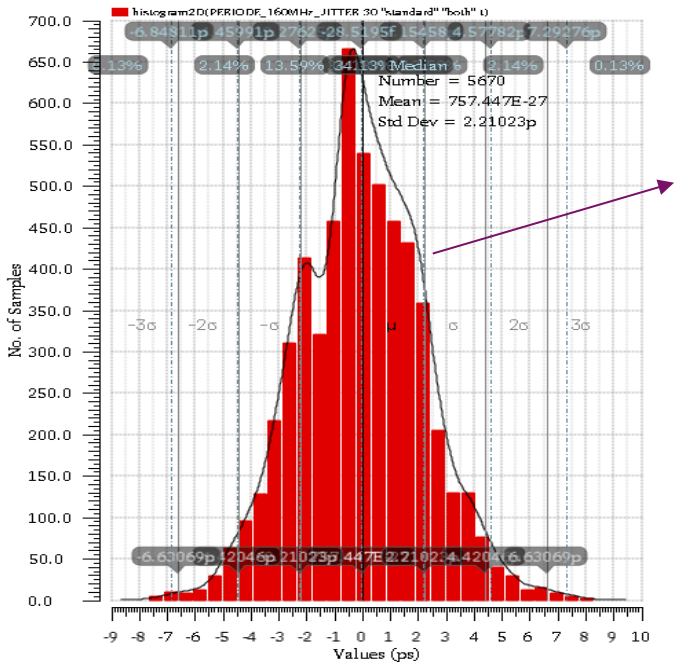
40 MHz input

35 ps rms



160 MHz output

2.2 ps rms



35 ps rms jitter noise added to perfect 40 MHz input clock (left) and the jitter of the 160 MHz output (right)

DESIGN STATUT

TDC	Statut
Schematics	OK
Temperature variation -40 to 40 °C	OK
Monte-Carlo (process & mismatch) -40 and 40 °C	OK
Layout	OK
Extracted view	OK
Fine characterization process (INL, DNL, etc…)	To be done

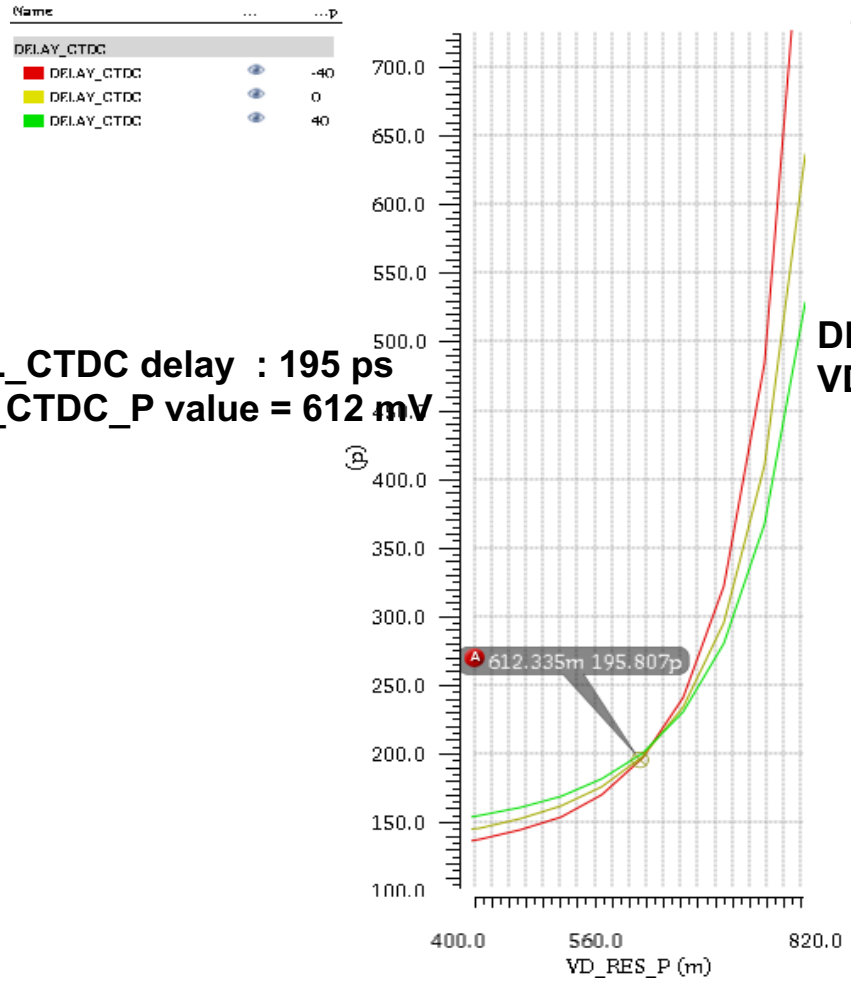
PLL	Statut
Schematics	OK
Temperature variation -40 to 40 °C	OK
Monte-Carlo (process & mismatch) -40 and 40 °C	OK
Layout	OK
Extracted view	OK
Fine characterization process	To be done

Next steps	Statut
32 Multi-channel TDC & PLL	To be done
Connect the ToA TDC in HGROCv1	To be done
Add internal slow control registers	To be done
Add internal references (DAC)	To be done
PAD, drivers connections, etc…	To be done
DRC & LVS verifications	To be done
Final simulations	To be done

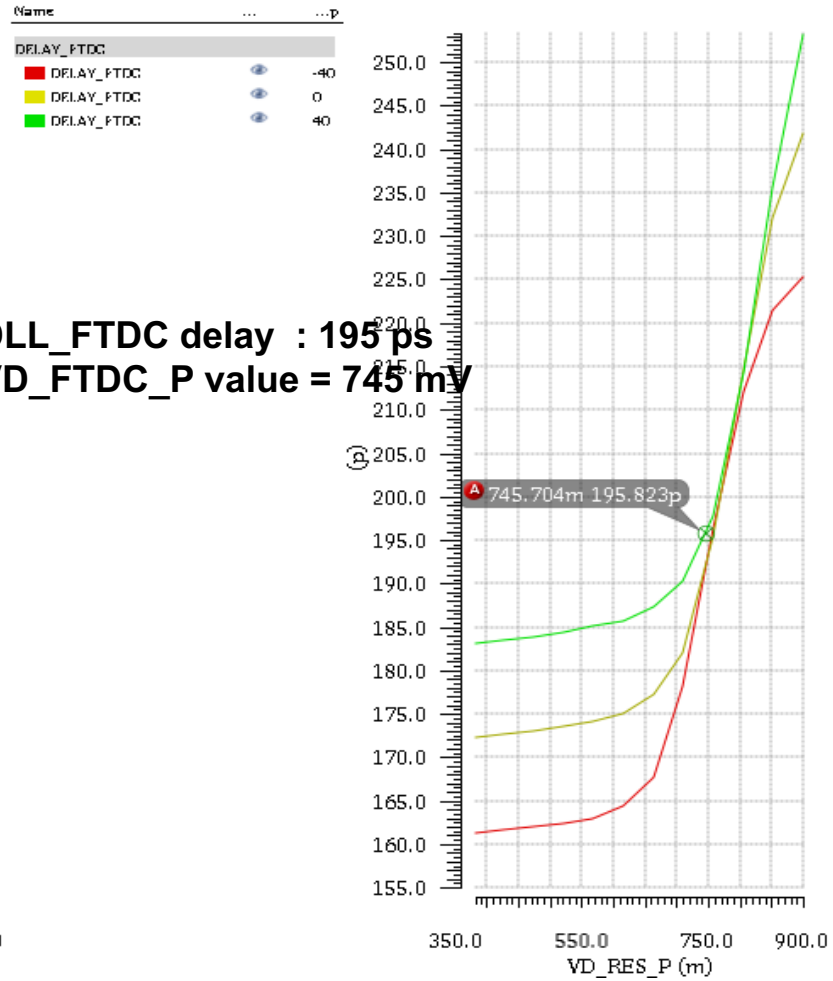
DLL_CTDC & DLL_FTDC DELAYS

DLL_CTDC & DLL_FTDC delays with VD_P variations, VD_N = 1,2 V and at -40, 0 and 40 °C [parasitics included]

DLL_CTDC delay : 195 ps
VD_CTDC_P value = 612 mV



DLL_FTDC delay : 195 ps
VD_FTDC_P value = 745 mV

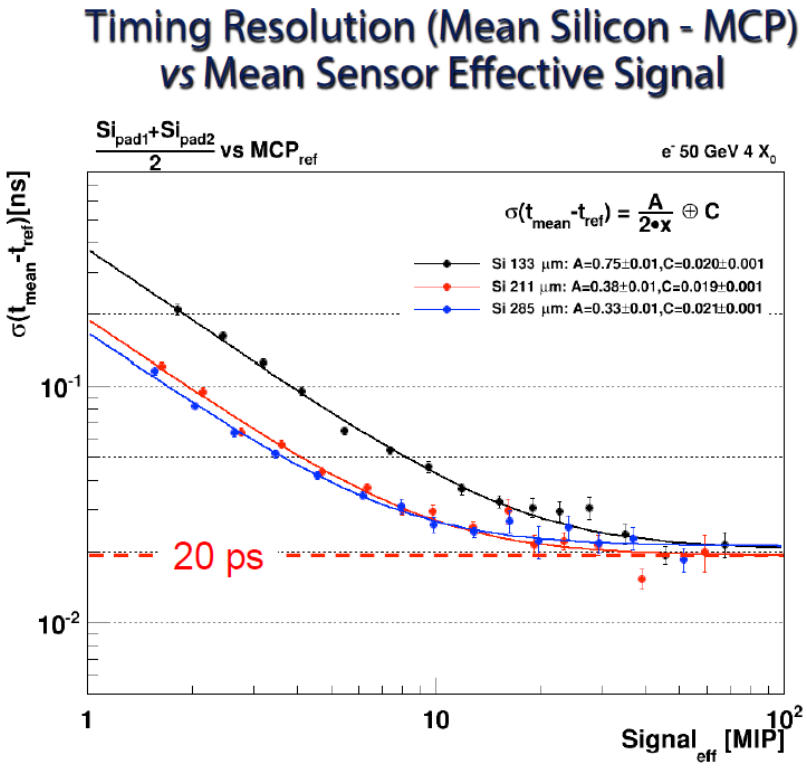


Simulation moderate Spectre APS ++aps NONE Preset

TOA PERFORMANCE

In testbeam : jitter = 500 ps/Q(fC) (+) 20 ps

In HGROC, simulated jitter = 1.2 ns/Q(fC)



GLOBAL ARCHITECTURE