Tutorial on Frequency Synthesis

Part I – Phase Locked Loop (PLL)

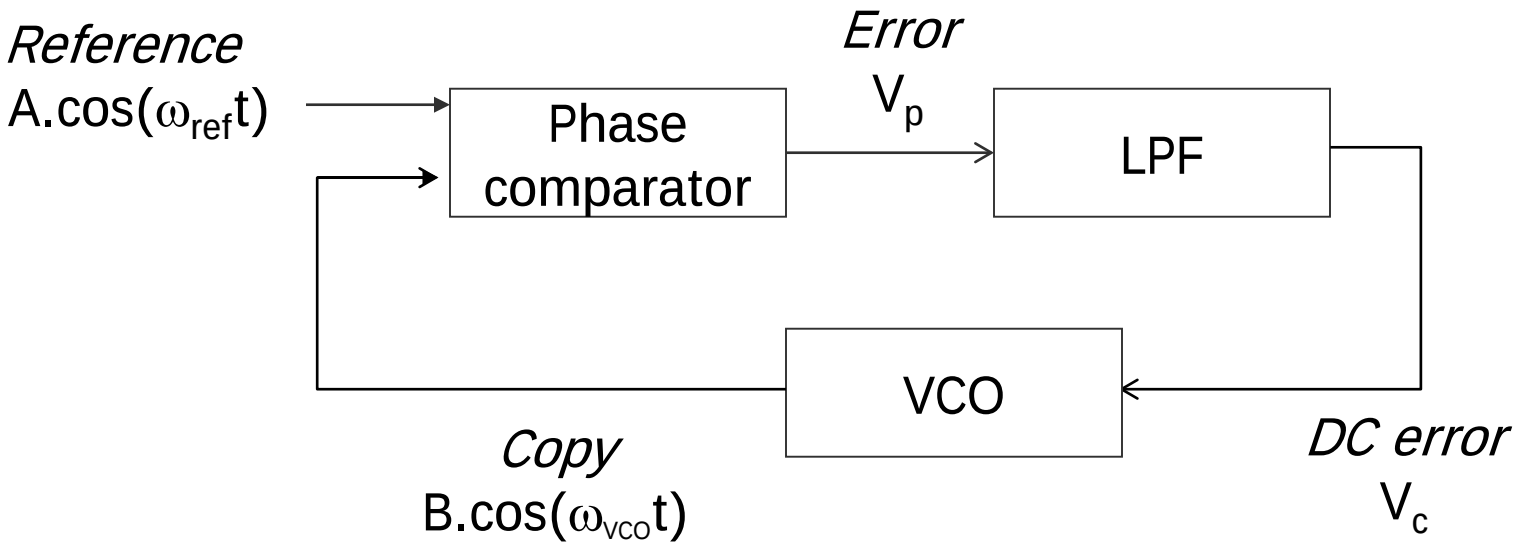
Pr. Yann DEVAL

May, 2017

Outline

- Principle of phase locked loops
- Key building block examples
- PLL as a frequency synthesizer
- The linear model
  - Open and closed loop equations
  - Transfer function
- Frequency ranges of interest

Principle



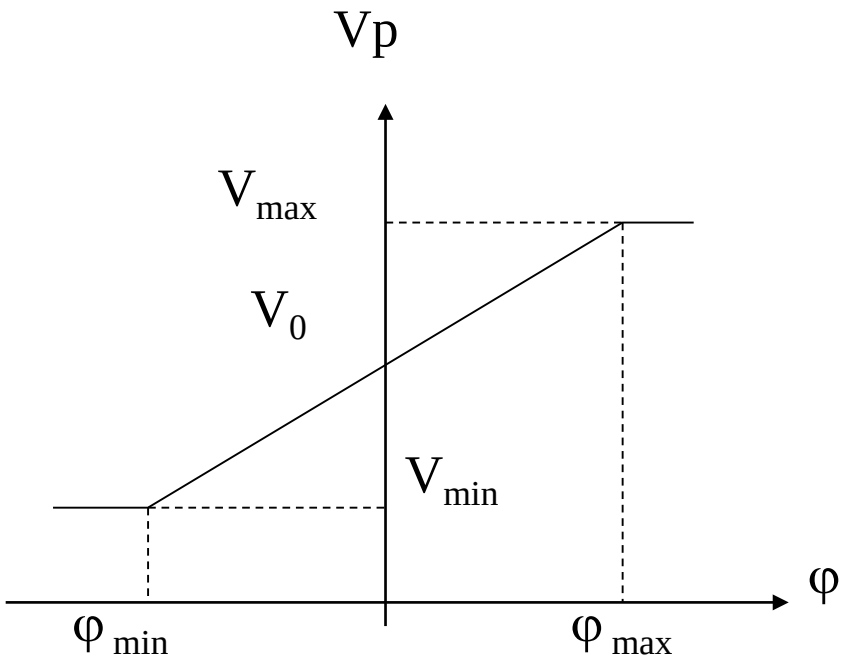
- Copying the reference frequency with the VCO frequency – thanks to phase lock

Outline

- Principle of phase locked loops
- Key building block examples
- PLL as a frequency synthesizer
- The linear model
  - Open and closed loop equations
  - Transfer function
- Frequency ranges of interest

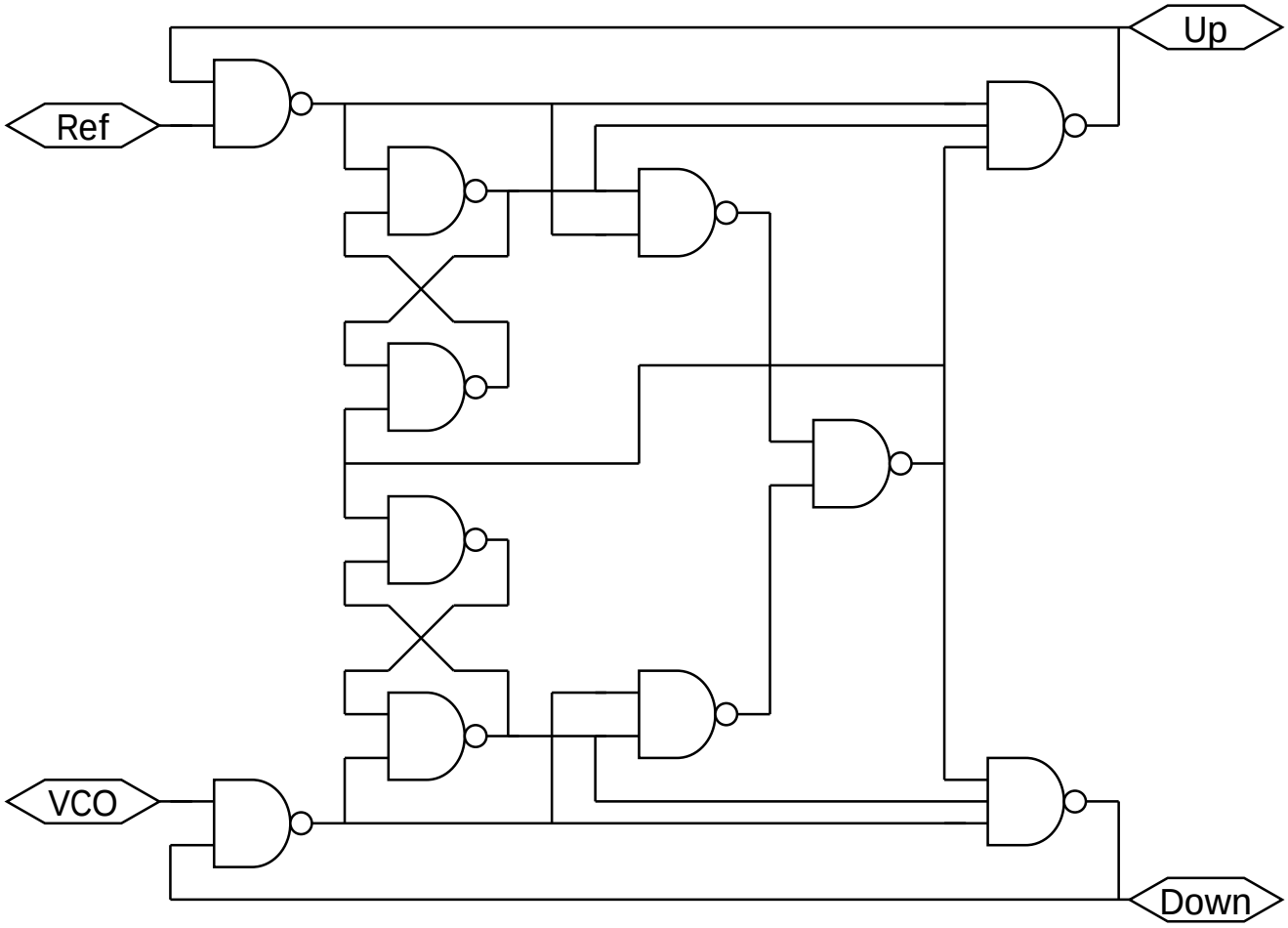
Phase detector

- Transfer function (theoretical)

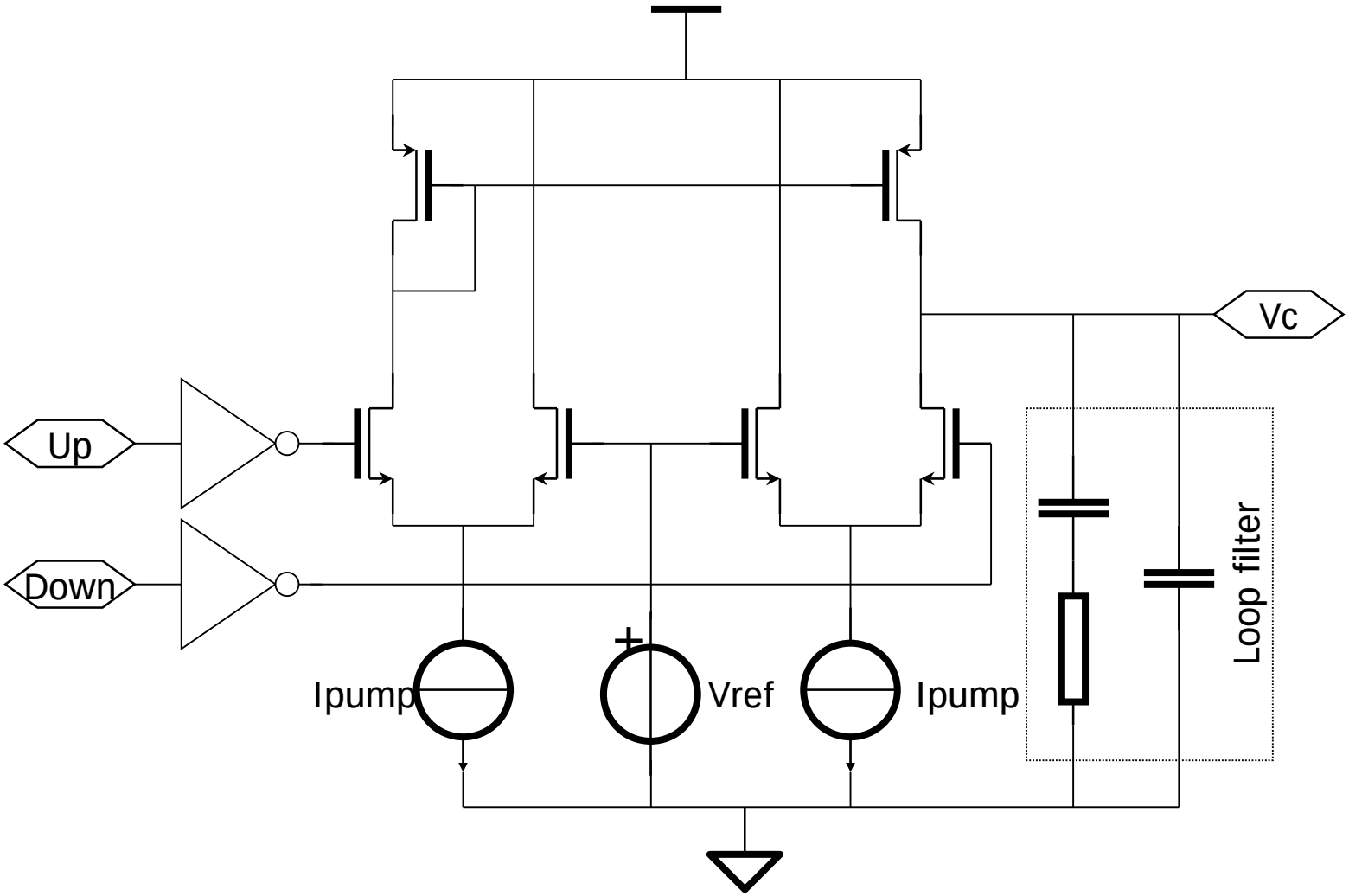


$$V_p = V_0 + \frac{V_{max} - V_{min}}{\varphi_{max} - \varphi_{min}} \varphi$$

Phase frequency detector

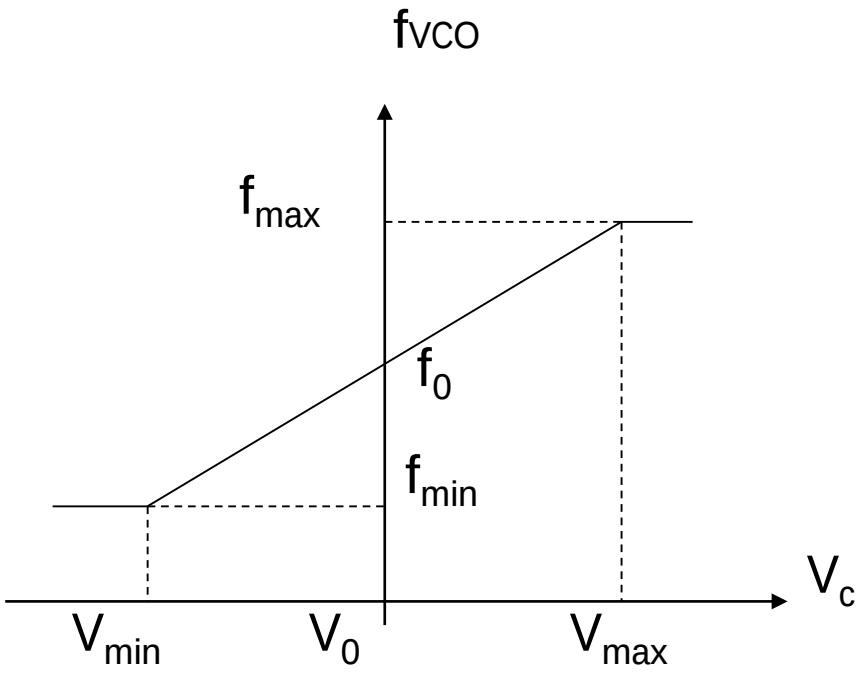


Charge pump



Voltage controlled oscillator

- Transfer function (theoretical)

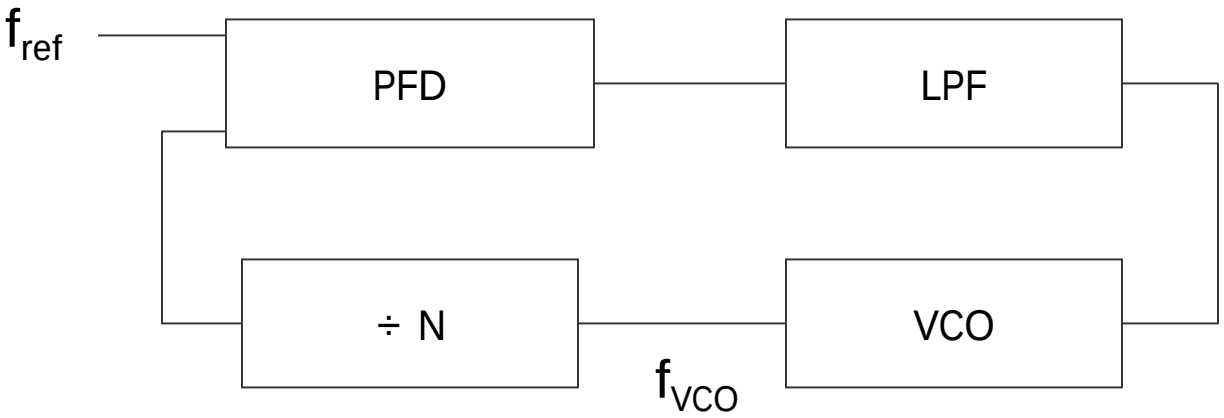


$$f_{VCO} = f_0 + \frac{f_{\max} - f_{\min}}{V_{\max} - V_{\min}}(V_c - V_0)$$

Outline

- Principle of phase locked loops
- Key building block examples
- PLL as a frequency synthesizer
- The linear model
  - Open and closed loop equations
  - Transfer function
- Frequency ranges of interest

PLL : application to frequency synthesis



When locked : $f_{VCO} = N \cdot f_{ref}$

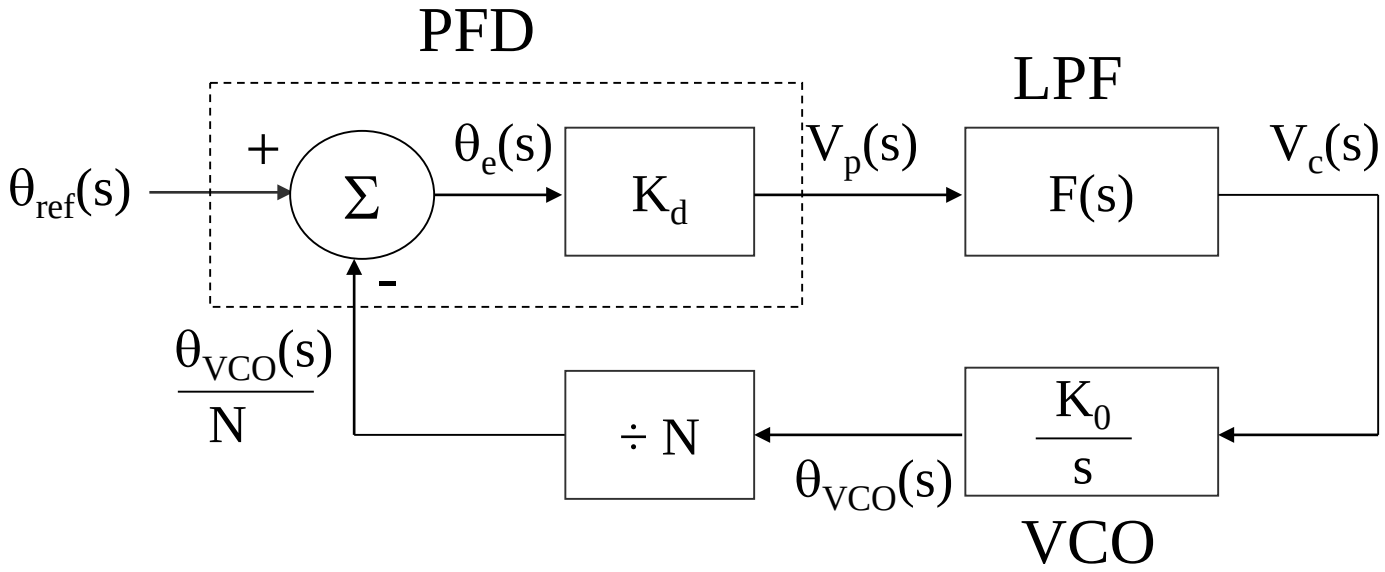
$$f_{01} = K \cdot f_{ref} \Rightarrow f_{02} = (K+1) \cdot f_{ref} = K \cdot f_{ref} + f_{ref} = f_{01} + f_{ref}$$

f_{ref} is the frequency step of the synthesizer !

Outline

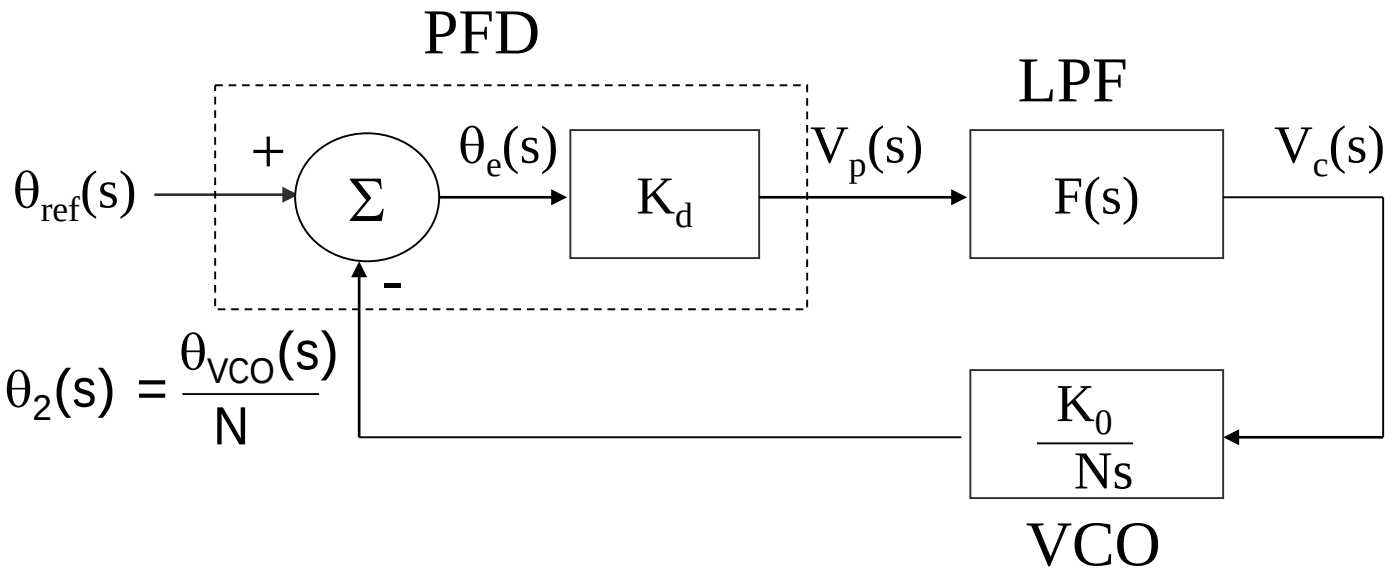
- Principle of phase locked loops
- Key building block examples
- PLL as a frequency synthesizer
- The linear model
  - Open and closed loop equations
  - Transfer function
- Frequency ranges of interest

Linear modelisation (phase)



$$\omega_{VCO}(t) = \frac{d\theta_{VCO}(t)}{dt} \qquad \theta_{VCO}(t) = \int_0^t \omega_{VCO}(t)dt \qquad \theta_{VCO}(s) = \frac{\omega_{VCO}(s)}{s}$$

Some equations



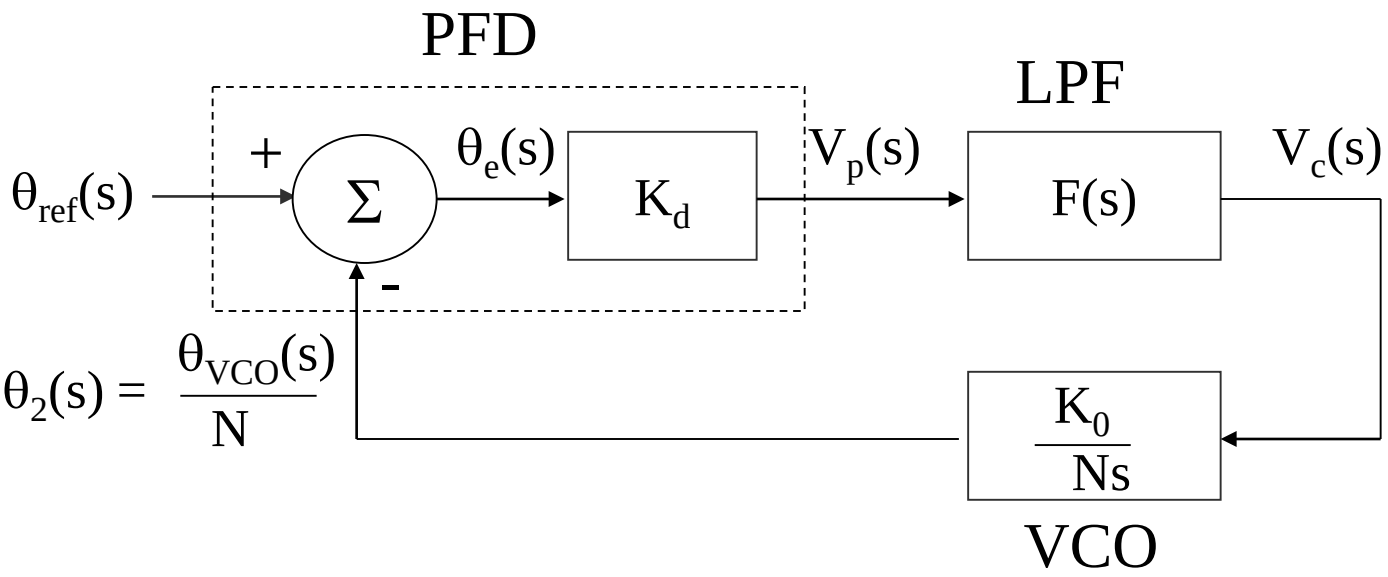
$$\theta_e(s) = \theta_{ref}(s) - \theta_2(s)$$

$$V_p(s) = K_d \cdot \theta_e(s)$$

$$V_c(s) = F(s) \cdot V_p(s)$$

$$\theta_2(s) = \frac{K_0}{N \cdot s} \cdot V_c(s)$$

Transfer function

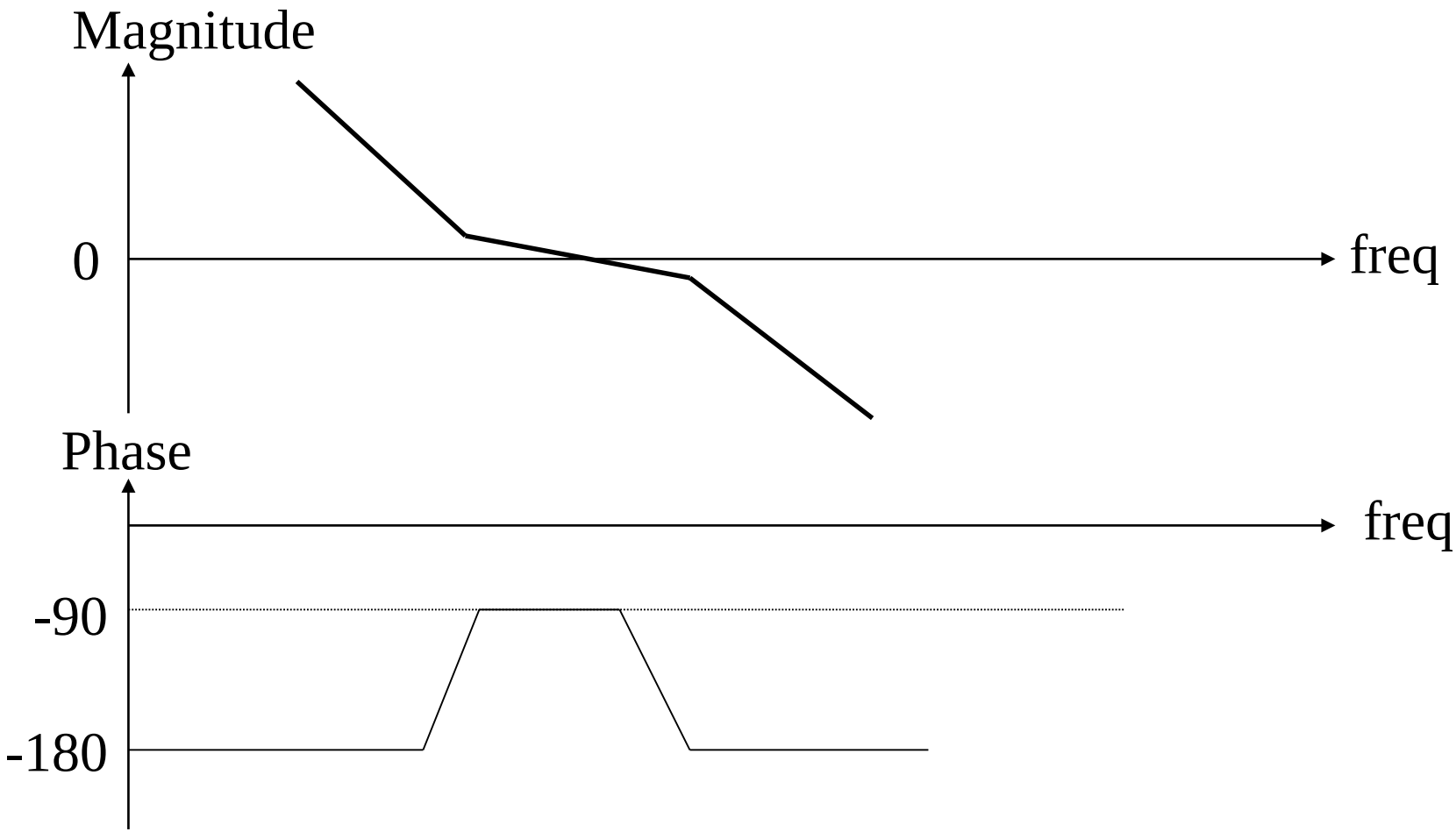


$$G(s) = \frac{\theta_2(s)}{\theta_{ref}(s)} = \frac{H(s)}{1 + H(s)}$$ ***(CL)***

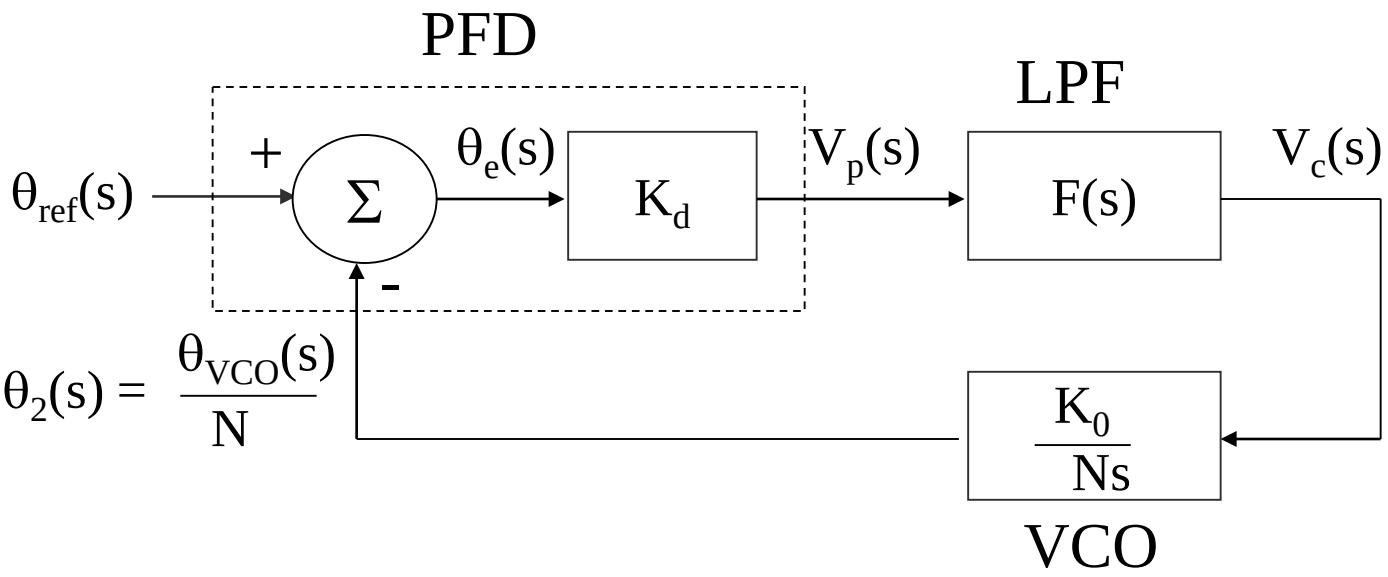
with

$$H(s) = \frac{K_0 \cdot K_d \cdot F(s)}{N \cdot s}$$ ***(OL)***

Transfer function - OL



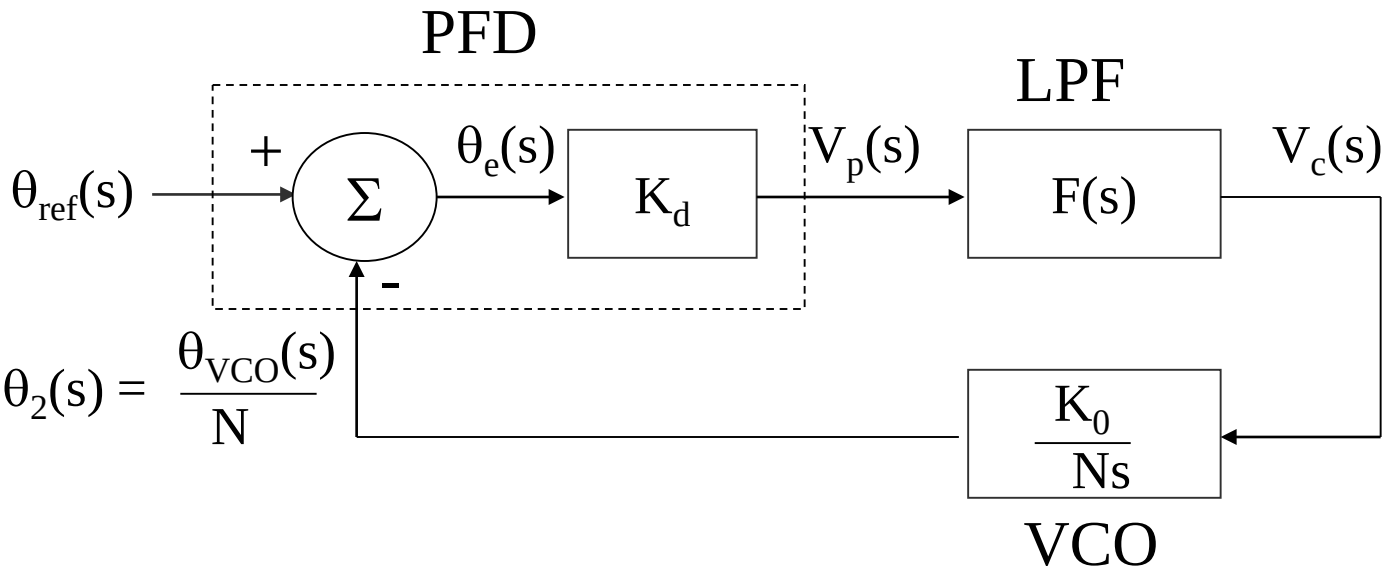
Transfer function (cont')



$$G(s) = \frac{K_0 \cdot K_d \cdot F(s)}{N \cdot s + K_0 \cdot K_d \cdot F(s)}$$

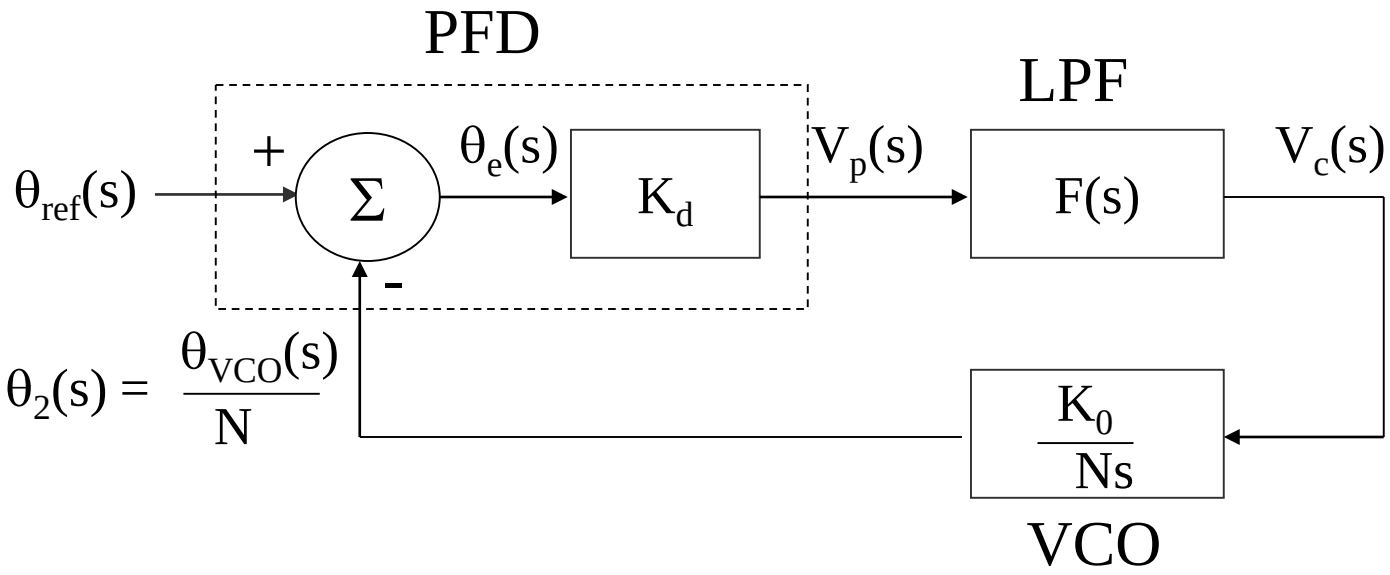
$$F(s) = \frac{1 + s \cdot \tau_2}{s \cdot \tau_1}$$

Transfer function (cont')



$$G(s) = \frac{\frac{K_0 \cdot K_d \cdot \tau_2}{N \cdot \tau_1} \cdot s + \frac{K_0 \cdot K_d}{N \cdot \tau_1}}{s^2 + \frac{K_0 \cdot K_d \cdot \tau_2}{N \cdot \tau_1} \cdot s + \frac{K_0 \cdot K_d}{N \cdot \tau_1}}$$

Transfer function (cont')

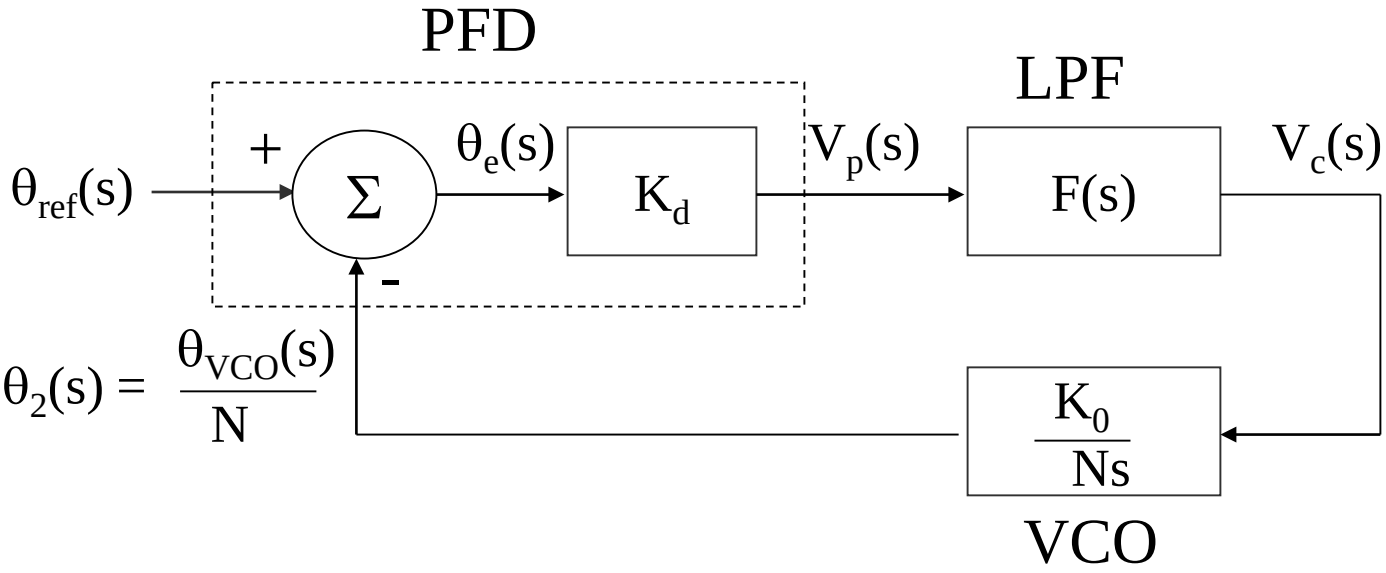


$$2^{\text{nd}}\ \text{order}: \quad s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2$$

Damping factor

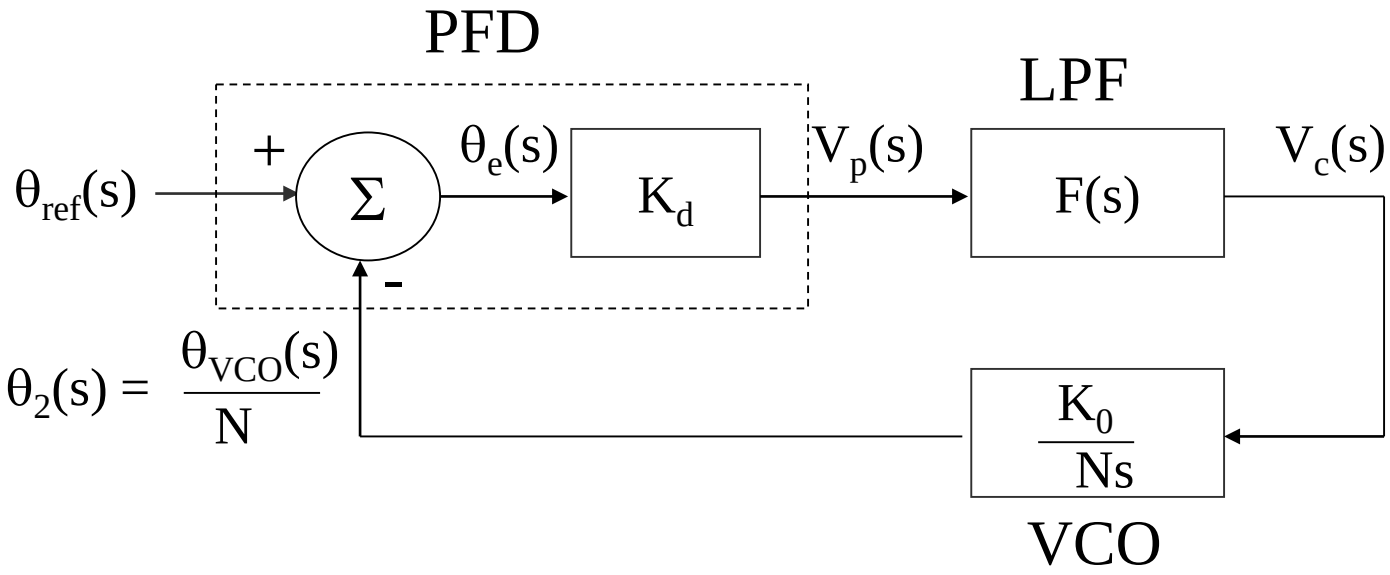
Natural frequency

Transfer function (cont')



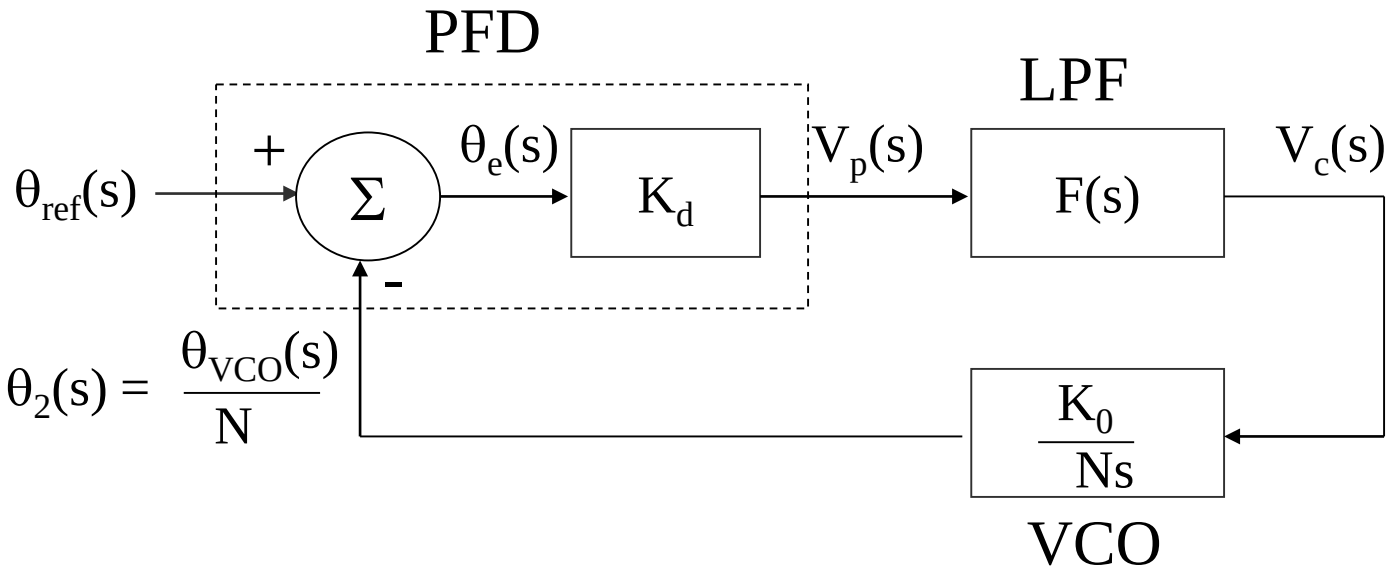
$$\omega_n = \sqrt{\frac{K_0 \cdot K_d}{N \cdot \tau_1}} \qquad \xi = \frac{\tau_2}{2} \cdot \sqrt{\frac{K_0 \cdot K_d}{N \cdot \tau_1}} = \frac{\tau_2 \cdot \omega_n}{2}$$

Transfer function (cont')



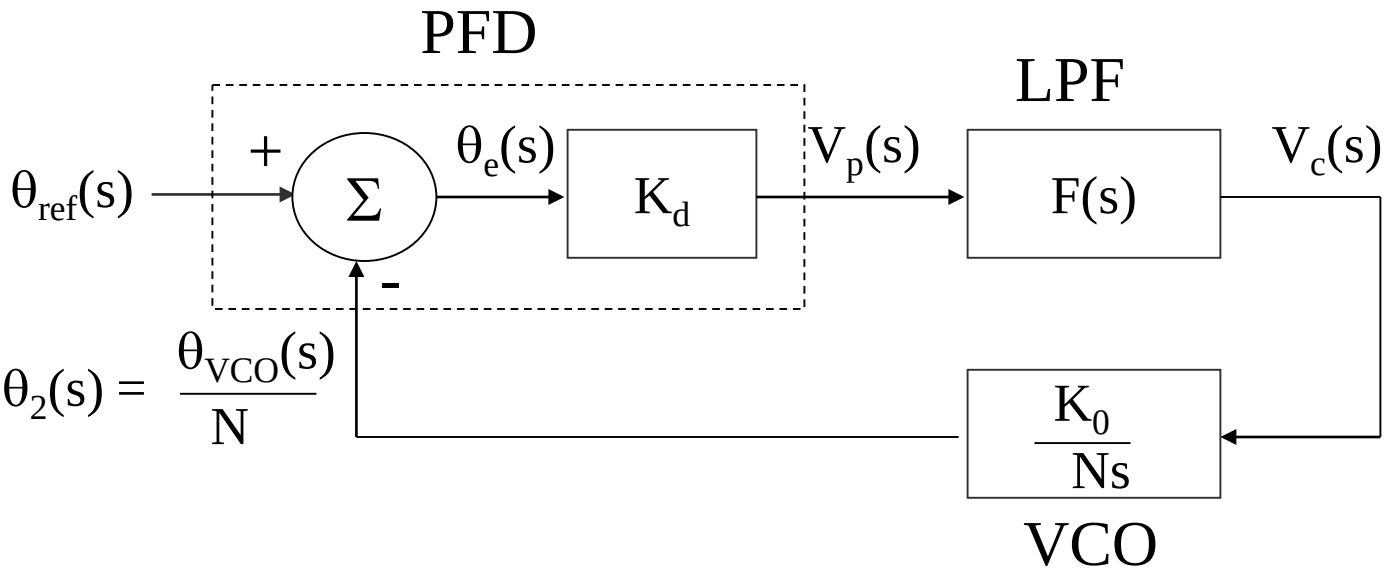
$$G(s) = \frac{2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

Closed loop bandwidth



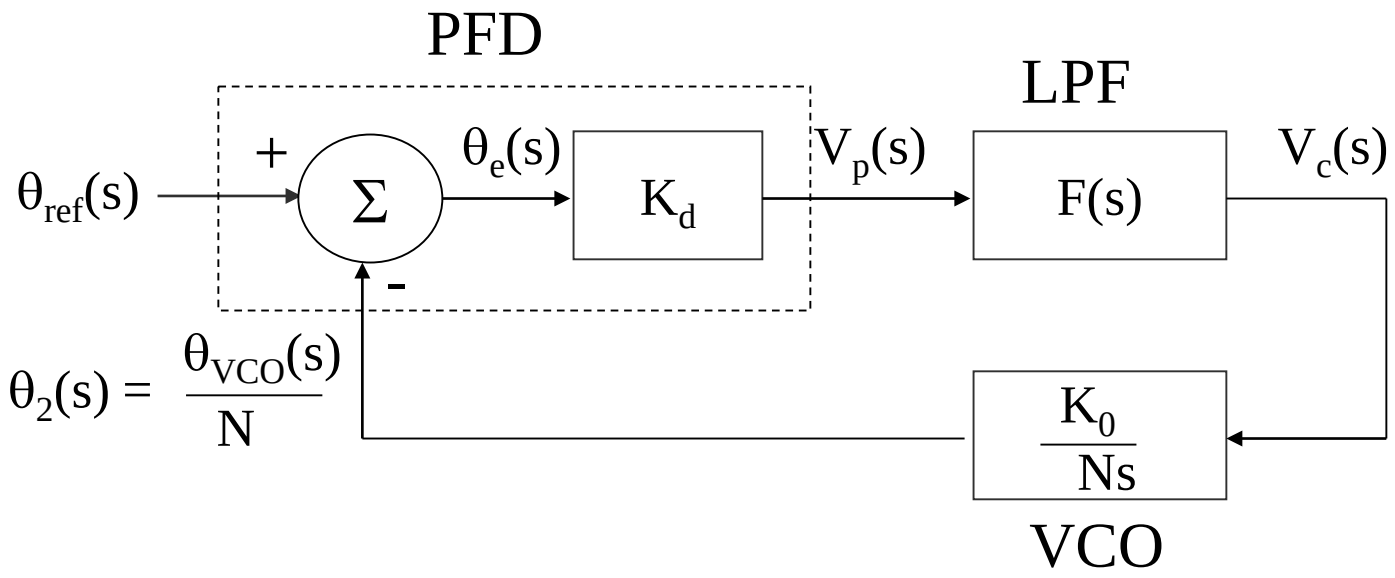
$$B_{3\,dB} = \frac{\omega_n}{2\pi}\sqrt{2\xi^2 + 1 + \sqrt{\left(2\xi^2 + 1\right)^2 + 1}} \approx \frac{\omega_n}{\pi}$$

Closed loop bandwidth (cont')



$$B_{3dB} \approx \frac{\omega_n}{\pi} = \frac{1}{\pi\sqrt{N}} \cdot \sqrt{\frac{K_0 K_d}{\tau_1}} = 2 f_n$$

Closed loop bandwidth

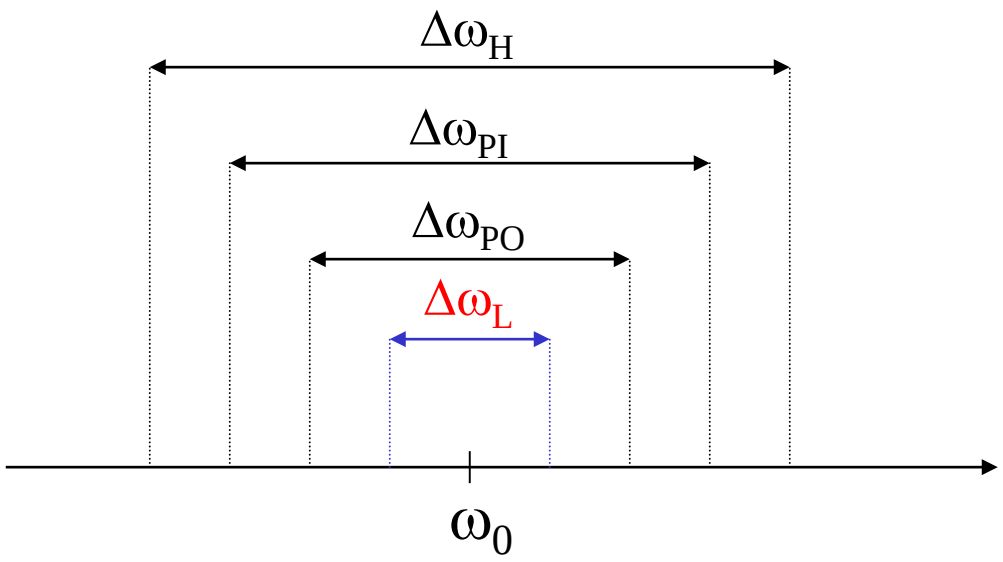


- V_p includes not only a DC value (of interest) but also an unwanted component at f_{ref} (among others)
- The loop filter (LPF) has to attenuate as much as possible this component : typically τ_1 is set one decade away from 1/ f_{ref}

Outline

- Principle of phase locked loops
- Key building block examples
- PLL as a frequency synthesizer
- The linear model
  - Open and closed loop equations
  - Transfer function
- Frequency ranges of interest

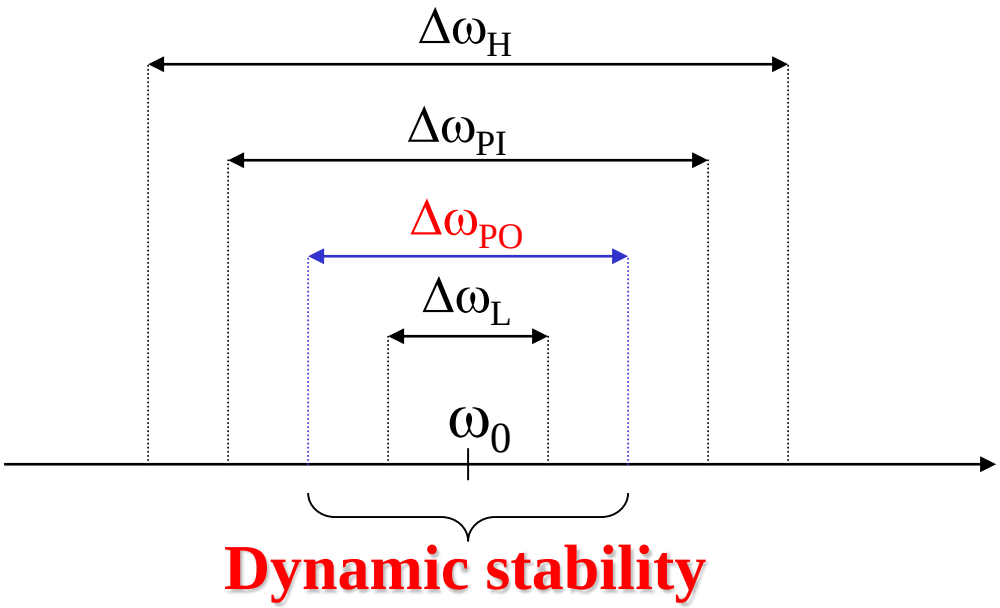
Frequency ranges of interest



$\Delta\omega_L$: Lock range

PLL is always locked, and quickly react

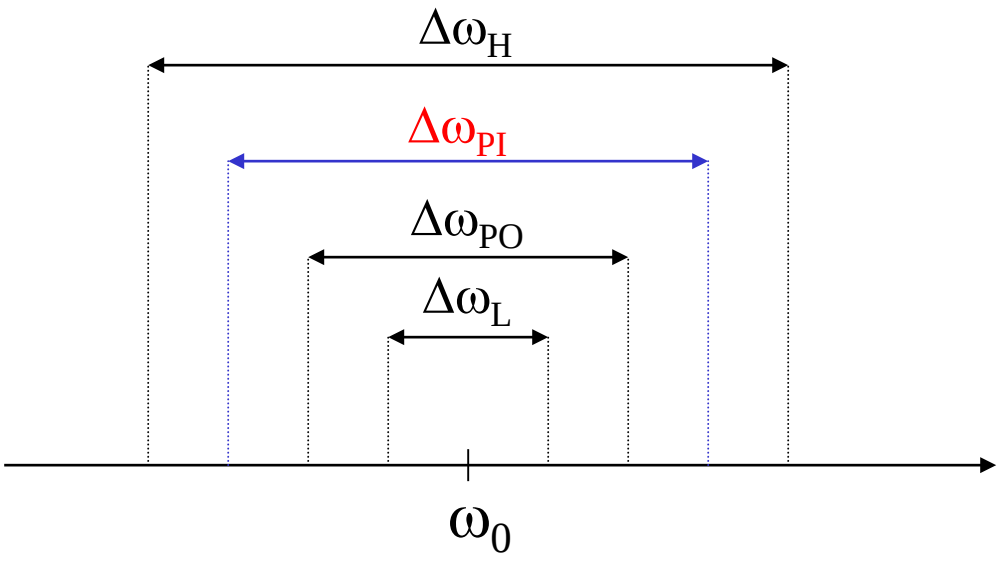
Frequency ranges of interest (cont')



$\Delta\omega_{PO}$: Pull-Out range

PLL reacts a bit more slowly, though it still relocks quickly.

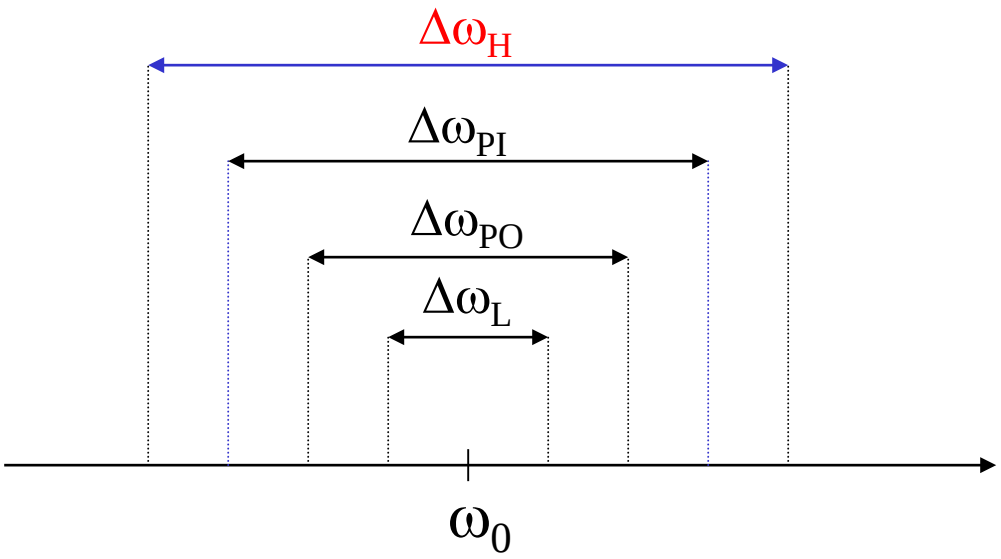
Frequency ranges of interest (cont')



$\Delta\omega_{PI}$: Pull-In range

A signal within this range will allow the PLL to lock – but it may be a long process to do so

Frequency ranges of interest (end)



$\Delta\omega_H$: Hold range

An already locked signal can be hold within this range

but if there is any variation the system will collapse

Summarize - PLL and synthesizer

- A complex system to deal with...
- A 2nd order system (or even more) in which the stability is a matter of concern
- As the divider is integer, the frequency step yields the reference, which determines the bandwidth in return
- A linear model used to define a sampled system is a bit non rigorous – but there's no way do avoid the liar...

Tutorial on Frequency Synthesis

Part II – Synthesizer architectures

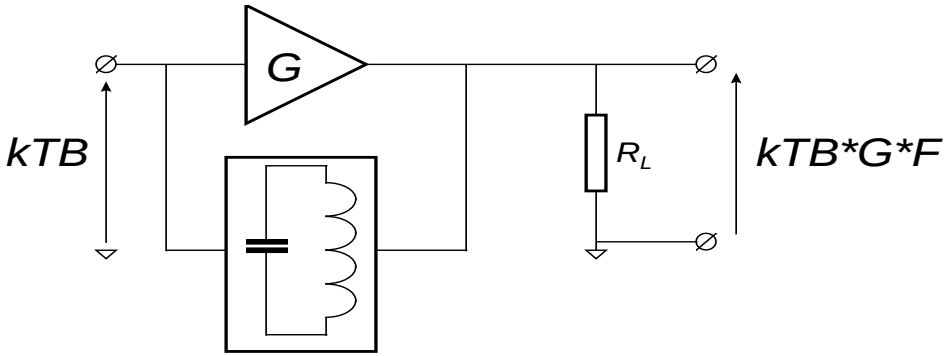
Pr. Yann DEVAL

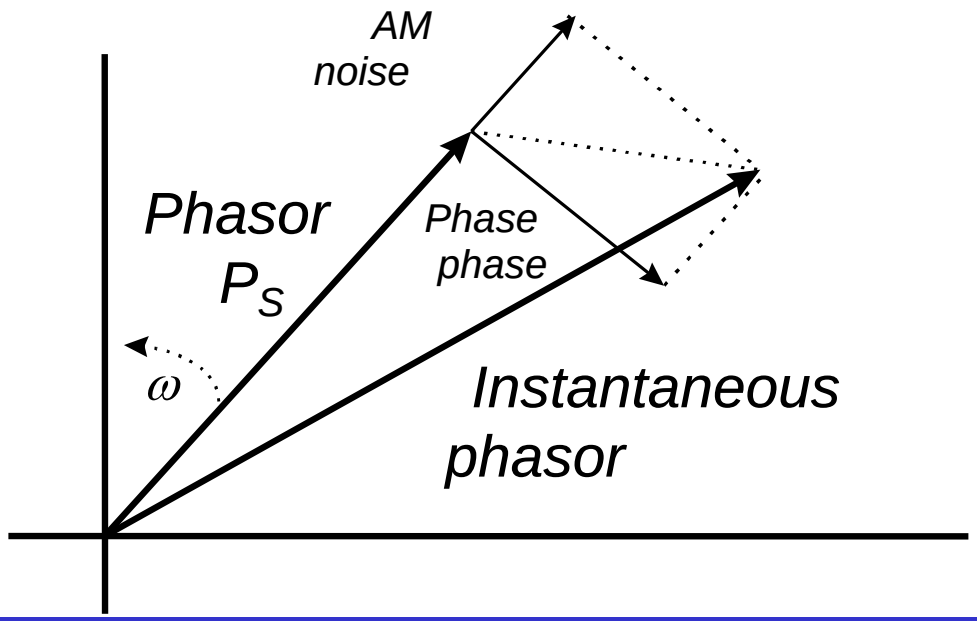
May, 2017

Outline

- Phase noise in oscillators
- Noise shaping in PLL
- PLL architectures

Phase noise

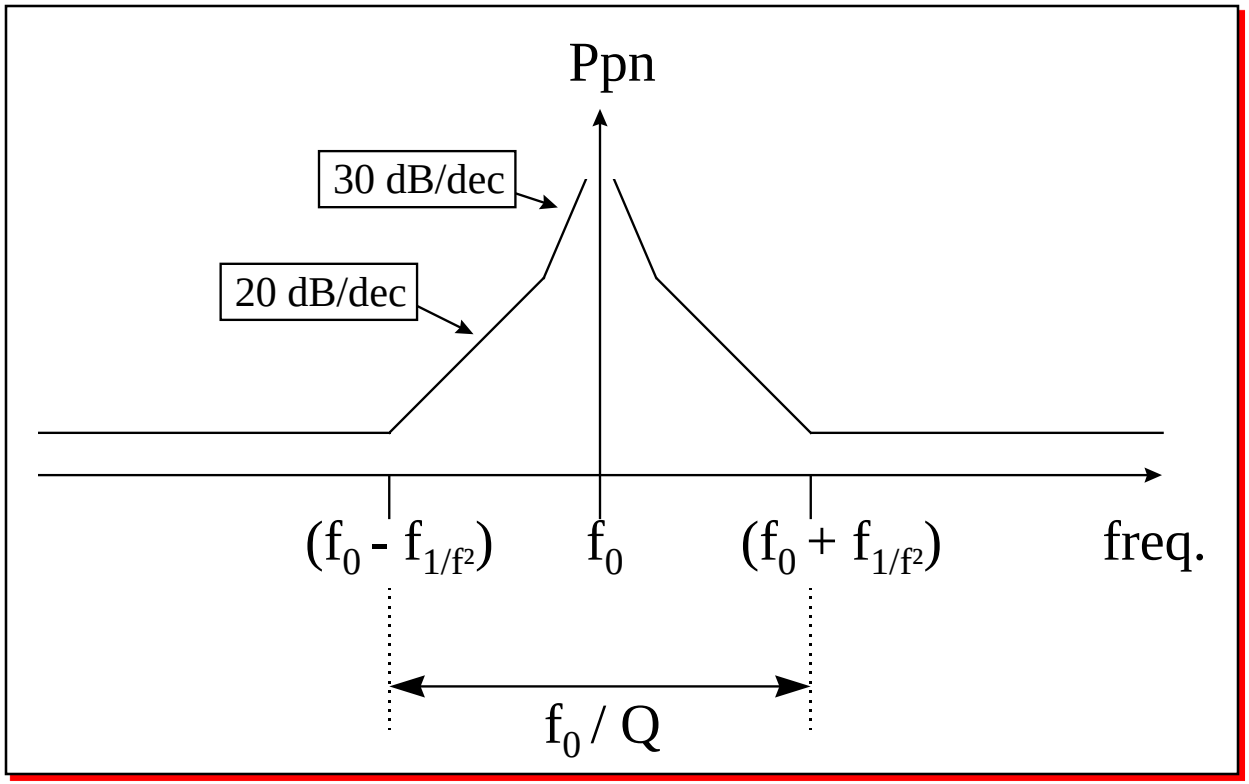

G
kTB
R_L
kTB*G*F


AM
noise
Phasor
P_S
Phase
phase
ω
Instantaneous
phasor

Phase noise : NCR calculation

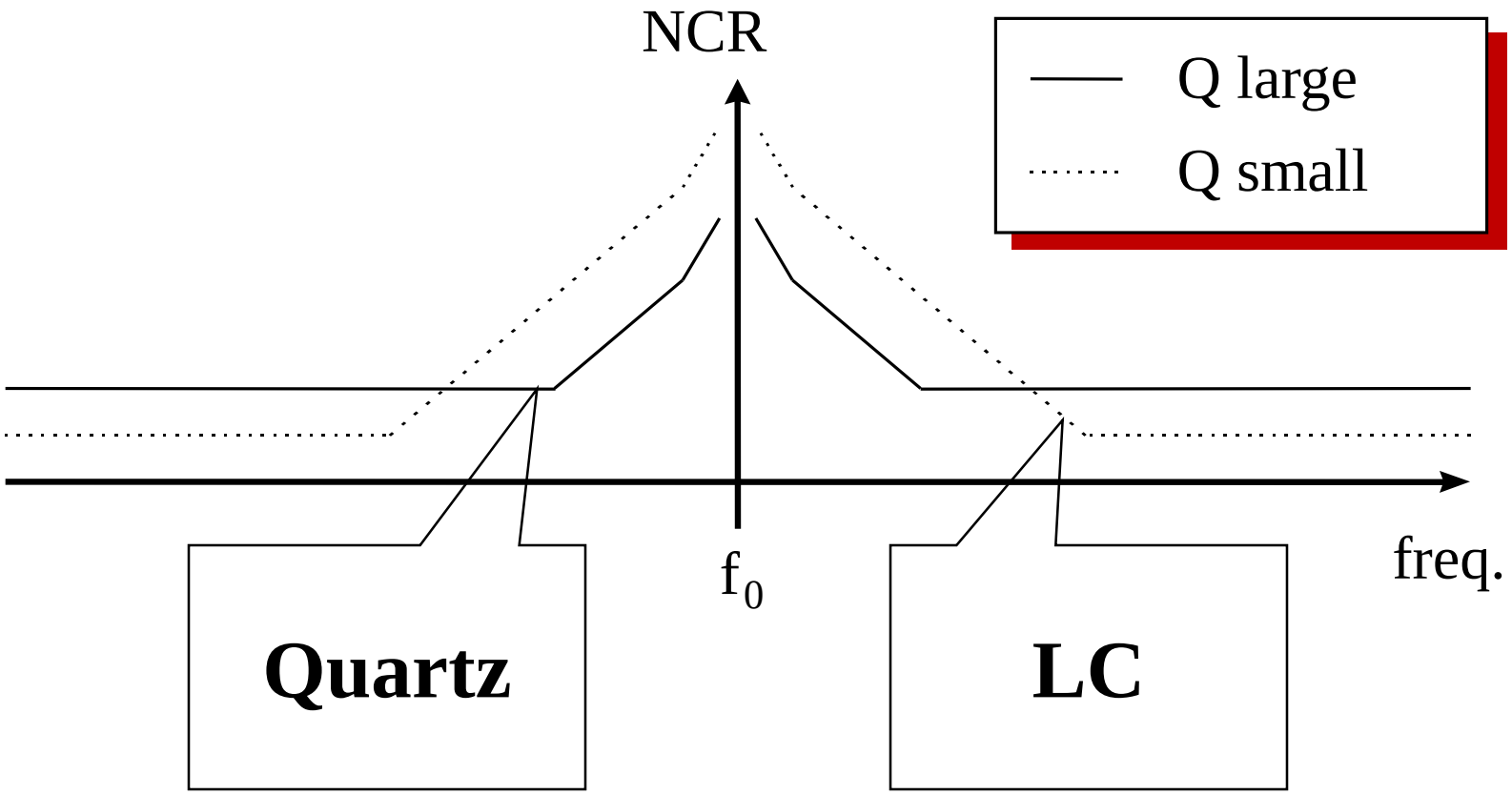
$$P_{pn} = \frac{kTBGF}{2}$$

$$NCR = \frac{kTGF}{2P_{sig}}$$



$$NCR_{ci} = \frac{kTGF}{2P_{sig}} \left(\frac{f_0}{2Q} \right)^2 \left(\frac{1}{f_m^2} \right)$$

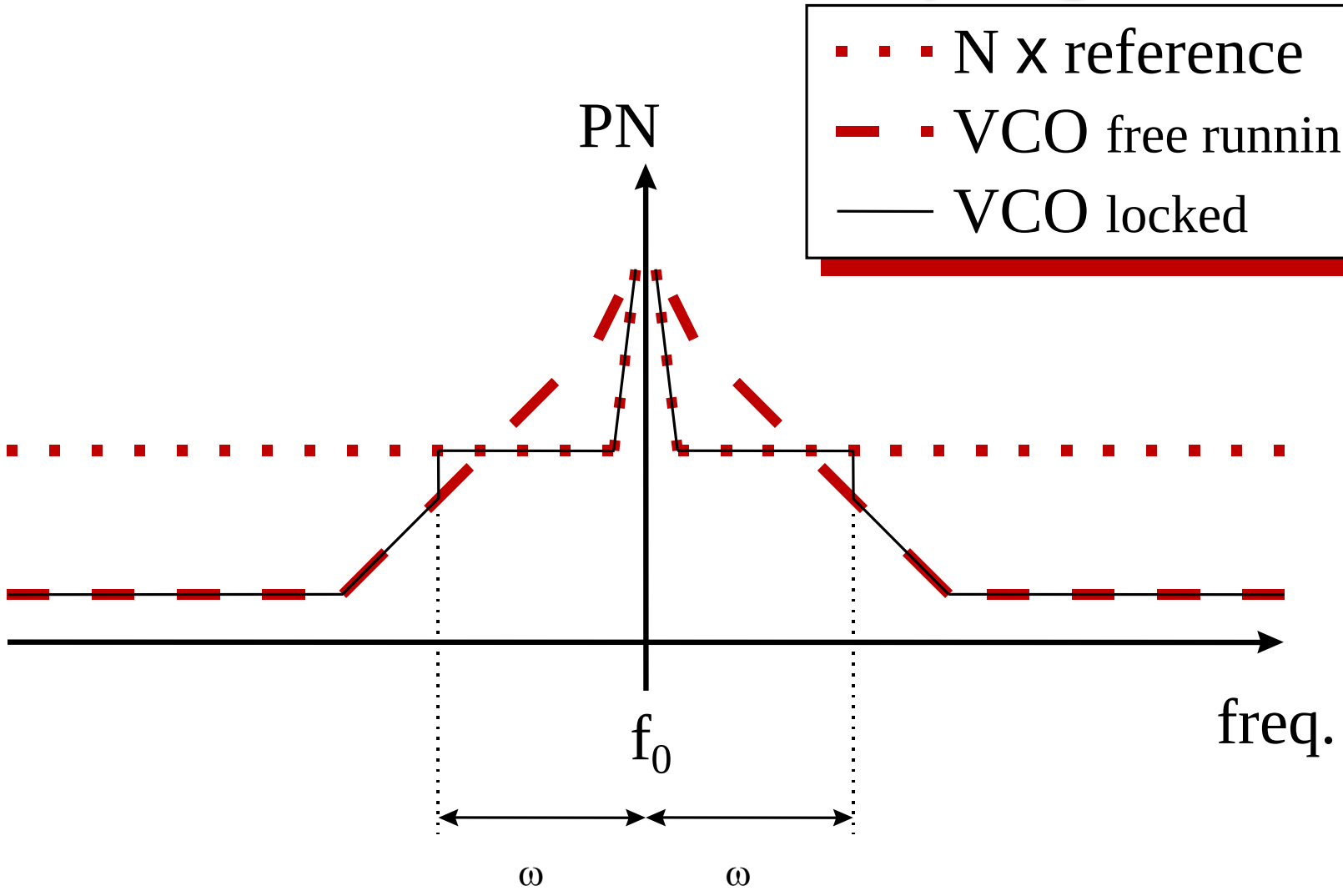
NCR : effect of Q



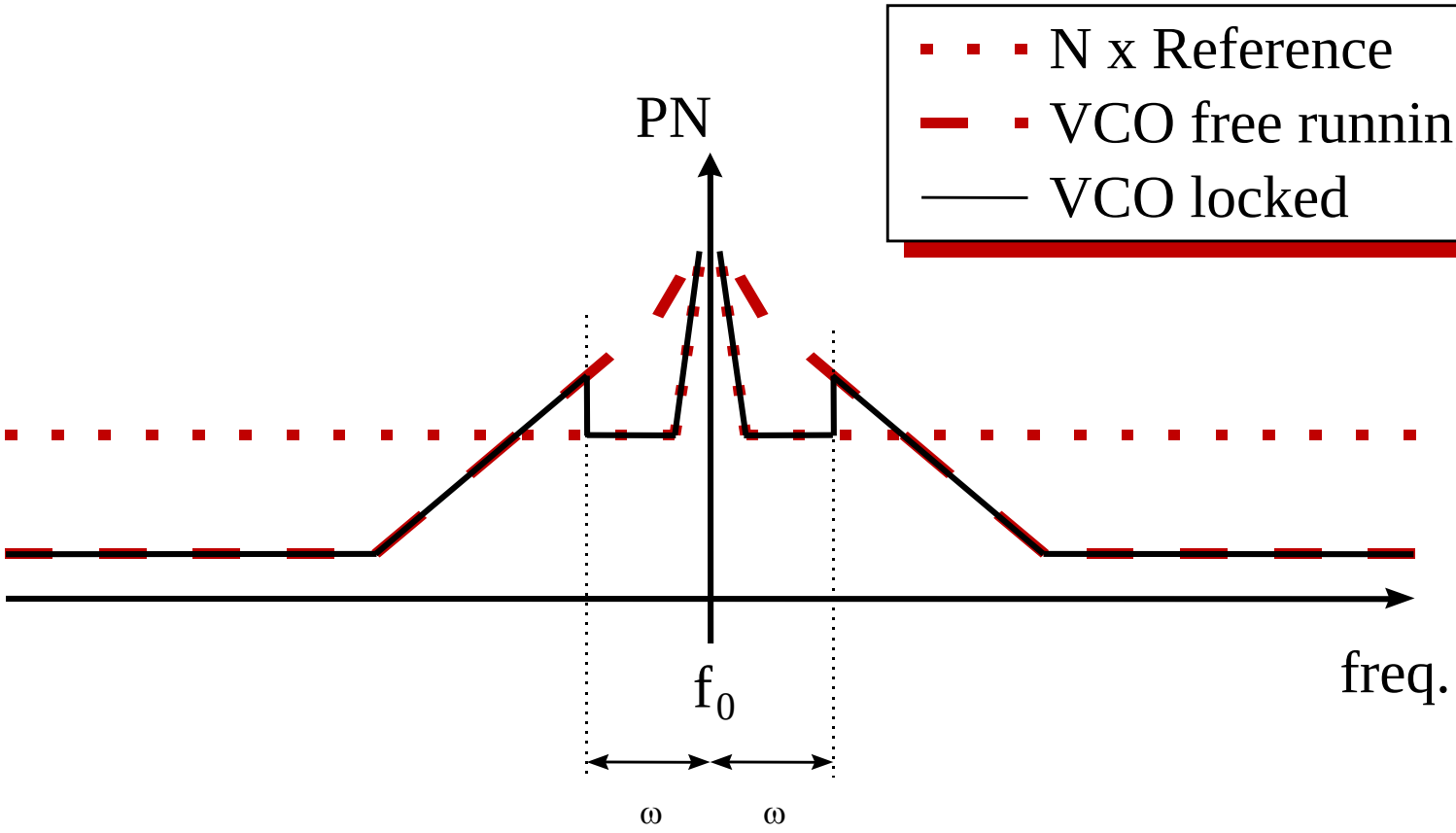
Outline

- Phase noise in oscillators
- Noise shaping in PLL
- PLL architectures

PLL noise shaping



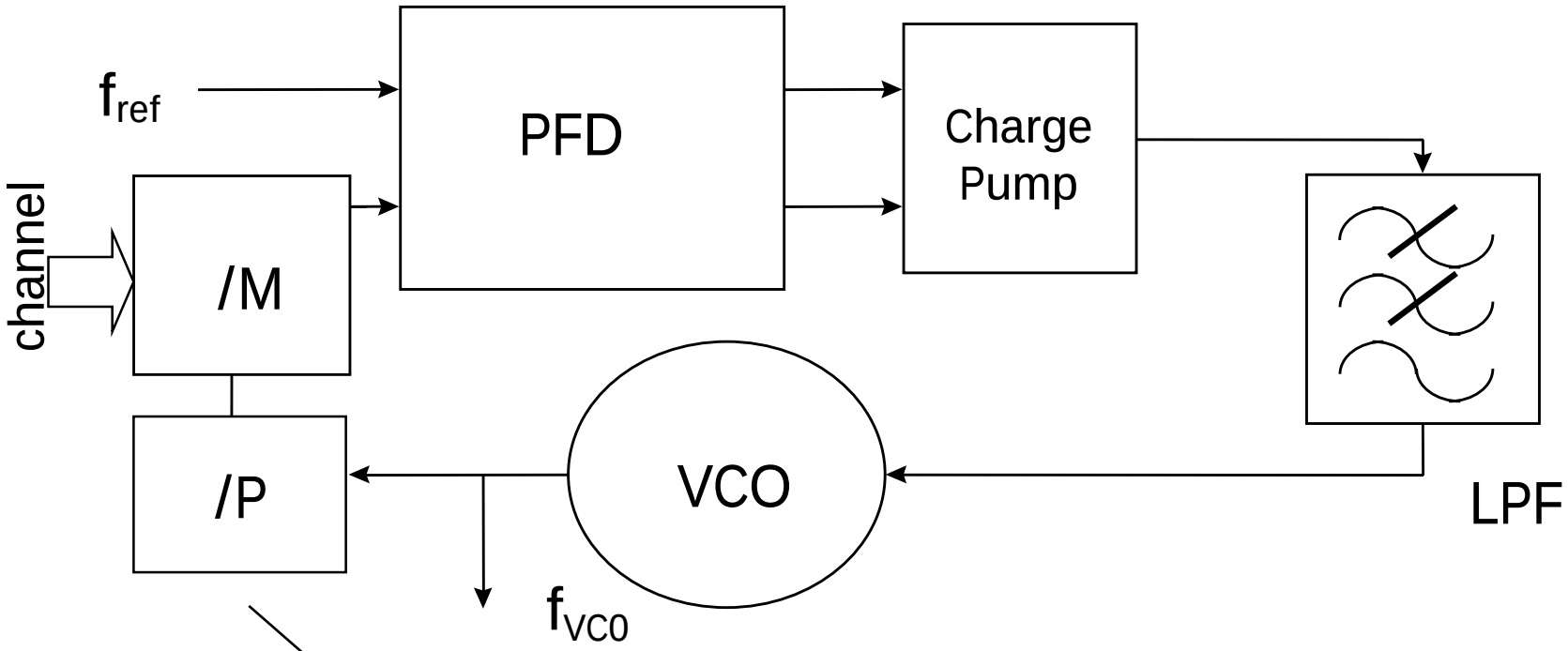
Limited PLL bandwidth



Outline

- Phase noise in oscillators
- Noise shaping in PLL
- PLL architectures

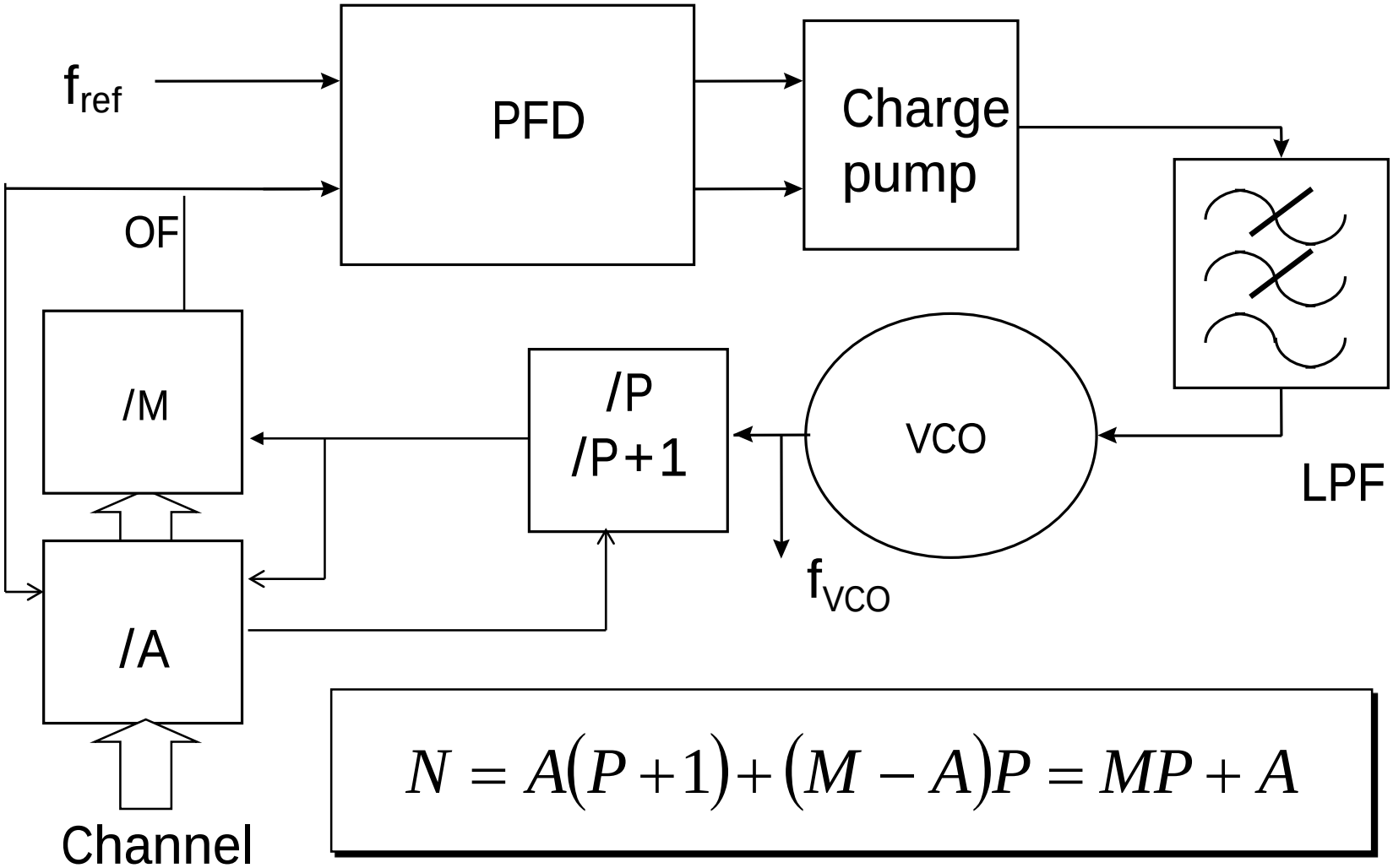
Integer-N PLL



Pre-divider used for very high frequencies

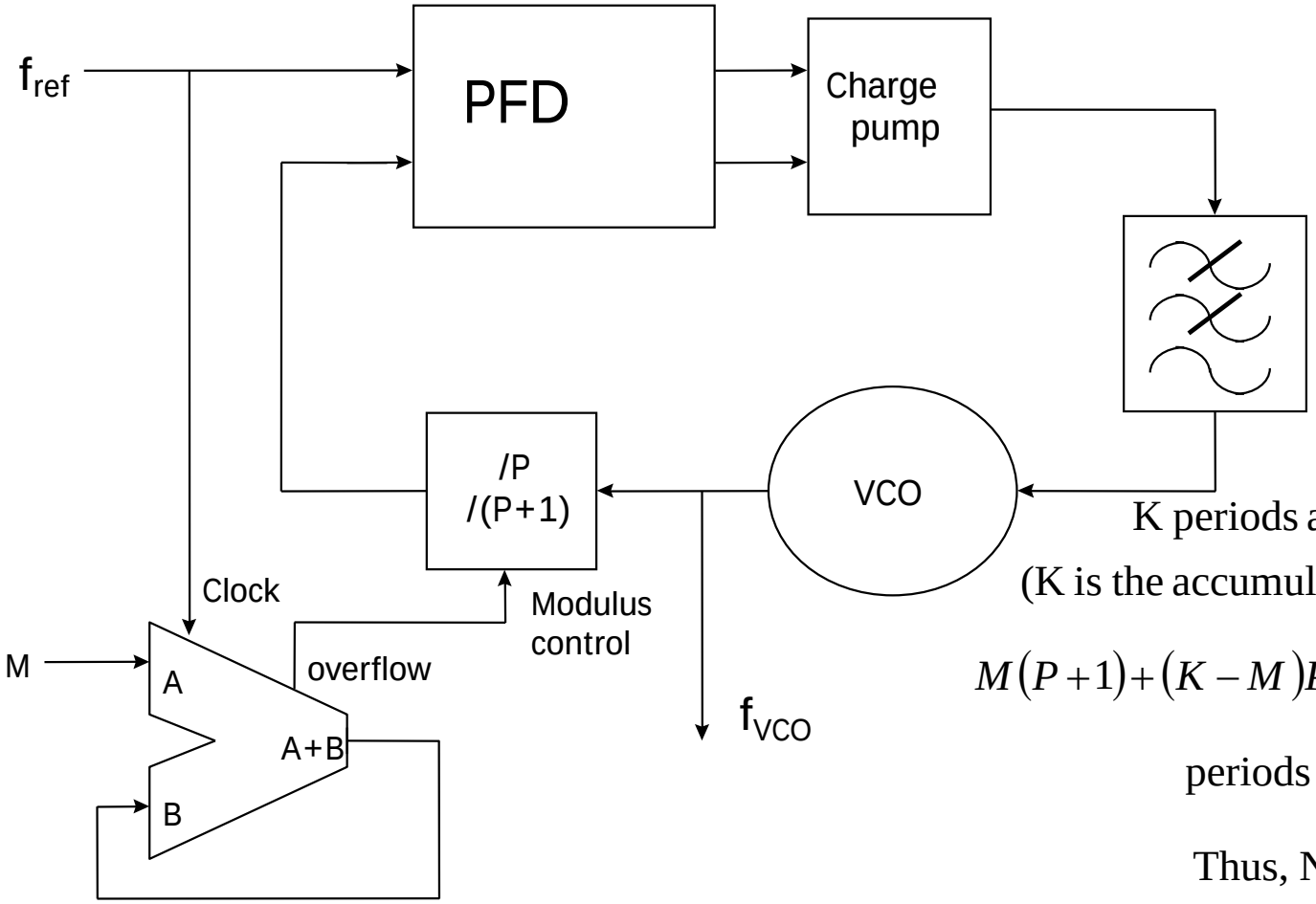
$$N = MP$$

Integer-N & dual-modulus



$$N = A(P+1) + (M-A)P = MP + A$$

Fract-N synthesizers



K periods at the input yield

(K is the accumulator lenght, so K > M) :

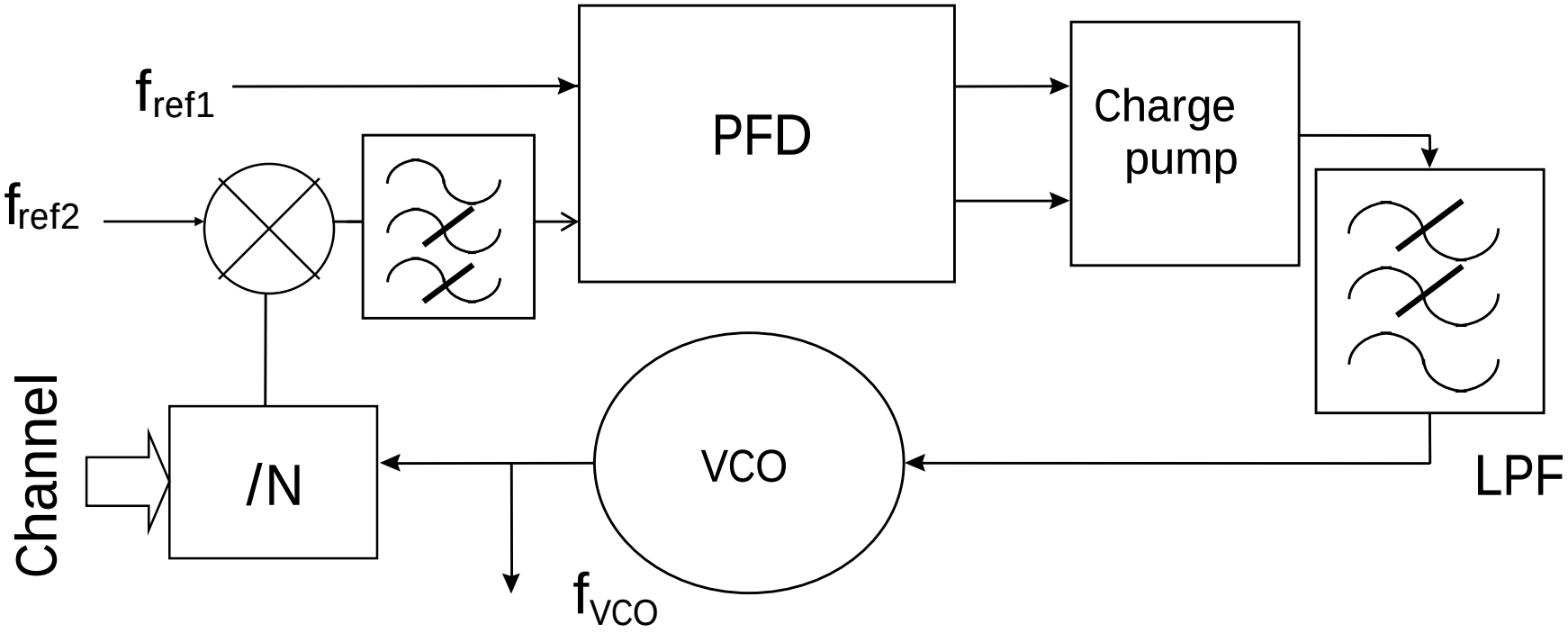
$$M(P+1)+(K-M)P = M+KP = K\left(P+\frac{M}{K}\right)$$

periods at the output.

Thus, $N = \left(P+\frac{M}{K}\right)$

N goes from P to (P +1) when M goes from 0 to K.

Offset synthesizer

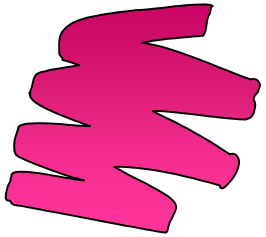


$$f_{VCO} = N \cdot \left(f_{ref\,1} - f_{ref\,2} \right) = N \cdot f_{ref}$$

Comparison is still preformed at f_{ref1} !

Conclusion

- Integrated VCO present strong limitations due to silicon technologies (low resistivity substrate)
- Low cost technologies for high volume production will not solve the problems
- Improvement of frequency generation relies on novel synthesizer characteristics



Hot topic

Tutorial on Frequency Synthesis

Part III – Advanced Architectures

Pr. Yann DEVAL

May, 2017

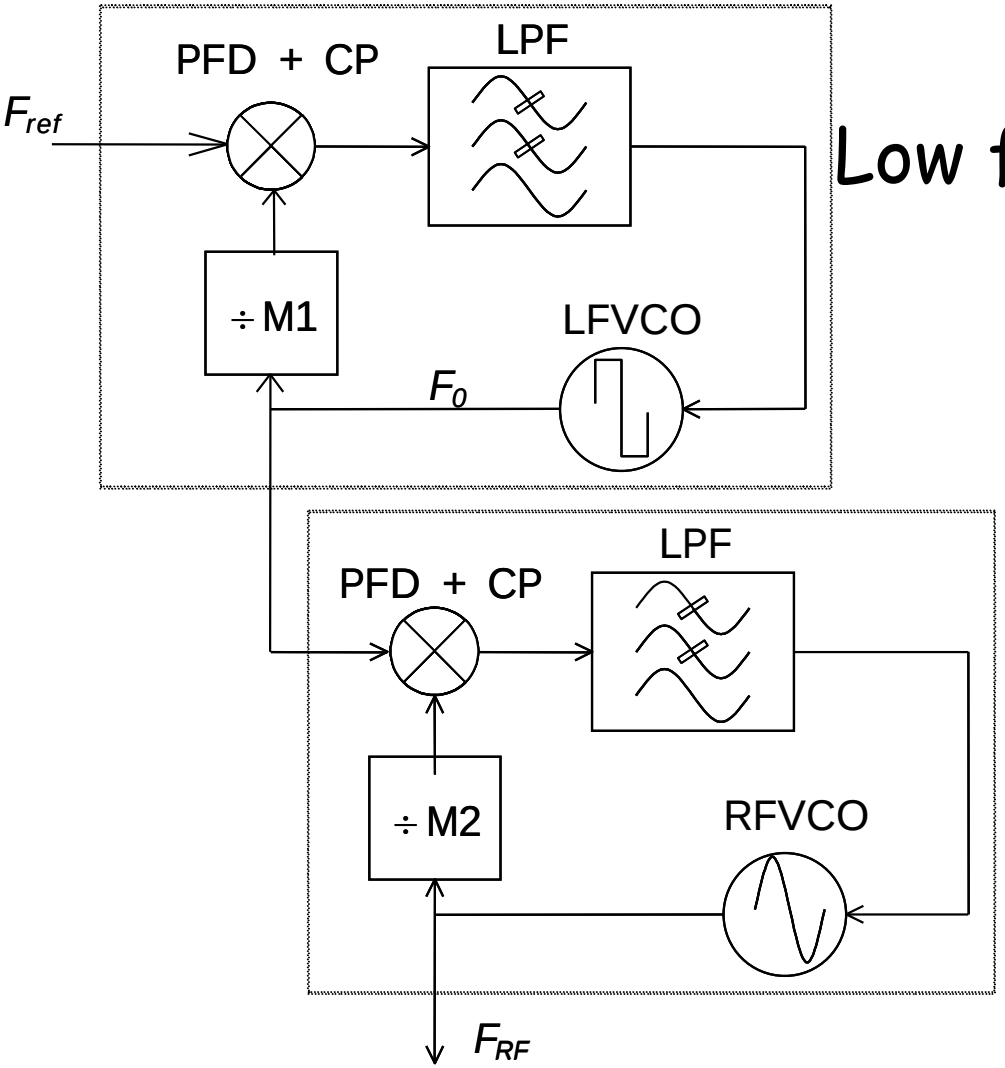
Outline

- Dual loop synthesizers
  - The Injection locked oscillator
- DLL-based synthesizers
  - Classical DLL
  - Factorial DLL
- All Digital PLL

Wide bandwidth synthesizer

- Swallow counter synthesizer
  - Channel spacing limitations
- Offset synthesizer
  - Several oscillators : coupling & pulling
- Fractional synthesizer
  - Spurious
- Multi-loop synthesizer
  - Complexity

Double-Loop Synthesizer



Low frequency loop

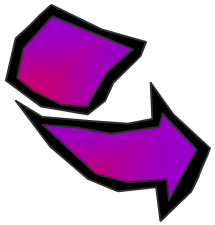
RF loop

Double-loop synthesizer : bandwidth improvement

$$B_{3dB} = \frac{\omega_n}{2\pi} \cdot \sqrt{2\zeta^2 + 1 + \sqrt{\left(2\zeta^2 + 1\right)^2 + 1}} \approx \frac{\omega_n}{\pi}$$

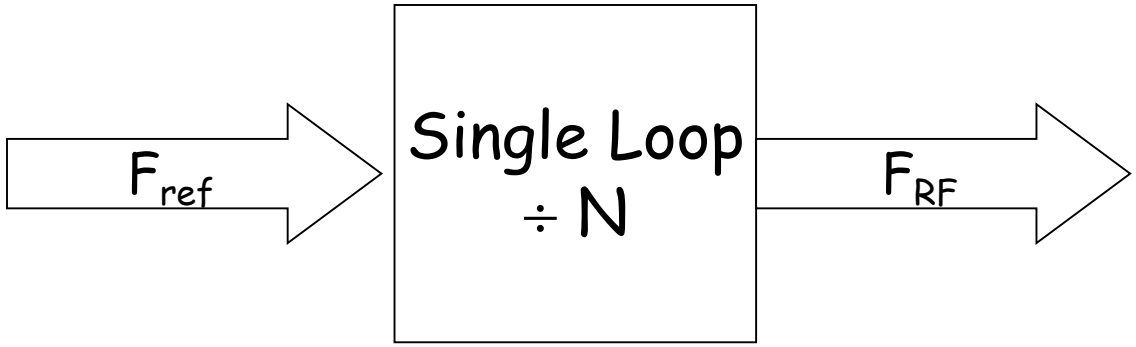
Natural frequency :

$$\omega_n = \frac{1}{\sqrt{N}} \bullet \sqrt{\frac{K_\phi K_0}{\tau_1}} = \frac{\omega_{PLL}}{\sqrt{N}}$$

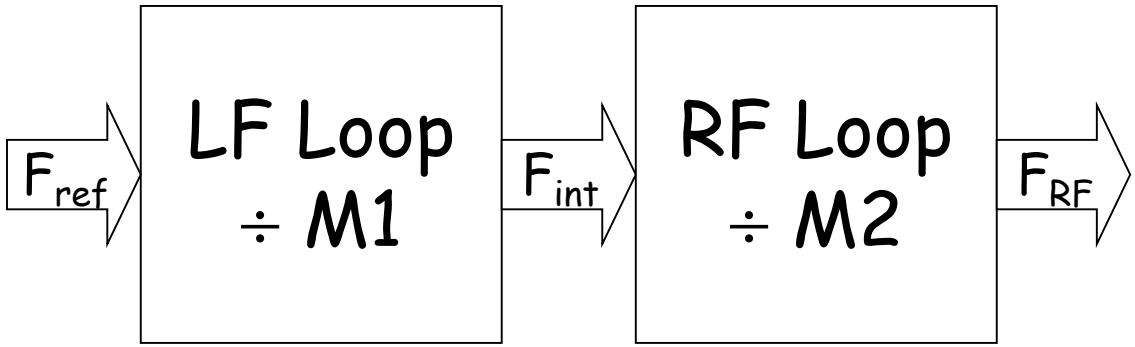


$$B_{3dB} \propto \frac{1}{\sqrt{N}}$$

Double-loop synthesizer : bandwidth improvement



$$B_{3dB} = \frac{K}{\sqrt{N}}$$



$$B_{3dB} \approx \frac{K}{\sqrt{M1}}$$

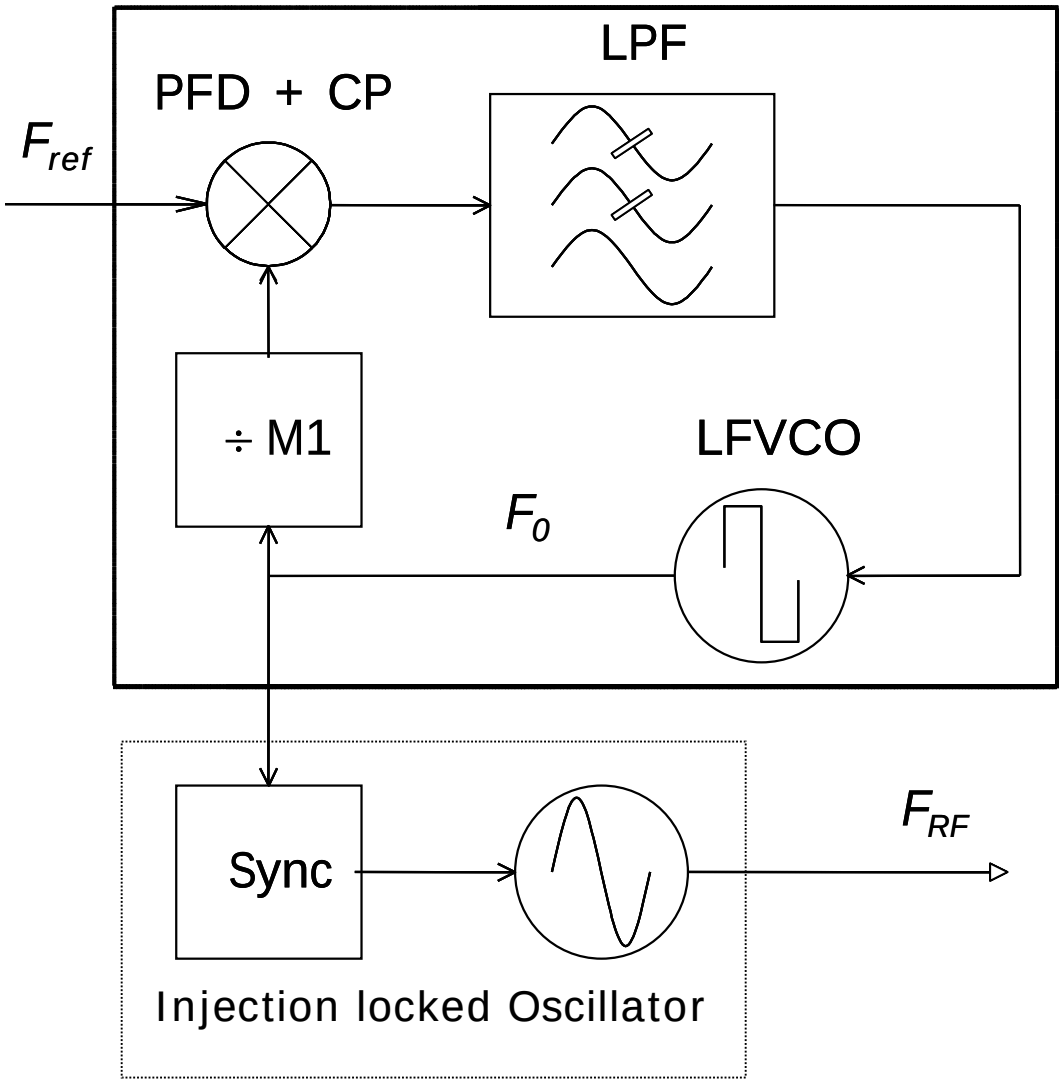
$$B_{3dB}^{LF} = \frac{K}{\sqrt{M1}} \qquad B_{3dB}^{RF} = \frac{K'}{\sqrt{M2}}$$

$$N = M1 \cdot M2 \Rightarrow B_{DLoop} \approx \sqrt{M2} \cdot \frac{K}{\sqrt{N}} = \sqrt{M2} \cdot B_{SLoop}$$

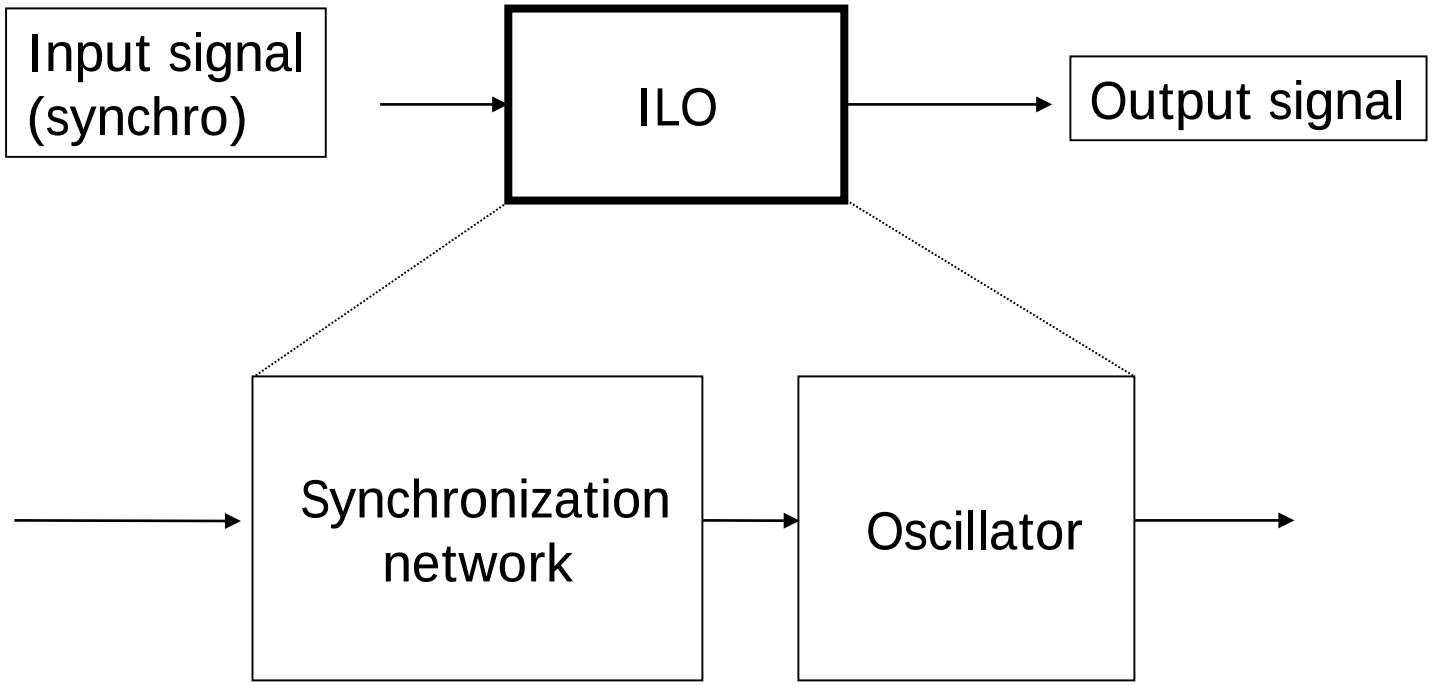
Double-loop synthesizer : the drawbacks

- Complexity
  - Silicon & power consumption
  - Coupling effects
- High frequency RF loop reference
  - PFD dead zone
  - Charge pump bandwidth

The ILO-based synthesizer



The ILO as the RF loop



The 'sub-harmonic' ILO principle

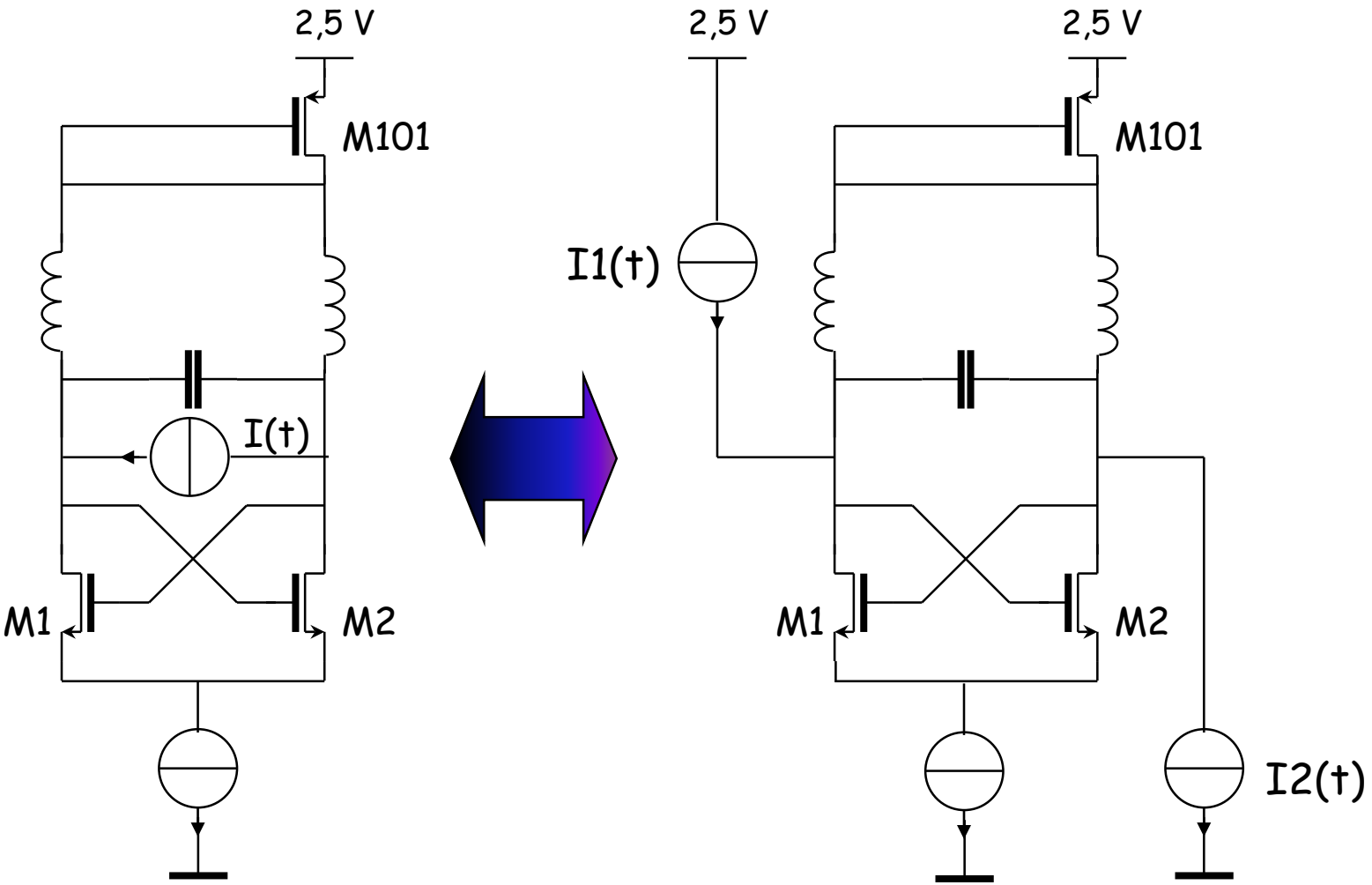
The ILO theory

Huntoon & Weiss (1947) and Badets (1999)

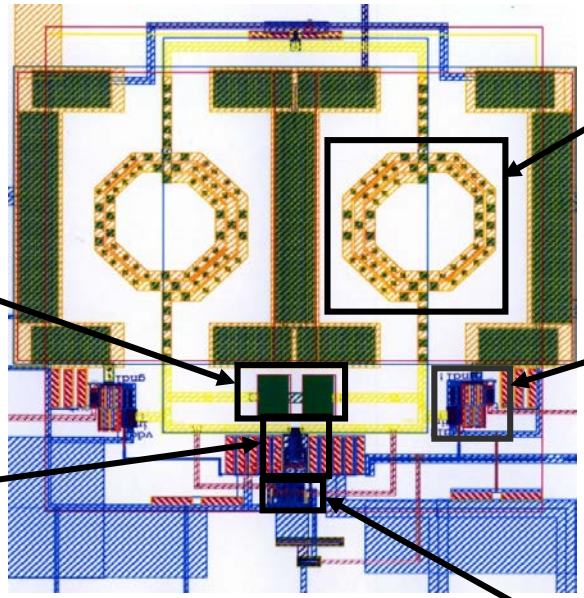
$$\Delta F = \mathbf{2} \cdot \frac{|I_{syn}|}{|V_0|} \cdot \sqrt{F_g^{\,2} + F_b^{\,2}}$$

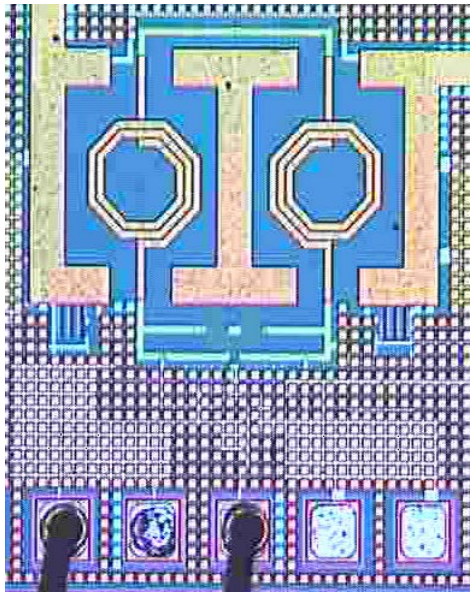
Wideband synthesizer → **Wide synchronization range ILO**

Differential current generator

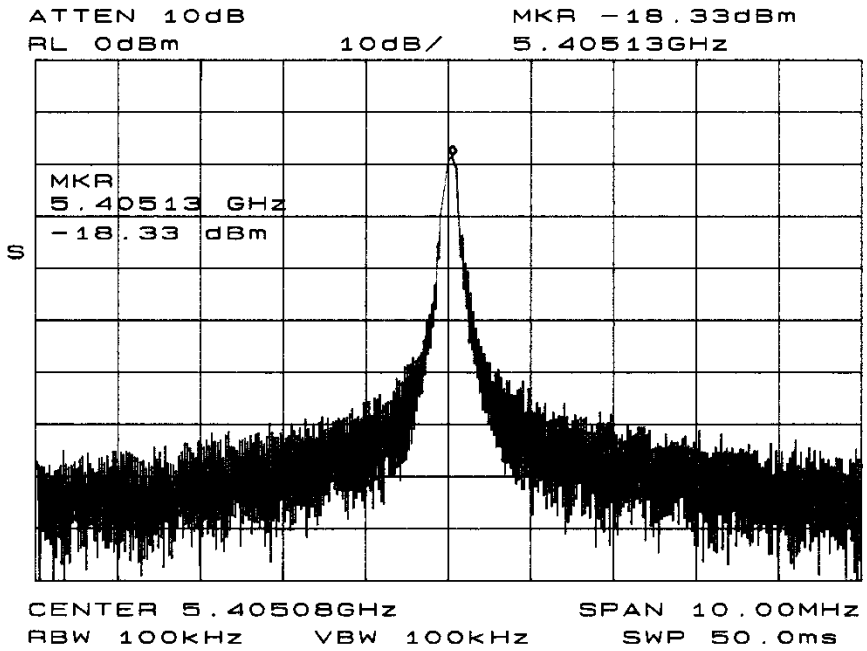


5.4 GHz SO test chip (6M 0.25µm VLSI CMOS)



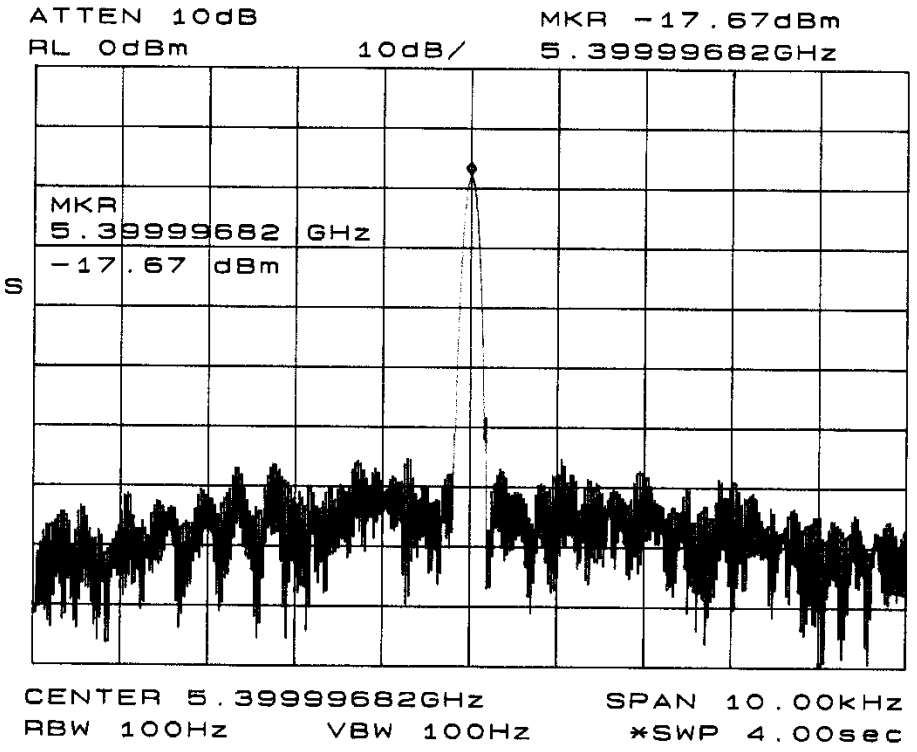


The CMOS version



SR = 150 MHz

12.5 mW



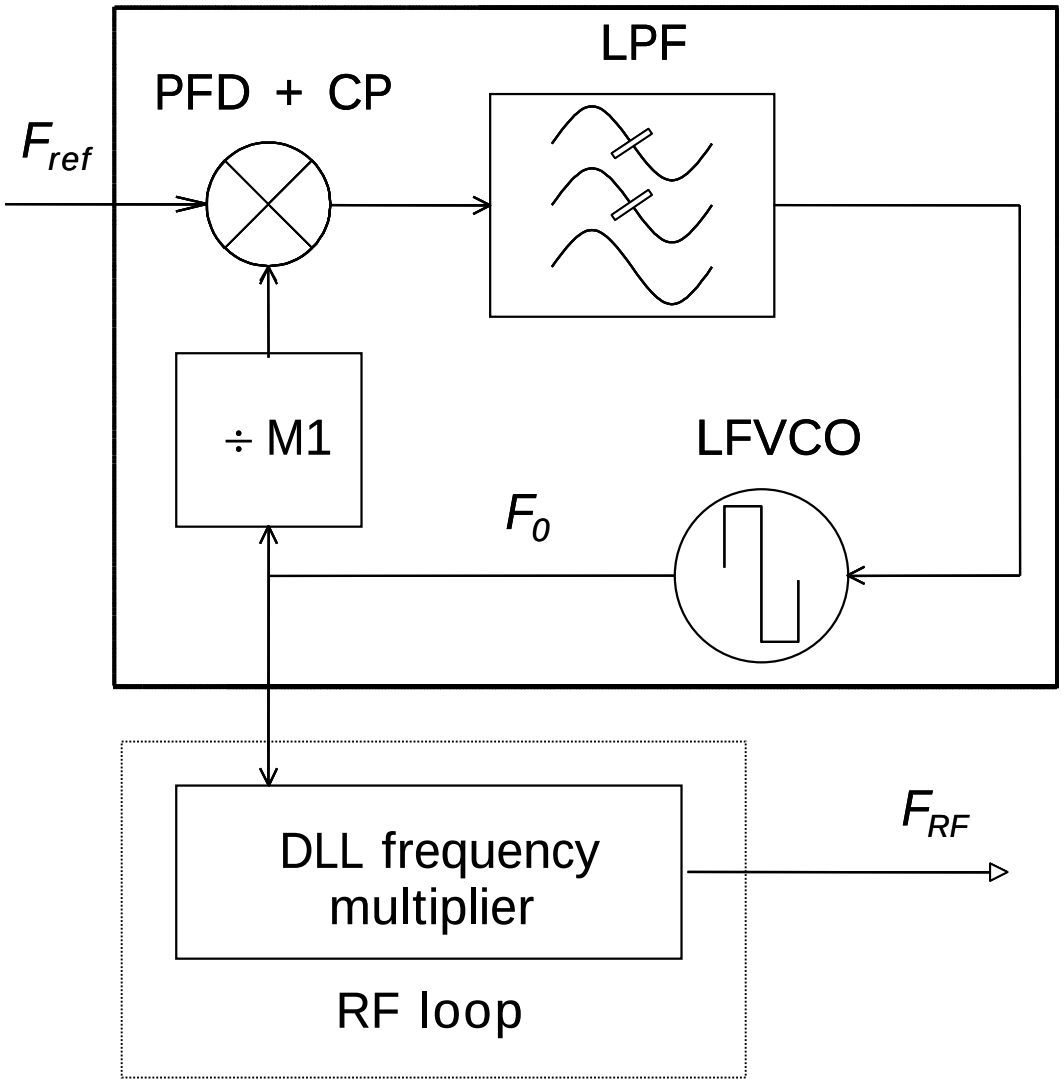
Summarize - ILO

- ILO as a frequency generation device
  - Easy to use - thanks to the theory
- ILO-based synthesizer
  - Wideband
  - Low-power
  - Low-complexity
  - Low silicon area

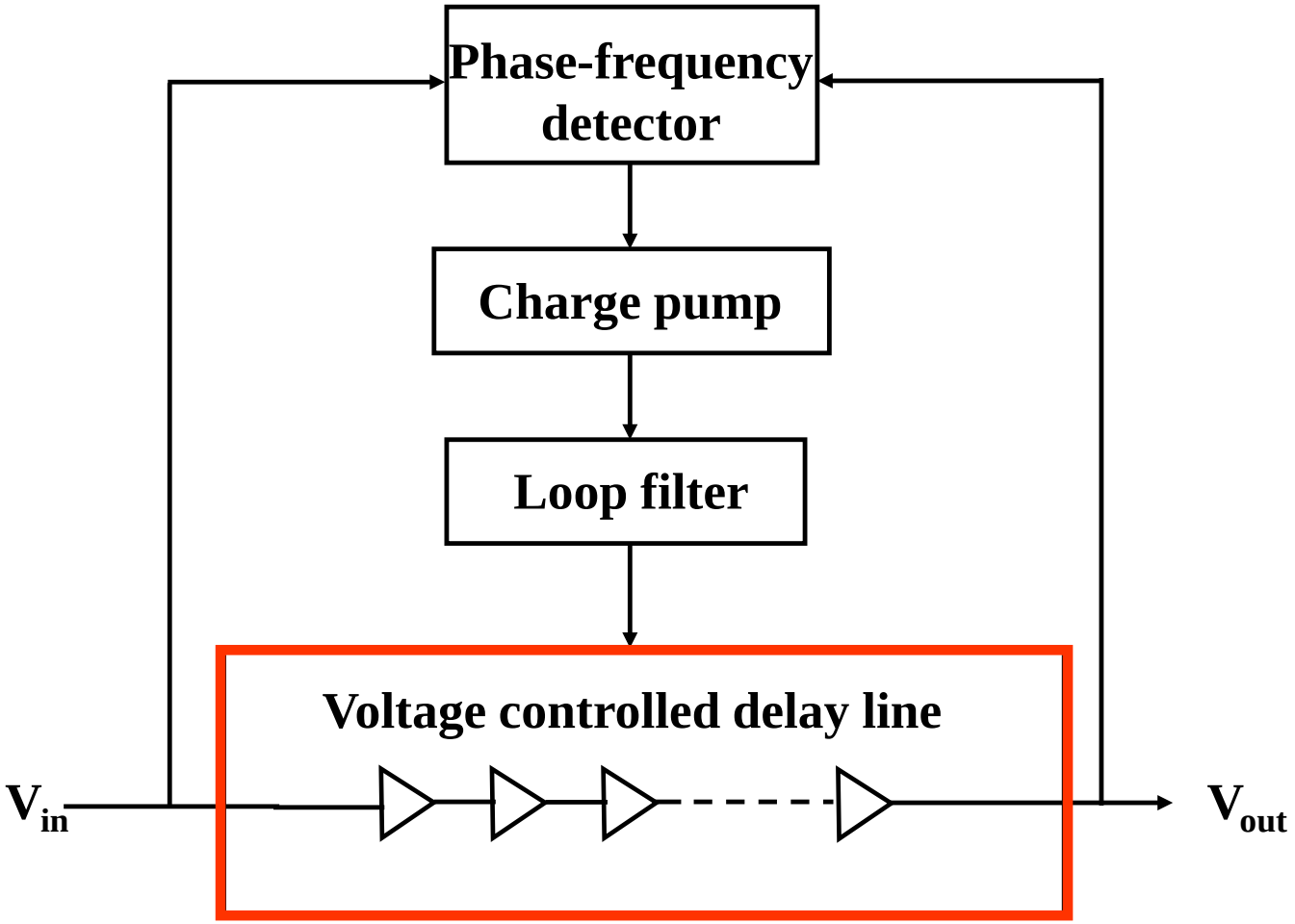
Outline

- Dual loop synthesizers
  - The synchronous oscillator
- DLL-based synthesizers
  - Classical DLL
  - Factorial DLL
- All Digital PLL

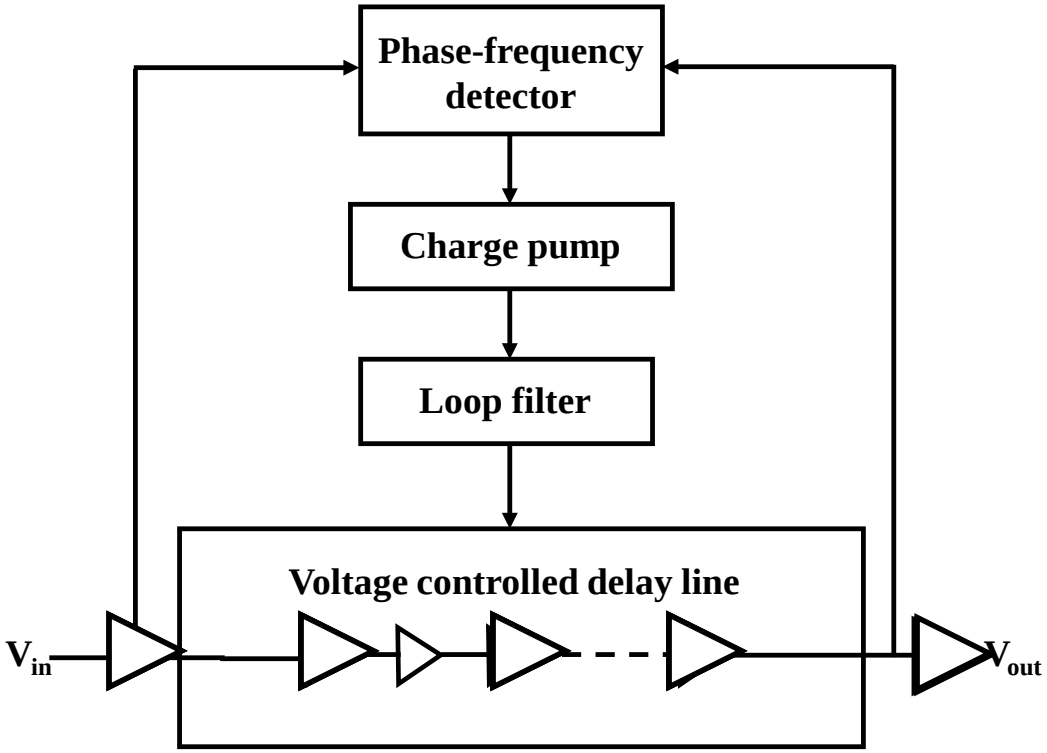
The DLL-based synthesizer

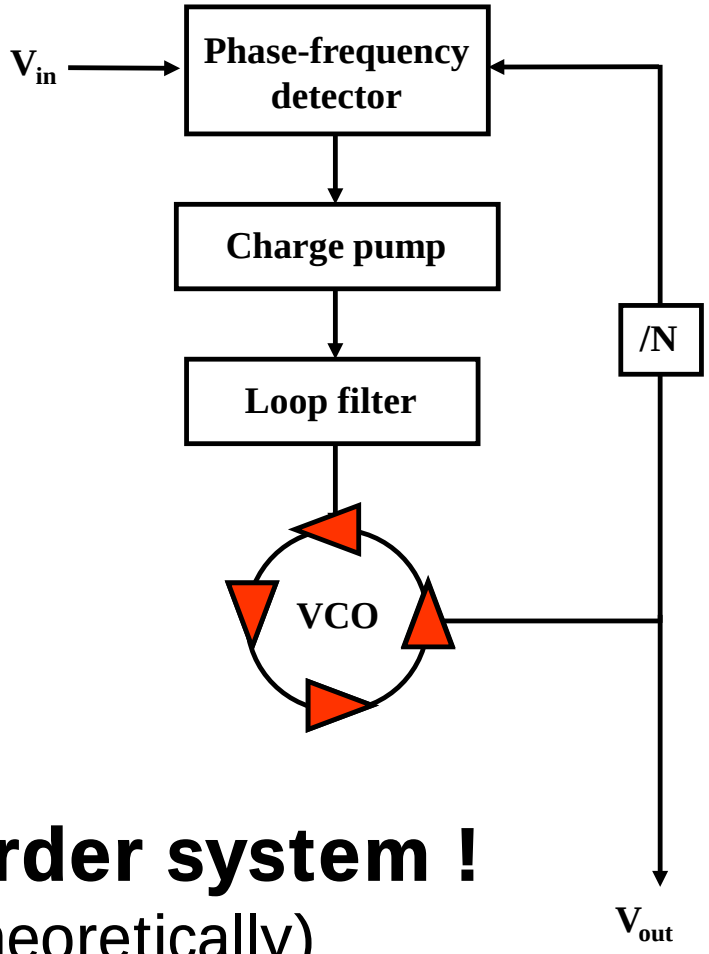


Delay Locked Loop



Delay Locked Loop / Phase Locked Loop

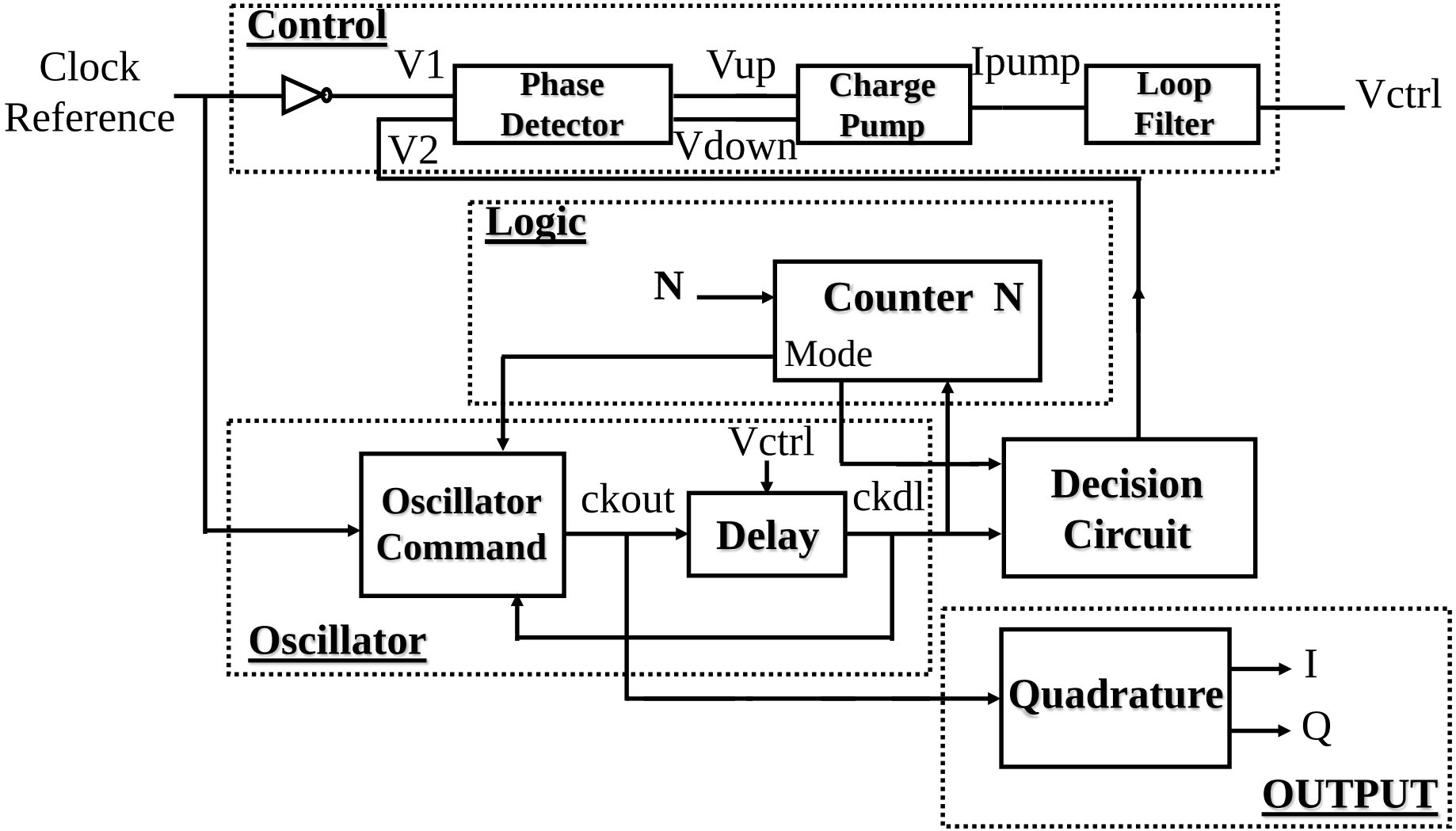




No VCO means 1st order system !

- Stability is guaranteed (theoretically)
- High bandwidth is feasible

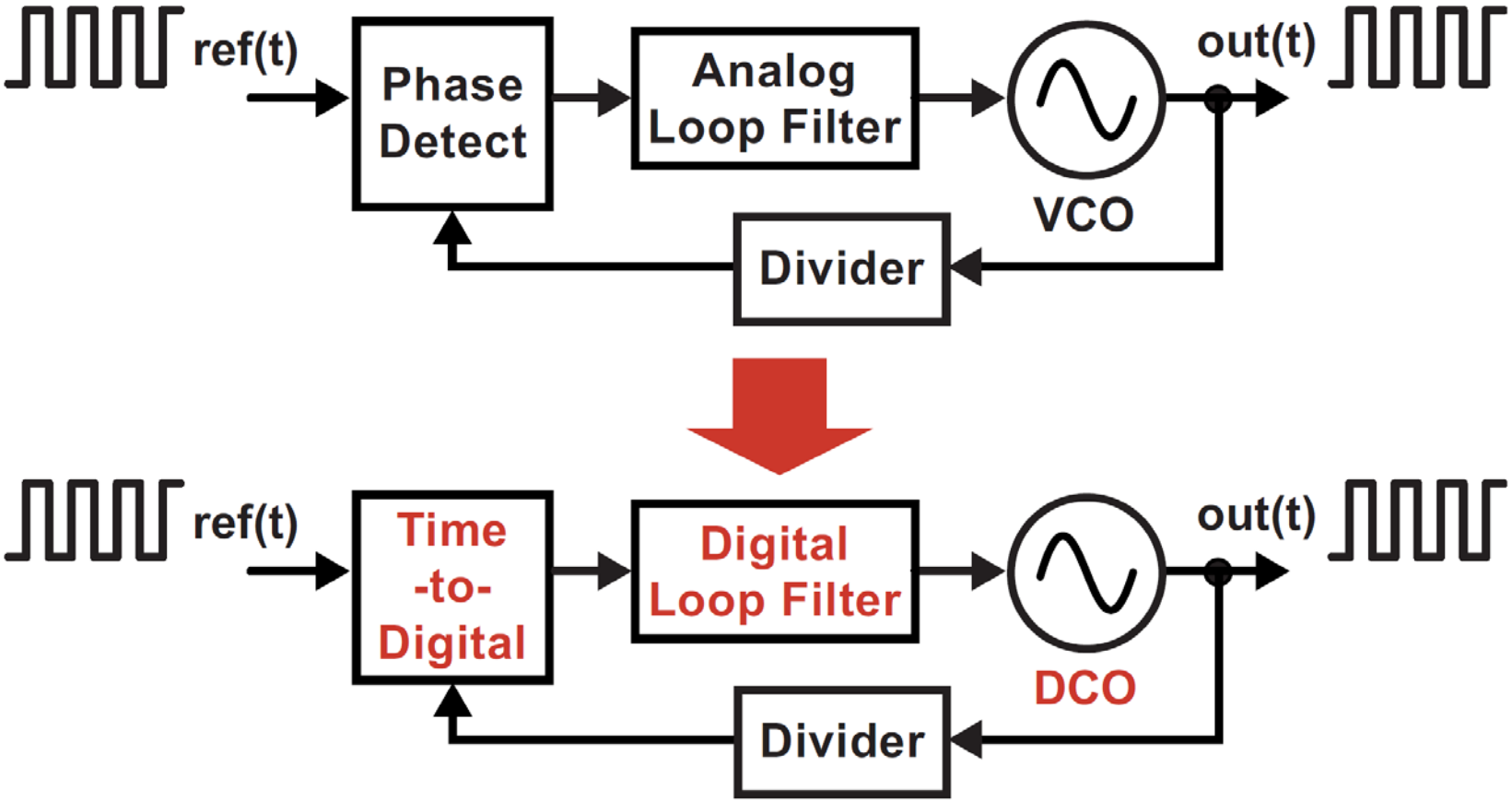
The Factorial DLL



Outline

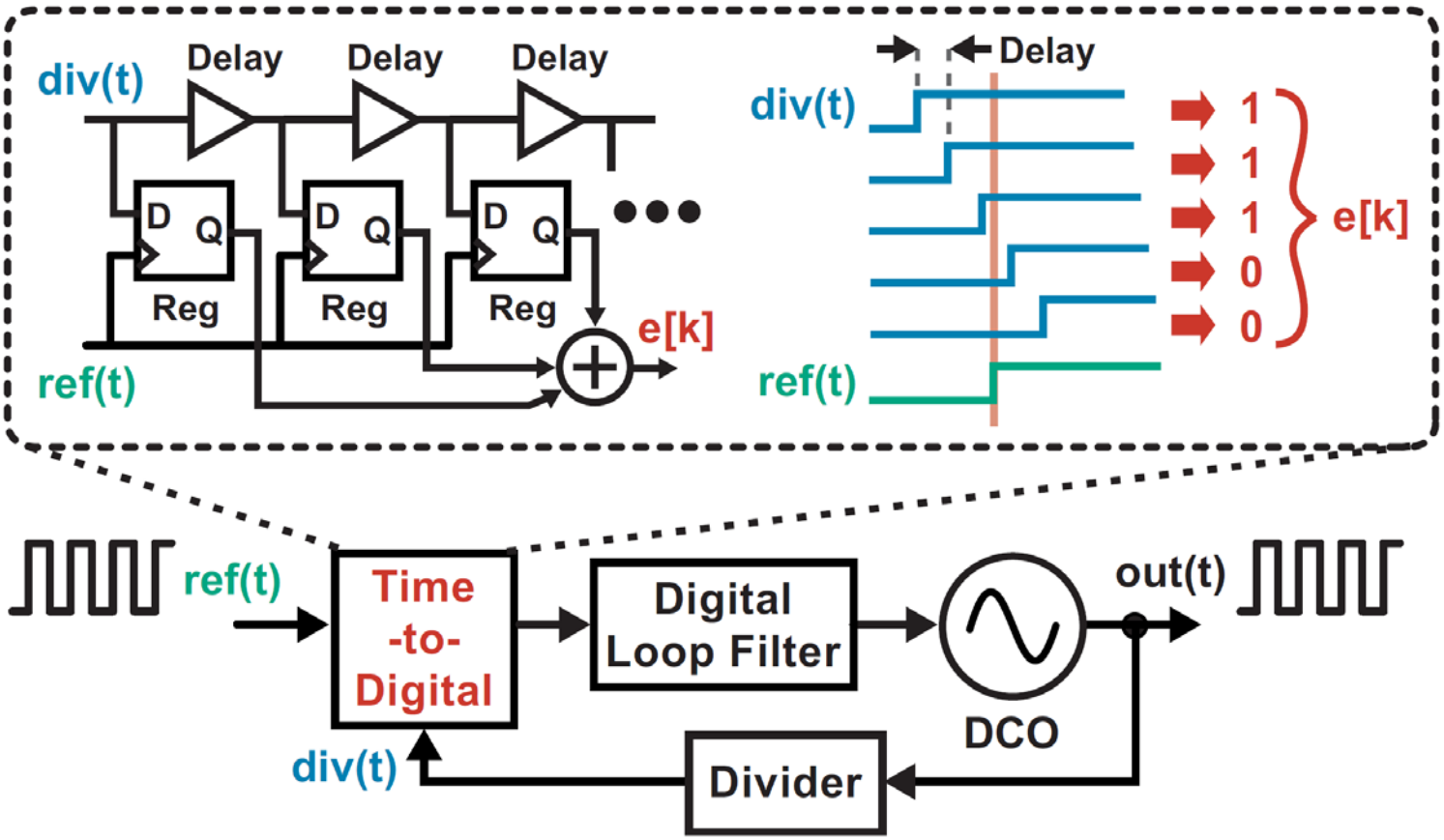
- Dual loop synthesizers
  - The synchronous oscillator
- DLL-based synthesizers
  - Classical DLL
  - Factorial DLL
- All Digital PLL

PLL : from analog to digital



From M. PERROTT

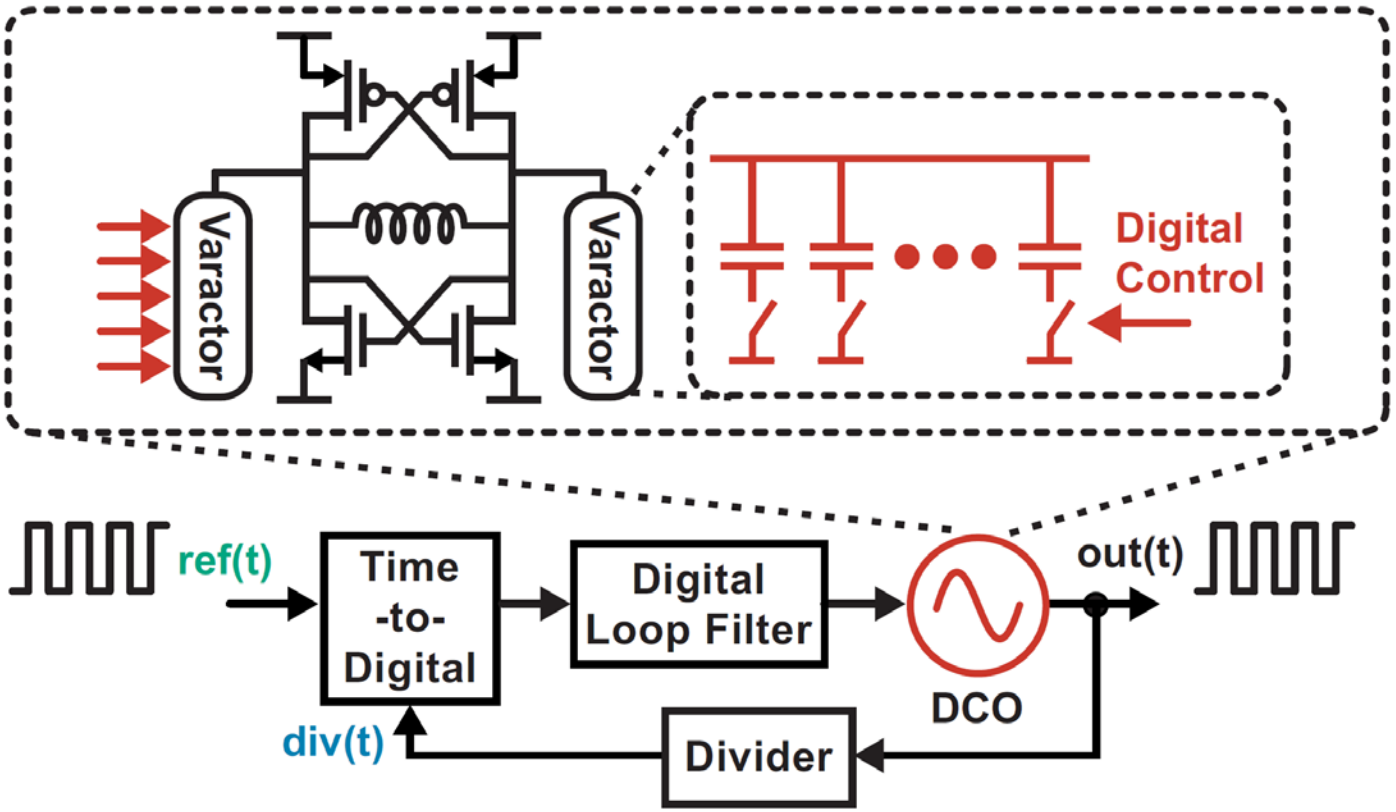
Time-to-Digital Converter (TDC)



- Time resolution is fixed by the delay line and its delay cell
- Similar to a flash converter

From M. PERROTT

Digitally Controlled Oscillator (DCO)

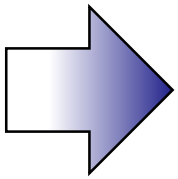


- Frequency resolution is fixed by the unit capacitor
- Flat C(V) zones are targeted to add noise margin

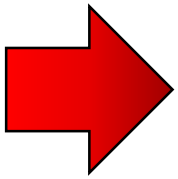
From M. PERROTT

AD-PLL issues

- Time resolution adds quantification noise from the TDC
- Frequency resolution generates spurs



Dithering is mandatory ($\Delta\Sigma$ modulator) to achieve proper accuracy and purity



Complexity dramatically increased

Conclusion

- Not only PLL are of interest whenever one wants to deal with frequency generation
- New architectures are still to be find
- The more digital the approach, the better for flexibility
- Wideband topologies are required to deal with noisy (fully integrated) oscillators
- Accuracy yields complexity
- CAD tools are not an option