Switched Mode Power Supply (DC/DC buck converter)

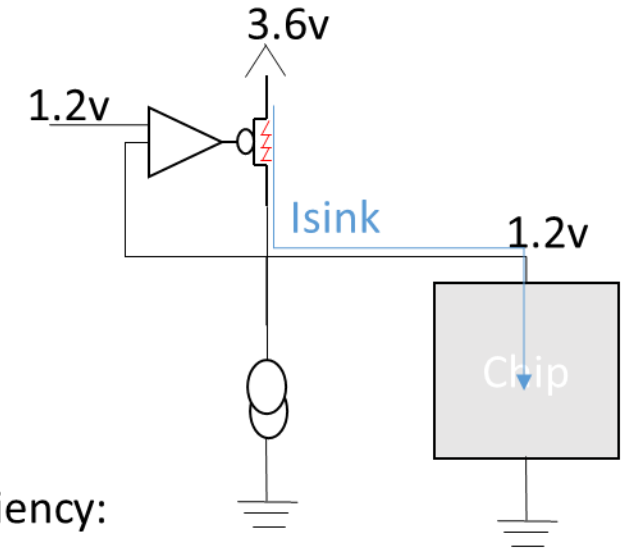
1-Why use a DC/DC converter ?
2-Architecture
3-Conduction modes
- Continuous Conduction Mode
- Discontinuous Conduction Mode

4-Stability
- Voltage Mode
- Current Mode
- Modulator transfer function
- Filter transfer function
- Compensator transfer function
- Overall transfer function

5-Efficiency
6-Characteristics

Why use a DC/DC converter ?

Regulation using a Low Drop Out regulator:



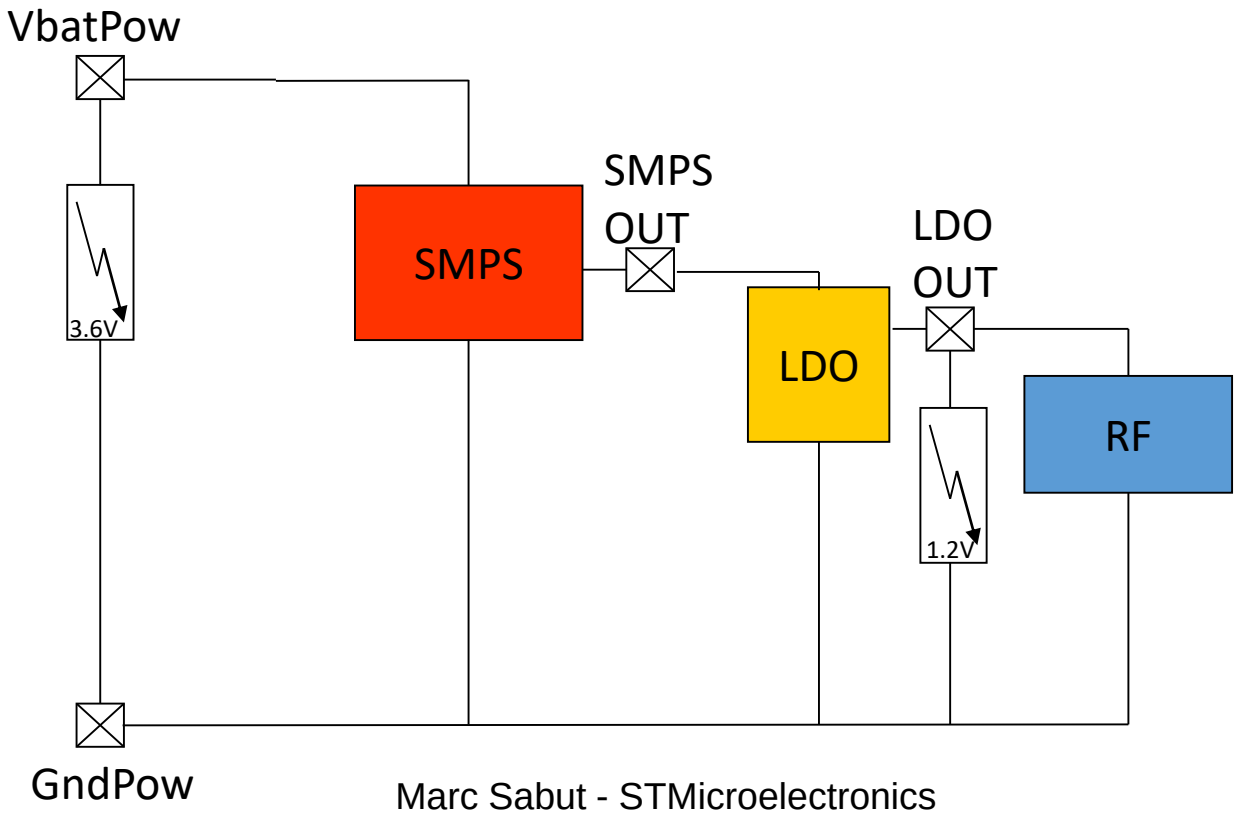
This kind of regulation leads to a poor efficiency:

$$P_{battery} = 3.6 * I_{sink}$$
$$P_{out} = 1.2 * I_{sink}$$

$$efficiency = {Pout}/{Pbat} = 1/3$$

Why use a DC/DC converter ?

The SMPS converts the battery voltage to a lower voltage with high efficiency. That is, little power is lost in the converter itself. An SMPS output voltage of only 100mV above the LDO output voltage is sufficient for the LDO to perform normally. Thus, the LDO efficiency is in turn greatly improved.
The role of the LDO is to filter the output voltage ripple produced by the SMPS.



Switched Mode Power Supply (DC/DC buck converter)

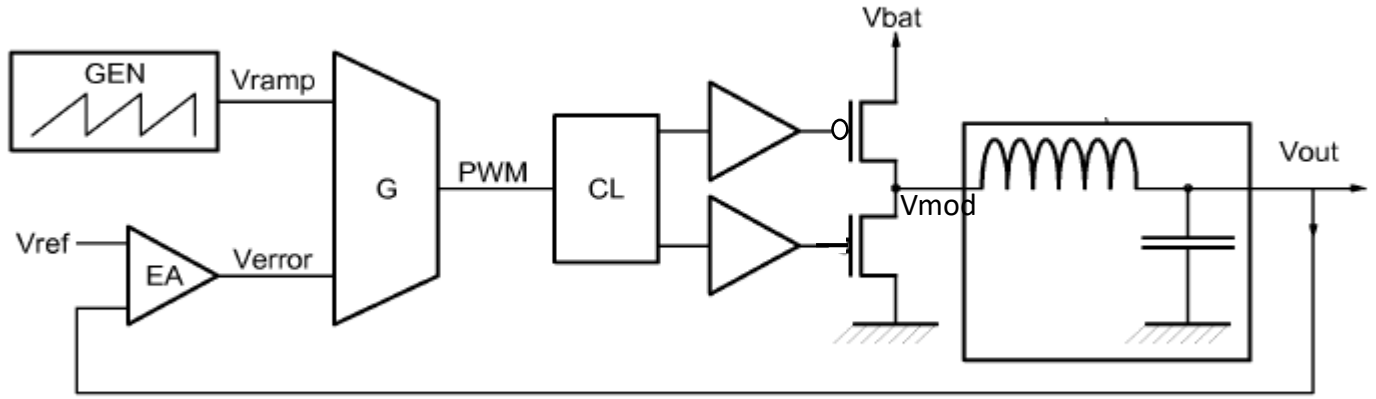
1-Why use a DC/DC converter ?
2-Architecture

Architecture

Buck or down converter: output voltage is lower than the battery voltage.

The following basic blocks combine to form a complete DC/DC converter:

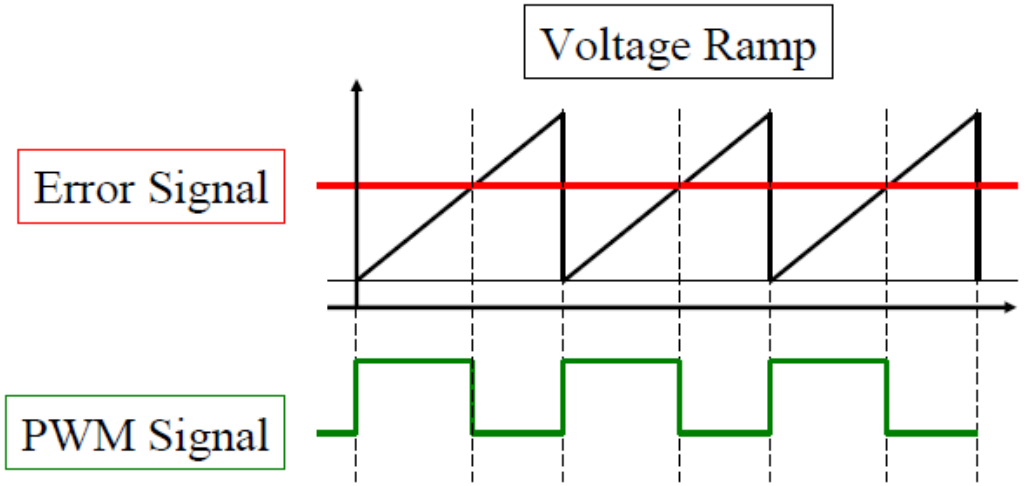
- Ramp generator
- Error amplifier
- Pulse Width Modulator
- Control logic
- Output filter



All elements can be integrated except the output filter which is made up of an external inductor (some microH) and capacitors (some microF). A parameter to keep in mind for integration purpose is the thickness of these components which must be compatible with the package.

Architecture

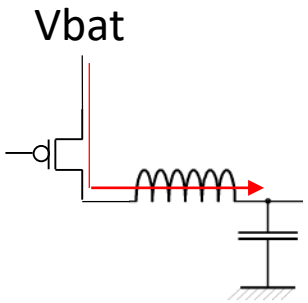
The error voltage is compared to the ramp voltage to produce a PWM signal which in turns set on or off the output power transistors.



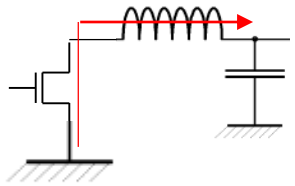
When the output voltage becomes lower than the reference voltage, the error signal increases so does the duty cycle of the PWM signal. Therefore, the power Pmos transistor is acting more frequently than the Nmos leading to a higher output current.

Architecture

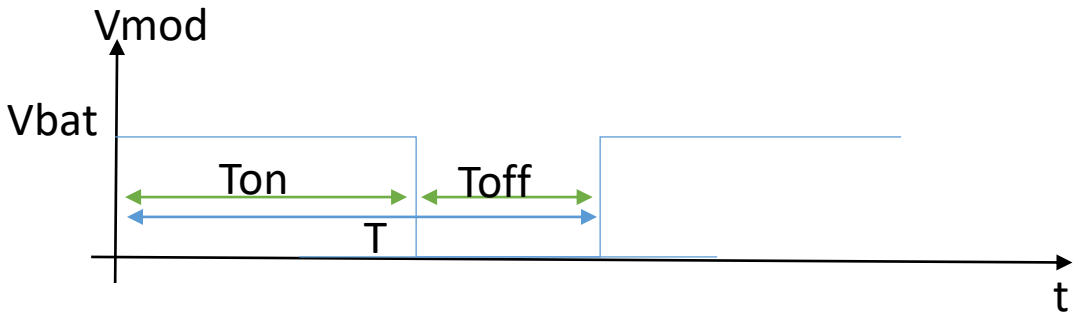
Pmos ON



Pmos OFF



The modulator output is a rectangular wave. This rectangle is averaged by the output filter and applied to the load.



The duty cycle is defined as :

$$D = \frac{T_{on}}{T_{on} + T_{off}}$$

Architecture

The output DC voltage is therefore the average of the rectangular pulse waveform, or:

$$V_{out} = \frac{1}{T}\int_0^T V_{mod}(t)dt = \frac{1}{T}\int_0^{t_{on}} V_{bat}\, dt = \frac{t_{on}}{T}V_{bat}$$

$$V_{out} = DV_{bat}$$

Where D is the duty cycle of the output and is defined as the time the output is connected to Vbat divided by the period of the witching frequency.
Notice that the frequency of the ramp signal determines the frequency of the modulator output, which is the switching frequency of the converter.

Switched Mode Power Supply (DC/DC buck converter)

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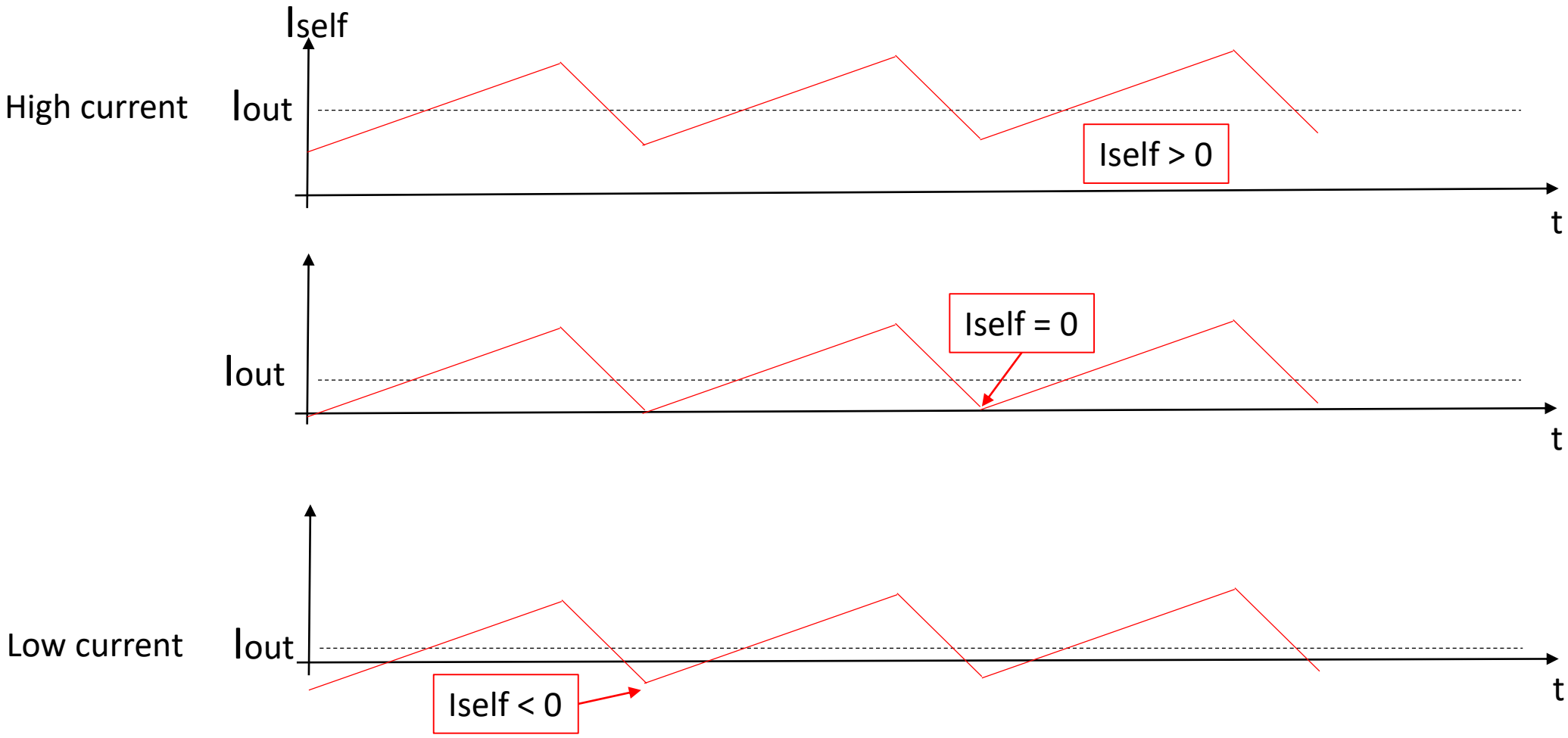
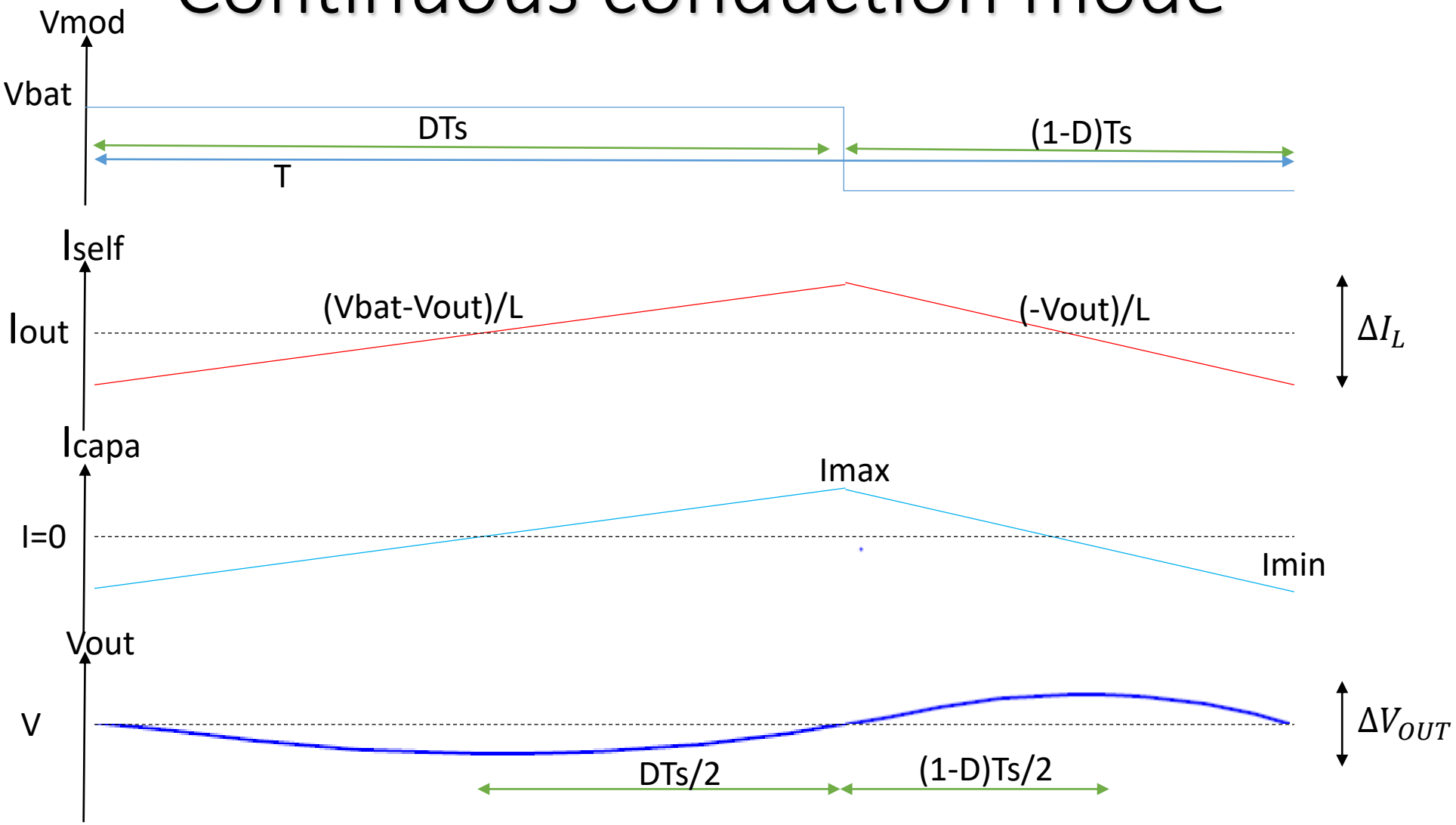
- Discontinuous Conduction Mode

Continuous conduction mode



Continuous conduction mode



Continuous conduction mode

Current ripple:

$$\Delta I_L = \frac{V_{bat} - V_{out}}{L} DTs = \frac{V_{bat}(1-D)D}{L.F_s}$$

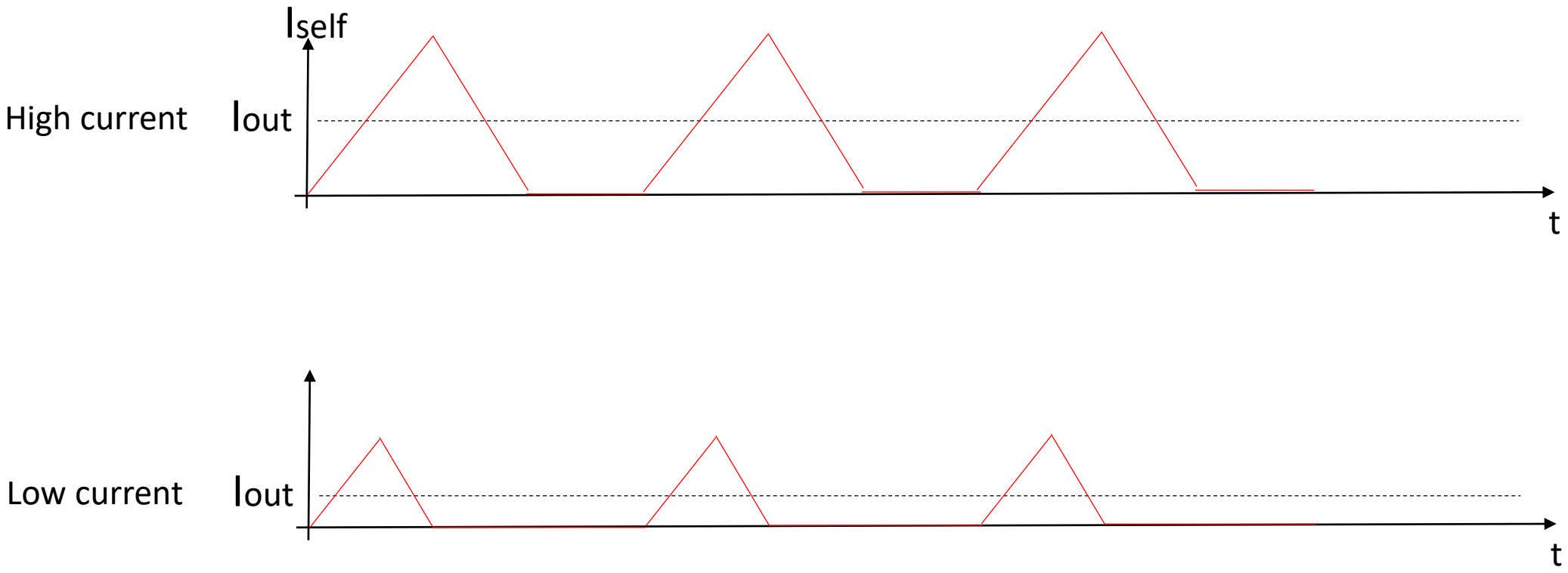
Voltage ripple:

$$\Delta V_{out} = \frac{1}{C}\left[\int_0^{DTs/2} \frac{(1-D)V_{bat}}{L} t\, dt + \int_0^{(1-D)Ts/2} \frac{DV_{bat}}{L} t\, dt\right]$$

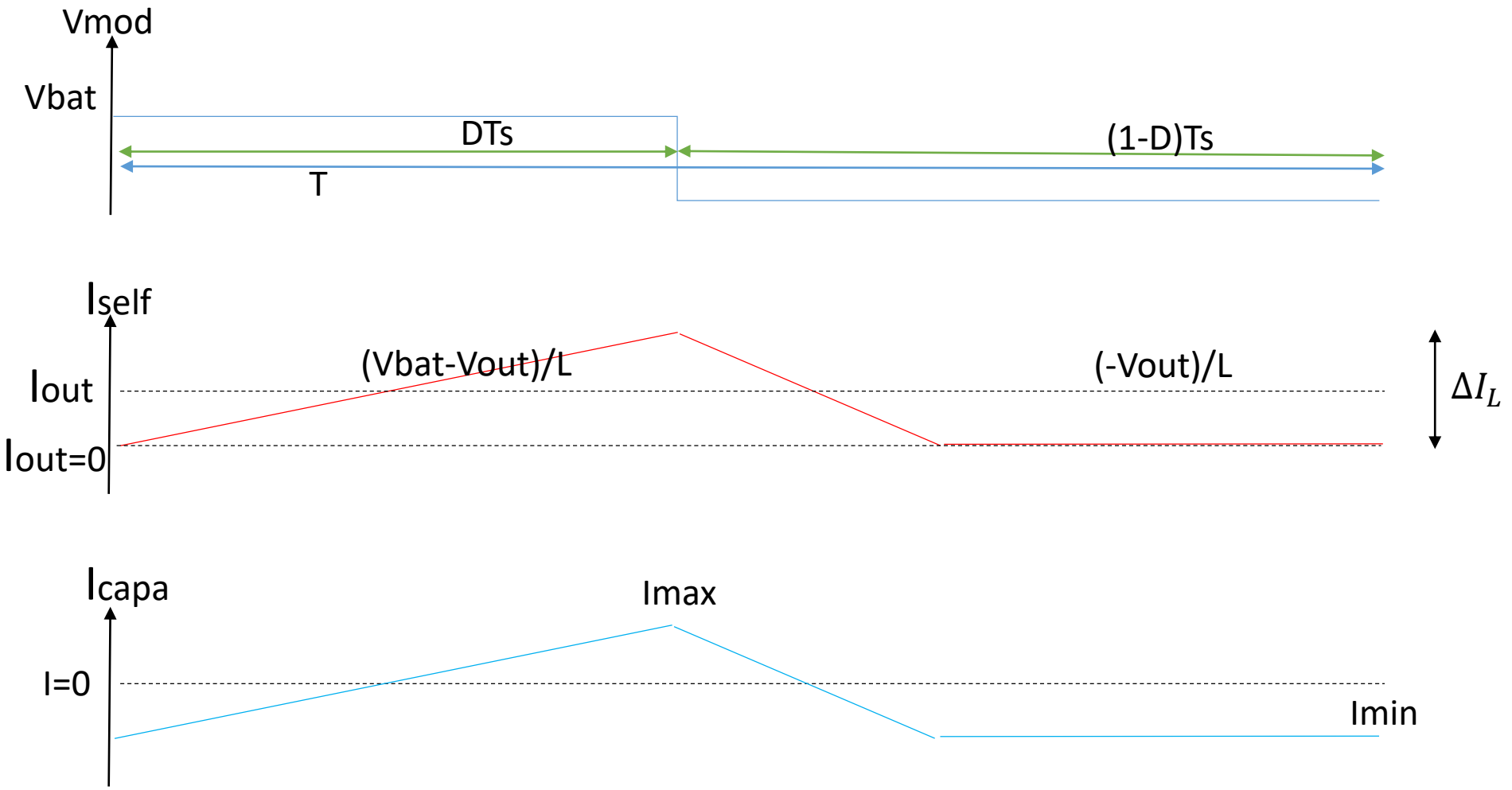
$$\Delta V_{out} = \frac{(1-D)V_{bat}}{LC} \frac{(\frac{DTs}{2})^2}{2} + \frac{DV_{bat}}{LC} \frac{(1-D)^2 Ts^2}{2^2.2}$$

$$\Delta V_{out} = V_{bat} \frac{1}{8LC{F_S}^2} D(1-D)$$

Discontinuous conduction mode



Discontinuous conduction mode



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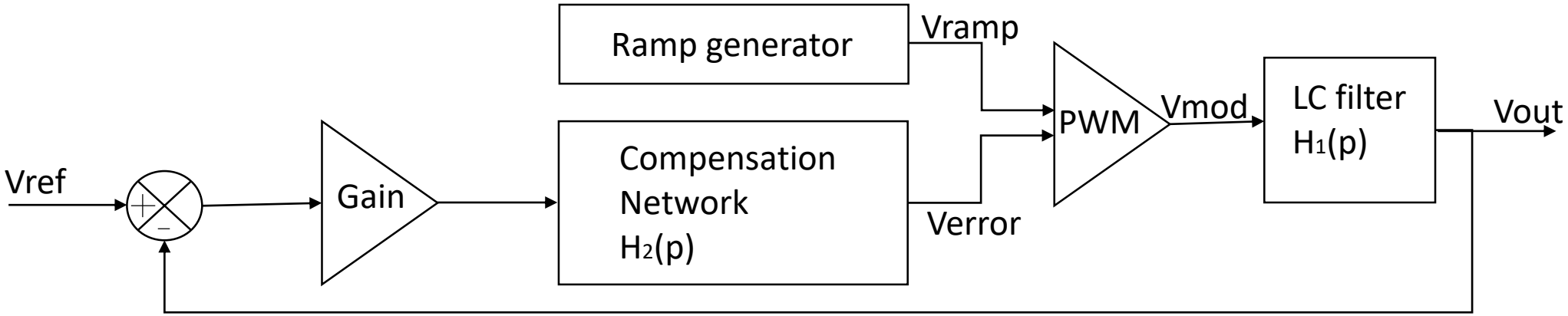
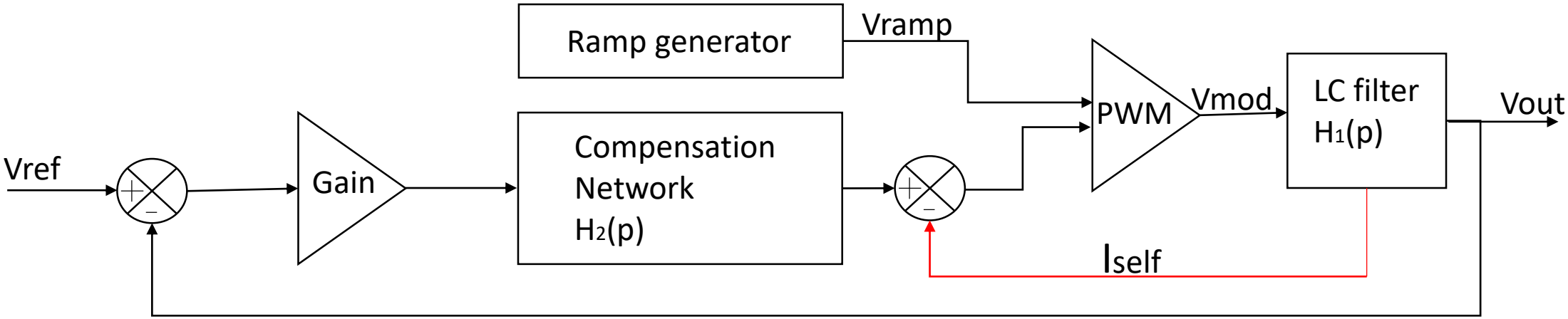
Voltage mode regulation



This scheme comprises an error amplifier, a PWM modulator and an LC filter. It also includes a compensation network around the error amplifier to make the loop stable.
This compensation network contains at least one pole and two zeros (to cope with the second order pole of the LC filter), the ultimate goal being to obtain a closed loop transfer function equivalent to a first order system.

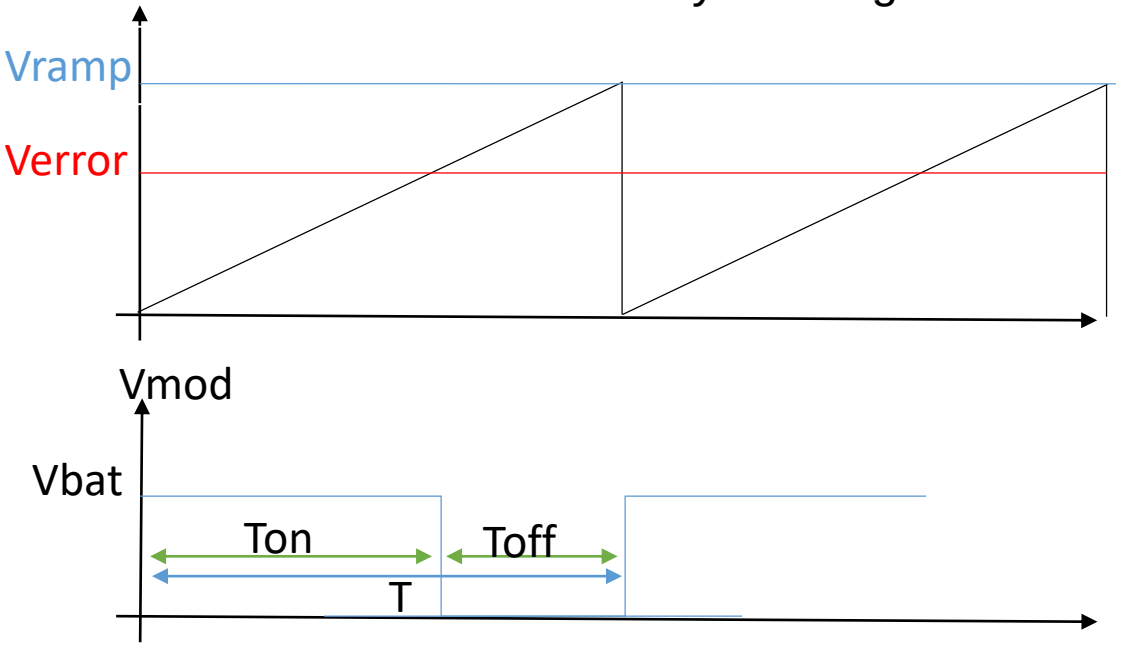
Current mode regulation



In this kind of regulation, the inductor current is just subtracted to the output of the compensation network. This second internal loop helps to stabilize the system by forcing the loop to behave like a first order system in high frequency

Modulator transfer function

Of the three blocks that make up the buck converter, the modulator is the only one with no frequency dependence. The modulator is basically a voltage-controlled rectangle wave generator.



Thus, the duty cycle can be expressed as:

$$D = \frac{T_{on}}{T_{on} + T_{off}} = \frac{V_{error}}{V_{ramp}}$$

Modulator transfer function

The modulator transfer function is the change in the average value of Vmod divided by a change in the error voltage:

$$A_{mod} = \frac{d\widetilde{V_{mod}}}{dV_{error}} = \frac{dV_{out}}{dV_{error}} = \frac{d}{dV_{error}}(DV_{bat}) = \frac{d}{dV_{error}}\left(\frac{V_{error}}{V_{ramp}}V_{bat}\right)$$

$$A_{mod} = \frac{V_{bat}}{V_{ramp}}$$

This is the gain of the modulator. In reality, this block has also time delays which cause phase shift. However, this phase shift usually is not a problem for the calculation of loop gain and phase and can be neglected in a first step. It will be addressed later in the design phase through transient simulation. (or by use of more advanced SPECTRE RF simulation).

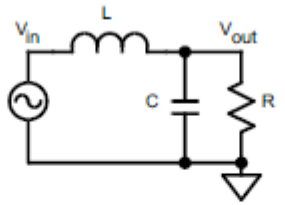
Filter transfer function

The modulator provides a pulse train, bounded by the battery voltage, whose duty cycle is determined by an applied control voltage. The output filter performs the averaging function that converts this pulse train into the output voltage of the converter. The cut-off frequency of the filter must therefore be an order of magnitude lower than the switching frequency.

Because the goal of a dc/dc converter is to have high efficiency, the output filter consists of reactive components which do not dissipate power. This filter operates as a low pass filter in the frequency domain and is as simple as a second-order LC filter terminated by the load resistance. Therefore, the load resistance is a critical component of the filter and must be known in order to predict the filter' s performance, the loop response and the stability of the converter.

Filter transfer function

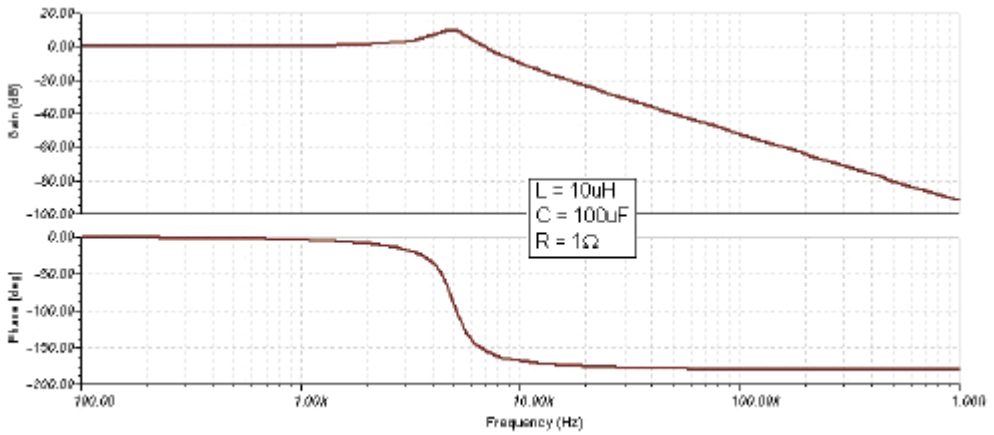
a.



b.

$$H_{RLC}(s) = \frac{R}{R + sL + s^2 RLC}$$

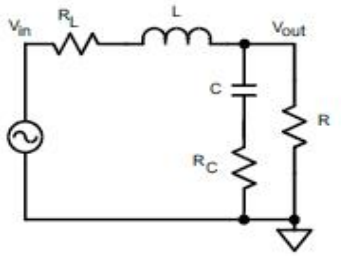
c.



Ideal LC filter

Filter transfer function

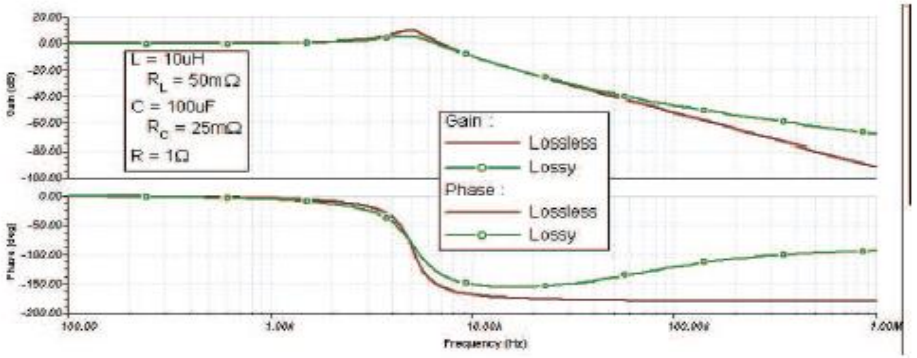
a.



b.

$$H_{Filter}(s) = \frac{1 + (C R_C)s}{1 + \frac{R_L}{R} + \left(\frac{L}{R} + R_C C + R_L C + \frac{R_L R_C C}{R}\right)s + \left(\frac{R + R_C}{R}\right) L C s^2}$$

c.



LC filter with parasitic

Filter transfer function

At the cutoff frequency $^{1}/_{\sqrt{LC}}$ the phase shift of -180dg is very sharp in an ideal filter and is somewhat smoothed in a real filter. These series resistances (usually referred to as ESR) in both the inductor and the output capacitor help to stabilize the loop.
The gain slope is –40 dB per decade of frequency increase above the LC cutoff frequency.

From these considerations, we guess that two zeros have to be inserted in the loop to compensate for this brutal phase shift.

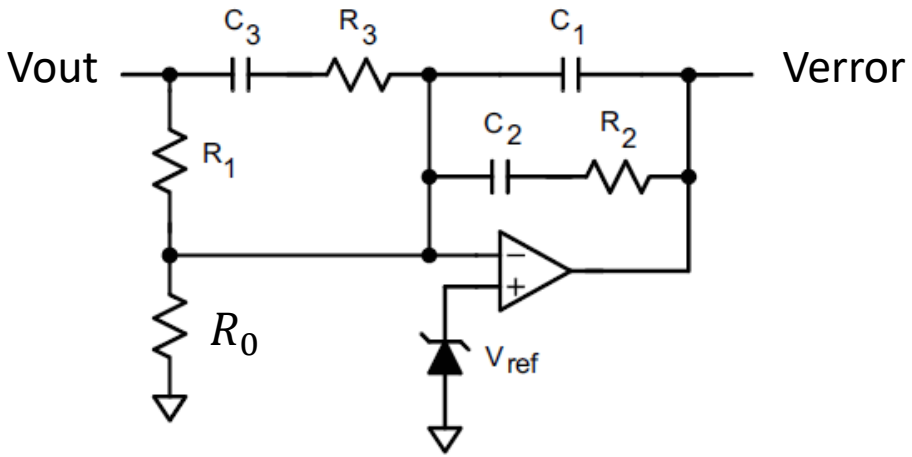
The filter transfer function is then at first order:

$$A_{filter} = H_2(p) = \frac{1}{1+\frac{L}{R}p+LCp^2}$$

Compensator transfer function

This chapter describes the design of the compensator for the voltage mode buck converter.
The error amplifier has to amplify the difference between the reference voltage and the output voltage with sufficient accuracy (i.e. low static error).
Its compensation network must also compensate for the 180dg phase shift of the LC filter in order to make the system stable (i.e. behaves like a derivator around the filter resonance frequency). Additionally, it must ensure sufficient bandwidth for the overall loop.

Compensator transfer function

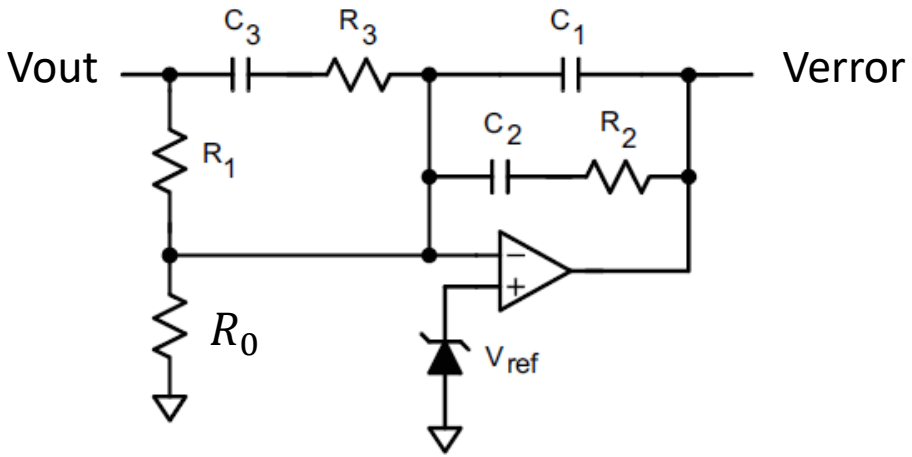


Compensator schematic

Ro is inserted to set the DC level on node Vout: $V_{out} = \left(1 + \frac{R_1}{R_0}\right) V_{ref}$

The compensator DC gain is then: $Gain_{DC} = \frac{R0}{R0+R1} . Gain_{opa}$

Compensator transfer function



Compensator schematic

The compensator transfer function is then: $A_{compensator} = H_1(p) = \frac{V_{error}}{V_{out}}$

Assuming an ideal opamp:

$$A_{compensator} = H_1(p) = \frac{1}{R1(C1+C2)p} \cdot \frac{(1+R2\,C2p)(1+(R1+R3)\,C3p)}{\left(1+R2\,\frac{C1\,C2}{C1+C2}p\right)(1+R3\,C3p)}$$

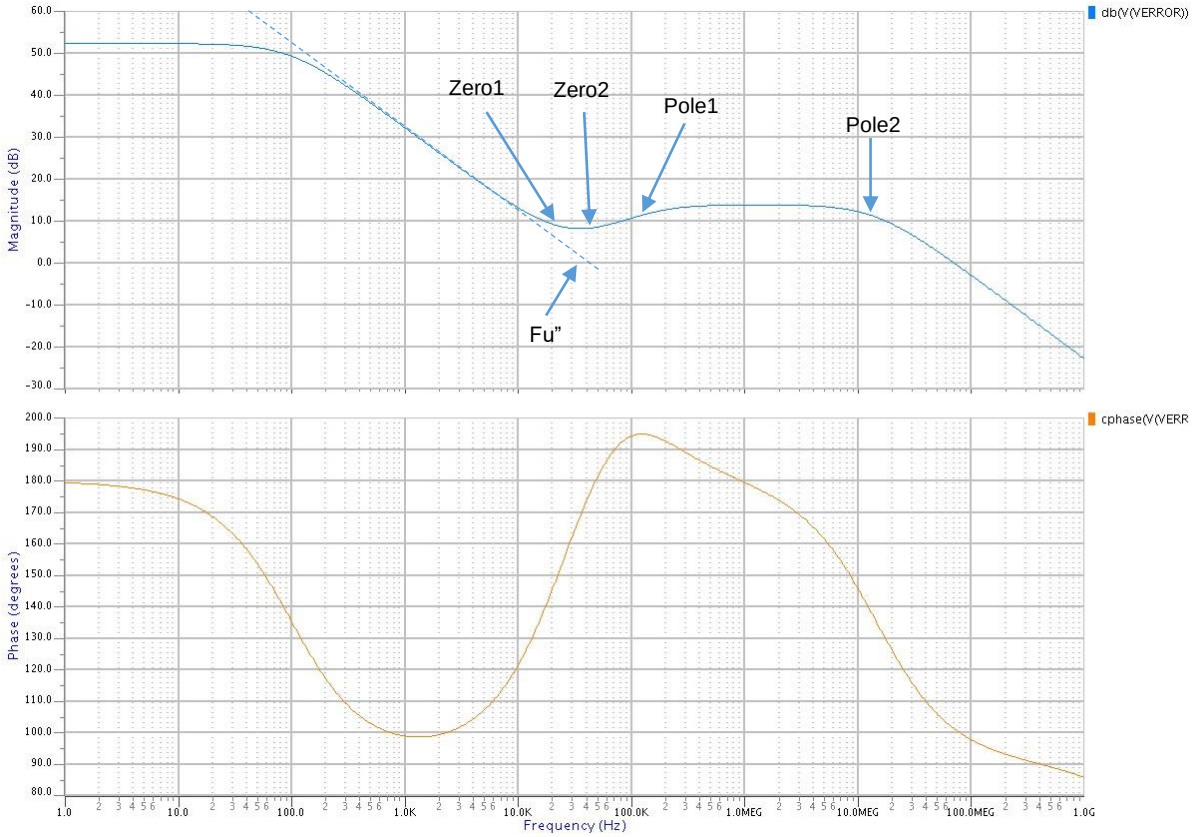
Compensator transfer function

$Gain_{opa}$=64dB
R0/(R0+R1)=-11.5dB
$Gain_{DC}$=52.5dB

Zero1: 1/R2.C2
Zero2: 1/R1.C3 (R3<<R1)

Fu' : 1/R1.C2 (C1<<C2)

Pole1: 1/R3.C3
Pole2: 1/R2.C1 (C1<<C2)

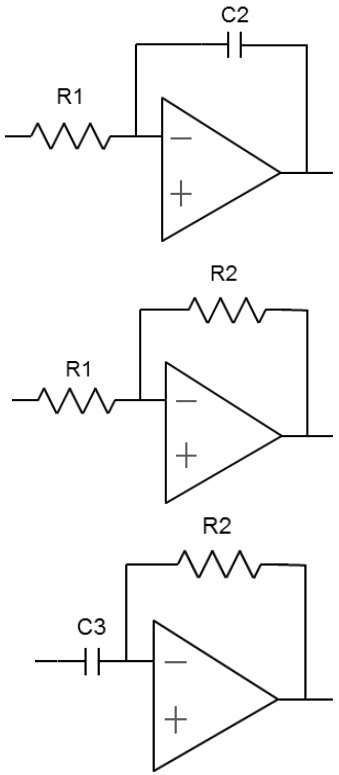


Compensator transfer function

f<z1 : integrator

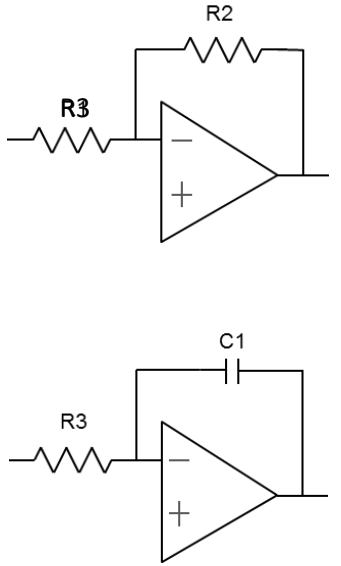
z1 < f < z2 : gain

z2 < f < p1: derivator

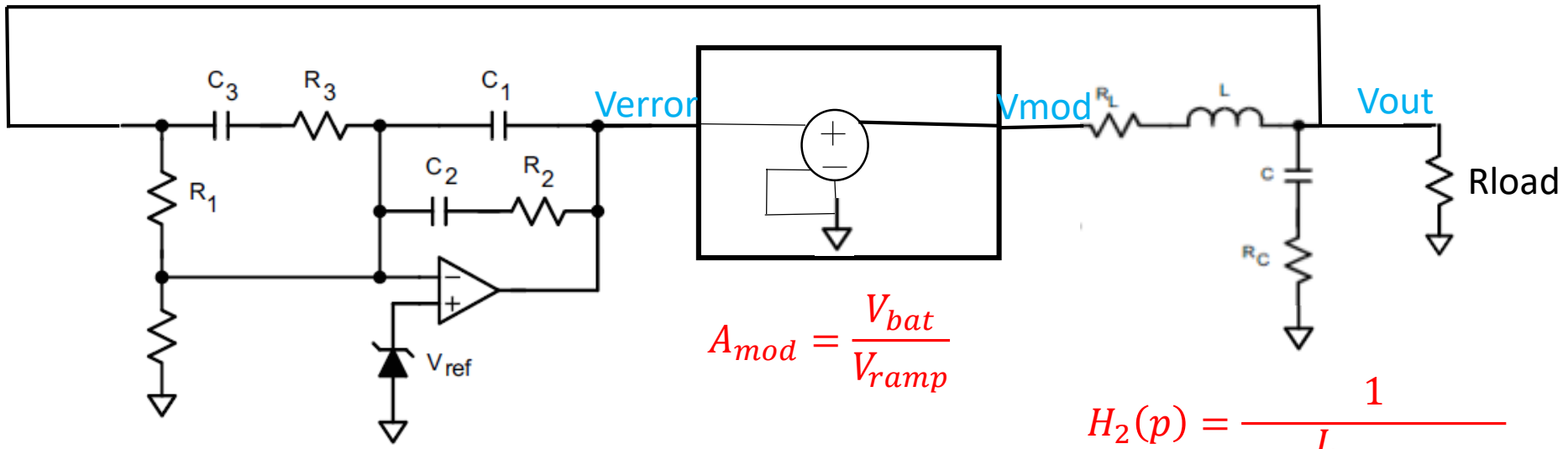


p1 < f < p2: gain

p2 < f : integrator



Overall transfer function



$$A_{mod} = \frac{V_{bat}}{V_{ramp}}$$

$$H_2(p) = \frac{1}{1 + \frac{L}{R}p + LCp^2}$$

$$H_1(p) = \frac{1}{R1(C1 + C2)p} \cdot \frac{(1 + R2\ C2p)(1 + (R1 + R3)\ C3p)}{\left(1 + R2\ \frac{C1\ C2}{C1 + C2}p\right)(1 + R3\ C3p)}$$

Overall transfer function

A classical strategy for placing the poles and zeros is demonstrated here. Besides deciding where to place the poles and zeros, the compensator gain also determines the crossover frequency of the loop. First, the loop crossover frequency has to be chosen and is based on the switching frequency and the desired loop transient response.

Although the selection of the filter components have not been discussed, they are mainly chosen based on dynamic issues in the circuit design. Remember that the current ripple (respect. the voltage ripple) is inversely proportional to the L value (respect. to the LC product).
Usually, the output inductor and capacitor are decided before the compensator design is started.
The ESR(Electrical Serial Resistor) of these components have to be taken into account due to their impact on the efficiency and the stability of the loop.
The roll-off behavior C=f(V) and the inductor saturation current L=f(I_L) have also to be considered. (i.e. the inductance must be compatible with the maximum current involved).

Overall transfer function

Step 1: Calculate the resistor R_0

Given a current consumption Iref through R0: $R_0 = {}^{V_{ref}}/_{I_{ref}}$

Step 2: Calculate the Resistor Divider Values

$$R_1 = R_0 \left({}^{V_{out}}/_{V_{ref}} - 1 \right)$$

Step 3: Calculate the filter's resonant frequency

$$f_{LC} = {}^{1}/_{2\pi\sqrt{LC}}$$

Step 4: Place a first zero slightly below the filter's resonant frequency

$$C_3 = \frac{1}{2\pi . 0{,}9 . f_{LC} R_1}$$

Step 5: Place a pole at the crossover frequency

$$R_3 = \frac{1}{2\pi . f_{crossover} C_3}$$

Overall transfer function

Step 6: Calculate the required gain of the compensator at the desired crossover frequency

$$H_1(f_{crossover}) = \frac{1}{A_{mod}.H_2\,(f_{crossover})}$$

Step 7: Set the gain of the compensator

$$R_2 = (R_1||R_3).H_1(f_{crossover})$$

(Note that at this frequency, the system behaves like an amplifier with a gain of R_2/R_3)

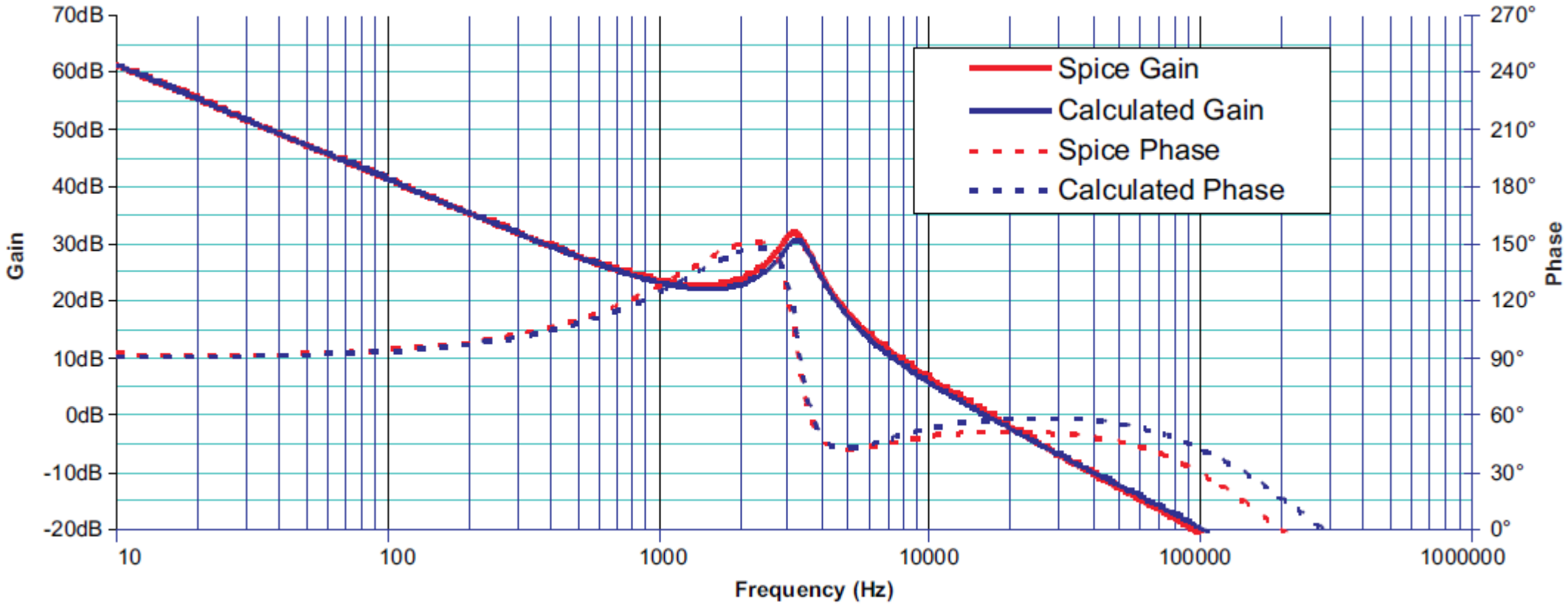
Step 8: Place a second zero just below the filter resonance

$$C_2 = \frac{1}{2\pi.0{,}9.f_{LC}R_2}$$

Step 9: Place a second pole about a decade above the crossover frequency

$$C_1 = \frac{1}{2\pi.10.f_{crossover}R_2}$$

Overall transfer function



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5-Efficiency

Efficiency

Since the battery provides an average current of Iout during the time D.Ts (and nothing during the remaining time (1-D).Ts), its average current along a period Ts is:

$$I_{BAT} = \frac{I_{OUT}.D.T_S}{T_S} = I_{OUT}.D$$

The power provided by the battery can then be expressed as:

$$P_{BAT} = V_{BAT}.I_{BAT} = V_{BAT}.\mathrm{D}.\ I_{OUT}$$

The output power is given by:

$$P_{OUT} = V_{OUT}.I_{OUT} = D.V_{BAT}.I_{OUT}$$

In case of an ideal DC/DC converter, the efficiency can then be expressed as:

$$Efficiency = \frac{P_{OUT}}{P_{BAT}} = 1$$

Of course, in a real world, some losses deteriorate the efficiency.

Efficiency

Three kinds of losses degrade the efficiency of an SMPS.

1-Joules losses:

They are due to the current which flows through the resistive path.

output power Pmos : $P_{pmos} = Ron_{pmos}.Iout^2.D$

output power Nmos : $P_{nmos} = Ron_{nmos}.Iout^2.(1-D)$

ESR inductor: $P_{esrL} = R_{esrL}.Iout^2$

ESR capacitor: usually negligible

•Example: Vbat=3V Vout=1.5V Iload=20mA, Ronp=0.96Ω, Ronn=0.53Ω, ResrL=1.5Ω, ResrC=5mΩ

output power Pmos : $P_{pmos} = 192\ uw$

output power Nmos : $P_{nmos} = 106uW$

ESR inductor: $P_{esrL} = 600uW$

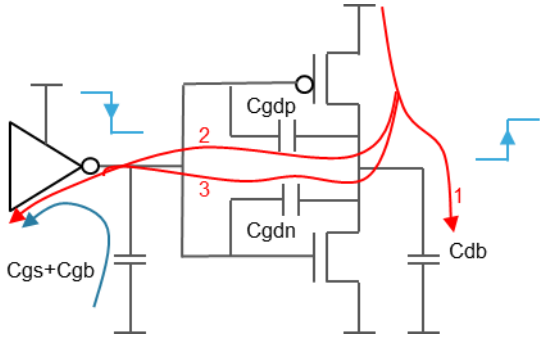
$$P_{joule} = (Ron_{pmos}.D + Ron_{nmos}.(1-D) + R_{esrL}).Iout^2$$

Efficiency

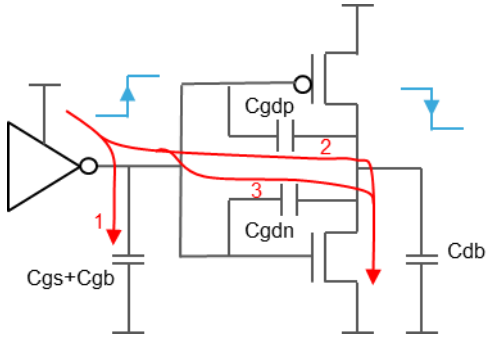
2-Switching losses:

They originate from the charging(discharging) of the parasitic capacitors associated with each device.

Dynamic power in switched capacitor system: $P_{dyn} = Vdd.I = Vdd.\frac{Vdd}{\mathrm{Re}\, q} = C.Vdd^2.Fs$



Phase 1



Phase 2

$$P_{switch} = \left[2.\left(C_{gdp} + C_{gdn}\right) + C_{db} + C_{gs} + C_{gb}\right].{V_{BAT}}^2.F_s$$

Efficiency

2-Switching losses:

- Example:

•Cgs: NMOS +PMOS grid/source capacitor : Cgs=2.51pF
•Cgb: NMOS +PMOS grid/bulk capacitor : Cgb=2.71pF
•Cdb: NMOS +PMOS drain/bulk capacitor : Cdb=2.8pF
•Cgd: NMOS +PMOS grid/drain capacitor : Cgd=1.88pF

- P_{switch}= 840uW

3-Quiescent losses:

This comes from the bias current of each stage.

$$P_{quies} = I_q . V_{BAT}$$

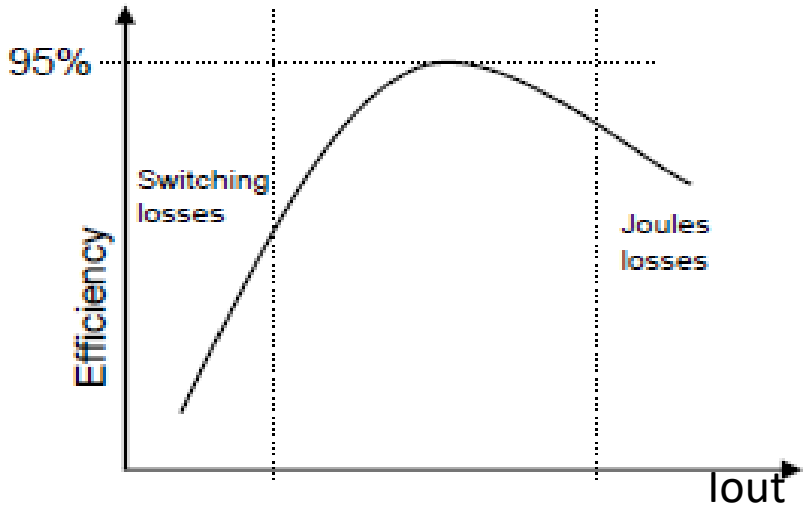
•Example: Iq=200uA, Vbat=3V
• P_{quies}=600uW

4-Efficiency:

$$\eta = \frac{P_{OUT}}{P_{quies}+P_{switch}+P_{joule}+P_{OUT}}$$

- Example: Pout=60mW
- $\eta = 96\%$

Efficiency



Switched Mode Power Supply (DC/DC buck converter)

1-Why use a DC/DC converter ?
2-Architecture
3-Conduction modes
- Continuous Conduction Mode
- Discontinuous Conduction Mode

4-Stability
- Voltage Mode
- Current Mode
- Modulator transfer function
- Filter transfer function
- Compensator transfer function
- Overall transfer function

5-Efficiency
6-Characteristics

Characteristics

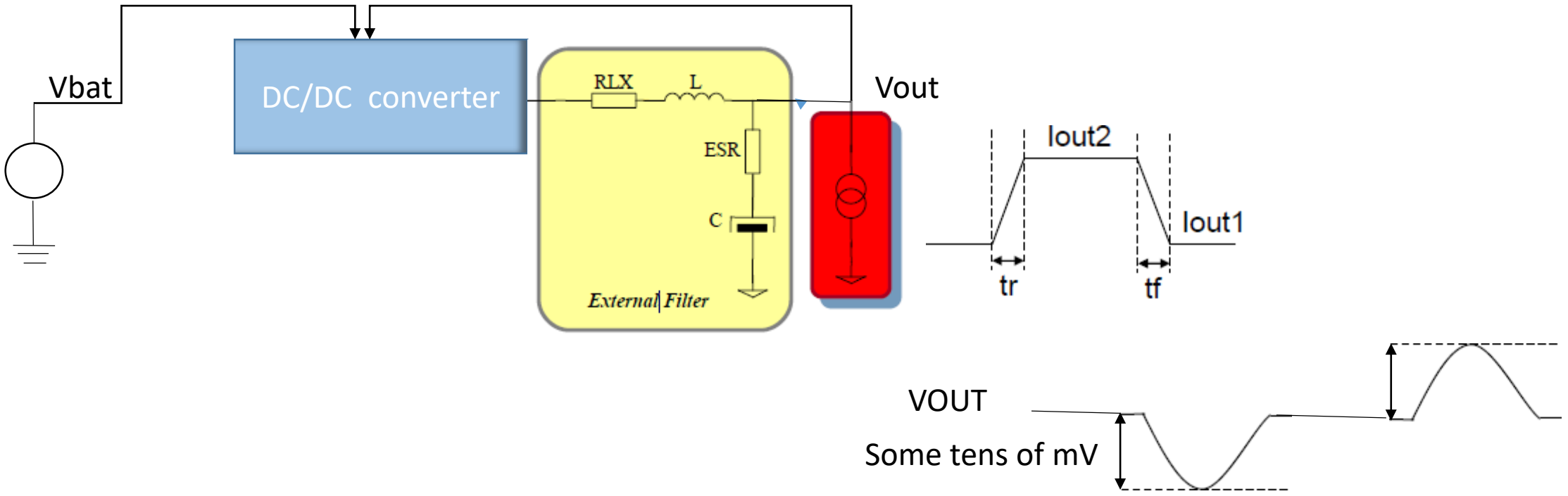
The various operating requirements are namely:
- Battery voltage (Vbat)
- Output voltage (Vout)
- Output current range (Iout some mA)
- Maximum output voltage ripple (Vripple some mV)
- Clocking frequency (Fck some MHz)

Notice that in RF design, the clock frequency must be chosen carefully depending on some spectrum specifications.

Some additional requirements:
- Load regulation : precision of output voltage while output current is changing
- Load transient : response to an output current step
- Line regulation : precision of output voltage while battery voltage is changing
- Line transient : response to a battery voltage step
- Efficiency (quiescent current)
- Startup time

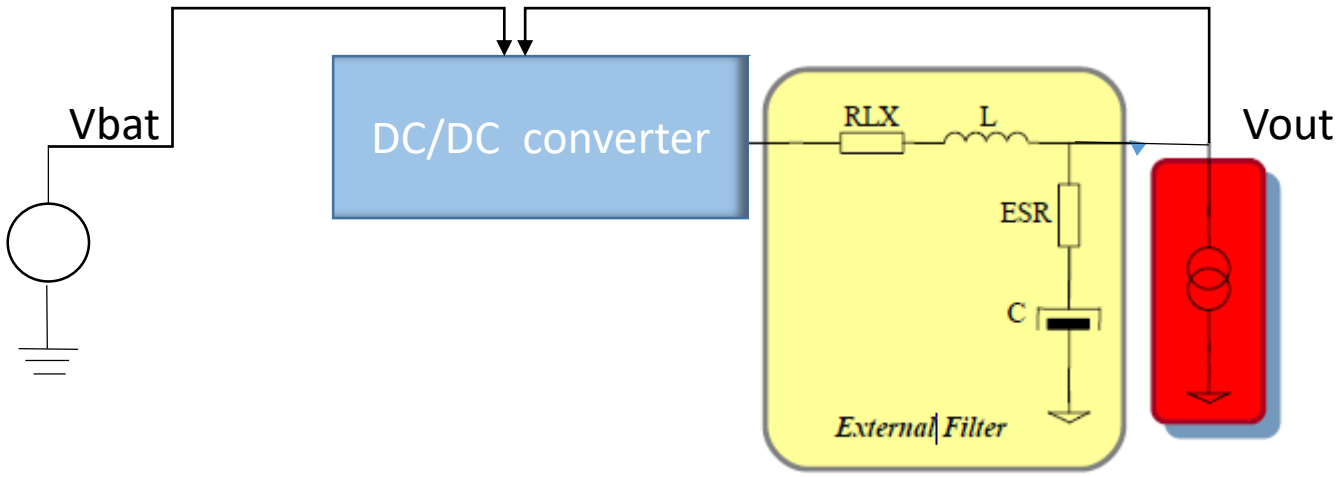
Characteristics

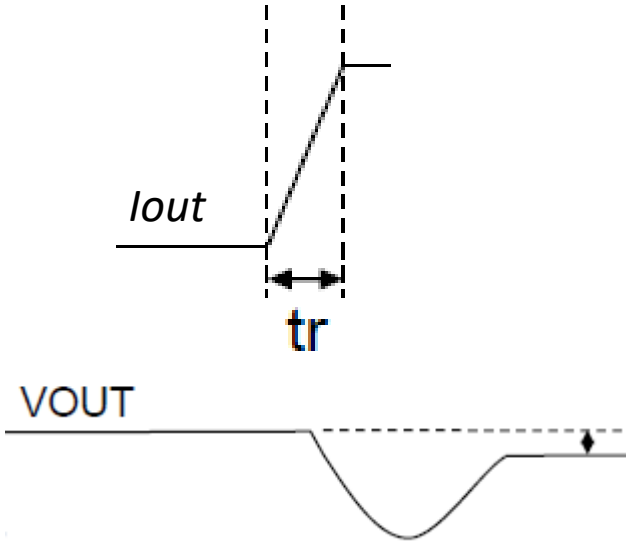
Load transient : response to an output current step



Characteristics

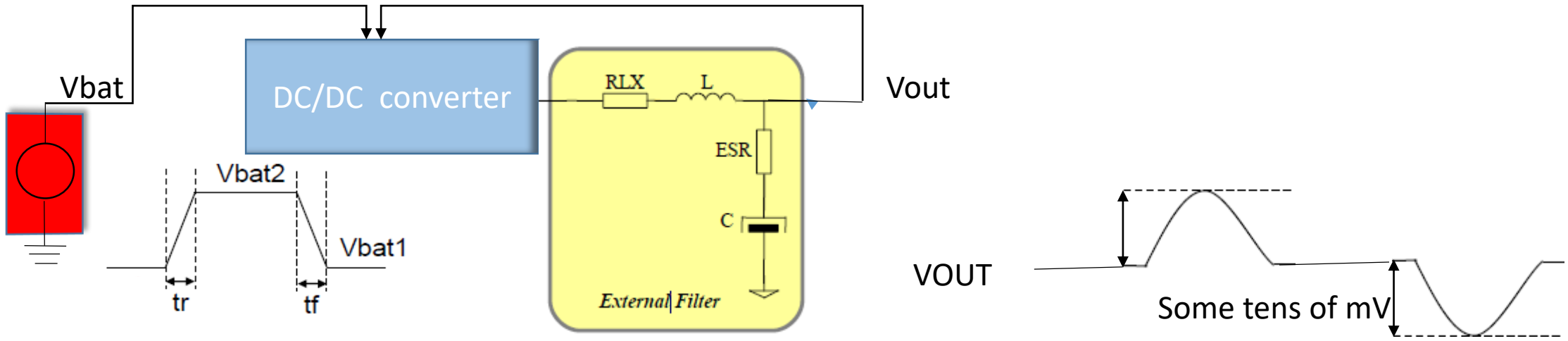
Load regulation : precision of output voltage while output current is changing





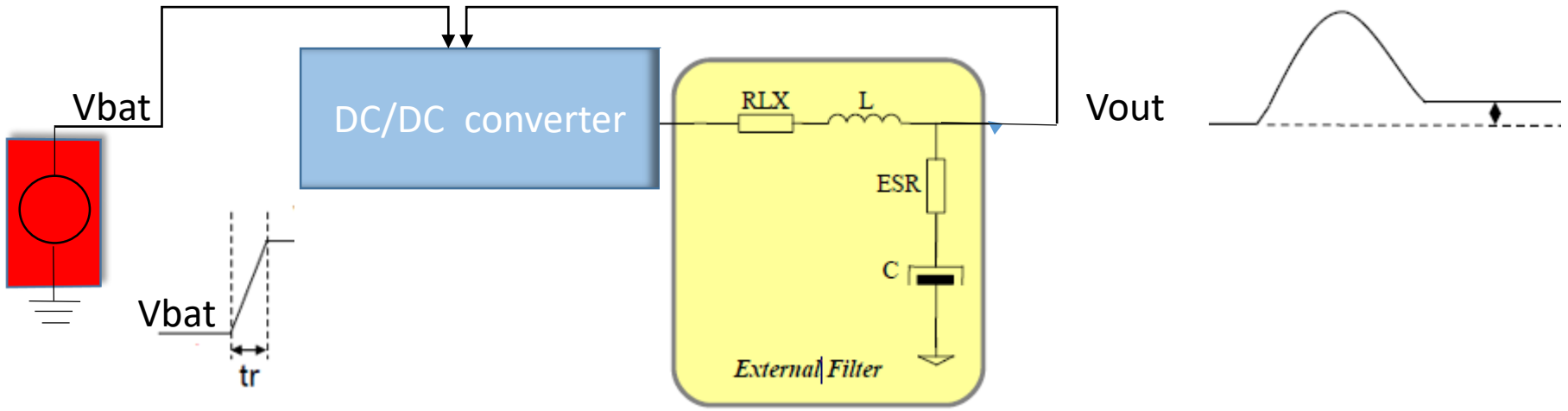
Characteristics

Line transient : response to a battery voltage step



Characteristics

Line regulation : precision of output voltage while battery voltage is changing



Patent 1 et 2

To add

Boucle locale _ boucle globale _ Article de geelen