# CRONOTIC 2, a multi-phase detector VRO TDC for CMS MG-RPC

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## CMS MG-RPC LHC detector

Resistive Plate Chambers (RPC), with their excellent efficiency and timing precision ($< 1$ ns), are used in LHC experiments as muon detectors, and the information they provide plays an important role in the trigger systems.

- RPCs consist of two parallel plates, anode and cathode, both made with low-resistivity material and separated by a gas volume

In their multi-gap version, the rate capability is increased and the time precision could reach a few ps using a low resistivity material.

- Bakélite have a low resistive $2 \times 10^{10} \Omega.cm$
- Excellent efficiency, good precision, and reasonable time resolution could be achieved with such a detector

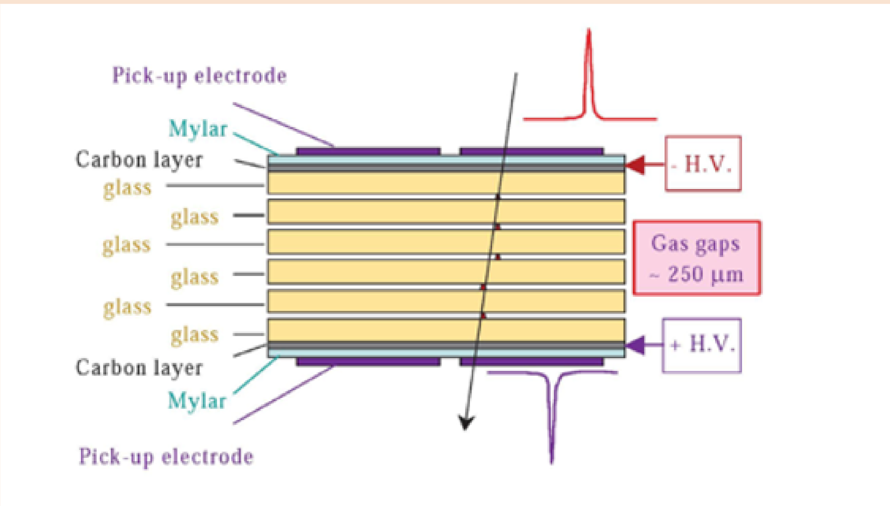


**Figure 1:** Multi-Gap Resistive Plate Chamber (RPC)

## Read system of the RPC

- PETIROC is the very front end chip designed for the readout of the RPC, and CRONOTIC2 a Time-to-Digital-Converter measures the time (dt) between two successive events
- To determine the position of particle collision in the RPC detector, tow reading channel are used

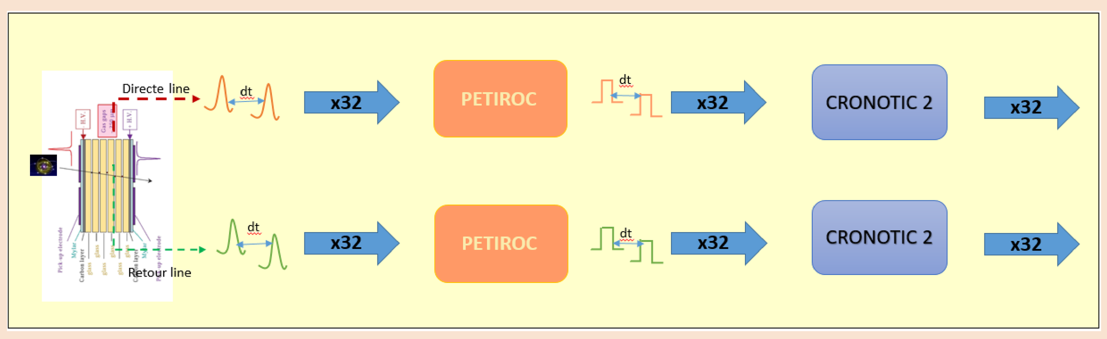


**Figure 2:** RPC Redaout system

| | |
|---|---|
| Technology | TSMC 0.13 $\mu m$ CMOS |
| Number of channel per ASIC | 32 |
| Resolution LSB | 1ps |
| Dynamic range | is determined by the global system |
| Noise (rms) | $< 1$ps |
| Power | $3mW_{RMS}.DR.N_{events}$ |
| Power supply | 1.2 V |

**Table 1:** Requirements for Cronotic2

## Conclusion

High resolution, high precision and low power consumption can be achieved with the proposed time-to-digital converter (TDC). Thanks to a multi-phase detection in a matrix configuration, the dead time improves significantly with the accumulated jitter. Theoretically, we can achieve less than 1 ps resolution with this architecture, it's a good start to fabricate a prototype chip in standard 130nm digital CMOS process and compare it with actual results.

## Cronotic 2 a Multi-Phase Time-to-Digital-Converter (TDC)

- $EN_{RO}$ generates the enable signals, $EN_{Slow}$ and $EN_{fast}$, to initialize oscillation in slow RO and fast RO, respectively (RO: ring oscillator)
- The phase detectors matrix with $N \times N$ single phase detectors observe the phase between each transition from the slow RO, $S_i$, and the fast RO, $F_j$. Whene they are in phase, $PD_{ij}$ turn to a logic "1"
- Detection-Array-End-of-Conversion is used to decoder the 64bits code from the matrix to N exploitable bits, and also to determine the end of the conversion
- The fine counters $CNT_s$ and $CNT_f$ records the numbers of laps that the slow signal and the fast signal, respectively, propagated before the phase detection
- Once the conversion is completed, the reset logic will turn off both ROs and counters.
- Data operates the three elements : the slow counter value $Ns$ the fast counter value $N_f$ and the offset code from the phase detector matrix to determine the Out code

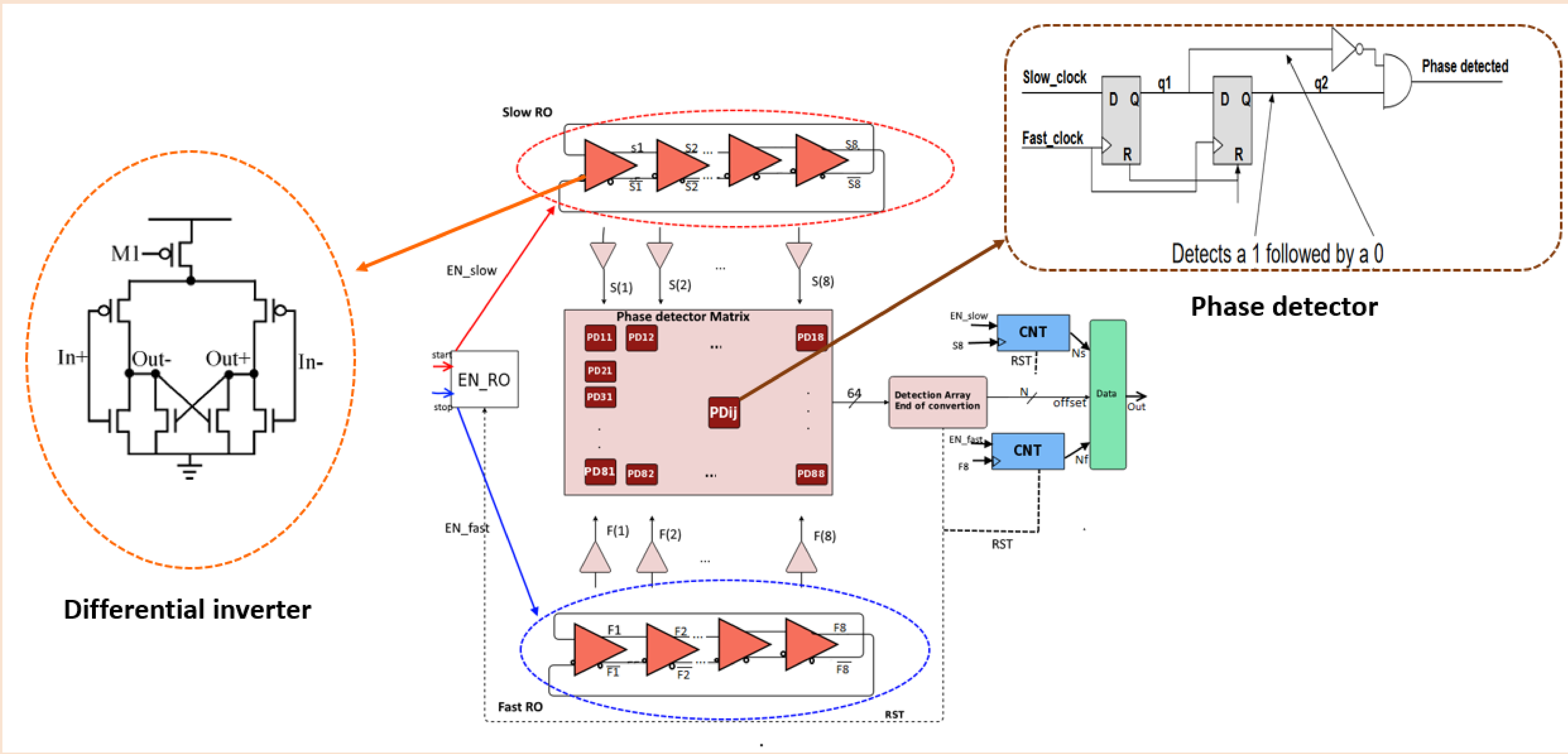


**Figure 3:** Block diagram of the multi-phase detector Vernier ring oscillator TDC

## Timing diagram of Cronotic2

- Each ring has 8 stages of inverters, a slow ring with larger propagation gate delay $\tau_s$ and a fast ring with smaller propagation gate delay $\tau_f$
- The time resolution is given by : R= $\tau_s$ - $\tau_f$
- The measurement result can expressed as follows: $T_{Hit}$=(16N + n)R if $N_s = N_f = N$ and $n_s = n_f = n$ with $T_s = 16\tau_s$ and $T_f = 16\tau_s$

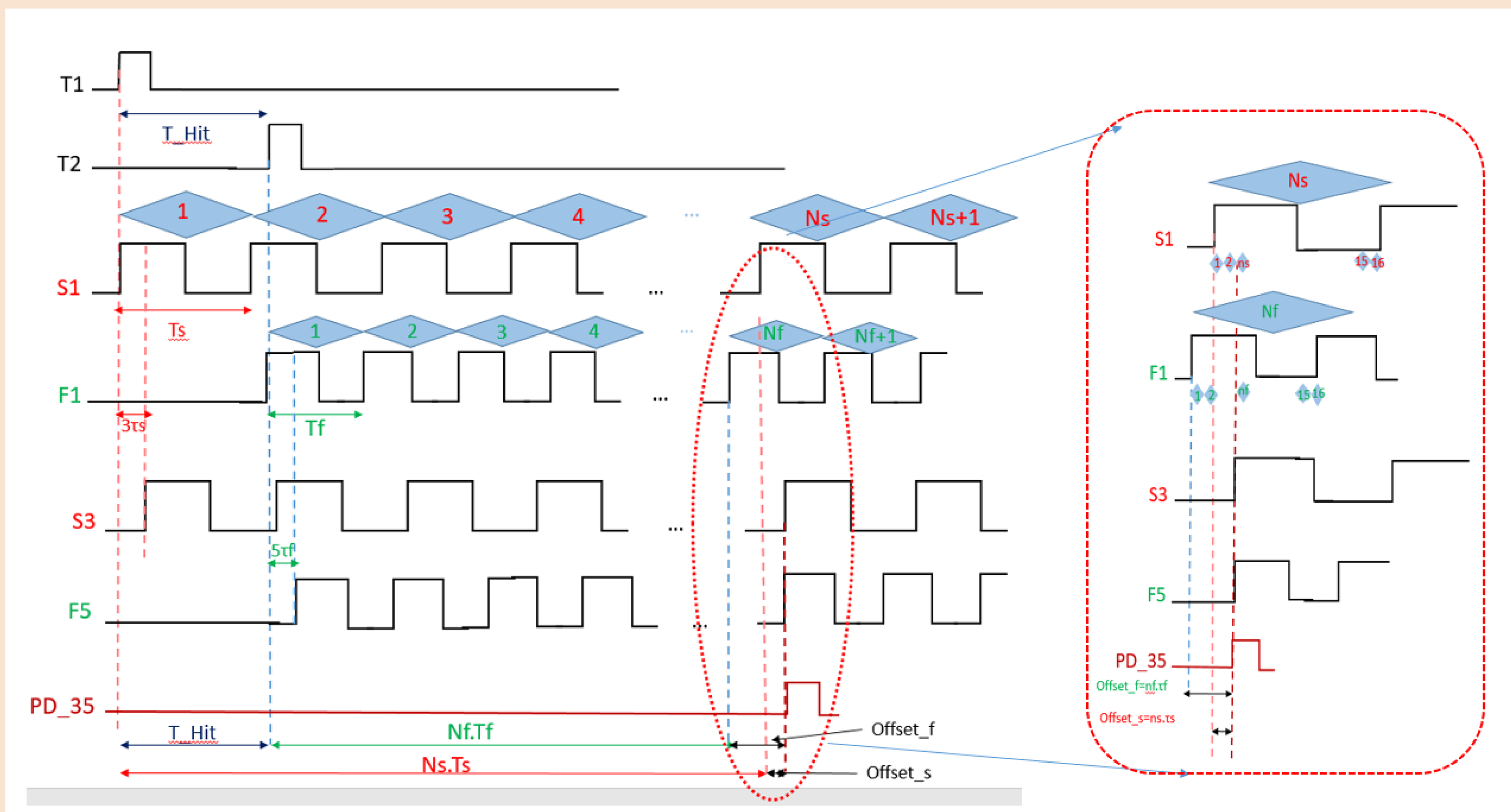


**Figure 4:** Timing diagrame of Cronotic 2: $T_{Hit} = (N_s \times T_s - N_f \times T_f) + (n_s \times \tau_s - n_f \times \tau_f)$

## Main results of simulation(Resolution, Dead time and jitter)

- In the figure 5, the first phase detection arrives at $PD_{51} = 7ns$ the dead time is significantly improved ($PD_{77} = 19ns$ compared to an architecture with one phase detection at the end of the delay line)
- The average of all phases detectors results will still improve the precision of the TDC
- Since the dead time is improved, the amount of cycle time in the ROs clock will decrease and also the accumulated jitter
- The differential structure helps in rejecting the substrate and supply noise commonly

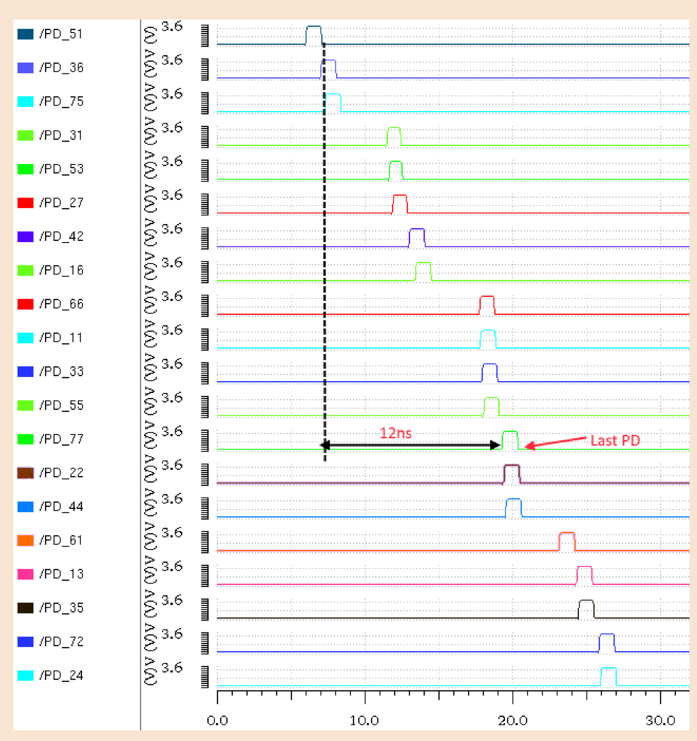


**Figure 5:** Output of the phase detector matrix