# Status SiW Ecal

Roman Pöschl

On behalf of

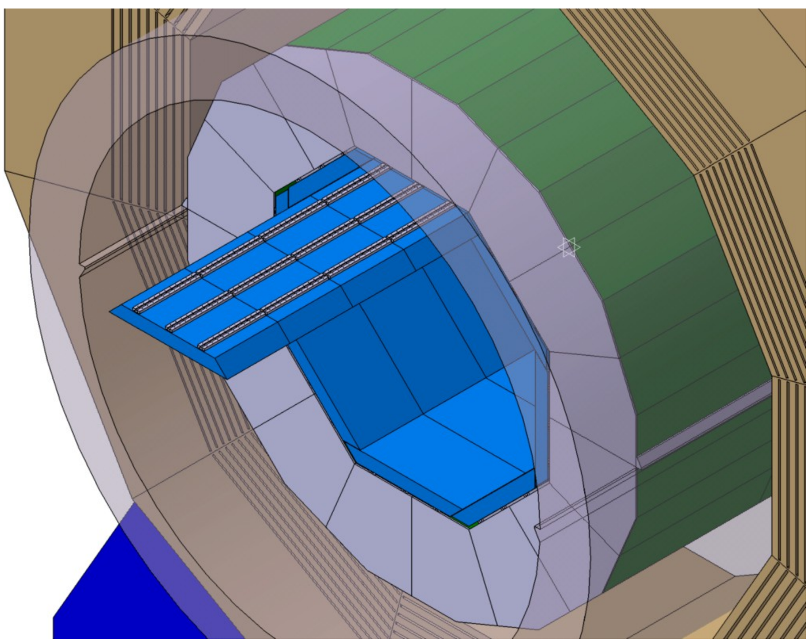
CALICE-France Meeting Paris – October 2016

# SiW ECAL for a future LC

- SiW ECAL is baseline for future LC detectors

→ Optimized for Particle Flow Algorithm:

Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

**Basic Requirements:**

- Extreme high granularity
- Compact and hermetic (inside magnetic coil)

**Basic Choices:**

- Tungsten as absorber material

  $X_0$=3.5mm, $R_M$=9mm, $\lambda_I$=96mm

  Narrow showers

  Assures compact design

- Silicon as active material

  Support compact design

  Allows for pixelisation

  Robust technology

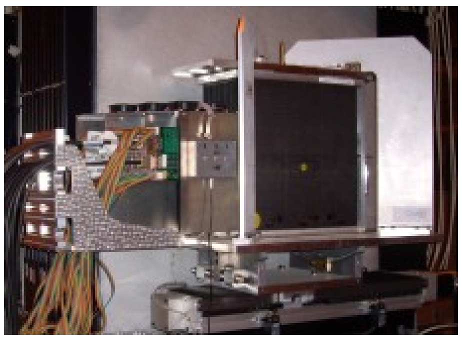
  Excellent signal/noise ratio: ~10

# SiW ECAL for a future LC

## Physics Prototype

Proof of principle

2003 - 2011



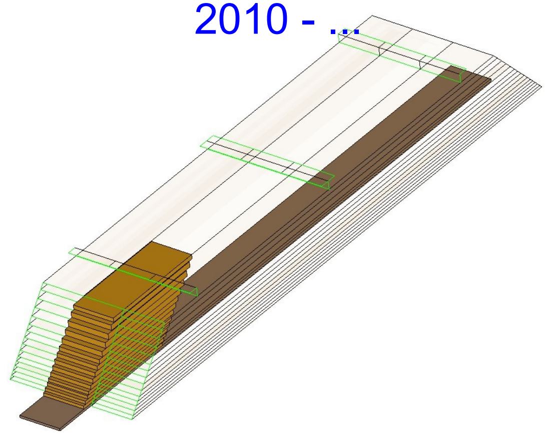
**Number of channels : 9720**

**Weight : ~ 200 Kg**

## Technological Prototype

Engineering challenges

2010 - ...

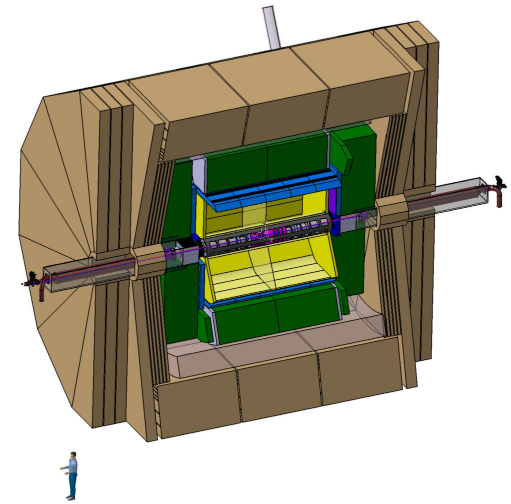


**Number of channels :**

**up to 45360**

**Weight : ~ 700 Kg**

## LC detector



**ECAL :**

**Channels : ~100 $10^6$**

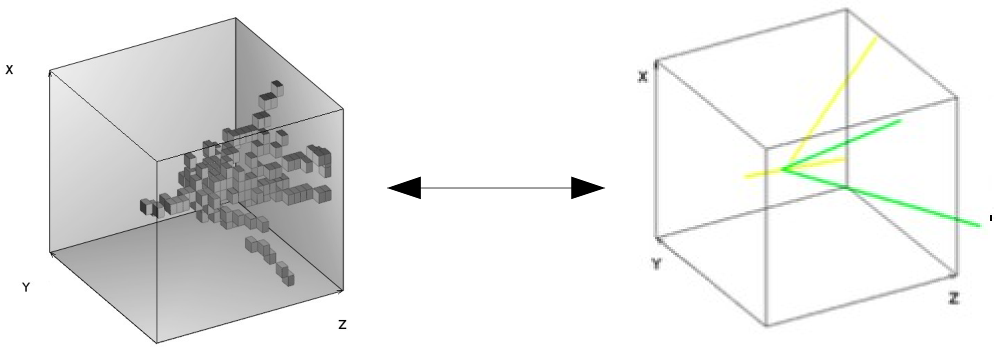
**Total Weight : ~130 t**

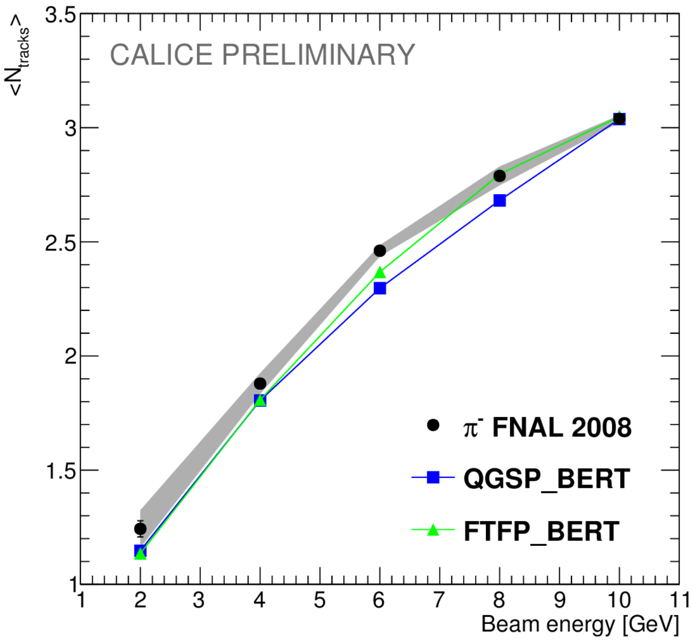
All well integrated in international collaborations as CALICE, AIDA-2020 and the ILD detector concept

- Jean Claude Brient Contact for ILD Ecal
- R.P. Coordinator of AIDA2020 WP14 on Calorimetry
- D. Grondin, V. Boudry, D. Zerwas: TL WP14
- H. Videau, Executive Team ILD

# Ongoing analyses – Physics Prototype

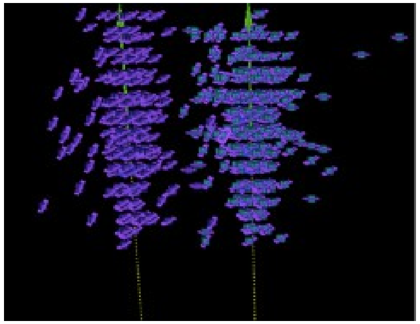
## Tracks in SiW Ecal

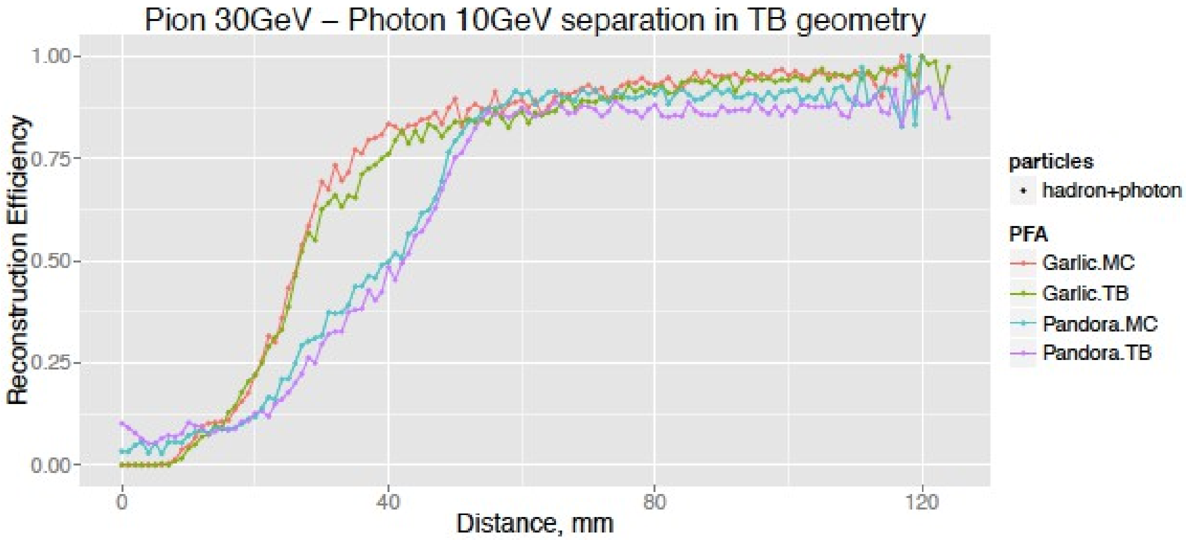



PhD Thesis S. Bilokin (LAL)
Accepted as CALICE Preliminary
Paper over winter

## Photon-pion: Separation






PhD Thesis K. Shpak (LLR)
In CALICE Editorial Board

# Our sponsors ...

Funding of SiW Ecal since 2002

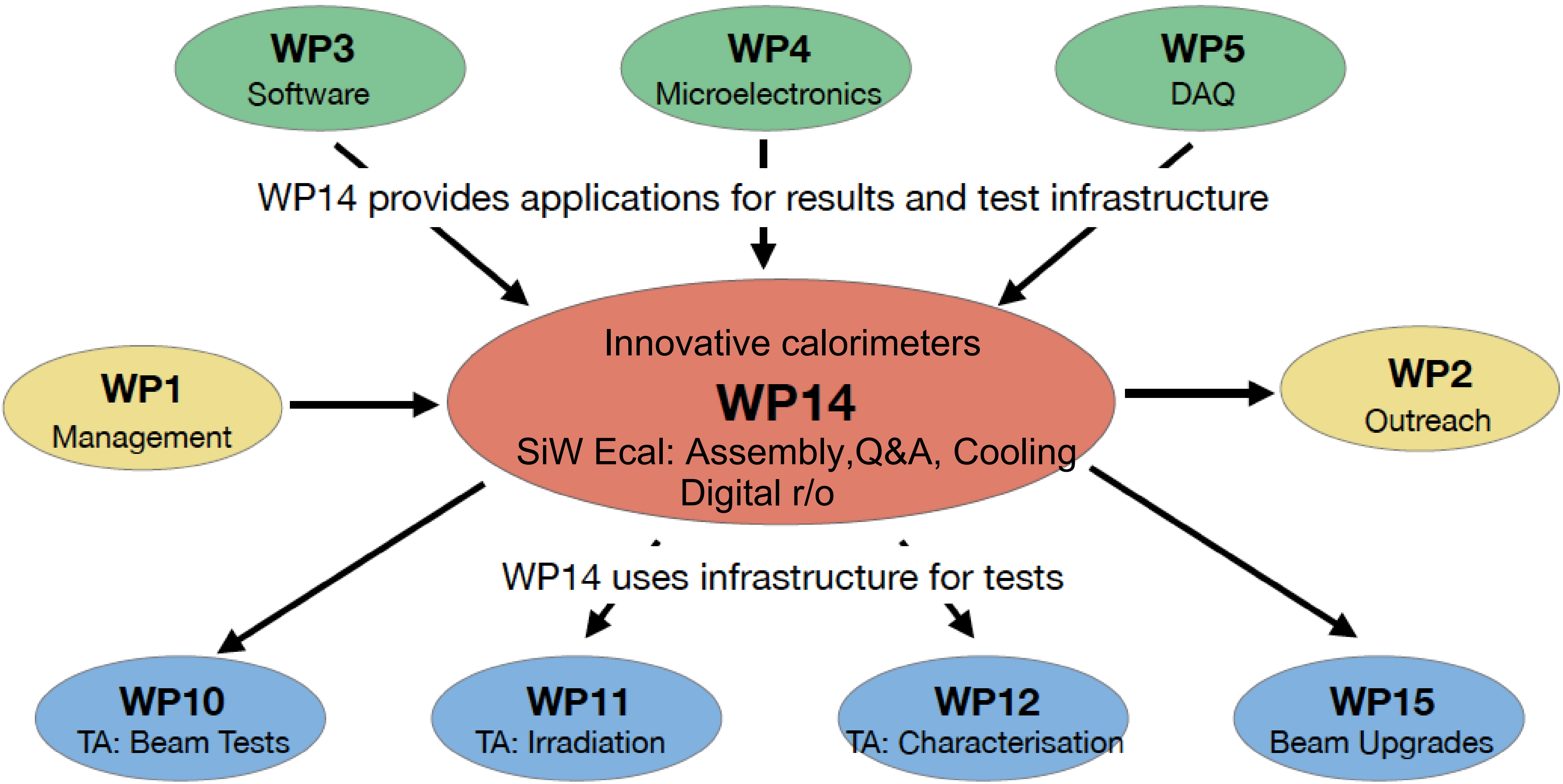
Horizon2020 European Research Infrastructure
SiW Ecal Beneficiaries: LAL, LLR, LPNHE, LPSC, OMEGA
Materiel, HR, Travel
2015 - 2019

P2IO “Projet emblematique”
SiW Ecal Beneficiaries: LAL, LLR
Material, HR, Travel
2016- 2019

European MSC RISE Action
Research stays in Japan for machine and detector related R&D
SiW Ecal Beneficiaries: All IN2P3 Institutes (in principle)
2015 - 2019

Support from partner bodies like Ecole Polytechnique, Universite Paris Sud, UPMC is herewith explicitly acknowledged as well

# AIDA2020 Workpackages



# First SiW Ecal AIDA2020 Milestone

AIDA-2020-MS14

**AIDA-2020**

Advanced European Infrastructures for Detectors at Accelerators

**Milestone Report**

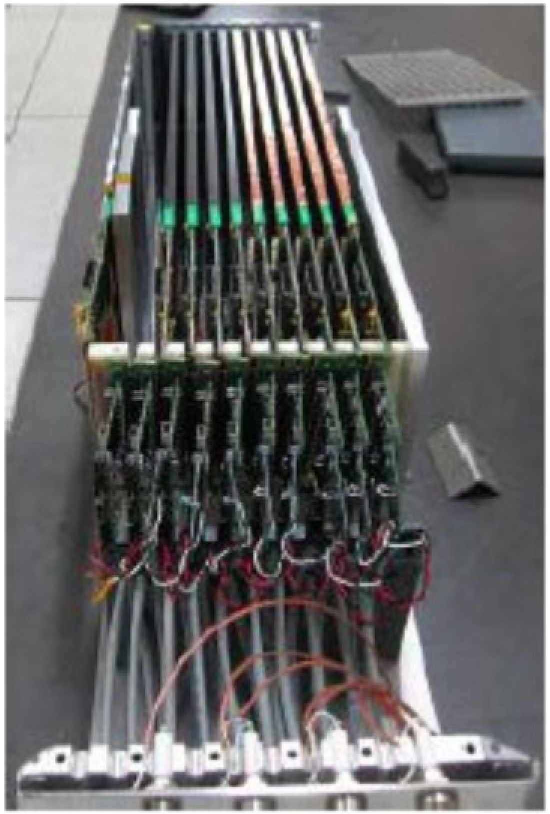
**Assembly and QA chain demonstration for highly granular silicon calorimeters**

Boudry, V. (CNRS) *et al*

23 June 2016

AIDA 2020

The AIDA-2020 Advanced European Infrastructures for Detectors at Accelerators project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

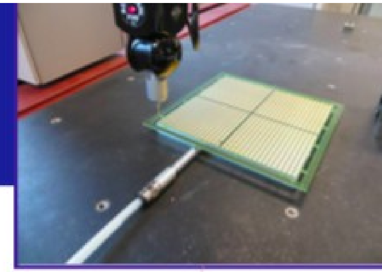


- Stack of short layers
- Important validation of procedures
- (Combined) beam test in June 2016
... to be continued in 2017

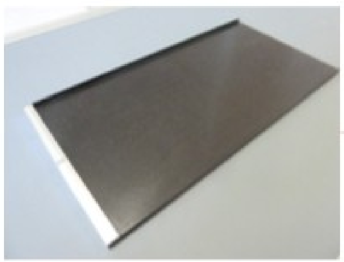
# Assembly chain - Overview

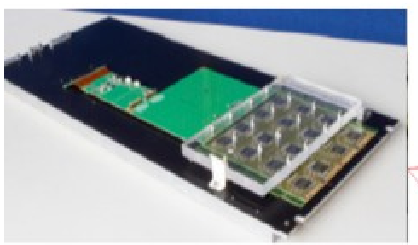
## Full assembly chain

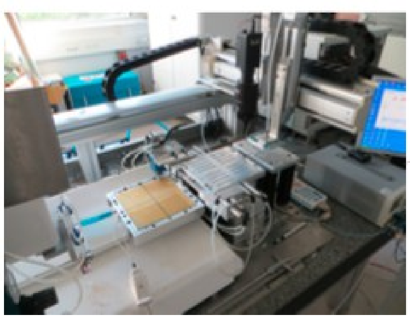
*resp: R. Cornat*

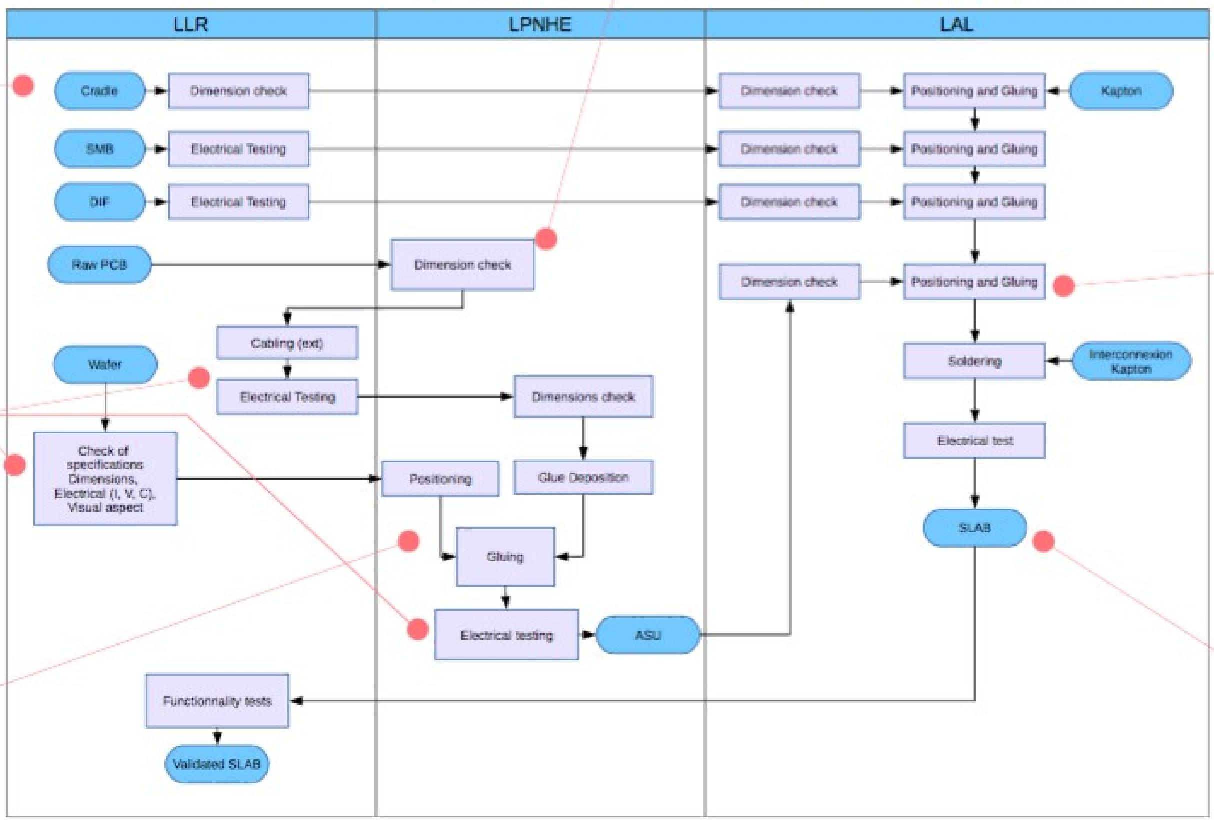


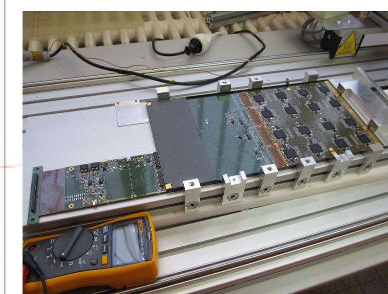
'Simplified view'







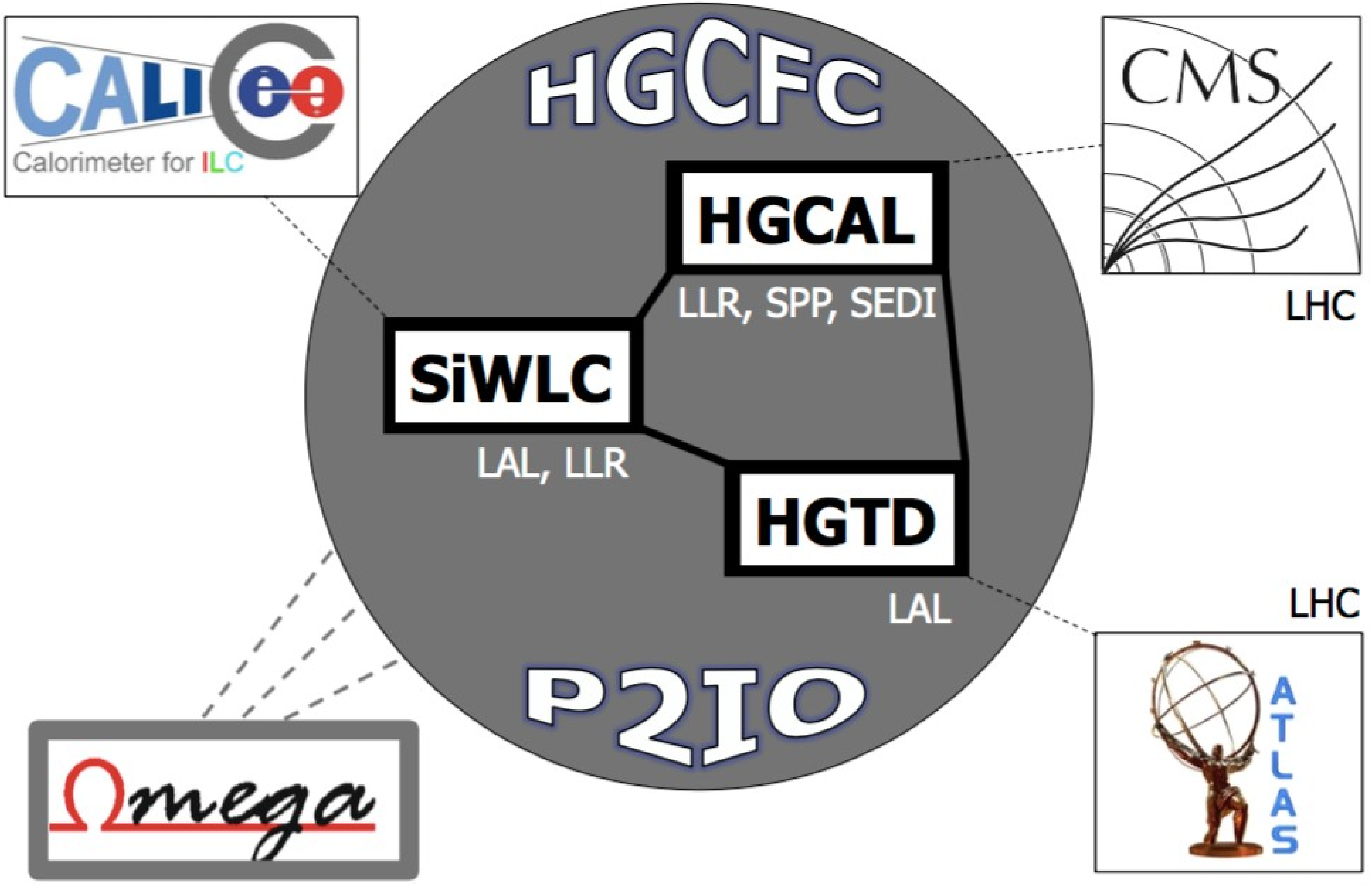


*V. Boudry, ECFA Workshop 2016*

# HIGHTEC

## The HIGHTEC Project at P2IO




LLR Palaiseau CNRS, LAL Orsay CNRS, SPP + SEDI Saclay CEA

13

# SiW ECAL – Long layer

<ins>A layer is composed of several short ASUs:</ins>

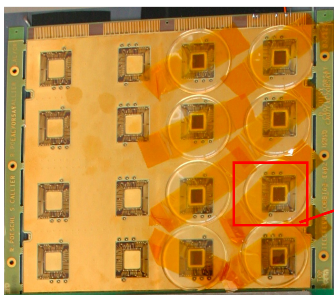
- A.S.U. : Active Sensors Units
- Similar layout for ATLAS HGTD

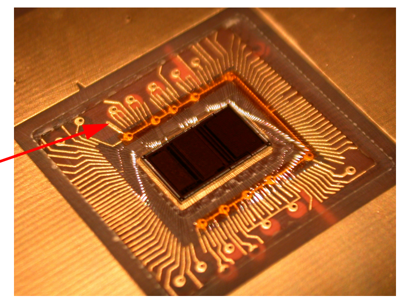
Interconnection
with
Flat flexible cable

**ASIC+PCB+SiWafer**
**=ASU, 18x18cm$^2$**

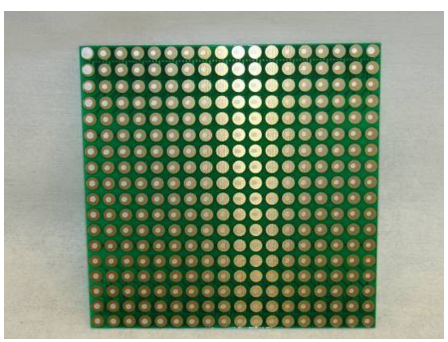
Wire Bonding or BGA

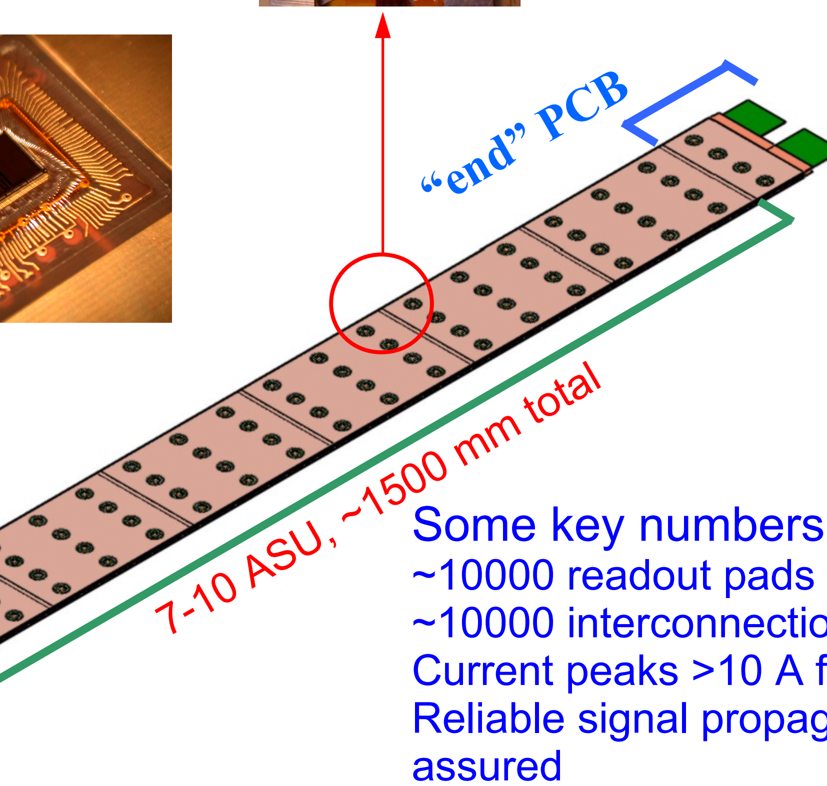
PCB
is glued
onto
SiWafers





using a gluing
robot

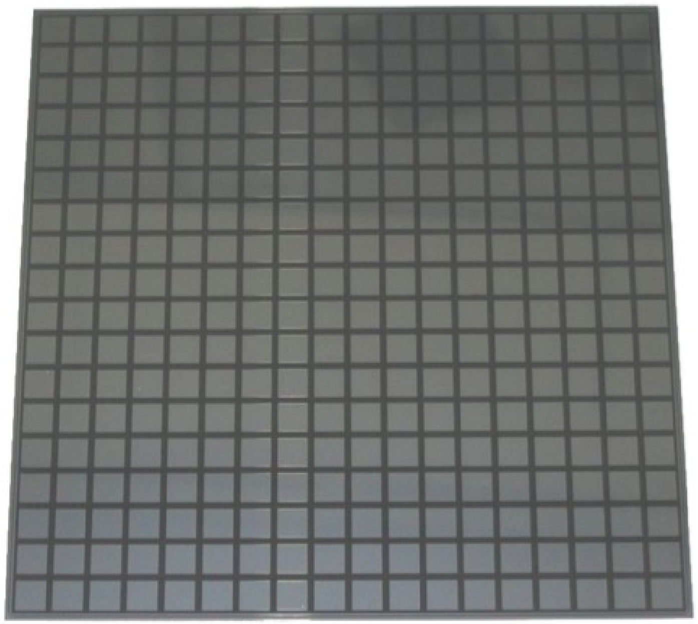





Some key numbers:
~10000 readout pads
~10000 interconnections
Current peaks >10 A for 2ms
Reliable signal propagation to be
assured
Further details in backup

Successful realisation of a long layer is maybe one of the most challenging R&D projects in worldwide detector R&D

# SiW Wafer R&D



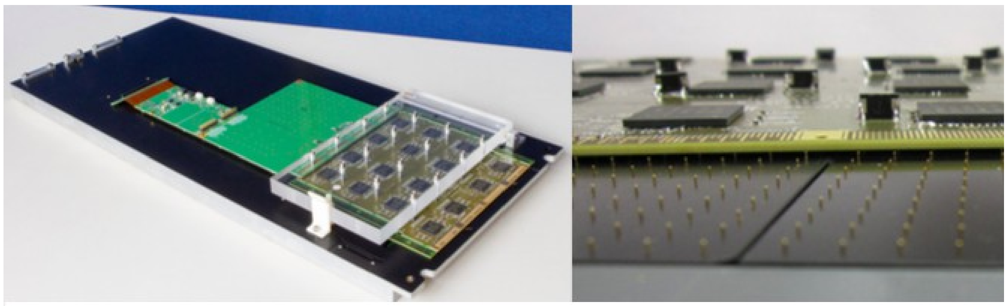
High resistive Si Wafer from Hamamatsu Photonics

- Excellent quality!!!
  e.g. leakage current O(nA/pixel)

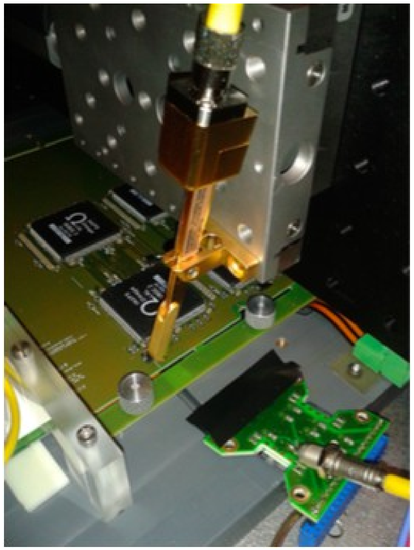
- However, expensive (2kEUR/wafer) and
  Large quantity needed requires quest for
  further producers e.g. Lfoundry, Infineon, ...

## SiW Wafer tests:

Desktop setup with unglued sensors



Laser station



Well advanced infrastructure for full wafer characterisation

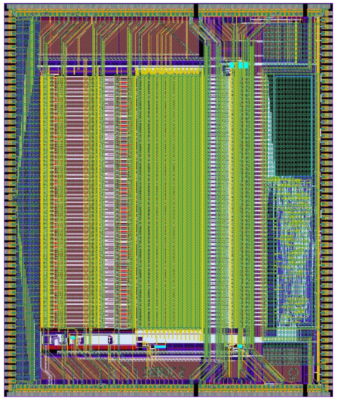
Common interest for LC, CMS, ATLAS

# Front end electronics and DAQ



## SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm, 64 channels
- High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)
- Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)
- Auto-trigger at ½ MIP, on chip zero suppression
- Low Power: (25µW/ch) power pulsing



## DAQ system

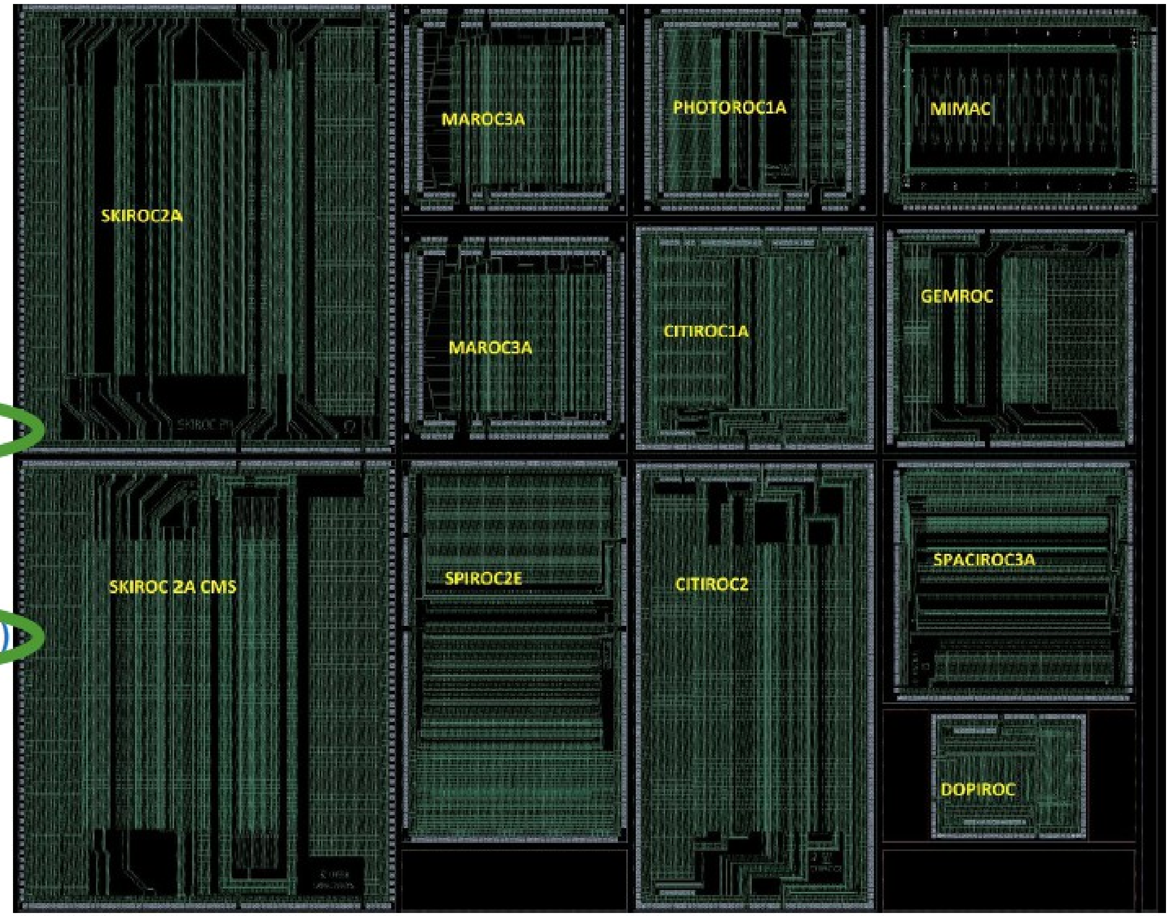
**Standard**: Giga-ethernet, 8b10b encoded local link, diff. pairs lvds signals over HDMI

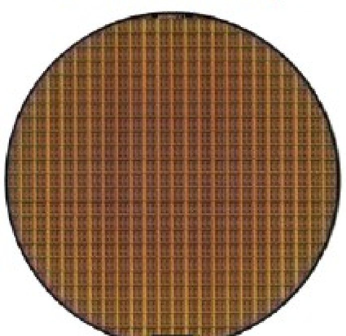
**Scalable**: architecture of a computing network w/o routing, modular software configured using XML, scripted using python.

**Compact**: one cable for slow control, data acquisition, fast signals and possibly power

# ASICs – Recent Production

- CITIROC1A
- CITIROC2
- DOPIROC
- GEMROC
- MAROC3A
- PHOTOROC1A
- SKIROC2A (PIN)
- SKIROC2-CMS
- SPACIROC3A
- SPIROC2E (SiPM)
- 1 other chip



Schedule : Chips expected for middle of May 2016

Dicing and packaging : June 2016

http://omega.in2p3.fr

callier@omega.in2p3.fr

2

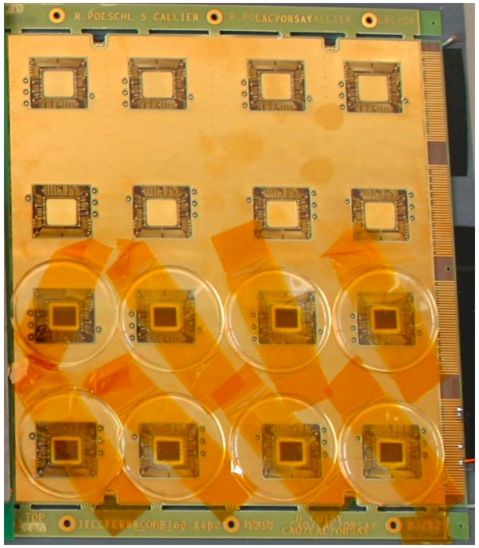
# PCB R&D

**Two options:**

**BGA packaged chips**

BGA version is safe incremental step:
test of chips before soldering ;
Space for external decoupling capacitors
Symmetric stacking will improve flatness,
good for wafer gluing
Optimal shielding of signal traces
Solution for technological prototype

**PCB with naked die**

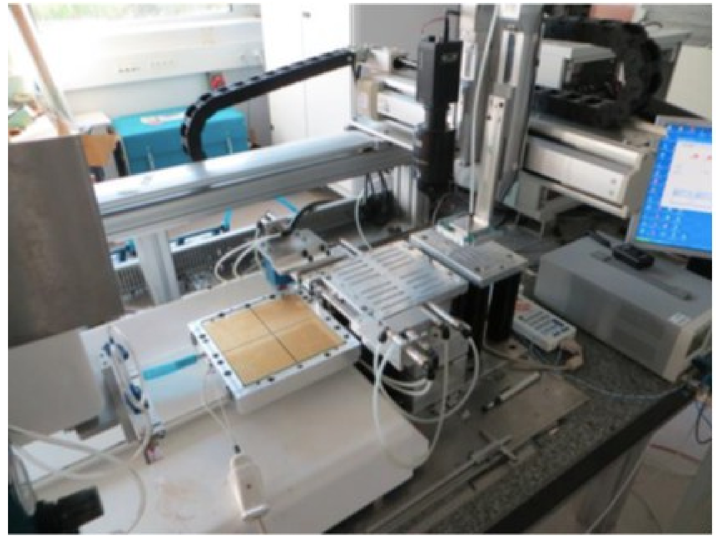


- Thin board (~1.2mm)
  => maximal channel density

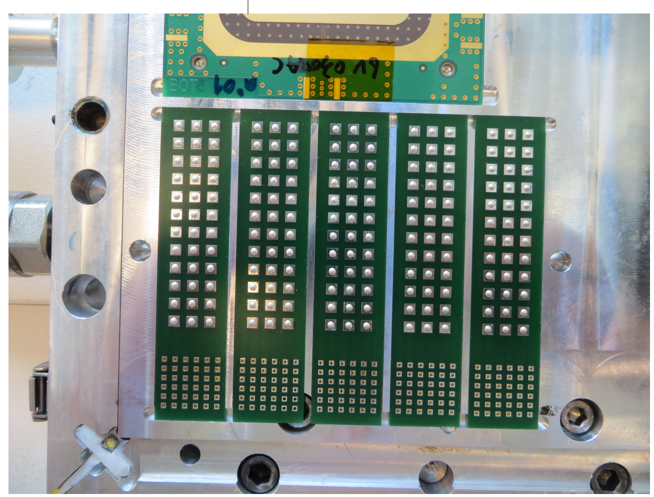
- Tests since 2015
  => Intensive test programme
  e.g. Noise and cross talk

- New production for 2017

# Versatile Gluing Robot



Done, FEV11_BGA

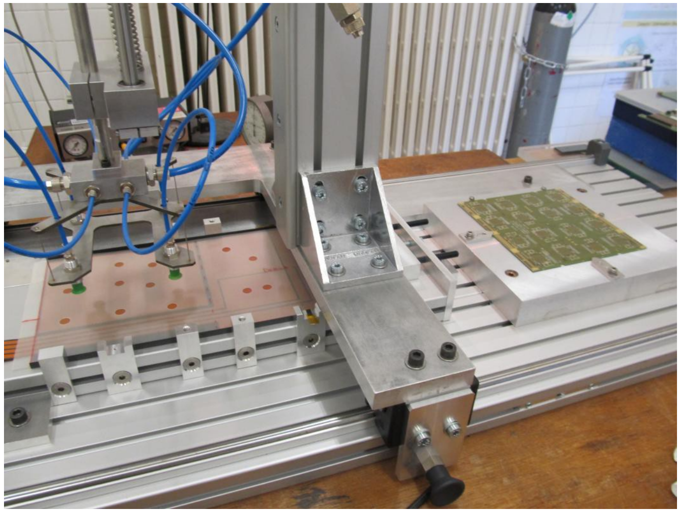


Done, HGTD-LGAD

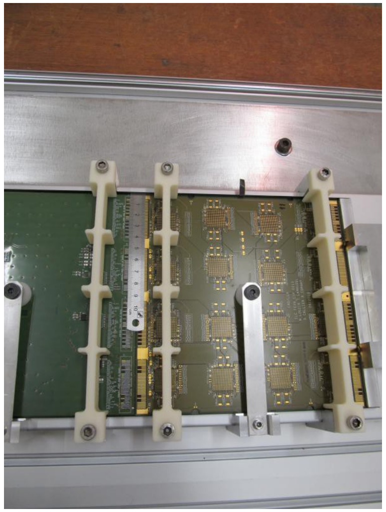
Under discussion, FEV_COB

# SiW ECAL Assembly

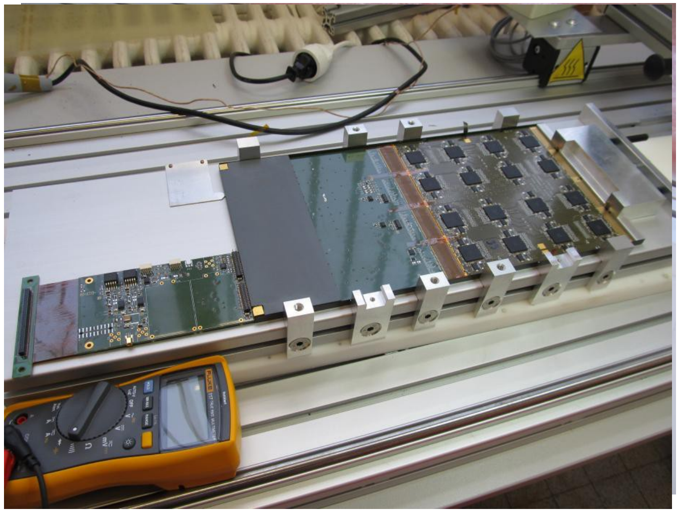
Pick and place



Precise alignment



Ready for test



- Assembly steps are validated with short layers (13 assembly steps)

- Need big step towards long layer to assure high quality product
  - Automated pick-and-place and alignment
  - Interplay of many different working steps
    a) Assembly proper
    b) Continuous control of up to 8 (14) ASUs during assembly

- Successful product requires a lot of testing and exercising of well trained technical staff!!!

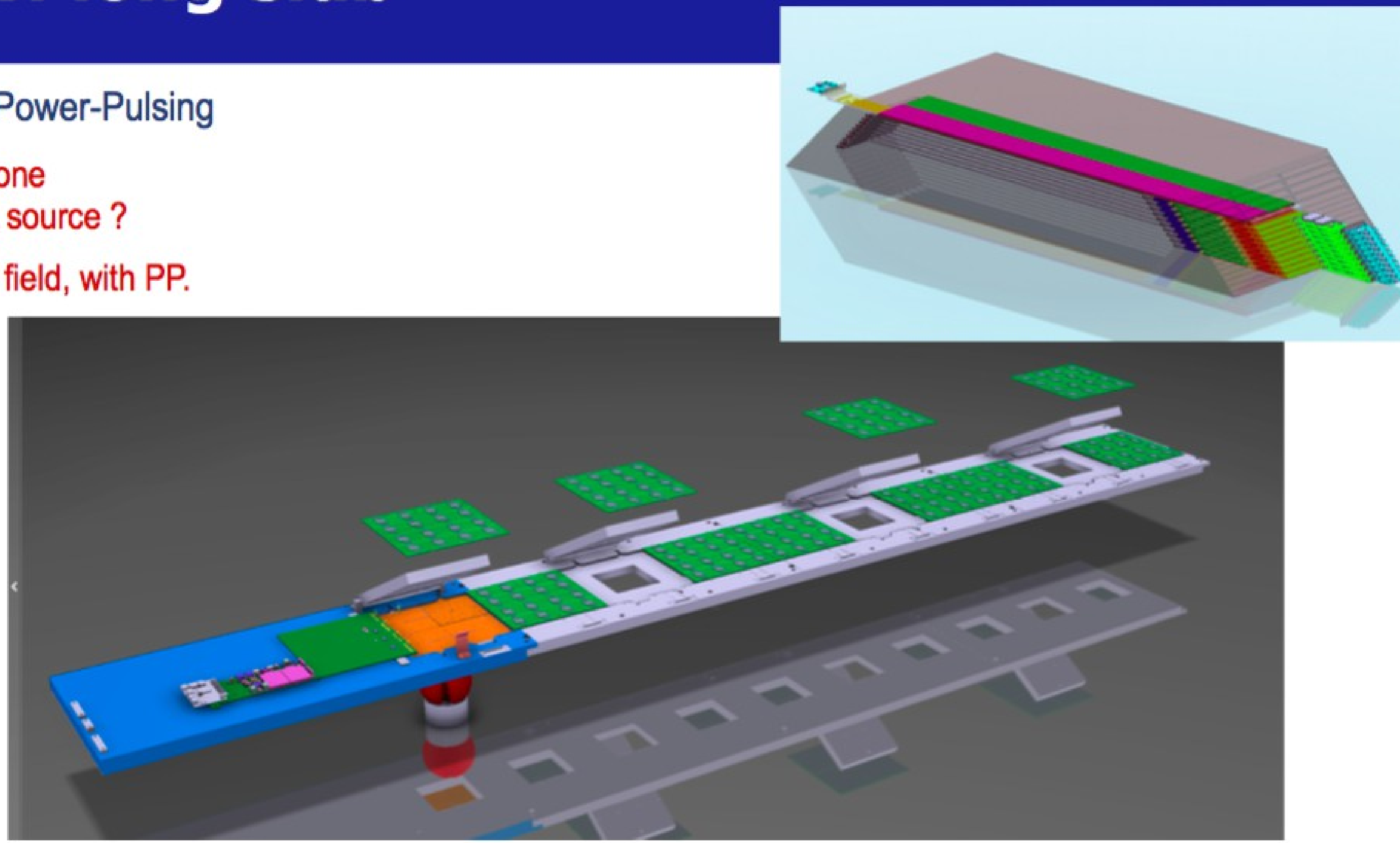
- Synergy with ATLAS HGTD and CMS HGCAL (?)

# Long slab – Test bench?

## Test of HW: long slab

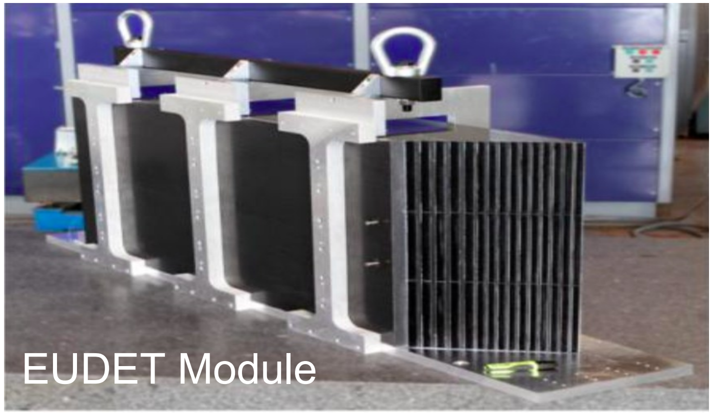
8–10 ASUs stitched in Power-Pulsing

- what can't be done
  with a small RA source ?
- perf in strong B field, with PP.



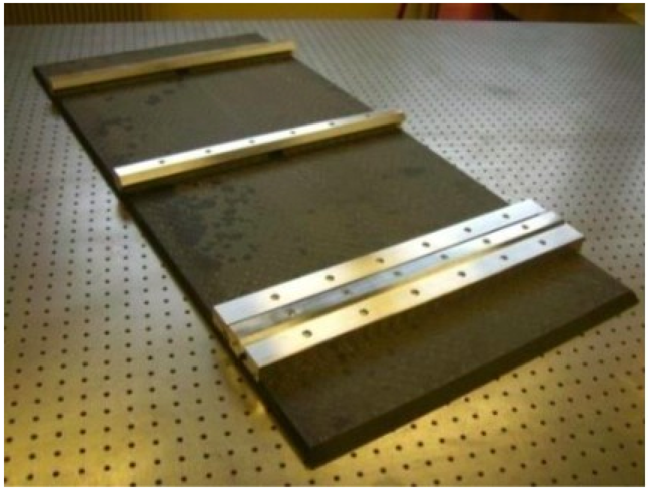
*V. Boudry, ECFA Workshop 2016*

# R&D on carbon/fibre structures




- Construction of full size mechanical C/Fibre structures

- up to 2.5m long alveoli
- Interface to other detectors i.e. HCAL in ILD



**Pioneering work by CALICE France for compact calorimeters**

# AIDA2020 Milestone on Cooling System

AIDA 2020 — DESIGN OF COOLING SYSTEMS FOR TUNGSTEN / CARBON FIBRE AND FOR HADRON CALORIMETER STRUCTURES — Milestone: MS31 — Date: Dd/09/2016

Grant Agreement No: 654168

**AIDA-2020**

Advanced European Infrastructures for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDA-2020

**MILESTONE REPORT**

**DESIGN OF COOLING SYSTEMS FOR TUNGSTEN / CARBON FIBRE AND FOR HADRON CALORIMETER STRUCTURES**

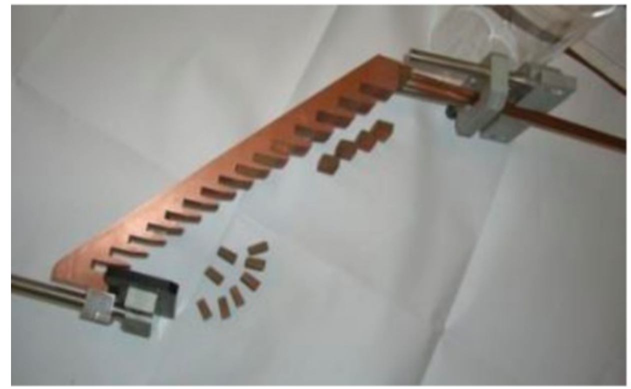
**MILESTONE: MS31**

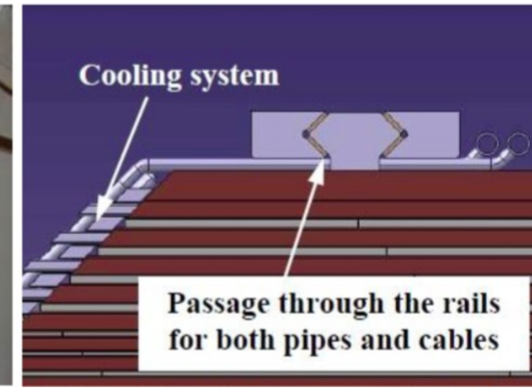
| | |
|---|---|
| **Document identifier:** | AIDA2020-MS31 |
| **Due date of deliverable:** | End of Month 18 (October 2016) |
| **Report release date:** | Dd/09/2016 |
| **Work package:** | WP14: Infrastructure for advanced calorimeters |
| **Lead beneficiary:** | DESY |
| **Document status:** | Draft |


**Abstract:**

The front-end electronics for both highly granular silicon-based electromagnetic and hadronic calorimeters requires a highly integrated and efficient cooling. Thermal properties of tungsten and carbon fibre based absorber elements drive the cooling concepts of electromagnetic calorimeters; it is the same with the properties of steel absorber stack for hadronic calorimeters. The feasibility and the development of a large leak less water cooling system has been successfully demonstrated for low power calorimeter readout electronics. Thermal modelling and measurements performed on demonstrators constructed within the EUDET project and distributed between two participating labs, fulfil the thermal requirements.

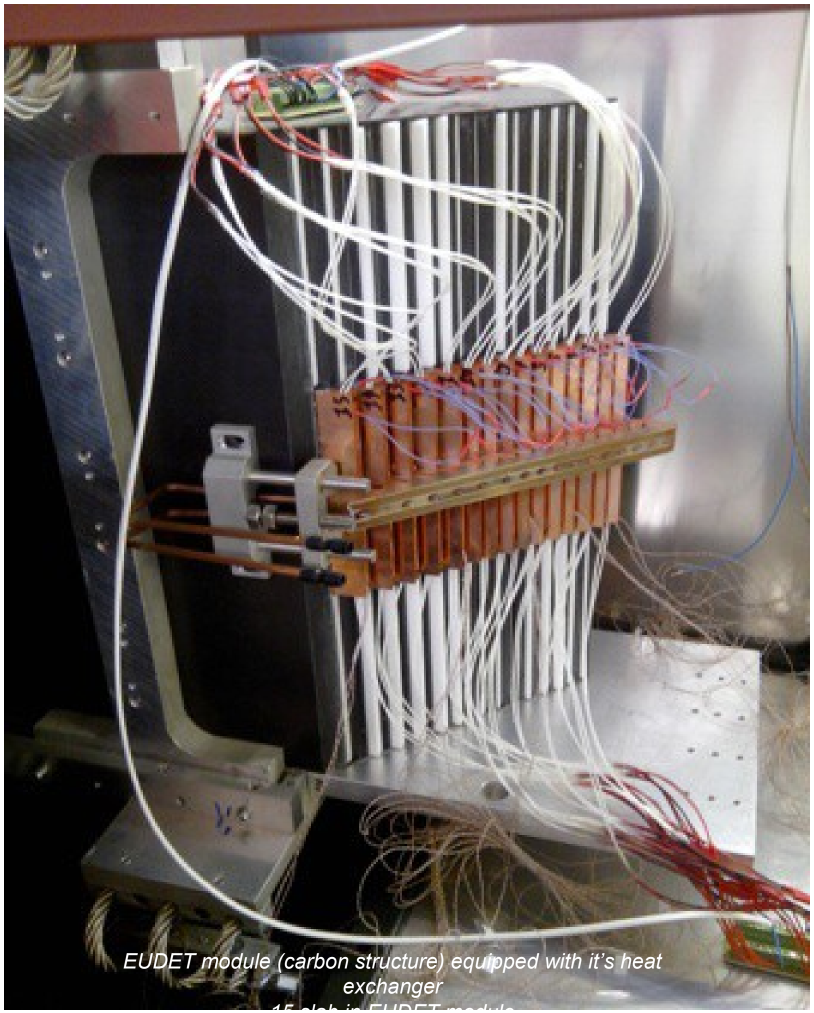

Grant Agreement 654168 PUBLIC 1 / 26



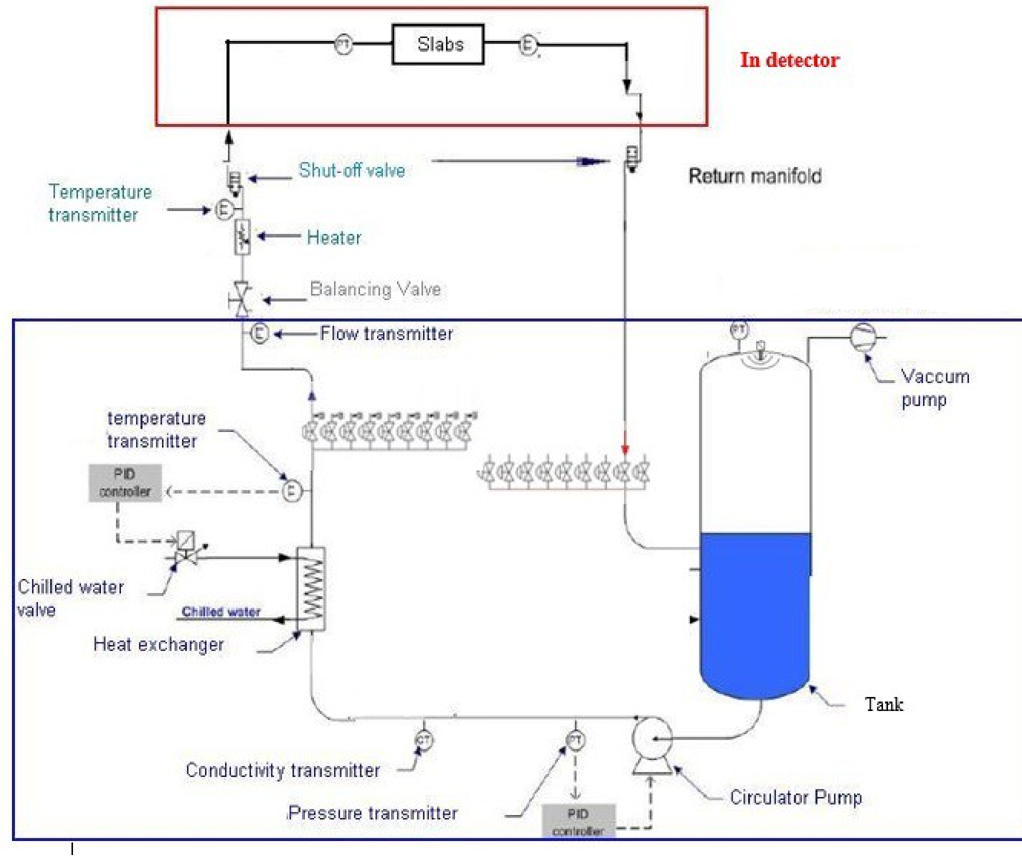



- Interface to cooling system for compact Carbon/Fibre structures
- Study for EUDET Module -> ILD Detector
- Design backed up by thermal simulation
- Can be adapted to other structures of same type

# Towards Full Sized Cooling system

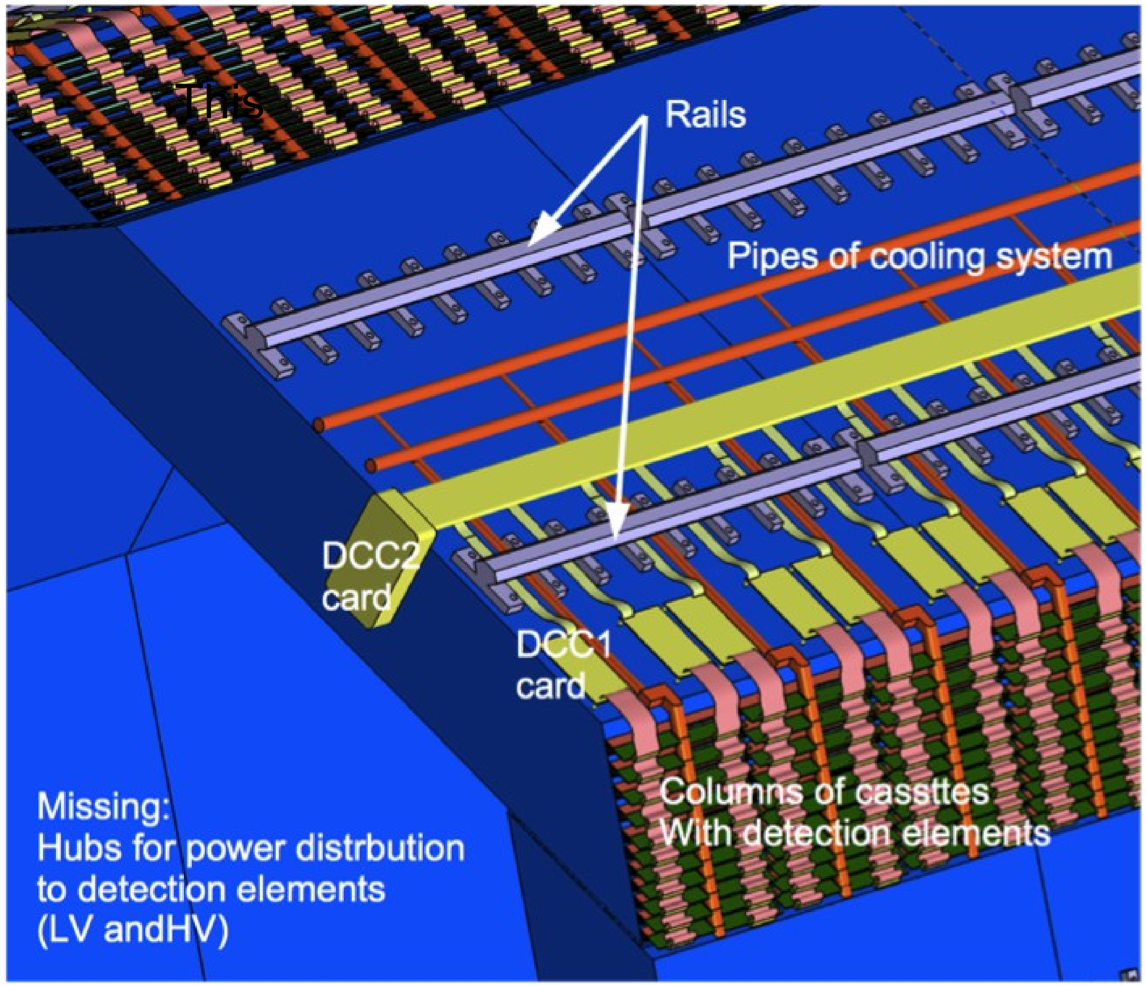


*EUDET module (carbon structure) equipped with it's heat exchanger*



# Readout, power supply and all that ...

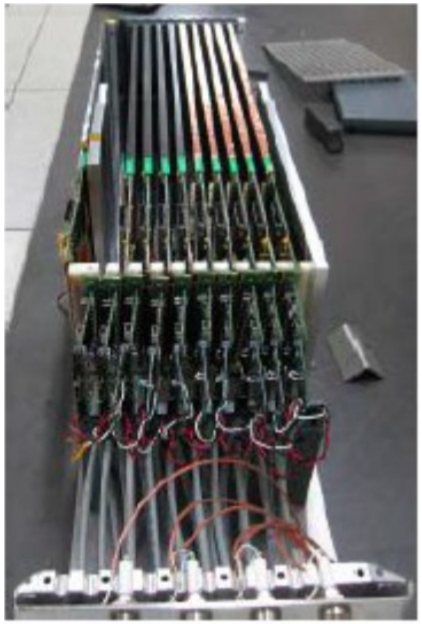
How to fit services into ~3cm between Ecal and Hcal in ILD

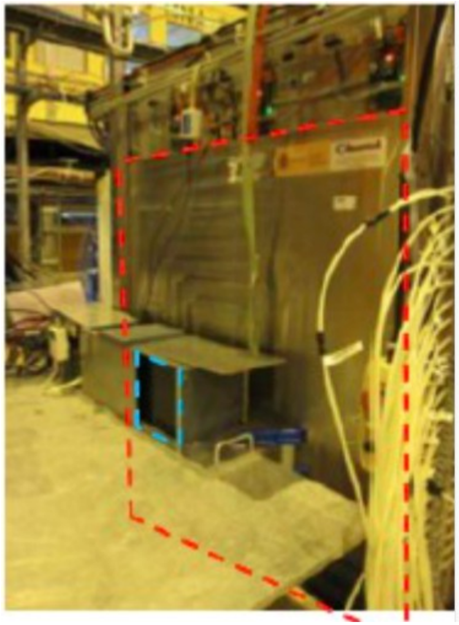



N.B.: Image by M. Anduze and H. Videau (plus some more or less intelligent addenda by R.P.)
Design under revision (but challenge remains unchanged)

# Testbeams 2017







## Standalone test beam

- Late Spring 2017 at DESY
  - ... after debugging of existing stack
    and progressive integration of supplementary layers
- Autumn 2017 at DESY or CERN
  - Option depending on conclusions of Spring beam test
- What about SLAC > 2017?

## Combined test beams

- Autumn 2017 at CERN with SDHCAL
  - \- Option if all works well
- More beam tests > 2017
  - ... with SDHCAL
  - ....with AHCAL

# Testbeams 2017 - Related needs

Material:

- Si Wafers
  - 10 additional short layers require 40 Si wafers + spare
  - to be shared between in2p3 and partners
  - Exact sharing to be discussed
  - Purchase would need to launched very soon

=> Conclusive results with technological prototype require investment in wafers

Travel:

- Plan for 2x2 weeks of beam tests in 2017
  - Cost DESY ~ Cost CERN

- Test beams need O(15) people from French SIW Ecal groups
  - Physicists and engineers

- Limited funding through AIDA-2020 TA and HIGHTEC
  - O(3) persons per beam test

=> Need funding for about 12 beam test participants
~24 weeks since not everybody needs to be there all the time

# Conclusions

- SiW Ecal R&D for LC is more challenging than ever
  - Well integrated in local and international R&D networks
    - AIDA-2020 and HIGHTEC until ~end of 2019
  - Cooperation with ongoing LHC detector R&D

- Beam tests with short layers
  - First tests in 2015 and 2016
  - Continuation with extended stack in 2017 (and beyond)

- Gradual move to system aspects
  - **Long layers**
  - Full sized cooling system
  - Service integration in tight space
  - Quality and assembly chain
  - Stress tests for alveolar structure (not shown today)

- R&D on core components and techniques
  - Silicon wafers
  - ASICs
  - Thin PCBs
  - Gluing

# Backup

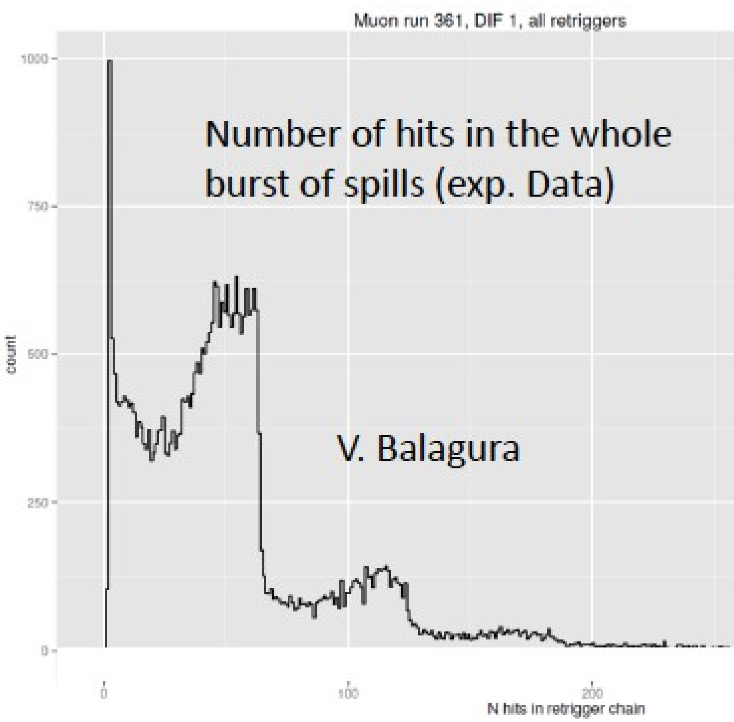
# SiW ECAL – Brief recap

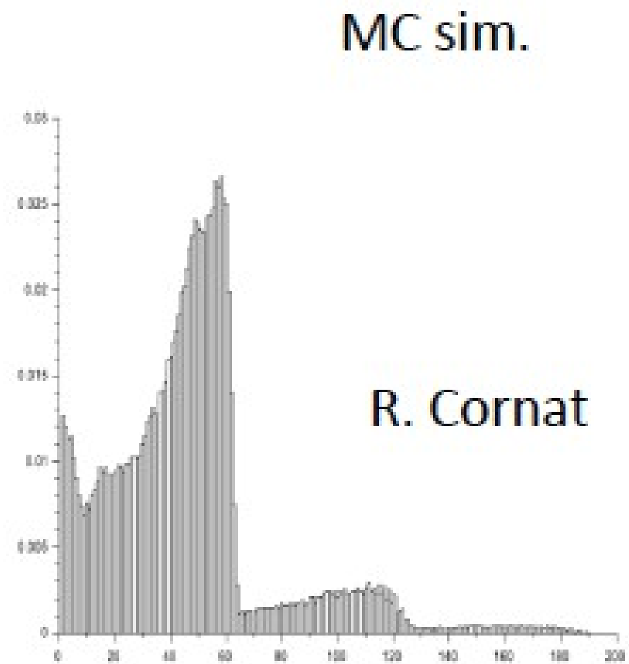
- Testbeams
  - Physics prototype
    - 2005 DESY (standalone)
    - 2006-2007 CERN (with analogue Hcal)
    - 2008 and 2011 FERMILAB (2008 with analogue Hcal, 2011 with digital Hcal)
  - Technological prototype
    - 2012-2013 DESY
    - 2015-2016 CERN (2016 with SDHCAL)

- Combined testbeams within CALICE, data management through grid vo calice (data storage at DESY and CC IN2P3)

- Publications
  - 6 papers in peer-reviewed journals out of which 5 with French groups as principal authors or with major contributions
  - Numerous contributions to major conferences including peer-reviewed conference proceedings

Retriggers in successive bunch crossings

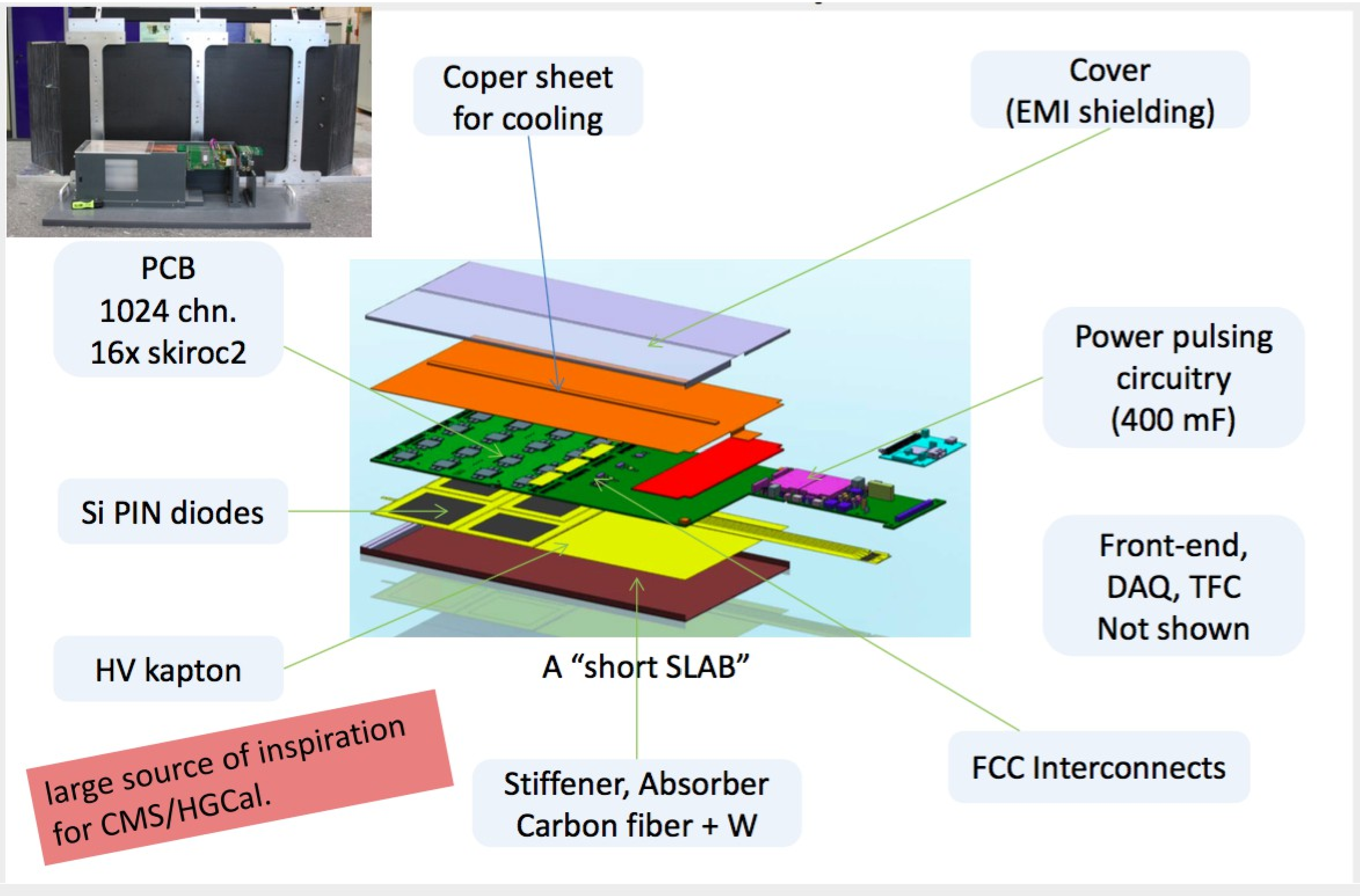



Towards model of hardware behaviour

=> Deep understanding of detector response

# SiW ECAL – Short layer



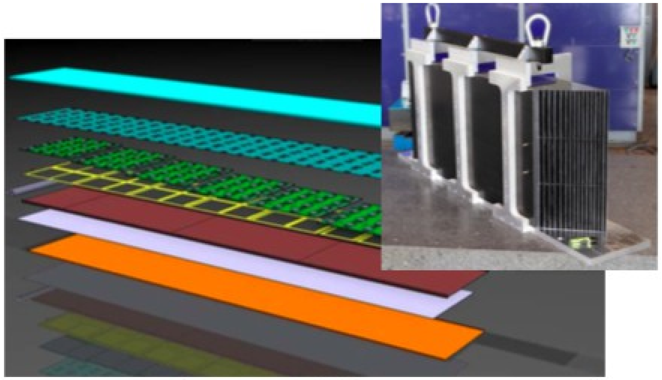

Between 12 and 15 short layers for HGCFC beam tests

*R. Cornat LLR*

# Long slab – More technical details

In principle, front-end boards will be chained forming up to 2m long detector SLAB, most of signals in bus

Issue 1 : clock distribution (5 & 50 MHz)
Interconnects are not impedance controlled (FFC)
One clock line may be loaded by 40 to 80 ASICS



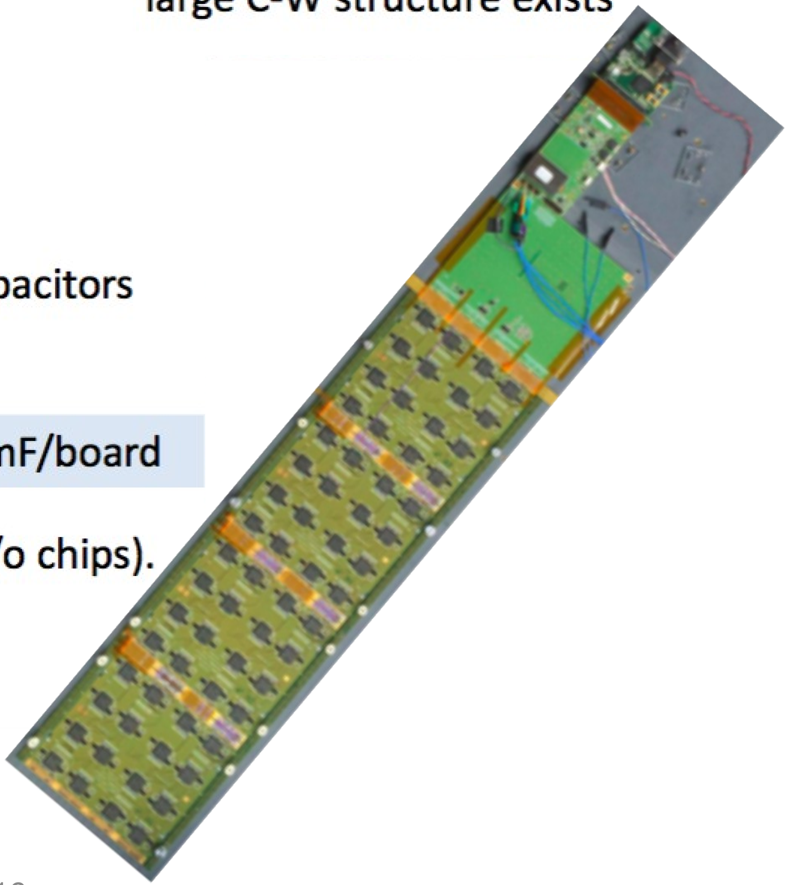
large C-W structure exists

- ⇨ Use of MLVDS adapted with 100 Ω on both sides, 100 mVpp remaining signal at the end (6 Ohms loss/board, 20-40 pF/board, up to 10 boards)
- ⇨ Next version ASIC will have a PLL generating the highest frequency

Issue 2 : Power distribution (12 A pulses) & blocking capacitors (tested with FET switches as loads)

- ⇨ Current taken from a 800mF super cap (16mΩ ESR) + 2mF/board

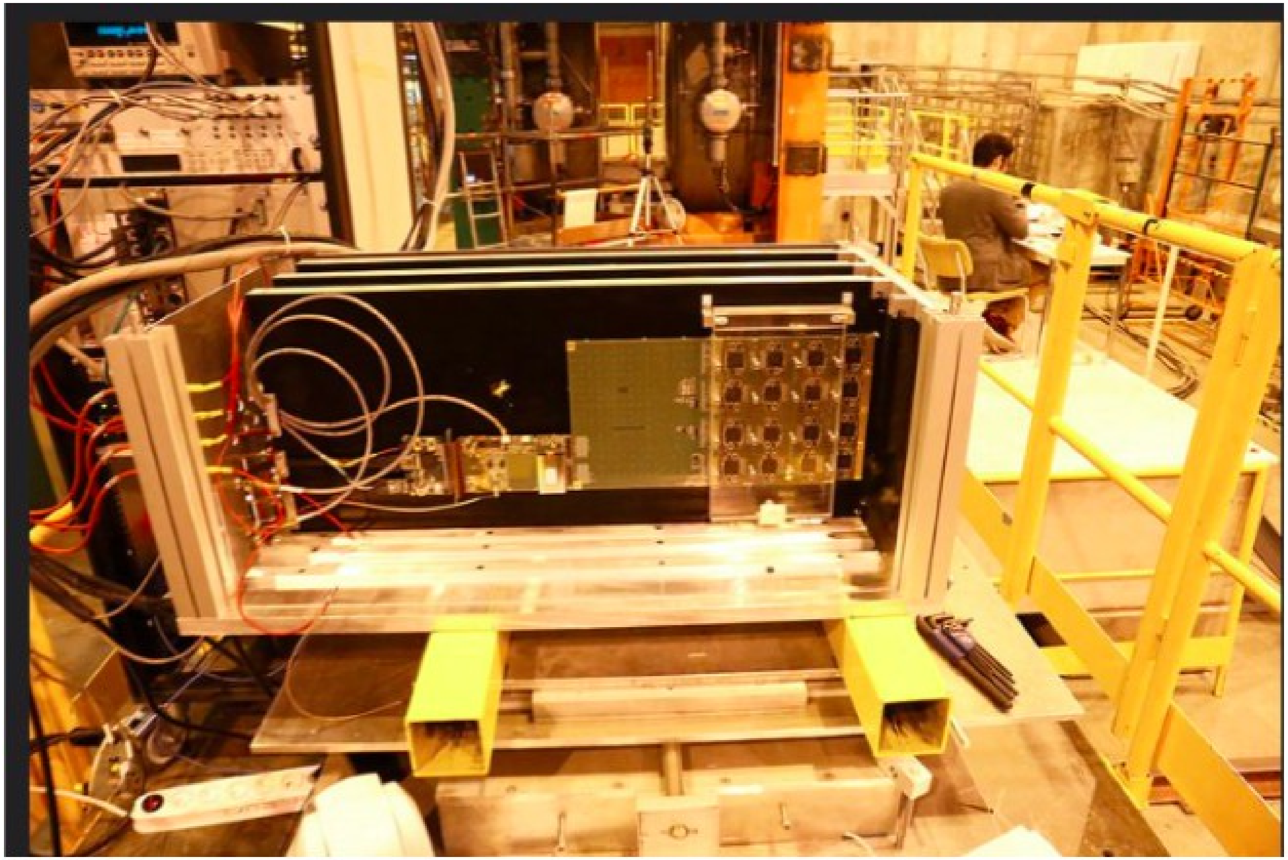
Along 6 boards, static loss is 250 mV due to connectors (w/o chips).
May foresee to distribute power in a star topology.
**4 boards SLAB being assembled at LAL**



*R. Cornat LLR*

# SiW ECAL – First short layers

Test bench and beam test setup of first short layers with preliminary assembly



*V. Boudry LLR*

# Assembly of SiW Ecal layers

# Study of composite structures

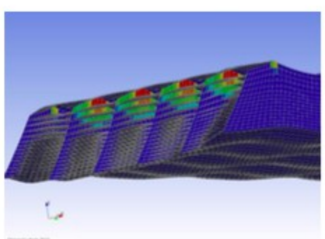
Use of Fiber-Bragg Gating Sensors for the characterisation of deformation of composites structures

## LLR demonstrator

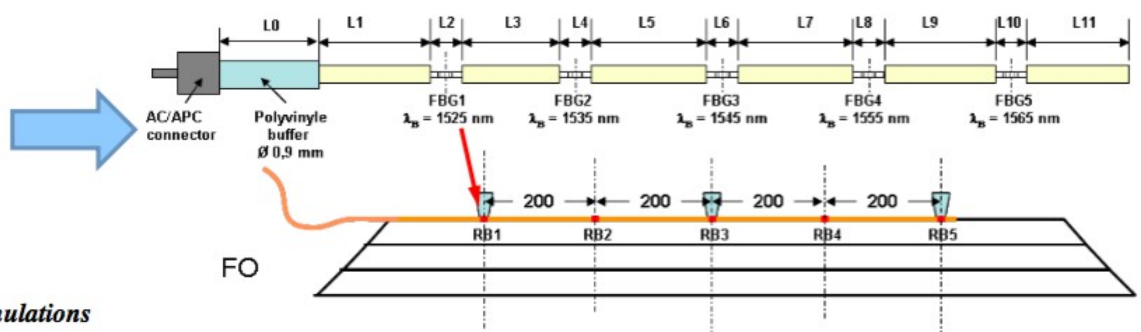
**Bending tests (3 and 4) on demonstrator equipped with 5 FBGs per fiber**

**Choice of demonstrator:**

1) A representative monolayer structure (3 cells)
2) implementation of FBG in the most stressed areas (directly under the rails: FBG1/FBG3/FBG5) + area with high elongation (FBG2/FBG4).

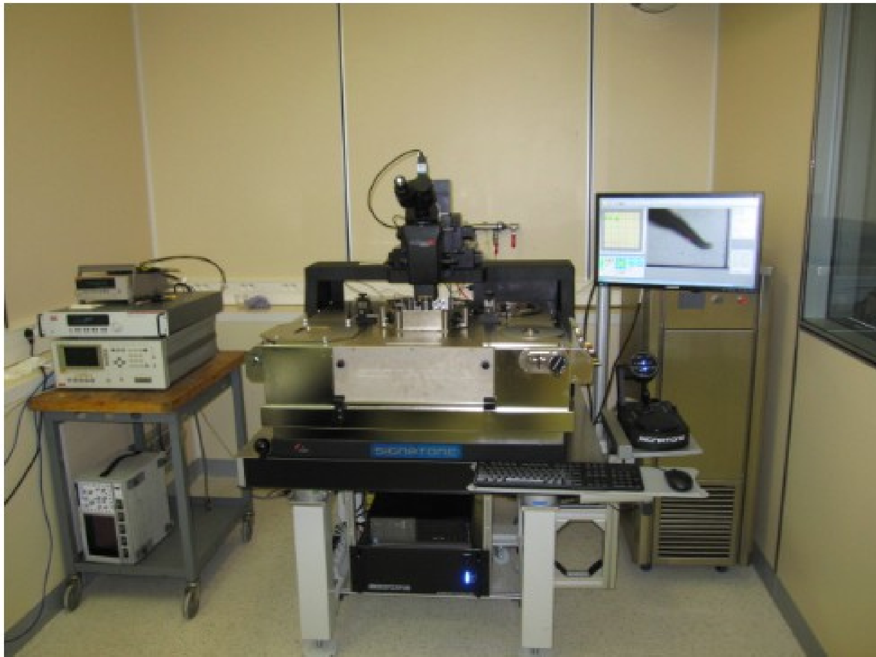


*Positioning of FBGs based on simulations*

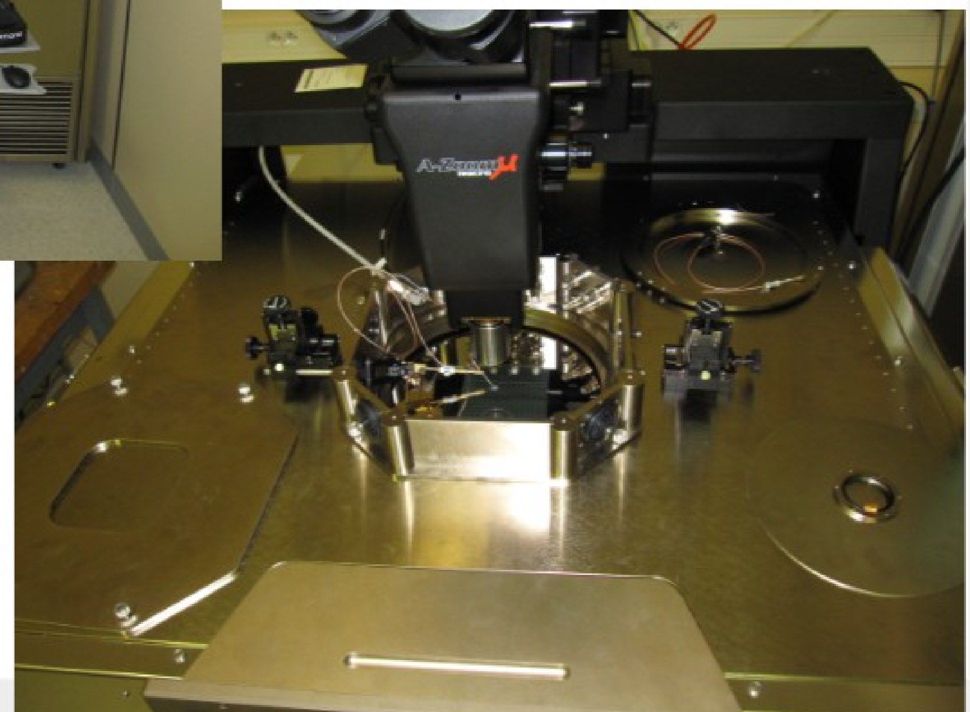



3) Optical fibers directly embedded into inter-cell walls, during the manufacture of the demonstrator

# Platform CAPTINNOV



A semi-automated test machine



Project of platform driven by CALICE developments (+ATLAS@LAL)

Interest from STM

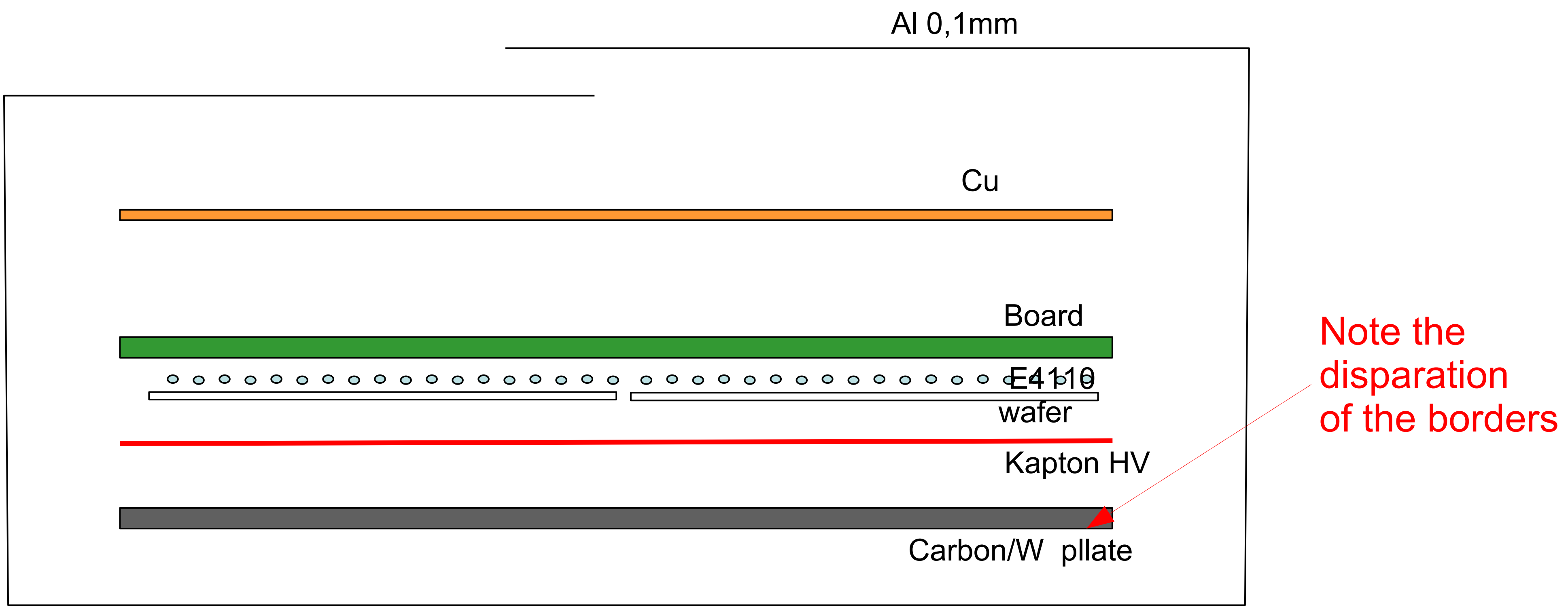
... has been already used for CALICE wafer cahracterisation

*R. Cornat LLR*

# SiW ECAL Assembly – Preliminary considerations



**Guiding lines :**
**Ease of assembly**
**Easetofabricate the elements**
**Robustness**
**Compactness**




J. Bonis/A. Thiebault