Application Specific Integrated Circuits for X-ray Detectors

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on behalf of ASIC Design Group

http://www.kmet.agh.edu.pl/asics

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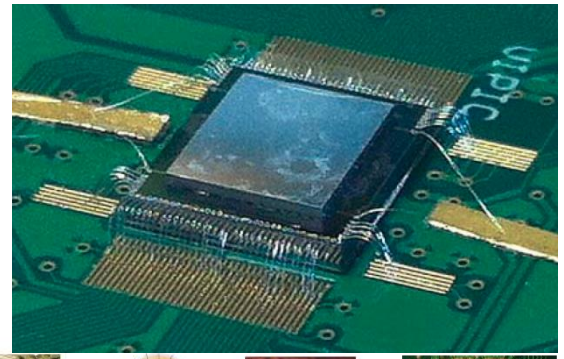
Outline

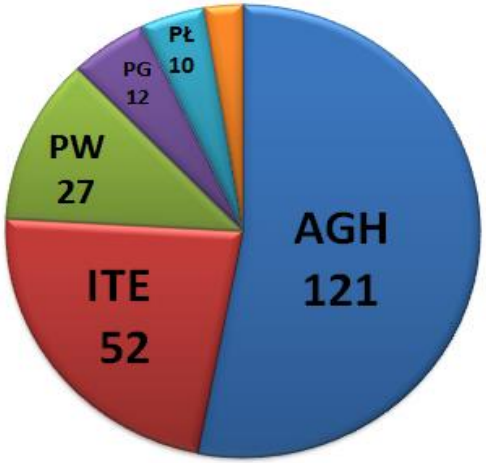
- Application Specific Integrated Circuit - AGH UST
- ASICs for semiconductor detectors: X-ray imaging
- Other ASICs applications - neurobiology

AGH University - ASIC Design

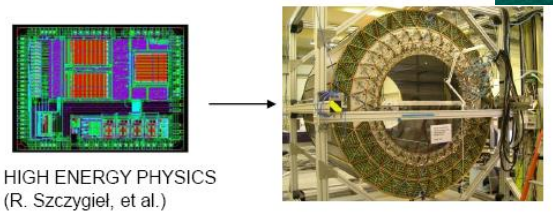
Universities and research institutes in Poland involved in Application Specific Integrated Circuit design

- AGH University of Science and Technology, Krakow,
- Institute of Electron Technologies, Warsaw ,
- Warsaw University of Technology,
- Technical University of Lodz ….

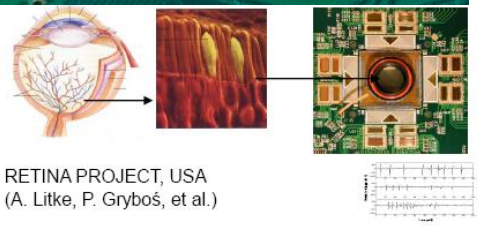




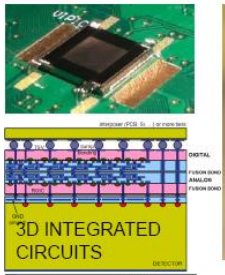
EUROPRACTICE statistics - chip design

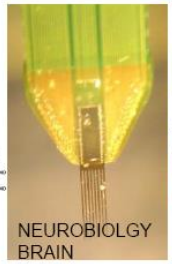


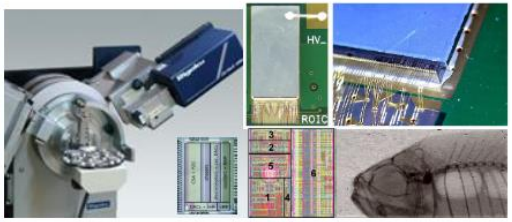
HIGH ENERGY PHYSICS
(R. Szczygieł, et al.)



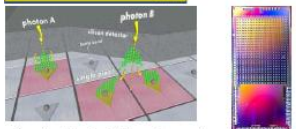
RETINA PROJECT, USA
(A. Litke, P. Gryboś, et al.)







ASICs for Rigaku Corporation, Japan



pixel chip in 40nm to solve
charge sharing problem

AGH University:

- IEEE SSCS Chapter Poland
- Cadence Academic Network

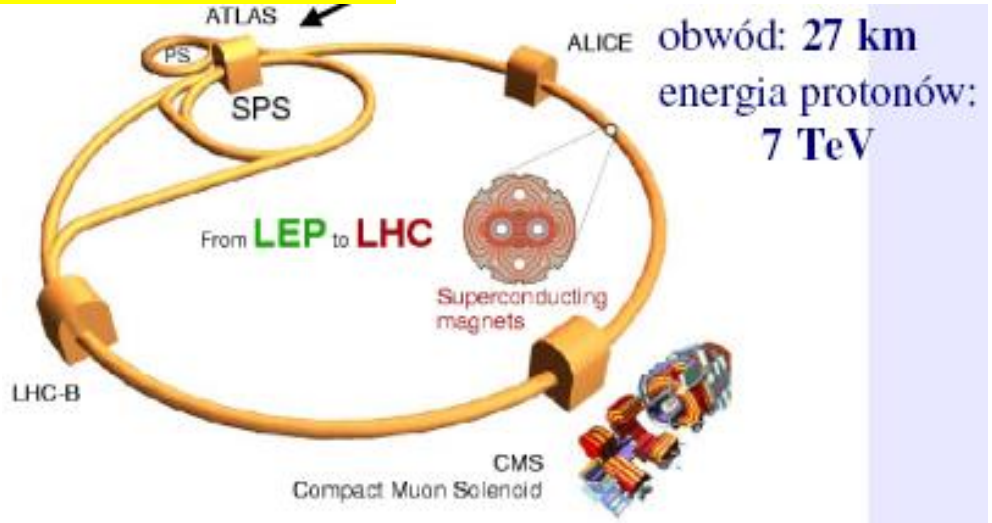
Most of designs are mixed-mode ASICs
Technology used: 0.35 um => 40 nm or 3D

ASIC for High Energy Physics, X-ray Imaging, Neurobiology Applications

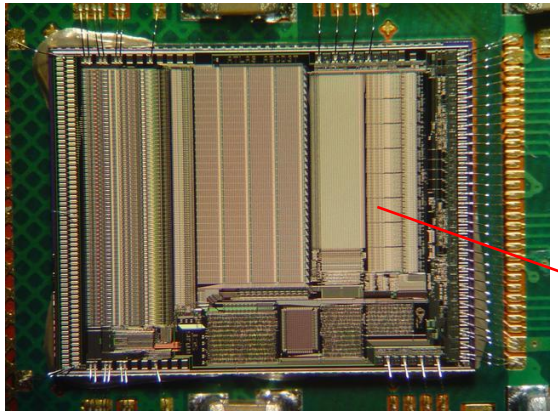
AGH University of Science and Technology

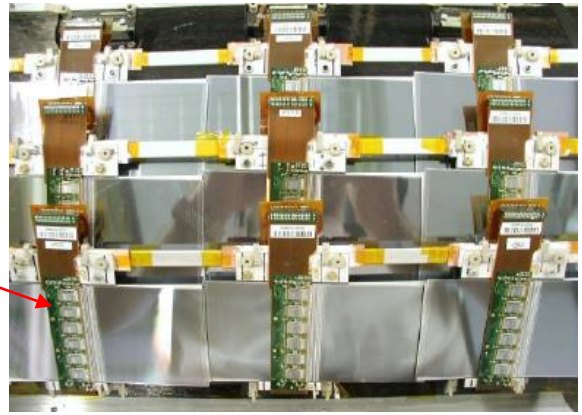
- One of the oldest and biggest Polish technical universities
- 16 faculties, 65 fields of study, more than 200 specializations
- Over 33 000 students
- Over 200 000 graduates
- 2 200 researchers including more than 650 associate and full professors
- Own attended campus area
- ~50% of budget from projects

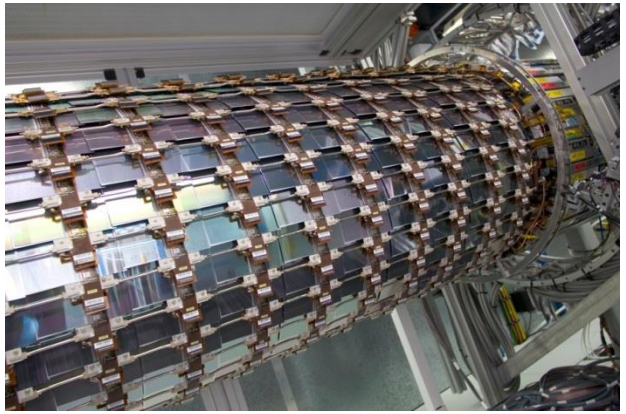
Example of AGH-UST project for European Center for Nuclear Research CERN



ATLAS experiments: readout of silicon strip detector – 6 millions channels

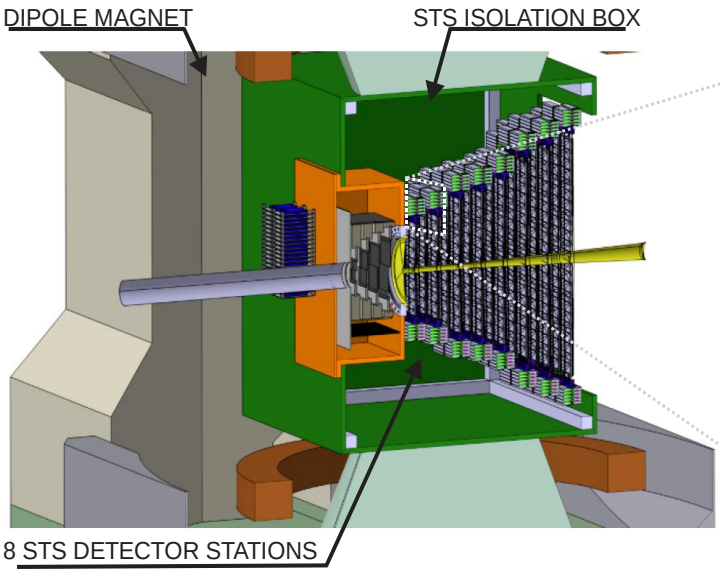


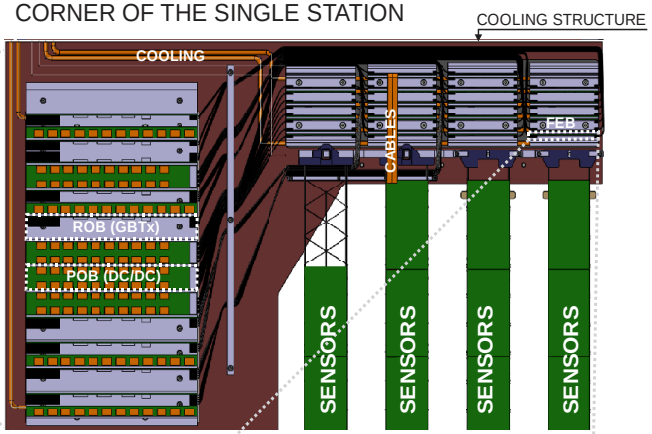


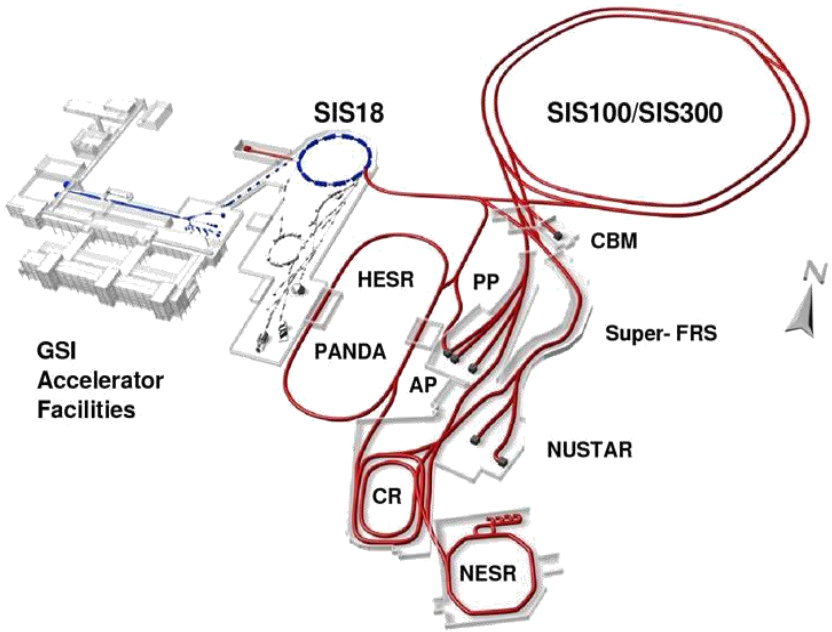


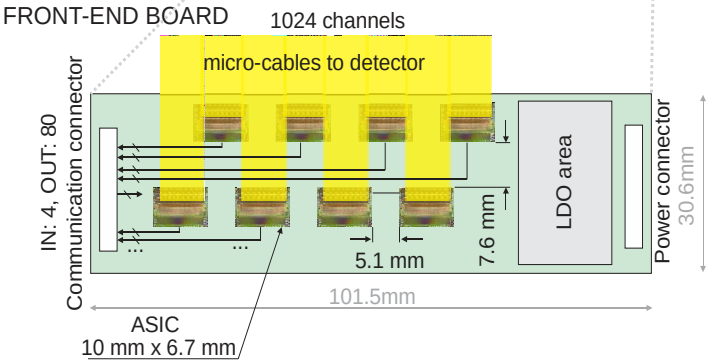
Integrated circuit (6.5 x 8.4 mm^2) in very advanced rad-hard technology designed by scientists from AGH.
W. Dabrowski, (R. Szczygiel), et al.:Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS semiconductor tracker, IEEE Trans. Nucl. Sci. 47 (2000) , pp. 382-9

GSI Accelerator Facilities



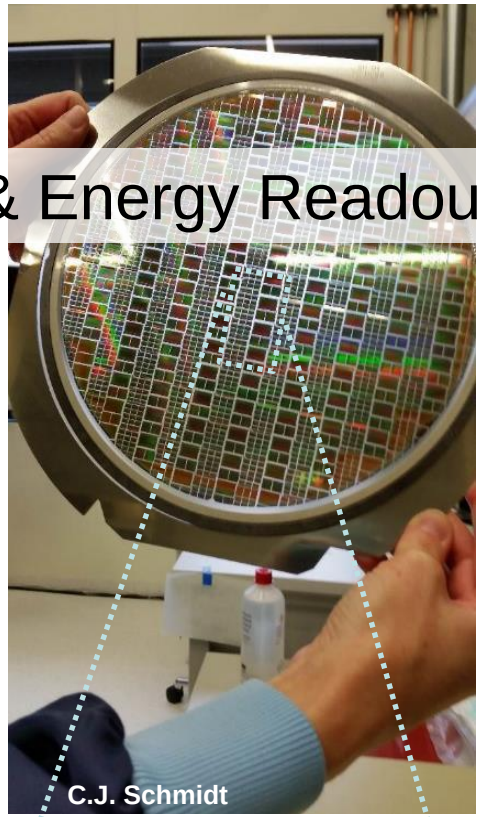






STS-XYTER2

Silicon Tracking System X and Y Time & Energy Readout

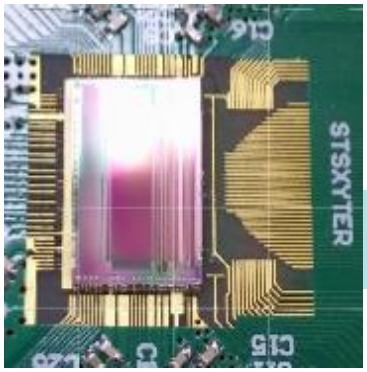


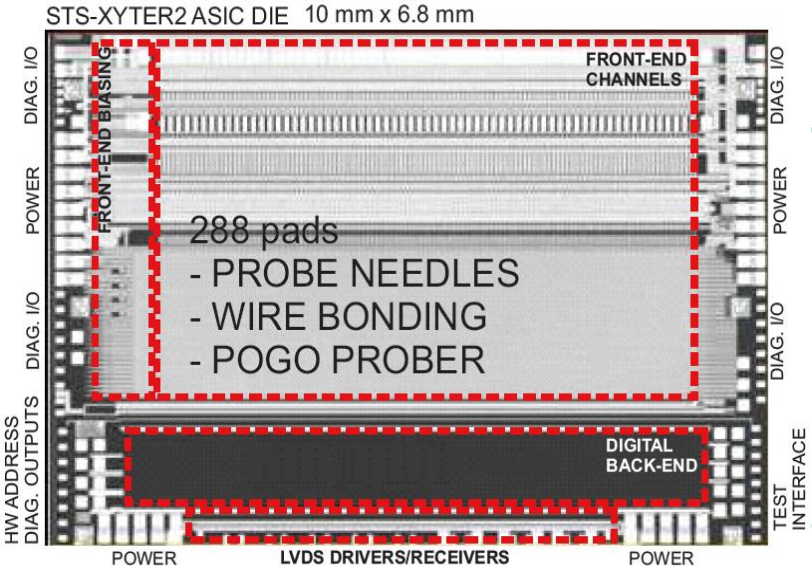
Engineering run wafer after dicing

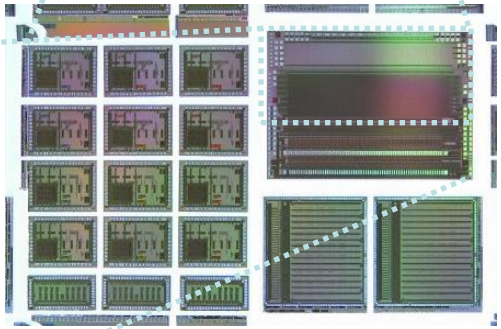
UMC 180 nm CMOS Engineering Run 2016 shared between other CBM chips
Thinning & stealth laser dicing
10 mm x 6.8 mm die size, 288 pads
130 channels + 2 diagnostic channels, Power: 1.1 – 1.3 W/chip
4420 bits of AFE configuration
54400 gates (after triplication), 12600 flops

Evolution of the STS-XYTER prototype

- New CSA & reset circuits
- Enhanced layout & schematics
- New back-end
- Dedicated protocol



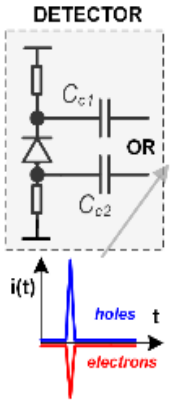




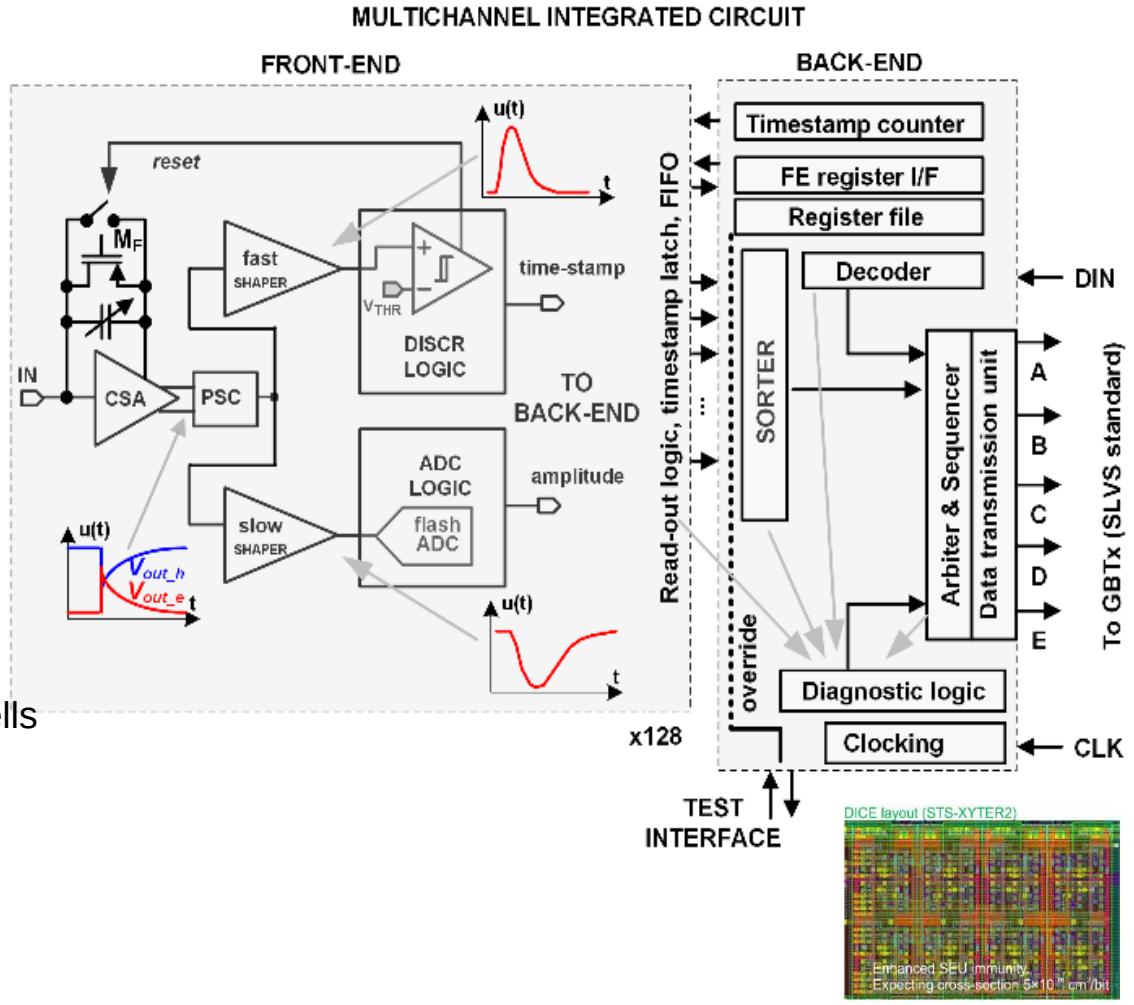
STS-XYTER2

128 channels
time (3.125 ns) & amplitude digitization (5-bit)

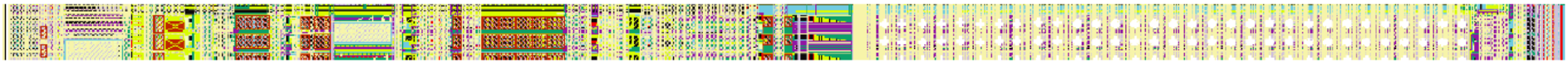
0-15 fC electrons & holes
gain switching & trimming
min. 250 khit/s rate (pulsed reset)
80-280 ns shaping time (slow path)
time-walk corrected offline
continuous-time ADC + peak det.
P=8.5-10 W/channel (incl. logic)



Back-end:
- control via synthesized reg & AFE DICE cells
- 9.41 – 42 Mhit/s/ASIC data BW
- throttling, diagnostic features
- link loopback (multi-level)
- 64-bit e-fuse for traceability

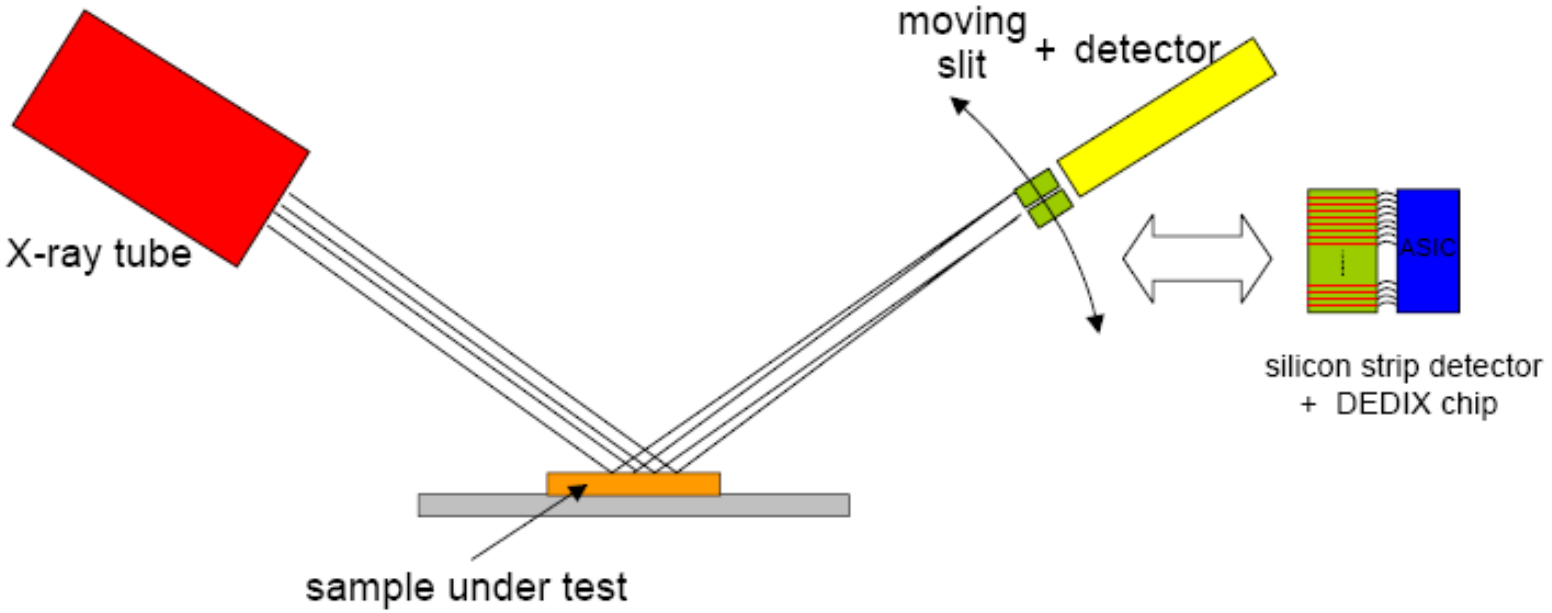


AFE Channel Layout



X-ray imaging
for diffractometry applications

Module for diffractometry
(128-512 channels)



100-times shorter measurement time!!!

Our target:

1) Count rate > 1 Mcps/strip (X-ray tube)
2) Keep low noise level < 200 el. (C=3pF, T=300K)
3) Matching: offset spread < 10 el. rms.
4) Energy window - even for high count rate

Scheme of imaging system

Single Photon Counting System based on SSD

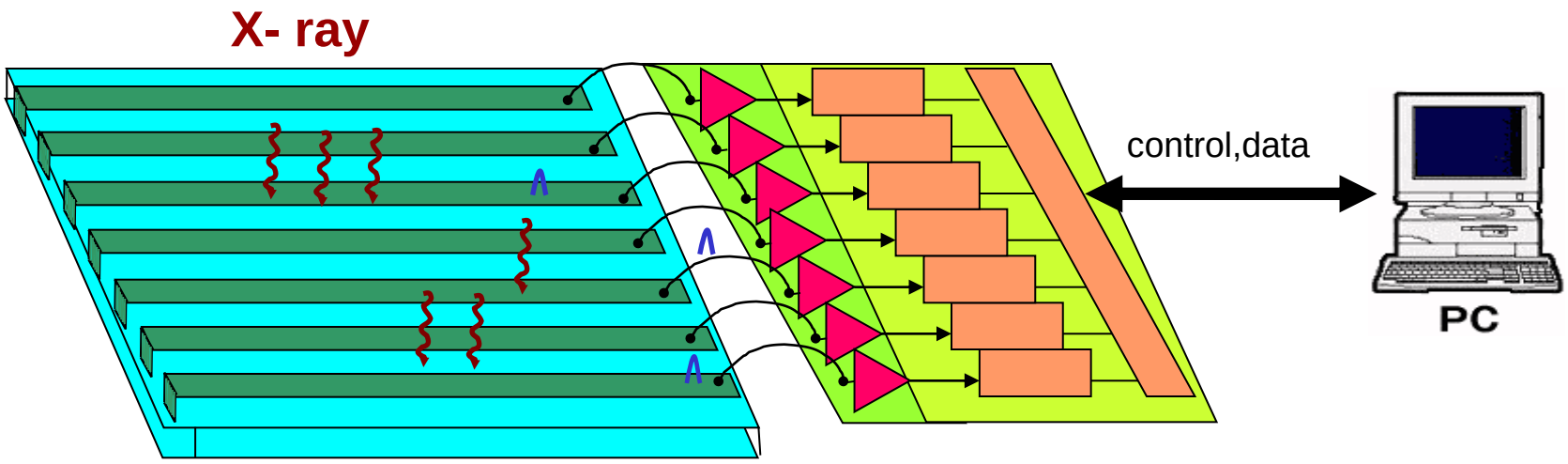
Diffractometry applications

(E = 8 keV Qin = 2200 el.)

Energy window selection for X-ray photons

High X-ray intensity

High count rate per channel



Silicon strip detector

⇓

- good spatial resolution: tens of μm
- energy resolution: 3.67 eV/e-h
- single photon counting mode
- good efficiency

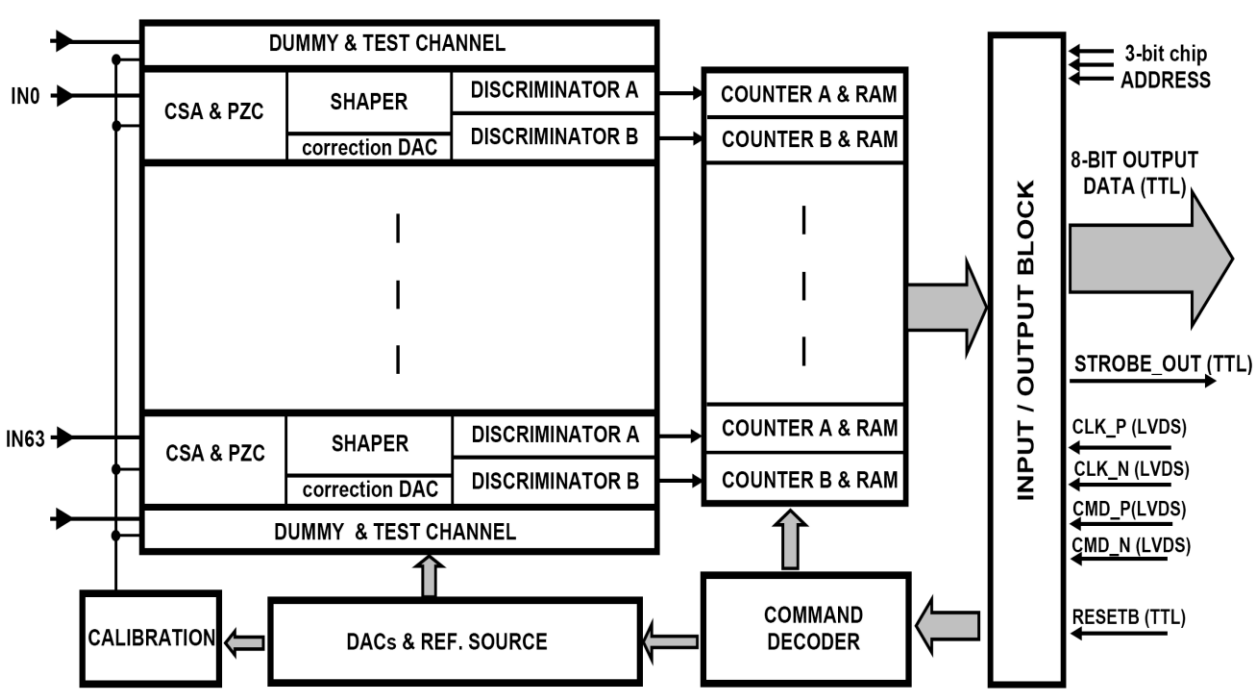
ASIC

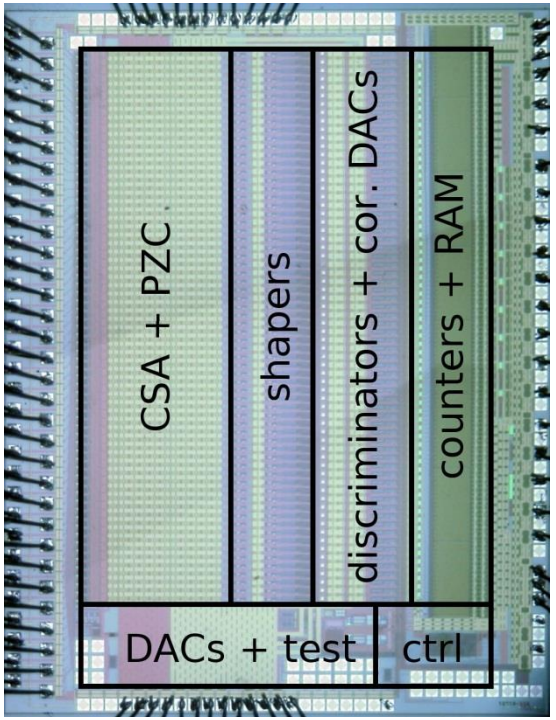
(analog processing + data storage)

⇓

- binary readout architecture to cope with high X-ray intensity
- selection of pulses according their amplitude

Block diagram of ASIC

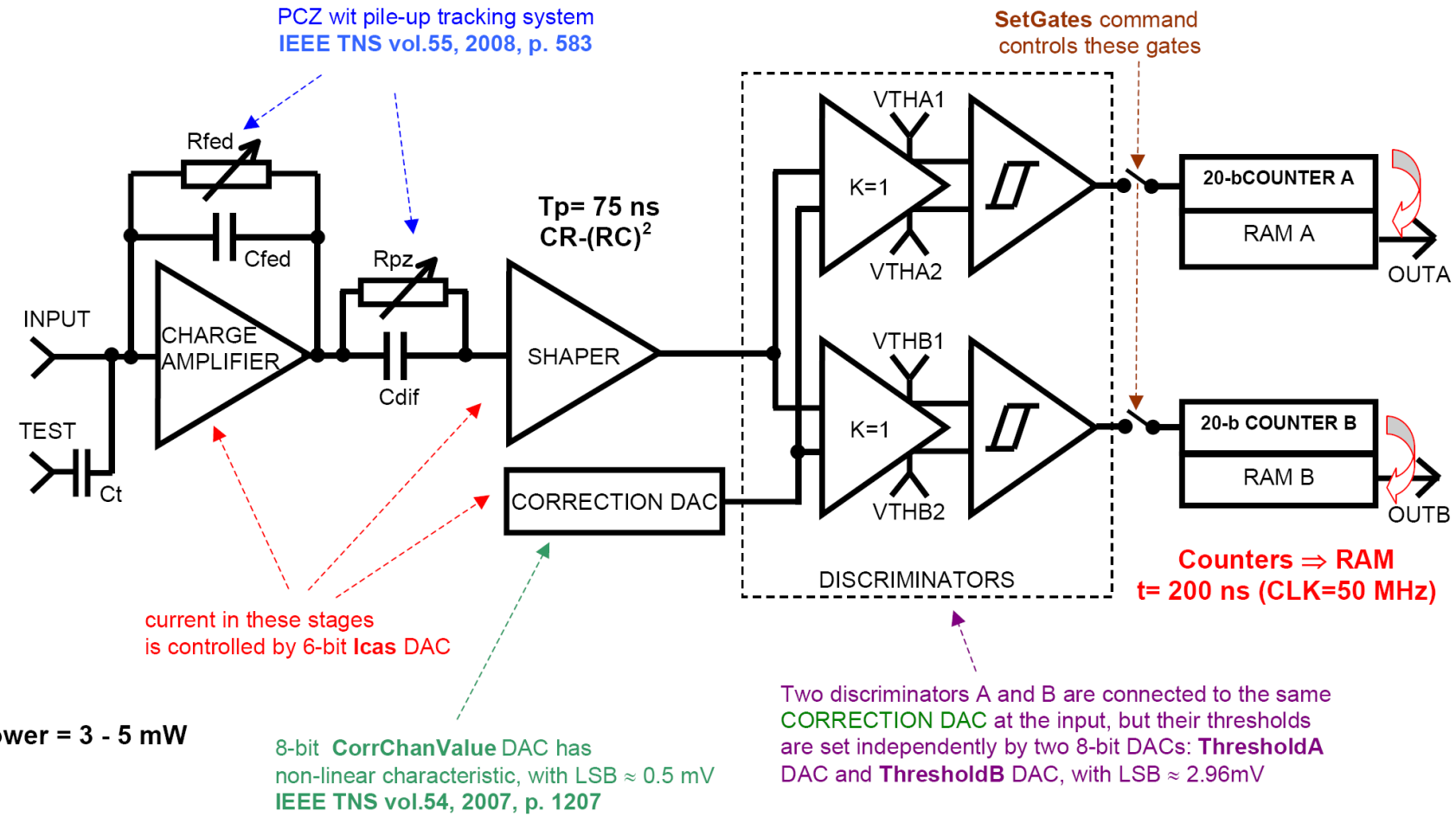




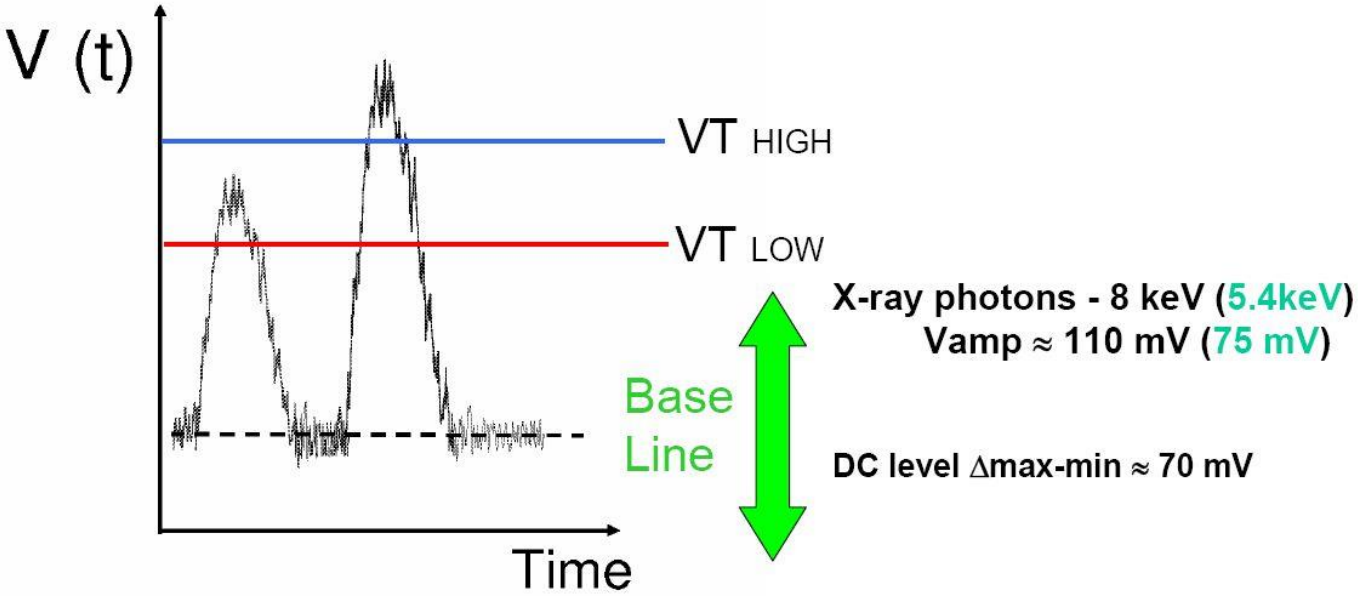
64 - channels, CMOS process 0.35 μm, 3.9 x 5 mm²

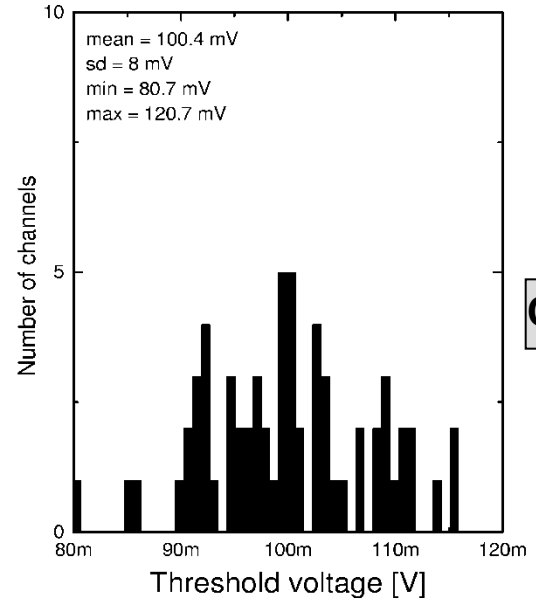
R. Szczygiel, P. Gryboś, P. Maj, A. Tsukiyama, K. Matsushita, T. Taguchi: *RG64 – High Count Rate Low Noise Multichannel ASIC with Energy Window Selection and Continuous Readout Mode*, **IEEE Transaction on Nuclear Science**, vol.56, no. 2, 2009, p. 487-495

Single channel architecture

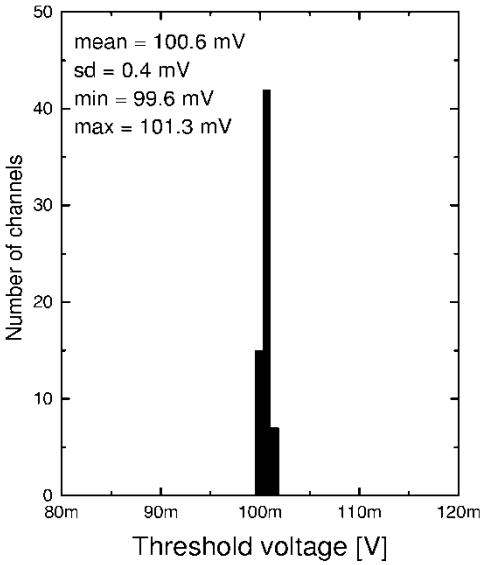


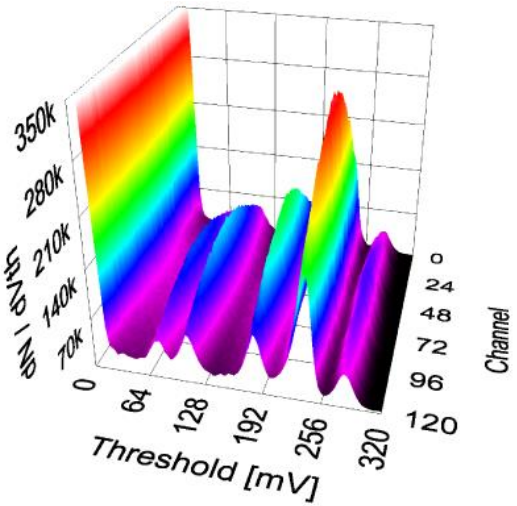
Matching: why correction is necessary?





Correction ON





D/teX ultra module, Rigaku Corporation, Japan

Technical specifications:

- Strip pitch: 0.1 mm
- Strip length: 20 mm
- Channel number: 128
- Count rate: >1x10^6 counts/strip/s
- Energy Range: 5 – 30 keV
- Dynamic range: 20 bits
- Trim DAC: 8 bits
- Energy resolution: < 25% (@8keV)
- Control board based on FPGA and a micro controller with ethernet link
- Dimensions: 93(H)×63(W)×151(L) mm^3

Replacing a conventional scintillation counter with D/teX Ultra on an in-house X-ray diffraction (XRD) system, one can reduce the data acquisition time by 1/100, or improve the sensitivity 100 times when the same data acquisition time is applied.

In practice, using D/teX Ultra, one can measure a specimen within a minute, or is able to measure a very weak diffraction peak easily.

Fluorescence suppression (Fe2O3)

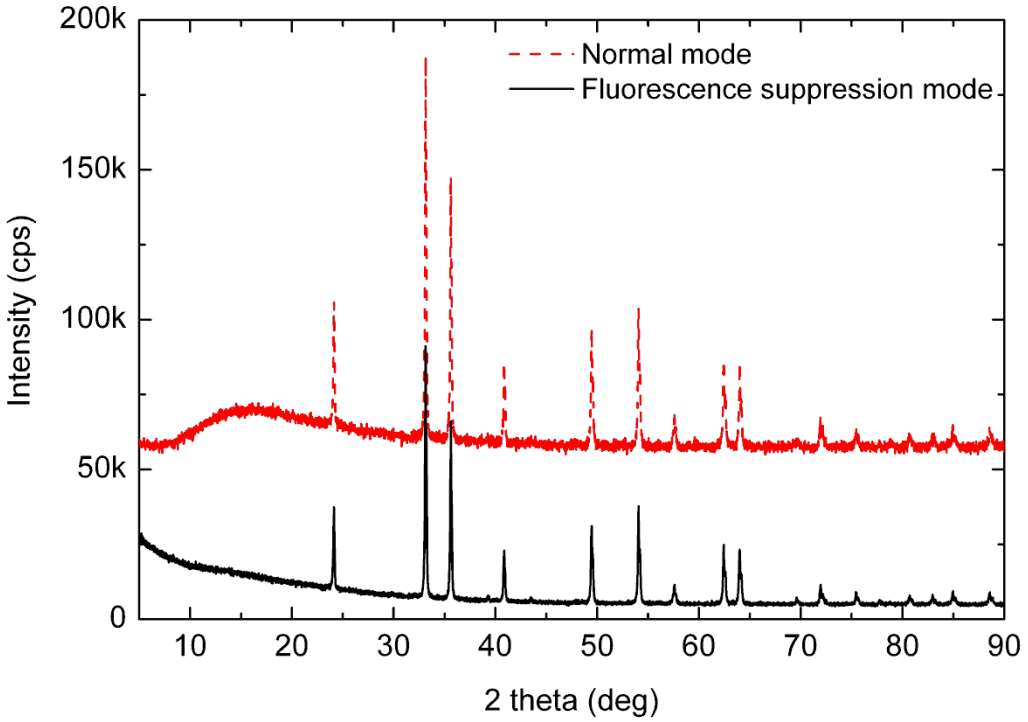
One of the fundamental problems the powder diffraction suffers from, is a fluorescence background from a sample. If the sample contains metals such as Fe, Mn, Ti or Cr, the fluorescence X-ray is induced and contributes as a noise to the diffraction pattern.

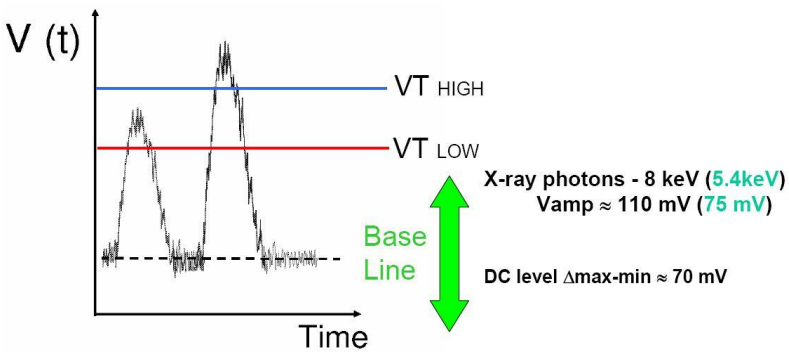
Solutions:

1) Si(Li) or pure Ge (cooled using liquid nitrogen & relatively slow < 100 kcps)

2) Use crystal monochromator - useful signals goes down to 30%

3) D/teX ultra: backgroud is reduced by 10x, while the diffraction signals remains at 80%



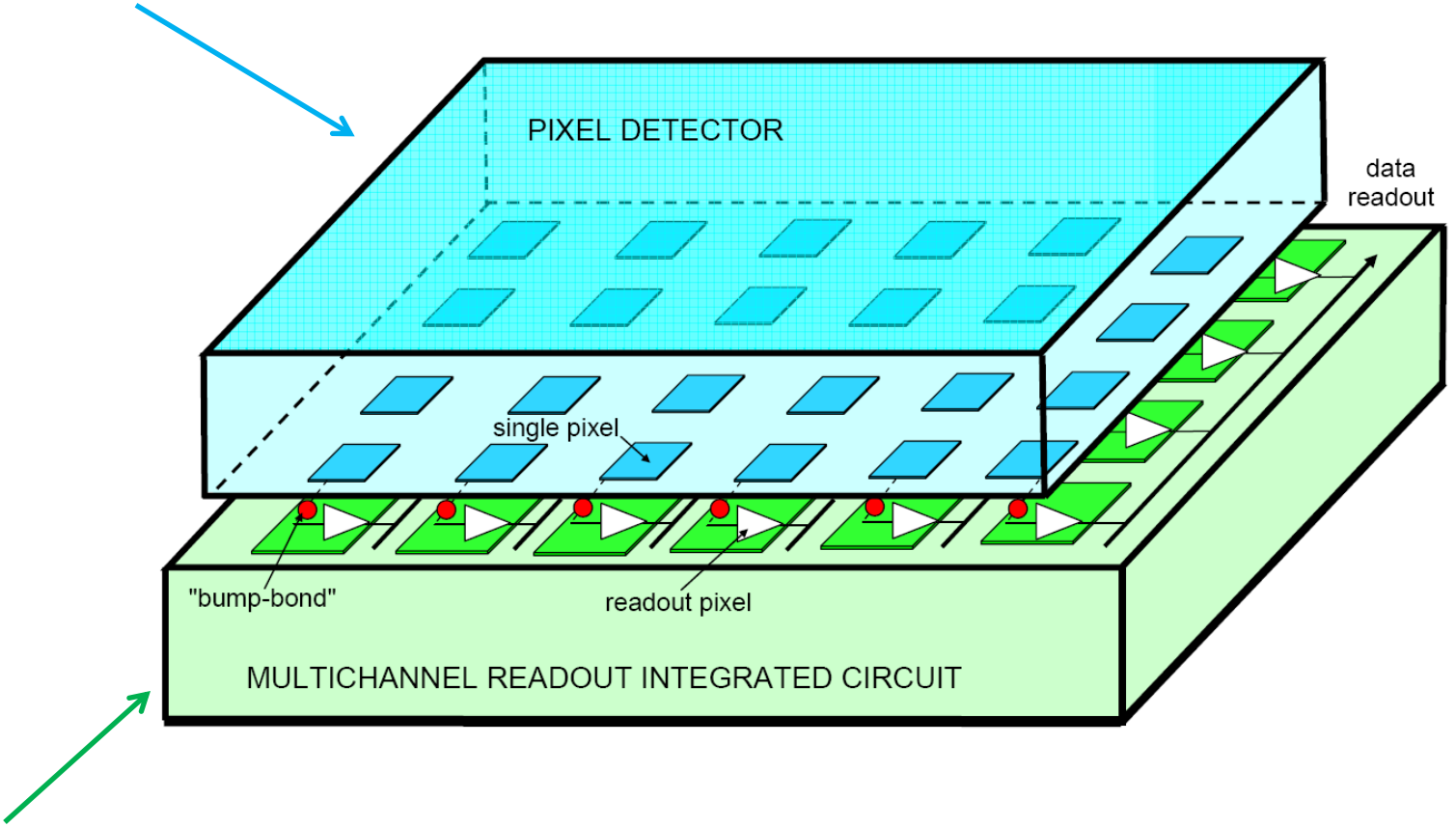


Energy window:
7 keV-9 keV

2D imaging

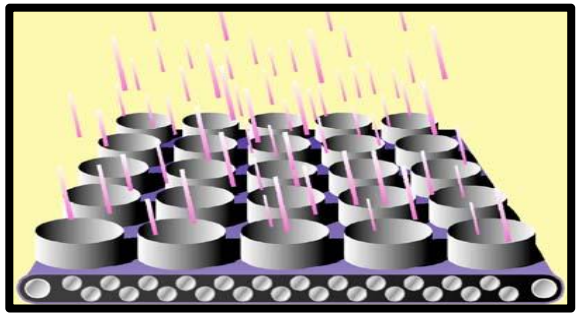
Hybrid pixel detector

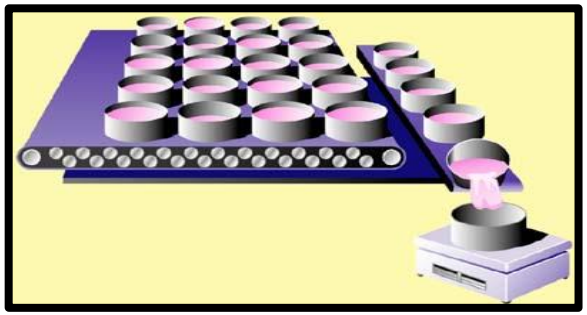
Detector material suitable for given application and X-ray energy range

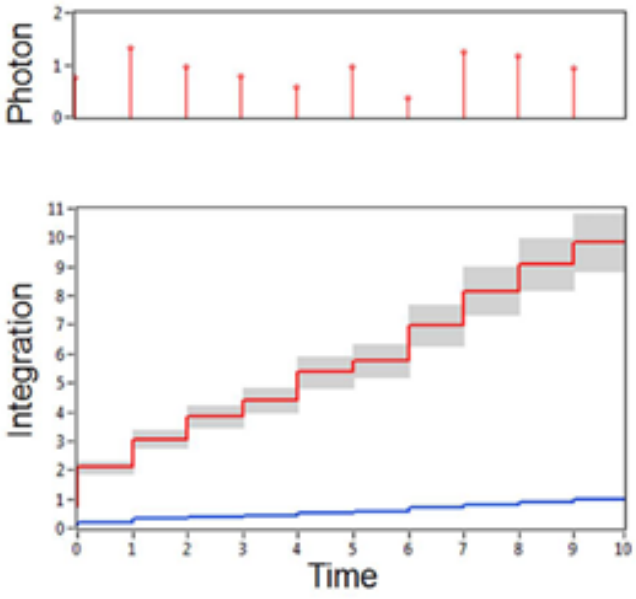


VLSI technology siutable for analog and digital block for readout electronics

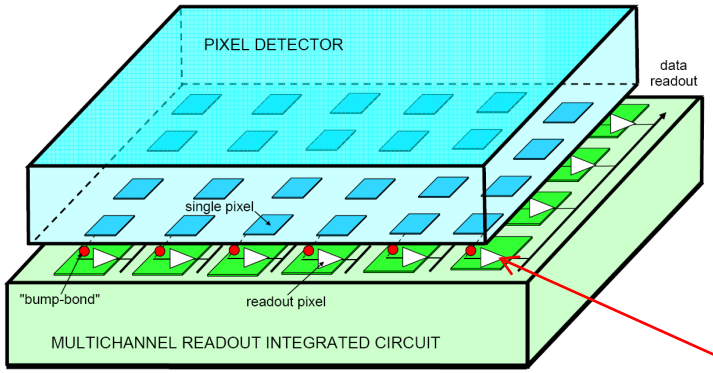
Integration type detector

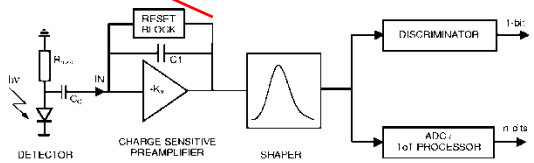


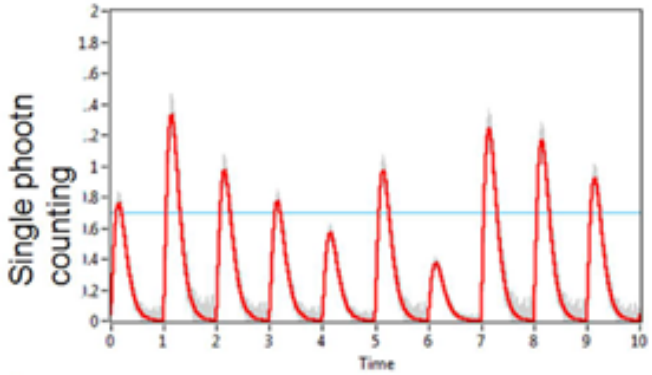


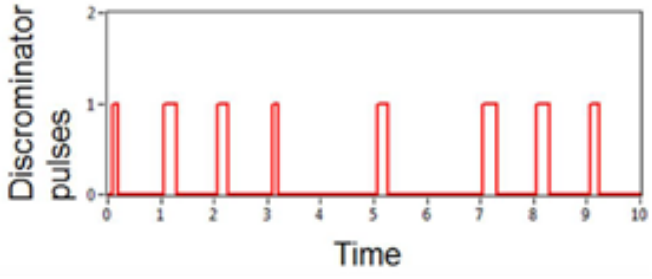


Single Photon Counting









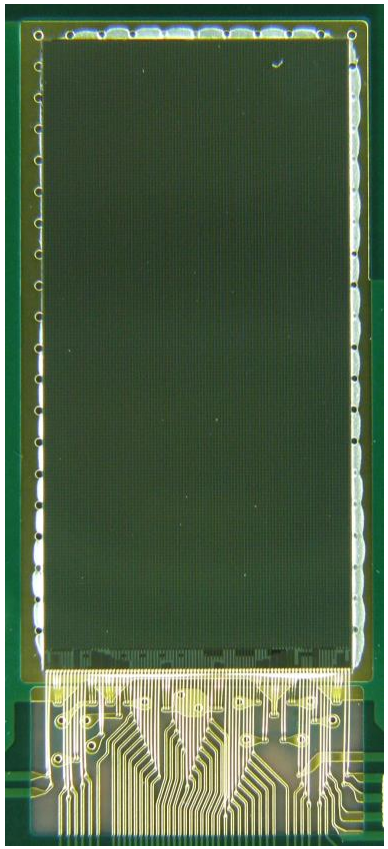
Trends:

1. Small pixel area
2. High count rate
3. Energy measurements
4. Large area detector
5. Continous readout

Large area chips for commercial applications

PXD18k – summarized performance

PXD18k chip



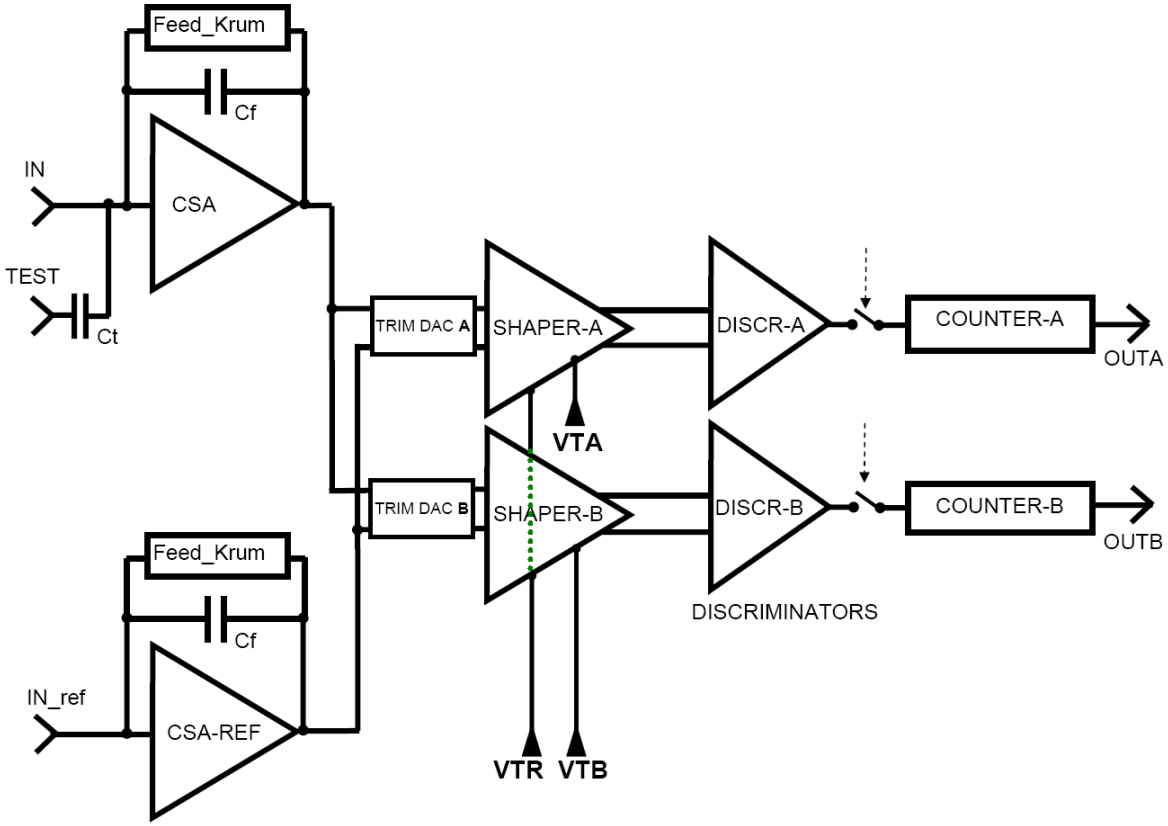
Summarized performance of the PXD18k IC.

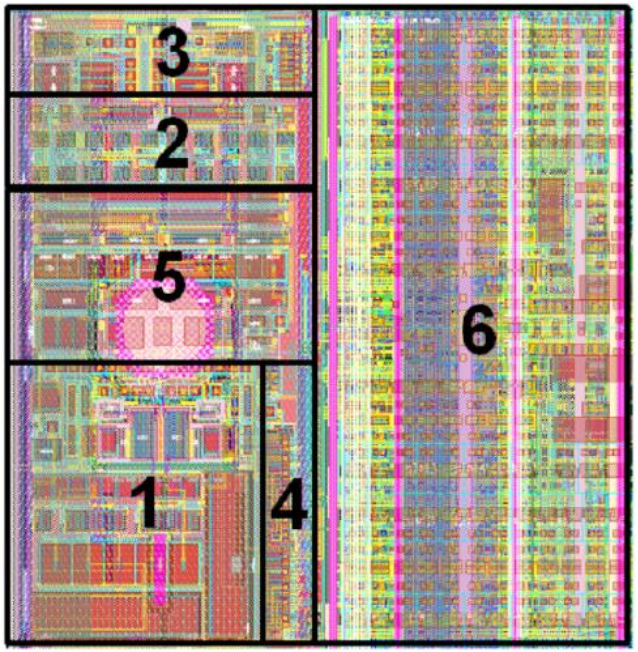
Parameter	
Technology	CMOS 180 nm
Die size	9.64 mm × 20 mm
Pixel dimensions	100 µm × 100 µm
Number of pixels	18,432
Supply voltage: core/LVDS	1.2 V/1.8 V
Power dissipation per pixel (analog)	23 µW
Peaking time	30 ns
ENC with bump-bonded detector	168 e^- rms
Gain	42.5 µV/e^-
Offset spread (after correction with 7-bit)	< 1.8 mV rms
Dead time (paralyzable model)	172 ns
Number of discriminators per channel	2
Counters capacity	2 × 16-bit
Readout dead time—standard mode (eight outputs, 2 × 16 bits/pixel) and continuous mode	740 µs and 0
Frame rate in continuous mode (16 bit/4 bit)	2.7 kHz/7.1 kHz
Communication	LVDS standard with 100 MHz clock

192 x 96 = 18.432 pixels (100x100 µm²)
CMOS 180 nm, chip size 9.64x20 mm²

P. Maj, P. Grybos, R. Szczygiel, M. Zoladz, T. Sakumura, Y. Tsuji "18k Channels single photon counting readout circuit for hybrid pixel detector", NIM A, vol. 697, 2013, pp. 32-39.

PXD18k – single pixel architecture

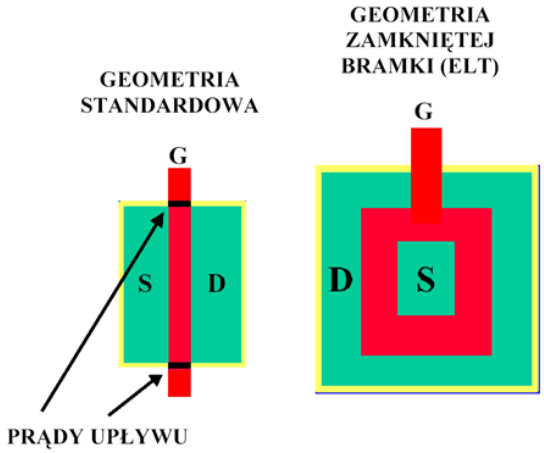




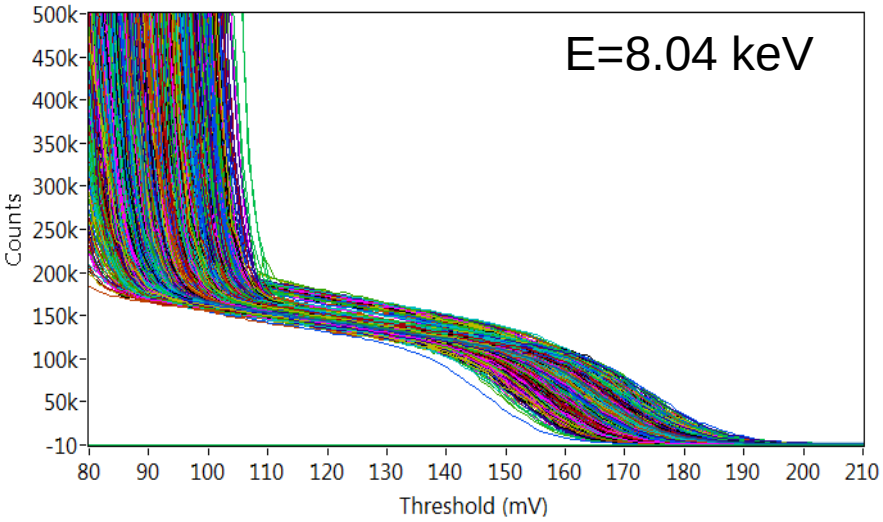
Blocks in single pixel (MET4-MET6 are removed):

1 - CSA & CSAREF,
2 - shapers,
3 - discriminators,
4 - trim DACs & test injection,
5 - reference blocks,
6 - counters and registers

Noise and gain:
calculated using X-ray source

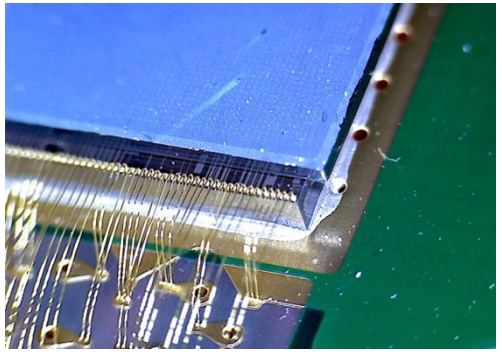


Threshold scan of **18.432 pixels**



$$f(x) = \frac{a}{2}\left(1 - \mathrm{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right)(bx + c)$$

a - average number of input pulses of given energy,
μ - threshold of the pixel for the given X-ray energy,
σ - related to the electronic noise and energy spectrum,
(*bx*+*c*) - linear term to model the charge sharing.



Gain:

Average: 42.5 μV/el.
Sigma: 5 μV/el.

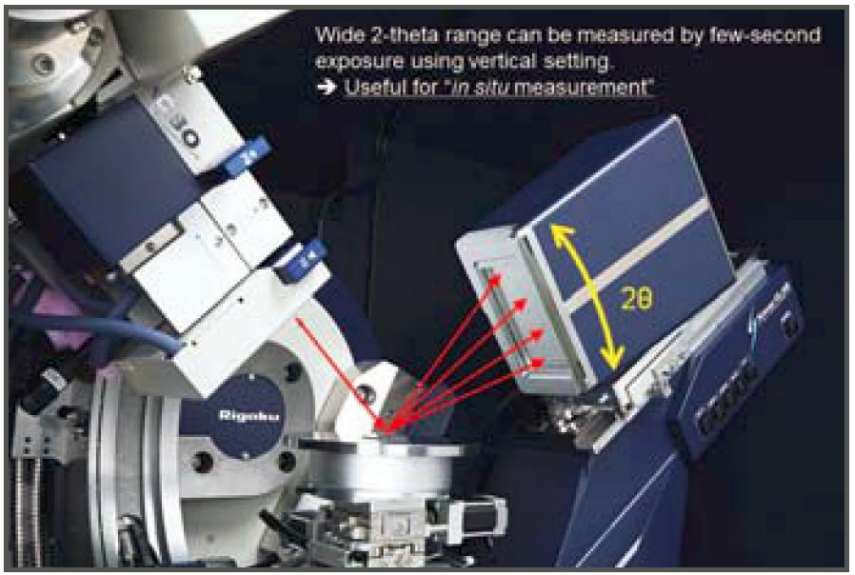
Noise:

Connected to the the detector:
Average: 168 el. rms
Sigma: 17 el. rms

PXD18k is used in HyPix3000 – Rigaku Corporation (www.rigaku.com)

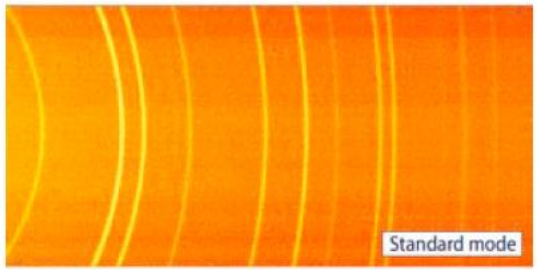
x 16

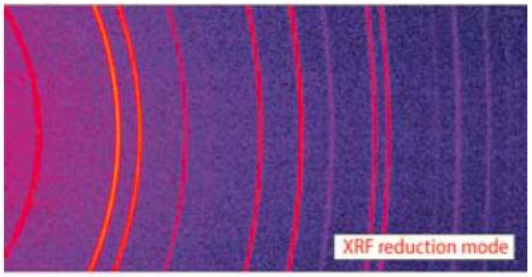
Specifications	
Sensors	Semiconductor pixel sensor
Active area	2984 mm^2 (77.5 × 38.5 mm)
Pixel size	100 × 100 µm
Number of pixels	775 × 385 = 298375 pixels
Threshold	2 ch
Counter mode	Differential/31-bit/zero dead time
Global count rate	>2.9 x 10^{11} cps (>1 × 10^6 cps/pixel)
Internal counter bit	Max.: 31-bit/pixel (Normal: 16-bit/pixel)
Efficiencies	Cr, Fe, Co, Cu: 99% Mo: 38%
Readout time	3.7 ms (0 ms for zero dead time mode)
Energy resolution	Better than 25% at Cu $K\alpha$
Dimensions	147(W) × 93(H) × 180(D) mm
Weight	Approximately 2 kg

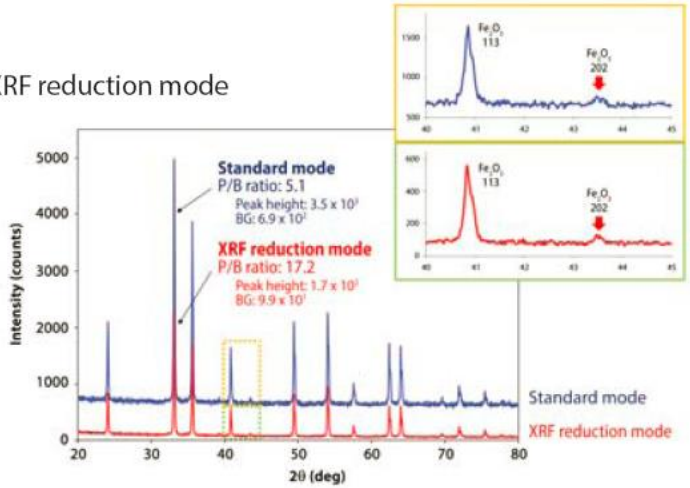


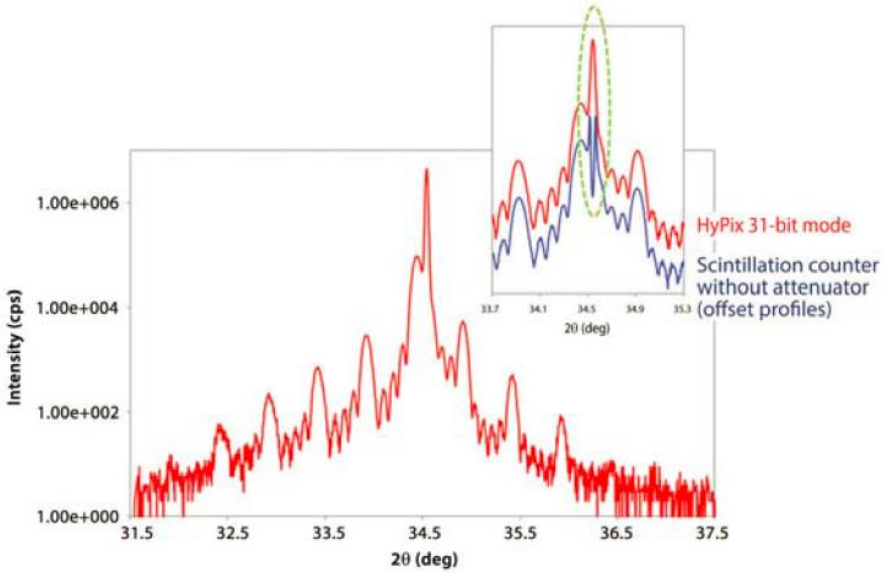
HyPix3000 – Rigaku Corporation

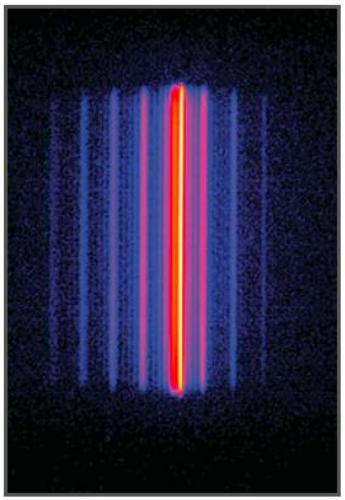
Figure 2. X-ray diffraction patterns of iron oxide powder, measured in standard mode and XRF reduction mode











Two-dimensional diffraction image of InGaN/GaN MQW

Figure 3. High resolution rocking curve profiles of InGaN/GaN MQW

www.rigaku.com

HyPix3000 – Rigaku Corporation

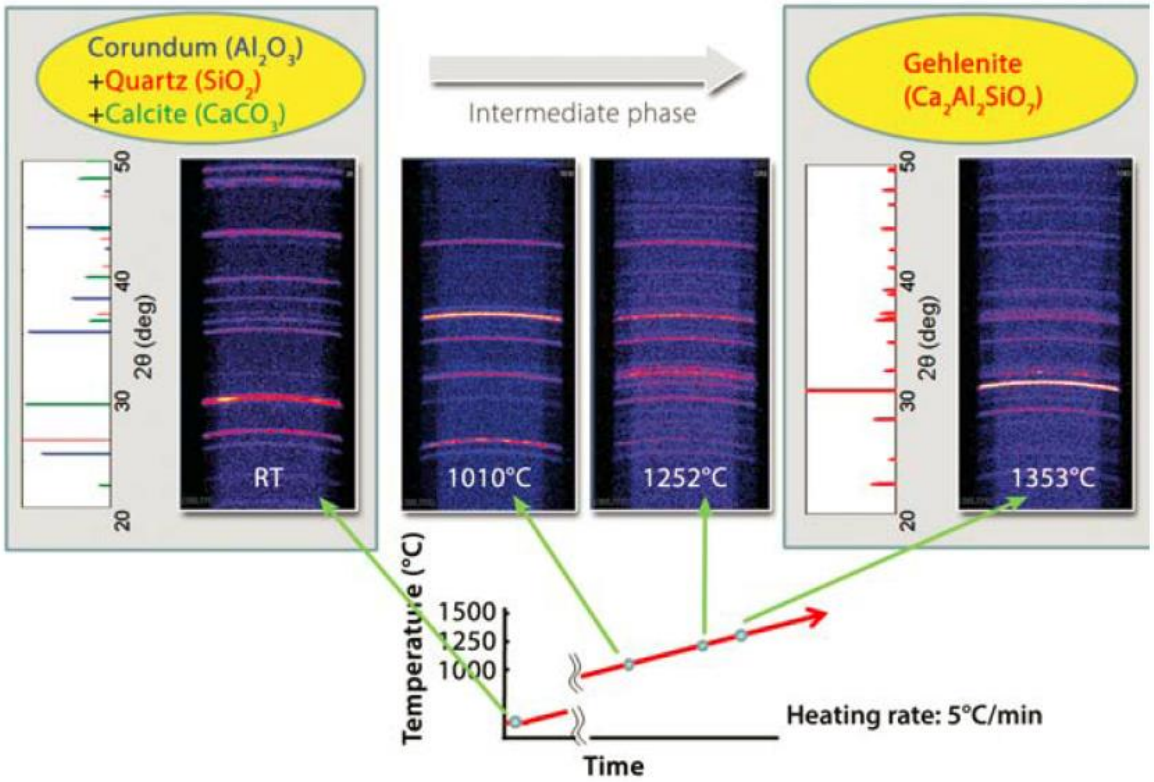
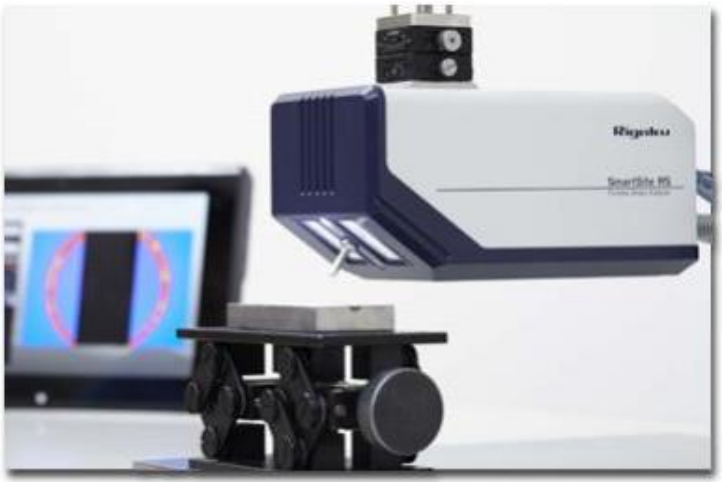


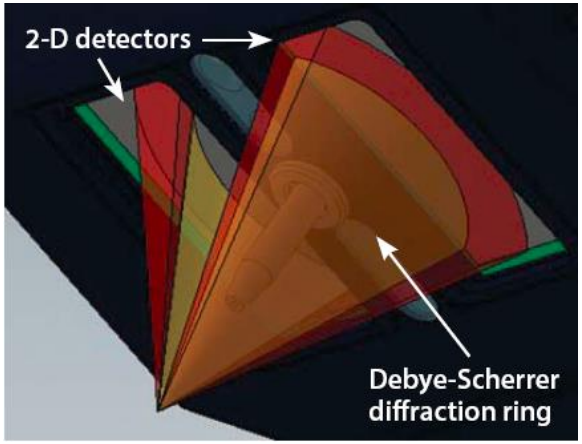
Figure 6. 2D *in situ* exposure measurement of ceramic

www.rigaku.com

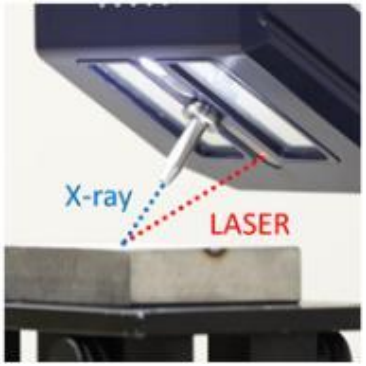
PXD18k is used in Portable Stress Analyzer – SmartSite RS (Rigaku Corp.)

The **SmartSite RS is the world's smallest portable stress analyzer** that is especially designed for field analysis. It enables to characterize residual stress of metal parts ranging from large construction projects to individual products, e.g. bridges, maritime vessels, aircraft, aerospace equipment, pipelines, heavy machinery and automobiles.

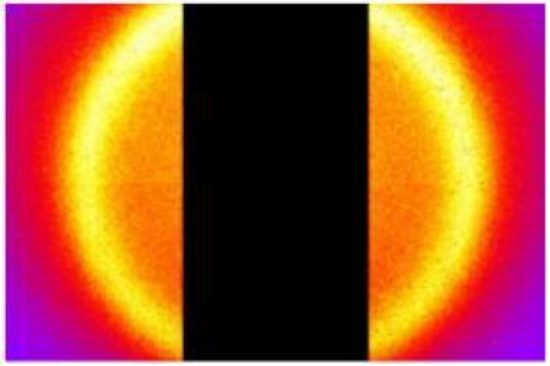




- Single exposure method
- High-speed 2-dimensional semiconductor detector
- 60 sec. (or less) for stress measurement



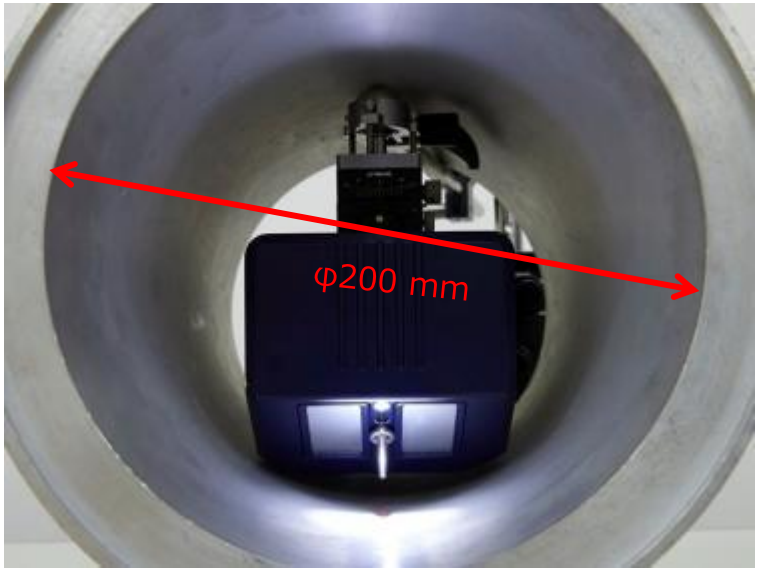
Arrangement of head unit and sample



α-Fe 211 Debye ring

www.rigaku.com

Portable stress analyzer – SmartSite RS (Rigaku Corporation)



The world's smallest measurement head has dimension of 114(W) x 248(D) x 111(H) mm and weights 3 kg. It enables to measure residual stress of inner surface of 200 mmφ bore.

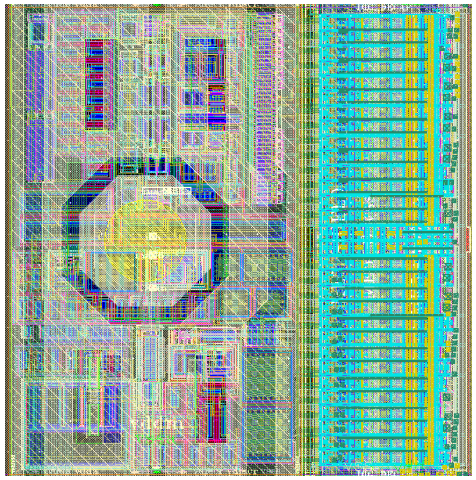
Applications

- Welded industrial products
- Aircraft & aerospace
- Marines
- Automobile

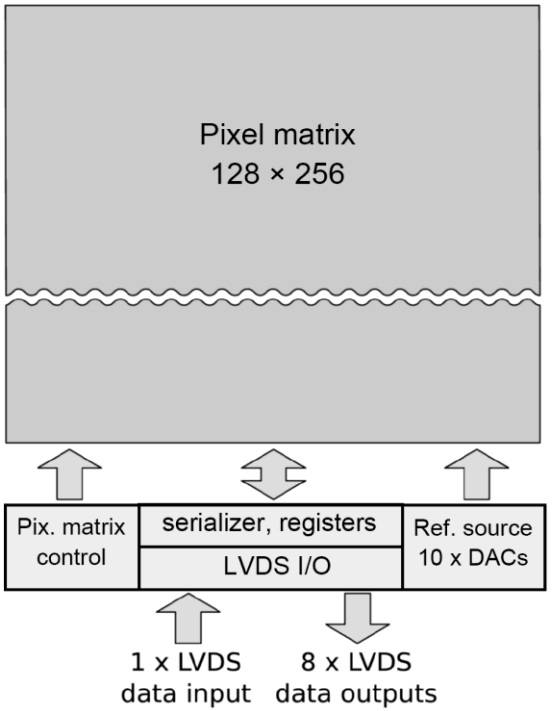
www.rigaku.com

Next step: UFXC chip: smaller pixel, lower noise, better correction

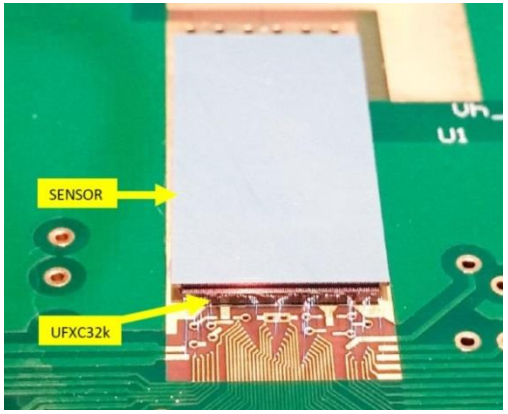
UFXC (TSMC130 nm)



75 x 75 μm²

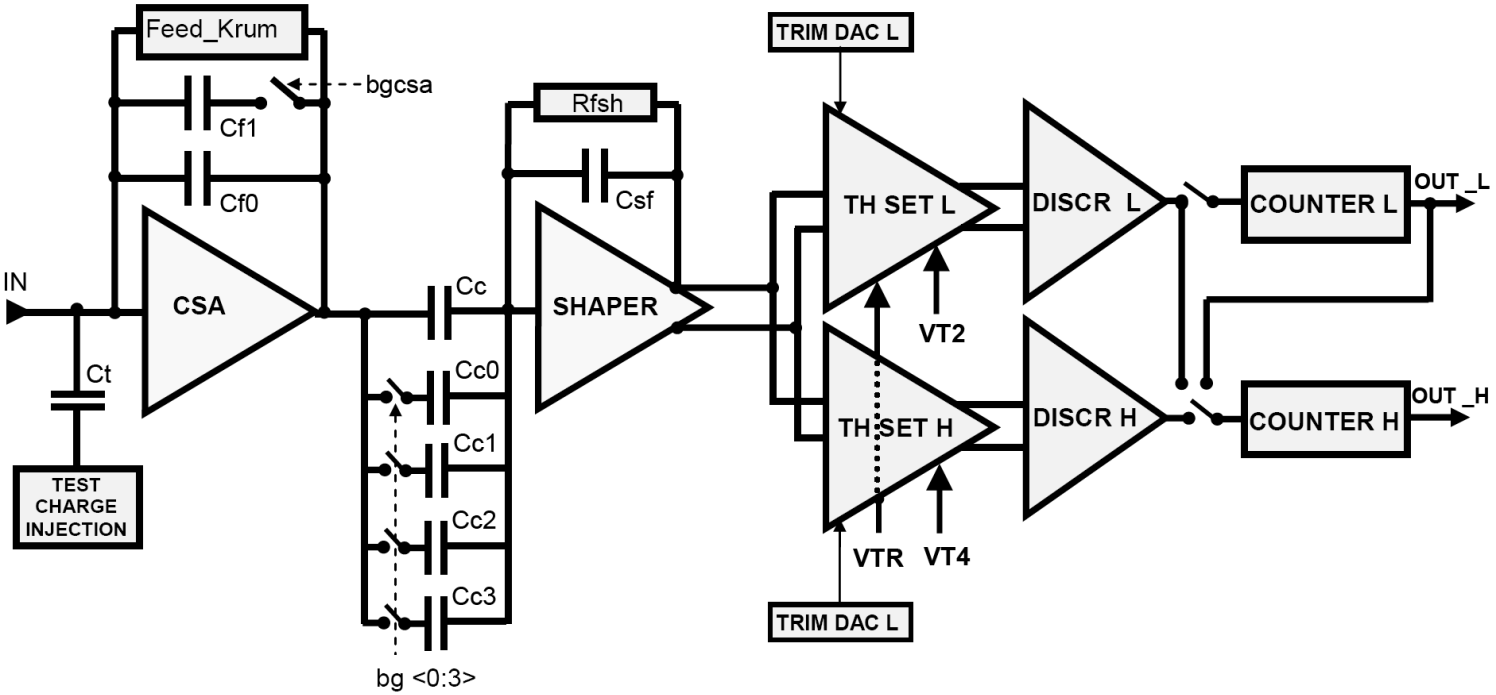


Supported by the National Center for Research and Development, Poland PBS1/A3/12/2012 in the years 2012-2015.

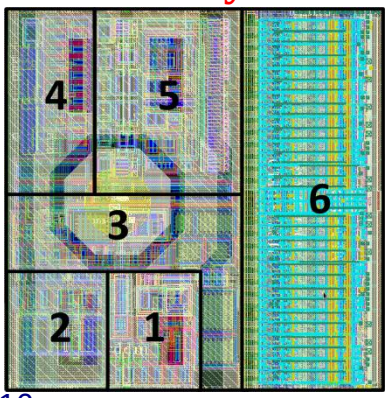


Single pixel architecture

Layout area: 75 × 75 μm²



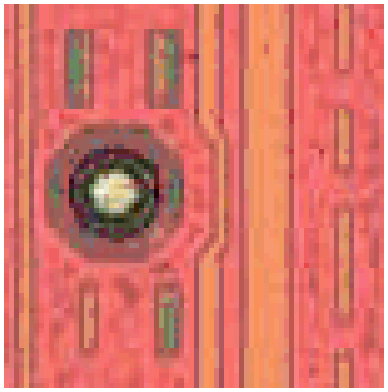
Pixel layout



1. CSA
2. Feed_Krum
3. SHAPER
4. Refences – bias currents
5. TH_SET, TRIM_DAC
6. Counters and registers

Bonding pad ϕ = 13 μm

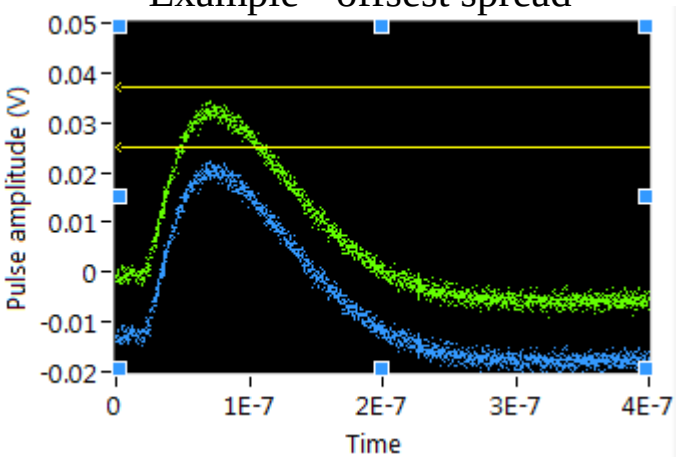
Pixel photo



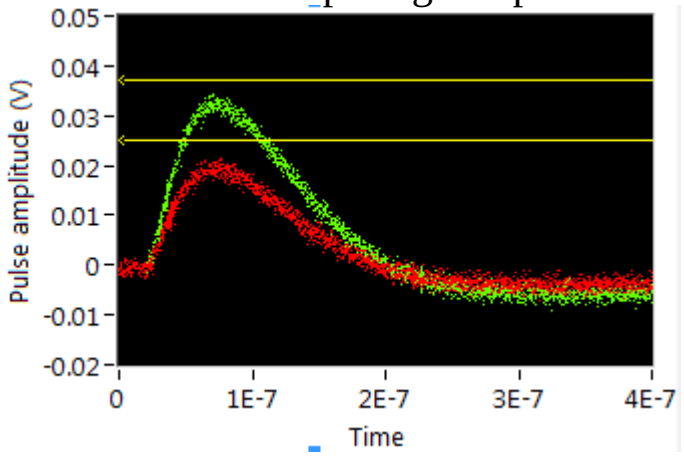
Single photon counting system

Offset usually corrected, gain should be corrected too

Example - offsest spread

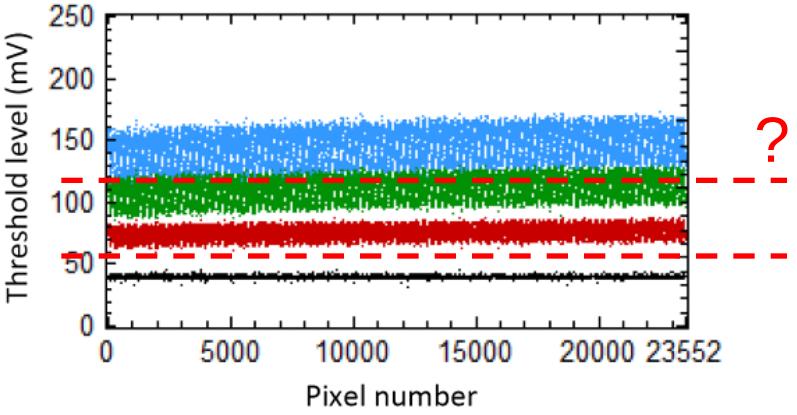


Example - gain spread

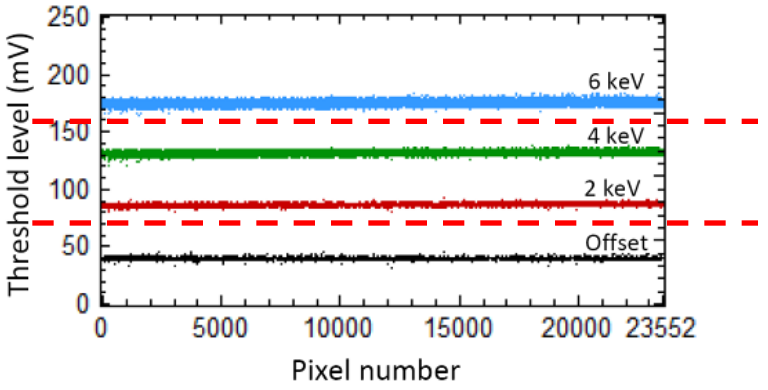


Solution:

use very precise offset trim



+ add gain trim



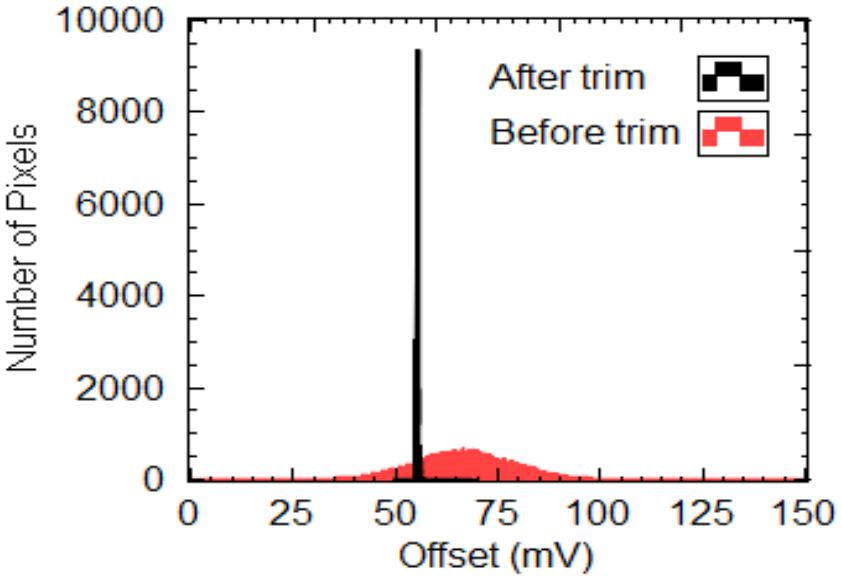
Offset and amplitudes of test pulses - prototype chip 128x184 pixels

More details see:

P. Kmon, P. Maj, P. Grybos, R. Szczygiel, "An Effective Multilevel Offset Correction Technique for Single Photon Counting Pixel Detectors" IEEE Transaction on Nuclear Science, vol.63, 2016, p. 1194-1201

DC offsets

before and after correction

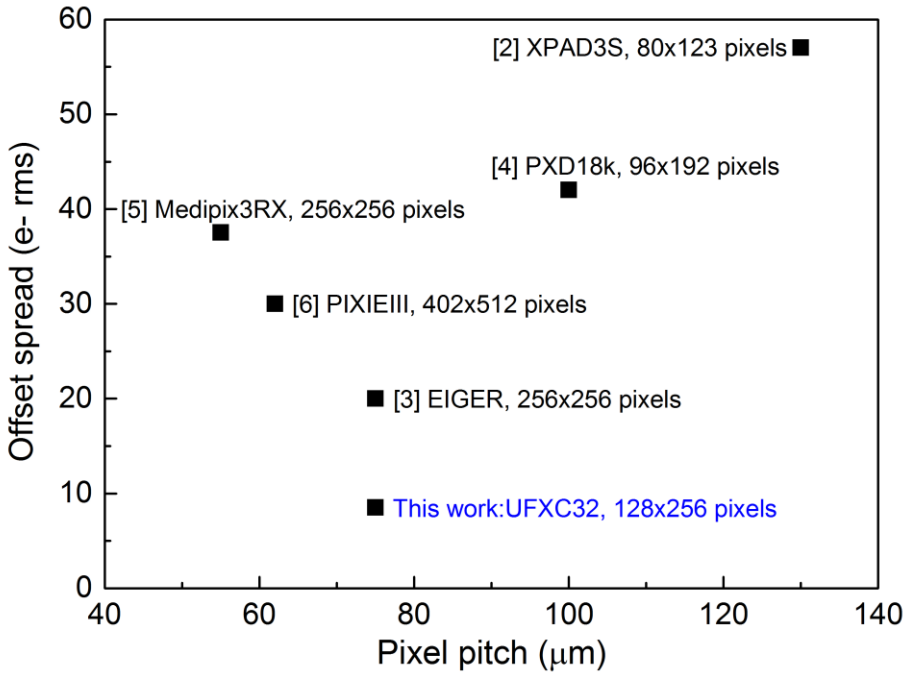


Before trim: sd = 12.1 mV

After trim: sd = 0.43 mV

nominal gain

After trim: sd = 8.5 e⁻ rms



Offsets spread in large area integrated circuits working in the single photon counting mode vs. pixel pitch – reference and pixel matrix size is speficied for each solution.

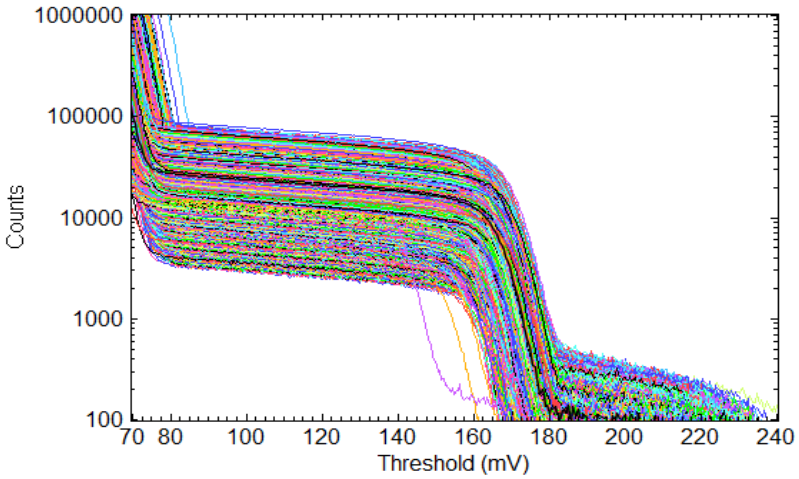
Comments:
correction time: 20 - 60 sec

Measurements with X-ray source (8.4 keV) – final UFXC32k chip

to calculate gain and noise

Integral spectra of 32761 pixels

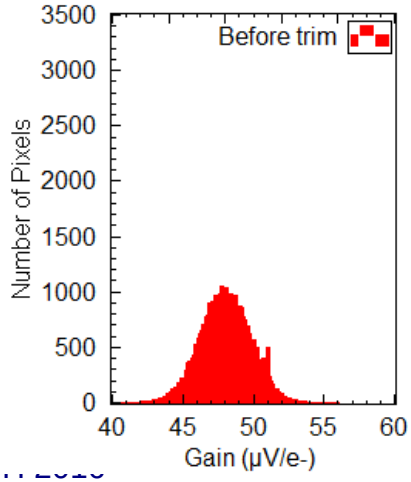
(only 7 pixels are missing due to errors in bump-bonding)

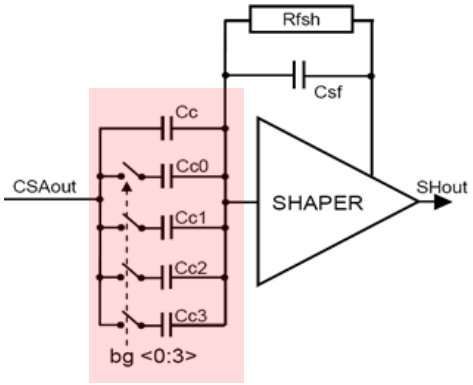


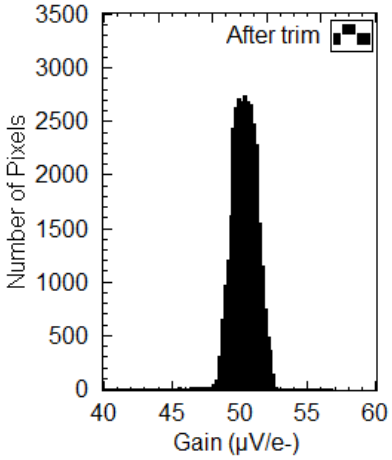
$$f(x) = \frac{a}{2}\left(1 - \mathrm{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right)(bx + c)$$

a - average number of input pulses of given energy,
μ - threshold of the pixel for the given X-ray energy,
σ - related to the electronic noise and energy spectrum
(*bx*+*c*) - linear term to model the charge sharing.

Gain histograms



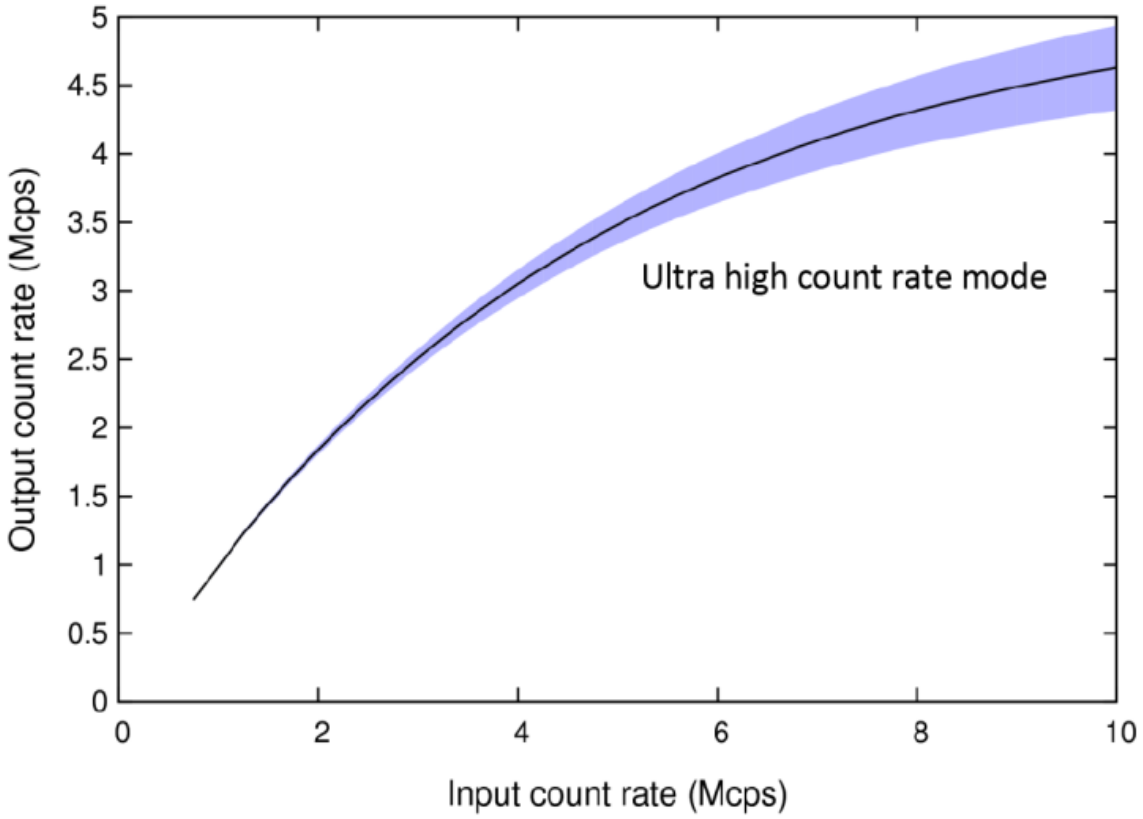




mean = 50.3 μV/e⁻
sd/mean = 1.9%

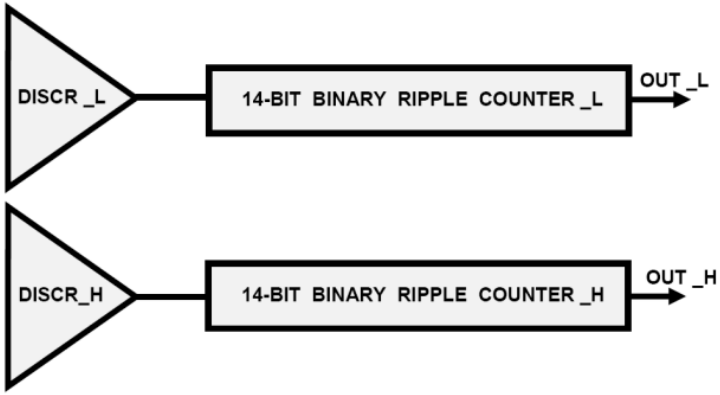
Single photon counting system

High count rate per pixel

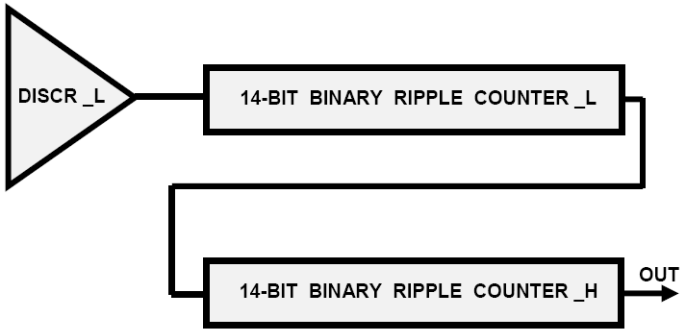


The shortest dead time of 67 ns, reported in literature, was measured for PILATUS3 IC with pixel size of 172×172 μm^2 . In our case for UFXC32k the dead time as small as 85 ns can be obtained, however the pixel area is 5.2 times smaller (only 75×75 μm^2) than for PILATUS3 IC, so the count rate per detector area is significantly higher.

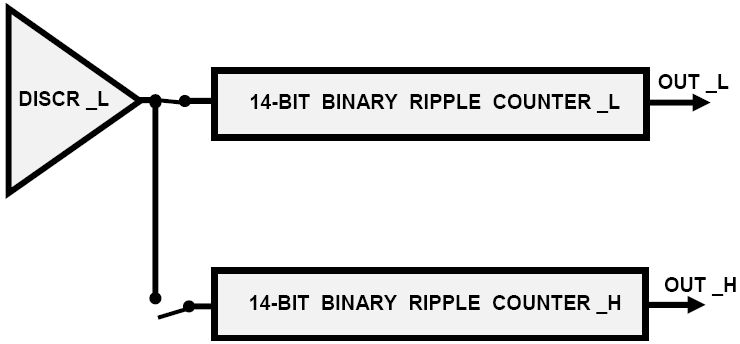
Two 14-bits counters in each pixel – 3 diffrent modes



STANDARD MODE
WITH ENERY WINDOW:
DISCR_L ⇒ COUNTER_L (14 bits)
DISCR_L ⇒ COUNTER_L (14 bits)



LONG COUNTER MODE
WITH SINGLE THRESOLD
DISCR_L ⇒
COUNTER_L + COUNTER_H (28- bits)

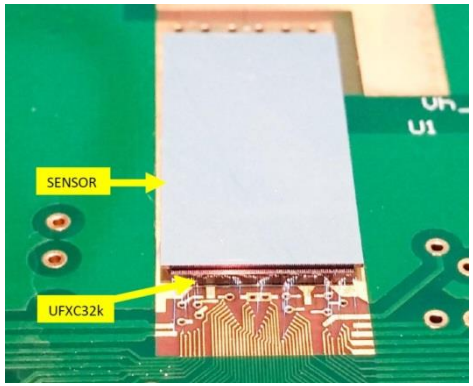


CONTINOUS MODE WITH SINGLE THRESOLD:
Phase 1 : DISCR_L ⇒ COUNTER_L (M-bits)
COUNTER_L (M-bits) ⇒ data readout

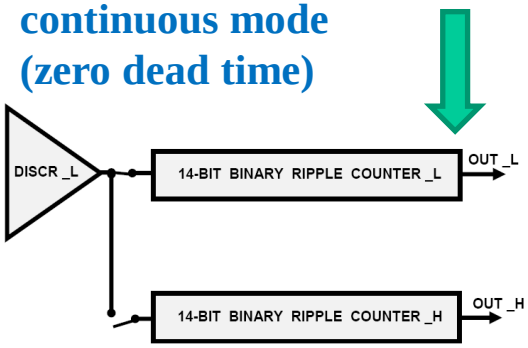
Phase 2: DISCR_H ⇒ COUNTER_H (M-bits),
COUNTER_L(M-bits) ⇒ data readout

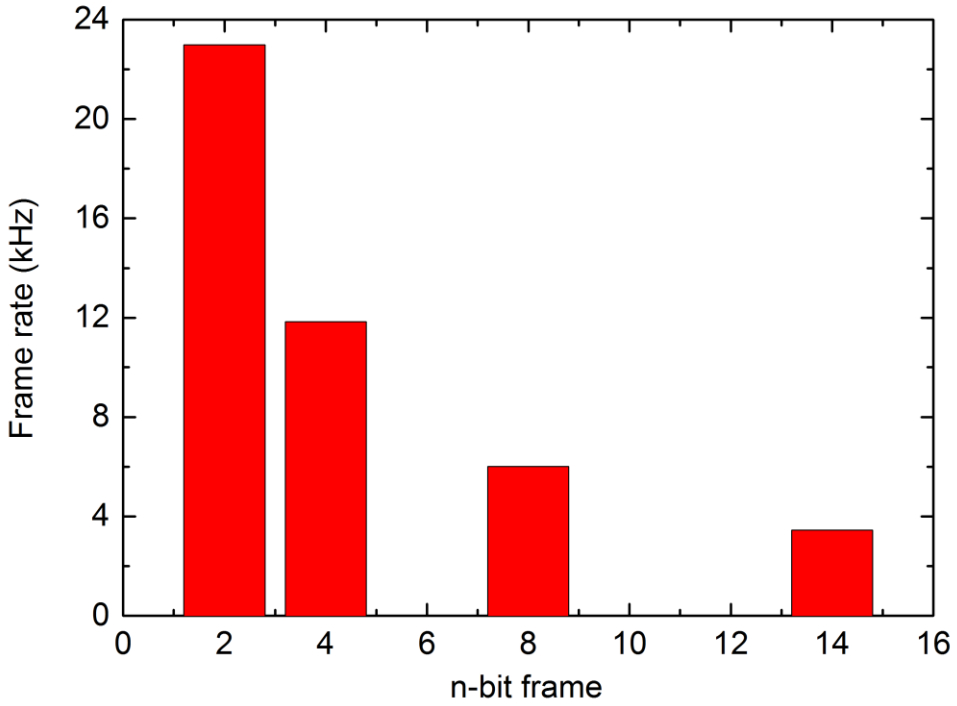
Number of readout bits M can be controlled
2-4-8-14 to increase the frame rate

Continuous mode of operation of UFXC32k



continuous mode (zero dead time)



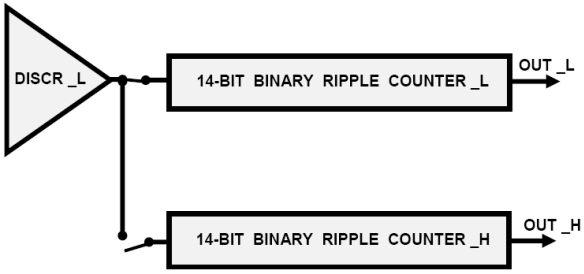


Phase 1 : DISCR_L ⇒ COUNTER_L (M-bits)
COUNTER_L (M-bits) ⇒ data readout
Phase 2: DISCR_H ⇒ COUNTER_H (M-bits),
COUNTER_L(M-bits) ⇒ data readout

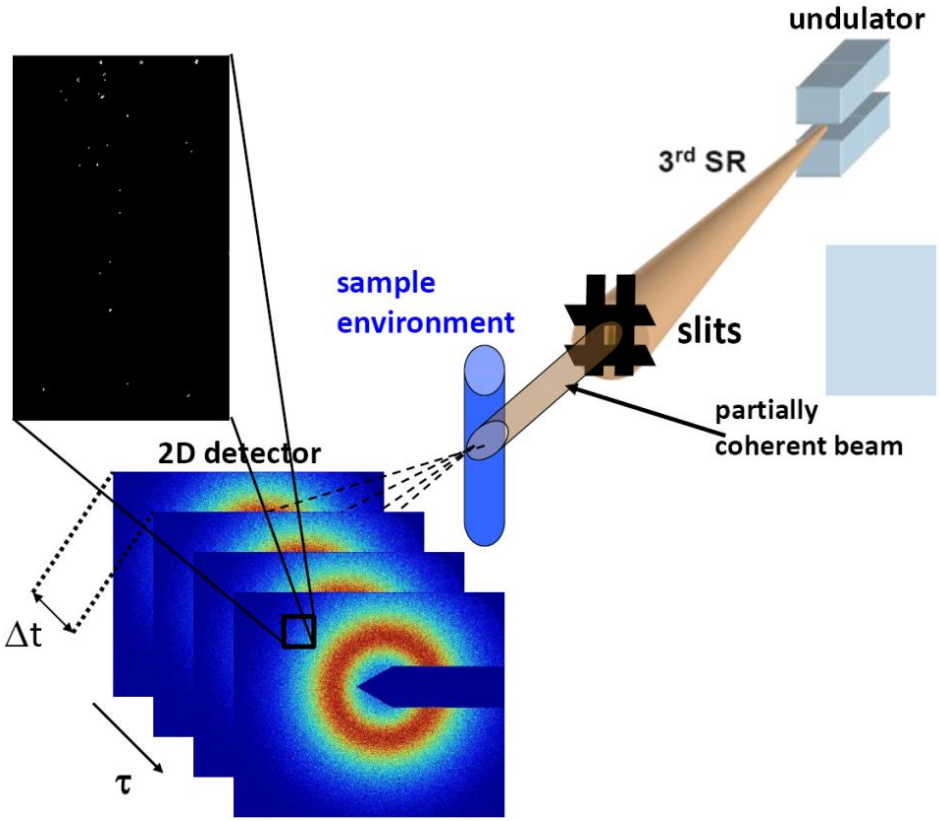
For reading out 2 bits/pixel with 200 MHz clock the frame rate is equal to 23 kHz. The performed tests have a significant limitation in the maximum clock frequency (Single Data Rate clock of 200 MHz) because of our test system based on NI PXI-6562 Digital Waveform Generator/Analyzer.

Tests for continuous mode of operation of UFXC32k
(X-ray Photon Correlation Spectroscopy at Advanced Photon Source in ANL)

Unique technique to probe the motion of nanoscale structures over a wide range of length (100 nm – 1 nm) and time scales (10^{-6} – 10^{3} seconds) in materials



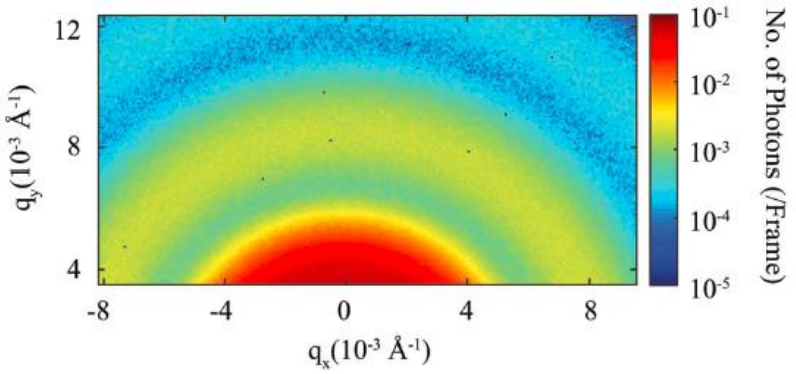
Phase 1 : DISCR_L ⇒ COUNTER_L (M-bits)
COUNTER_L (M-bits) ⇒ data readout
Phase 2: DISCR_H ⇒ COUNTER_H (M-bits),
COUNTER_L(M-bits) ⇒ data readout



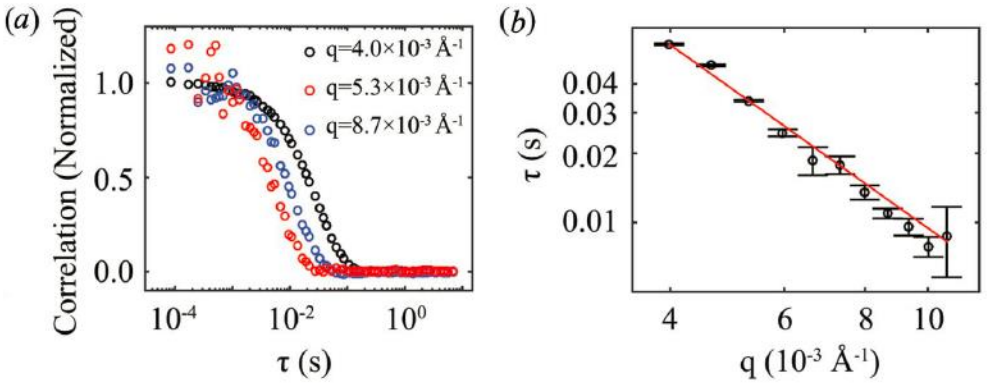
Thanks to : Alec R. Sandy, Suresh Narayanan, Eric Dufresne, Qingteng Zhang, ANL, US

Tests for UFXC32k usability for XPCS experiments at APS at ANL

The first test run: UFXC32k was set to operate in 2-bit readout mode at 100 MHz allowing to receive up to 180 000 images with 11.8 kfps (15 sec.)



(*a*) Time-averaged scattering from the latex nanoparticle suspension. The scattering intensity is indicated by the logarithmic color bar.



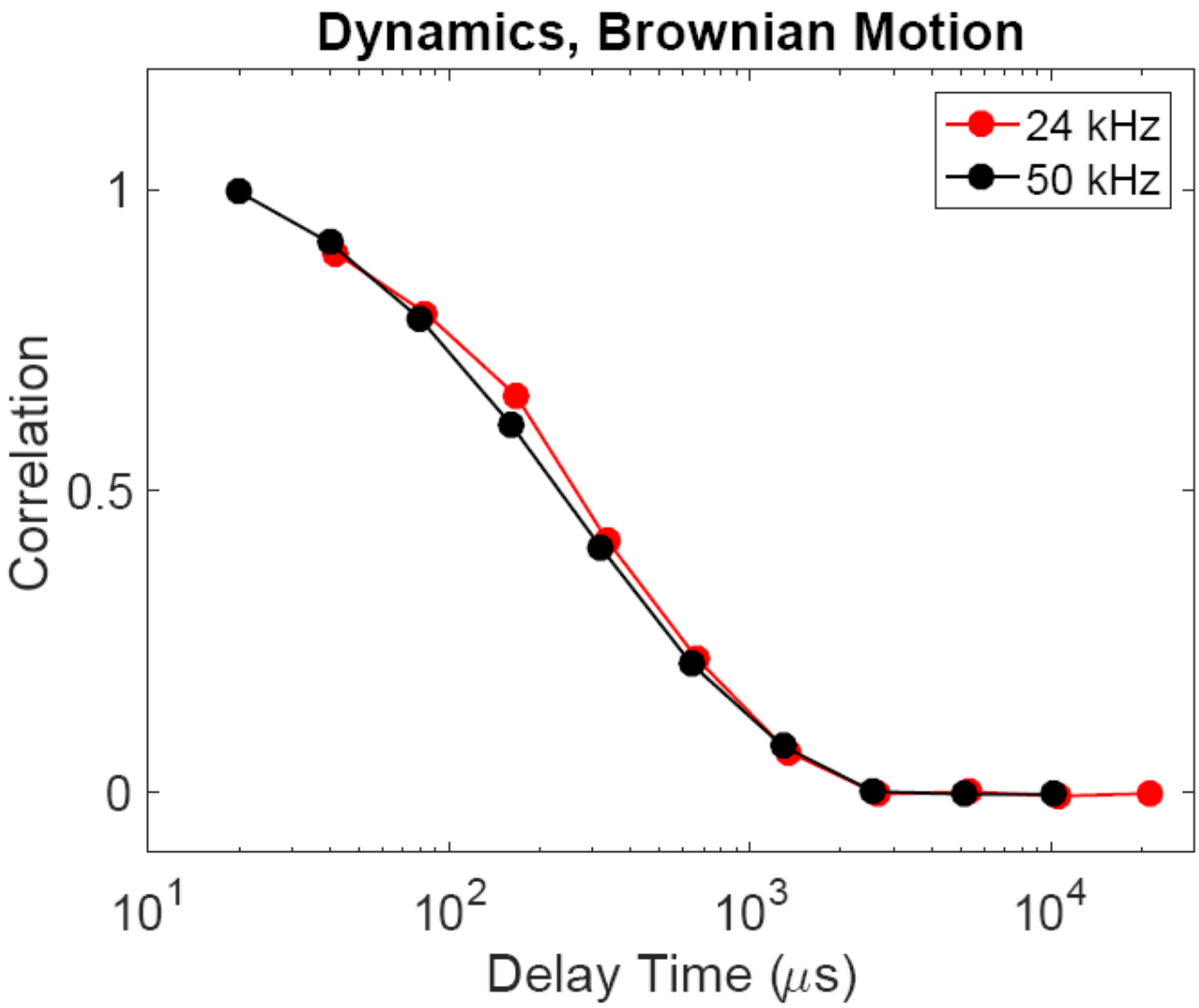
(*a*) Dynamics of latex nanoparticles indicated by $g_2(\tau)$ at different q. (*b*) Decorrelation time $\tau(q)$ *versus* q. The red line shows the inverse-square decay of the correlation time.

Ref. [24] Q. Zhang, et al, "Submillisecond X-ray photon correlation spectroscopy from a pixel array detector with fast dual gating and no readout dead-time", Journal of Synchrotron Radiation vol. 23, p. 679–684, 2016.

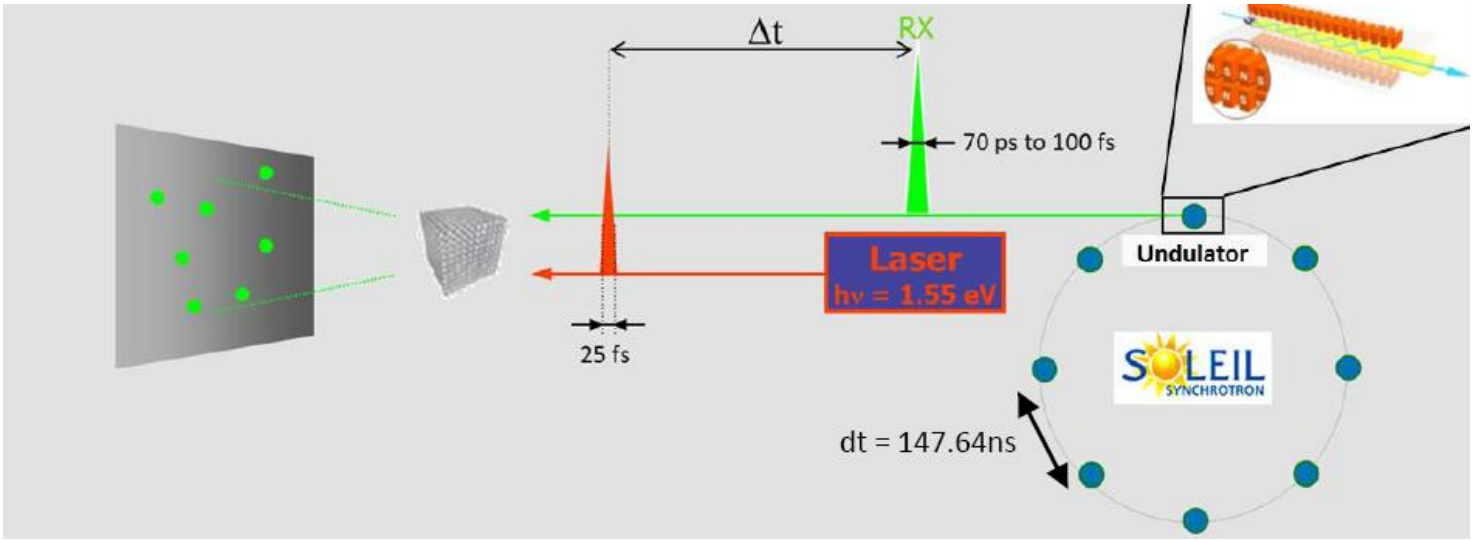
The second test run (June 2016): for reading out 2 bits/pixel with 425 MHz clock the **frame rate is equal to 50 kHz.**

The next test step will be: Double Date Rate Readout

Tests for UFXC32k usability for XPCS experiments at APS at ANL



Tests for pump-probe experiment in SOLEIL



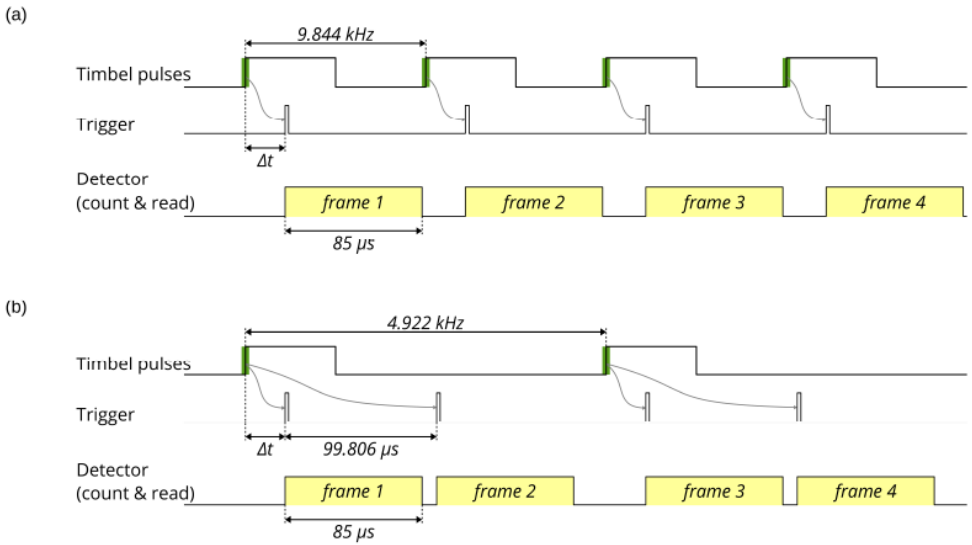


Figure 4. Two test scenarios prepared in order to evaluate UFXC32k detector performance for time-resolved studies: (a) scan of the storage ring filling mode and (b) acquisition of two images in the pump-probe-probe scheme.

Tests for pump-probe experiment in SOLEIL

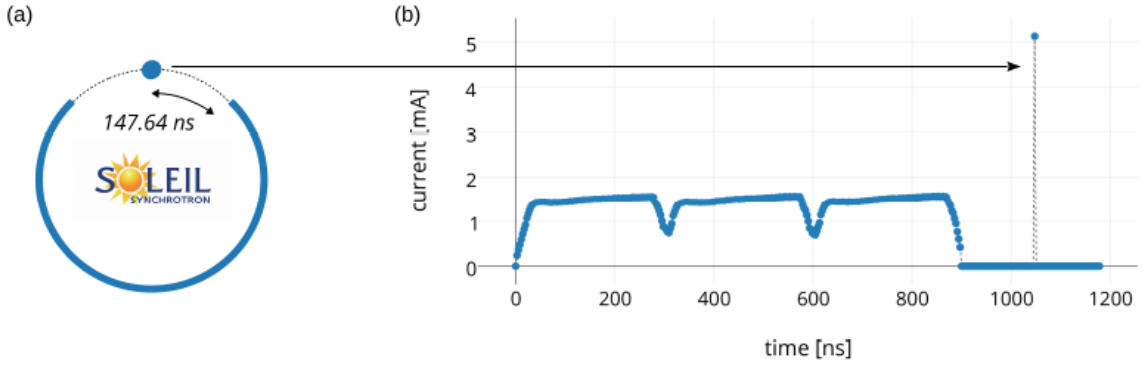


Figure 3. The hybrid filling mode at SOLEIL: (a) schematic view and (b) time-distribution of current per packet.

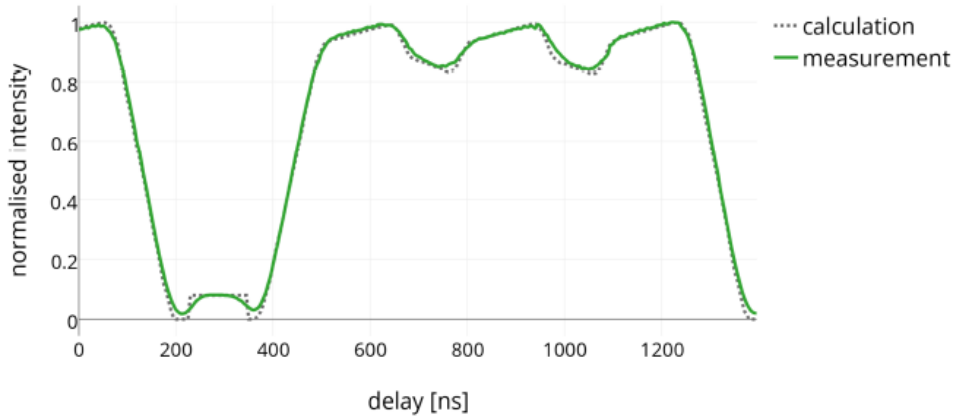
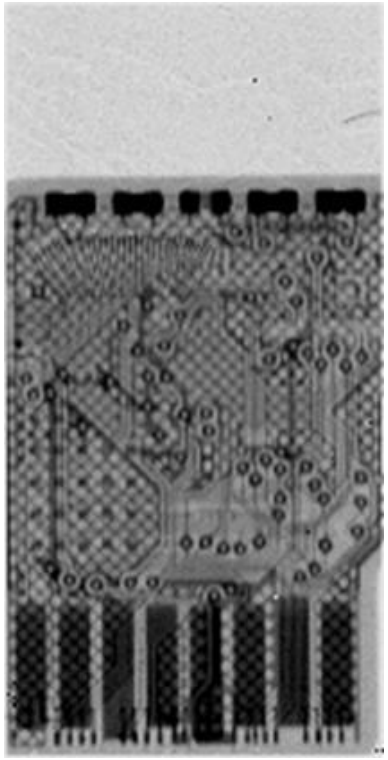


Figure 5. The hybrid filling mode of SOLEIL storage ring measured with the UFXC32k detector (green line) and calculated from the actual machine current values per packet (grey-dashed line). The measured scan was obtained by illuminating the detector with Ge fluorescence radiation (K_α = 9.9 keV), and registering a large number of frames of 120 ns with precisely controlled delay with respect to the storage ring clock.

UFCX32k – can collect holes or electrons

Examples of raw X-ray radiograms of micro SD card taken with X-rays of energy 17.4 keV and the UFXC32k chip bump-bonded to

a) CdTe detector (750 μm thick)



b) Si detector (320 μm thick).

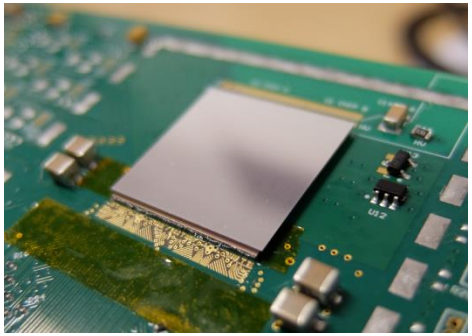
Next steps: 1) tests in Spring8 synchrotron in Japan, 2) possible medical application (computer tomography, mammography – **industrial partner is necessary**)

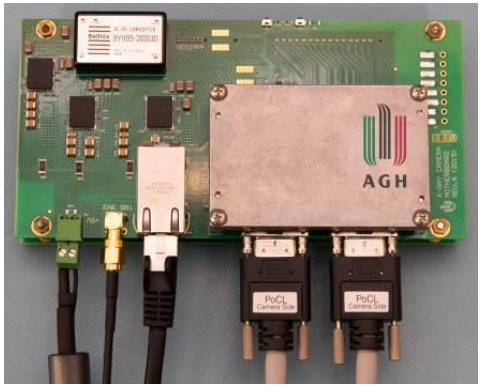
Multichip-module

(bump-bonding is completed)

2 - chip module

active area: 19.2 × 19.2 mm^2

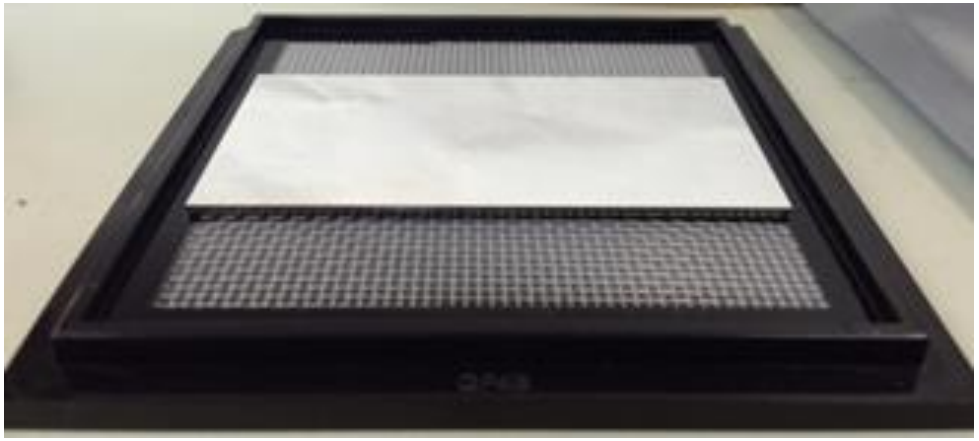




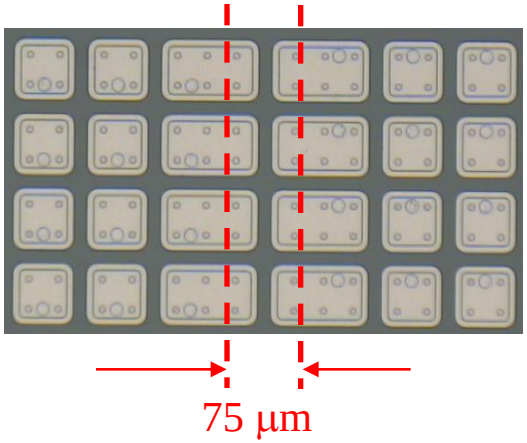
Backend based on NI System on Module and single software platform approach
Interfaces: Channel Link (full – 640MB/s), Ethernet, USB, dedicated triggering

16 - chip module

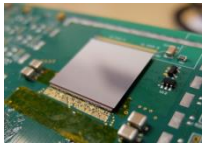
active area: 19.2 × 76.8 mm^2

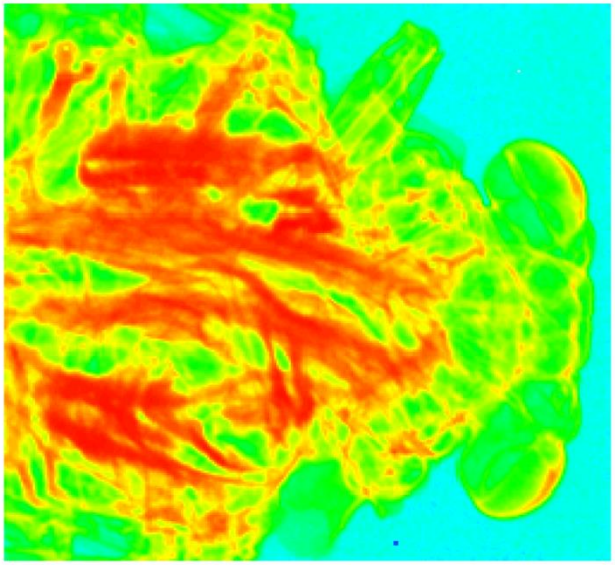


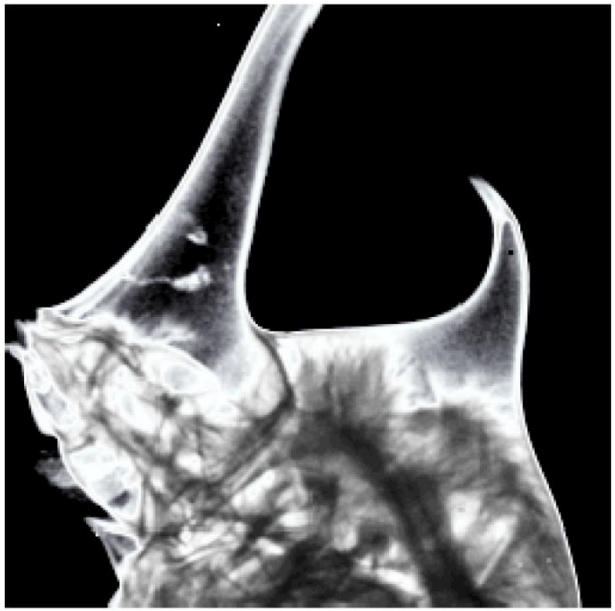
Space between the chips:
only 1 pixel (75 μm) – see detector photo below

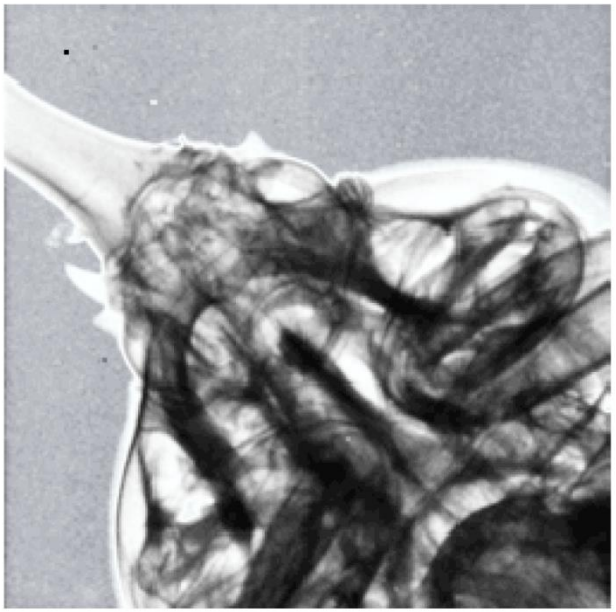


Some images with UFXC using 2-chip module
(rhinoceros beetle)



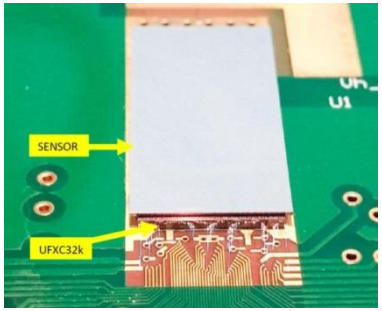


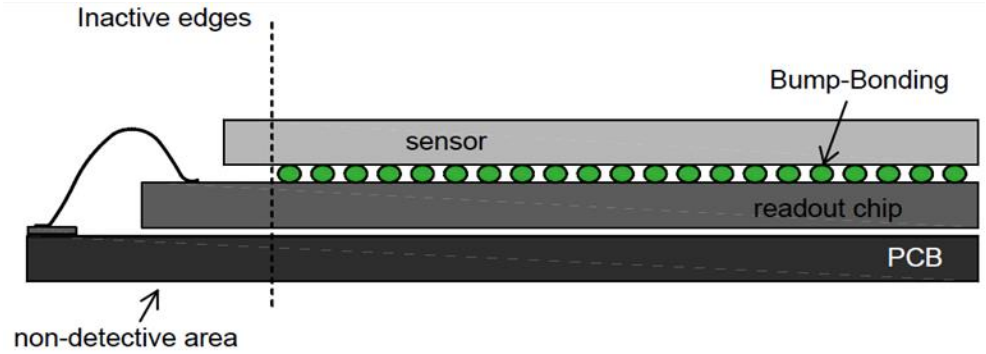


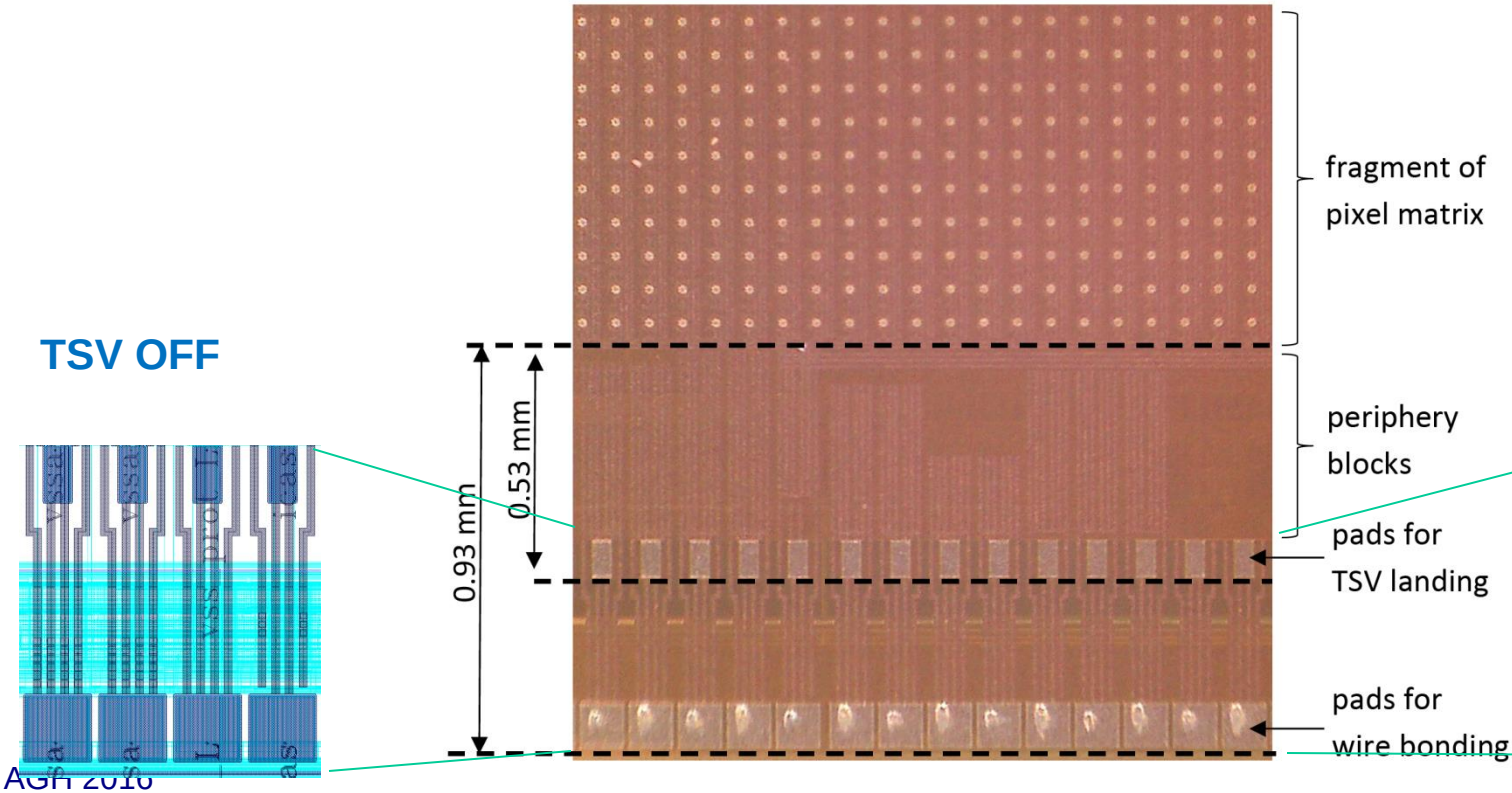


TSV option – two sets of wafers

Idea – to built large area module without dead zones

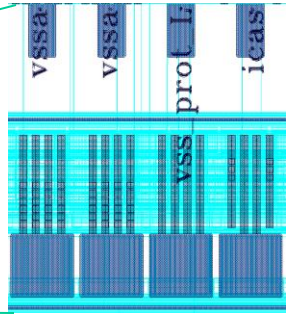






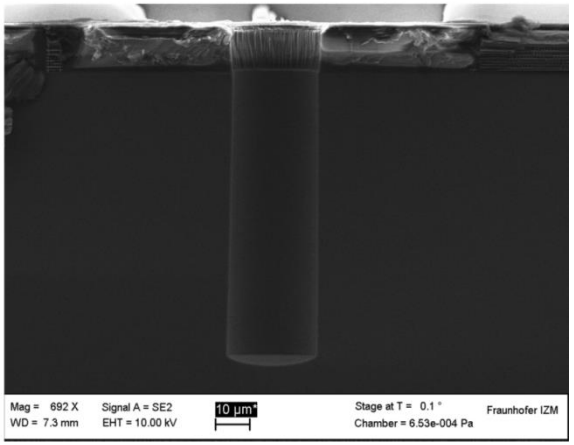
TSV OFF

TSV ON

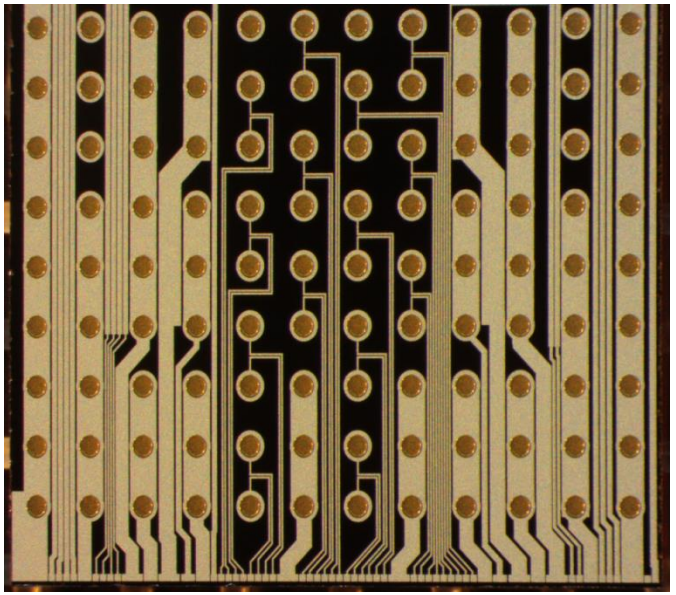


Progress in TSV processing

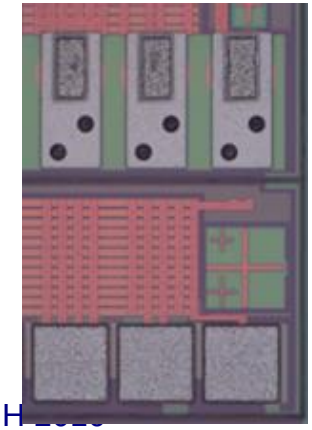
TSV cross-section

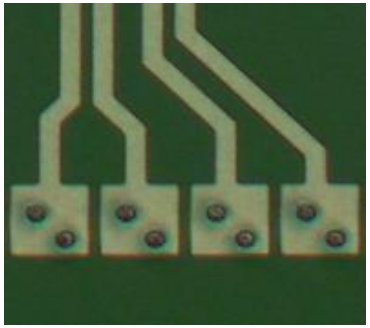


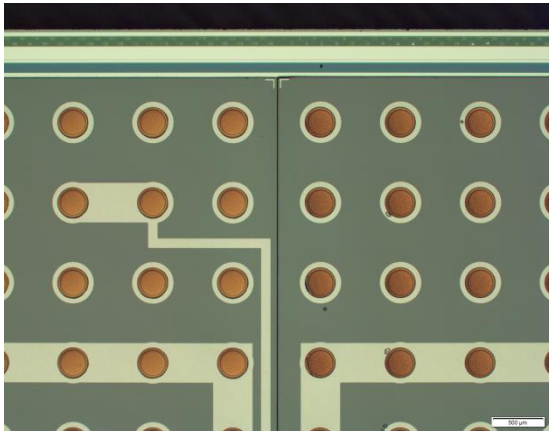
RDL - chip back-side



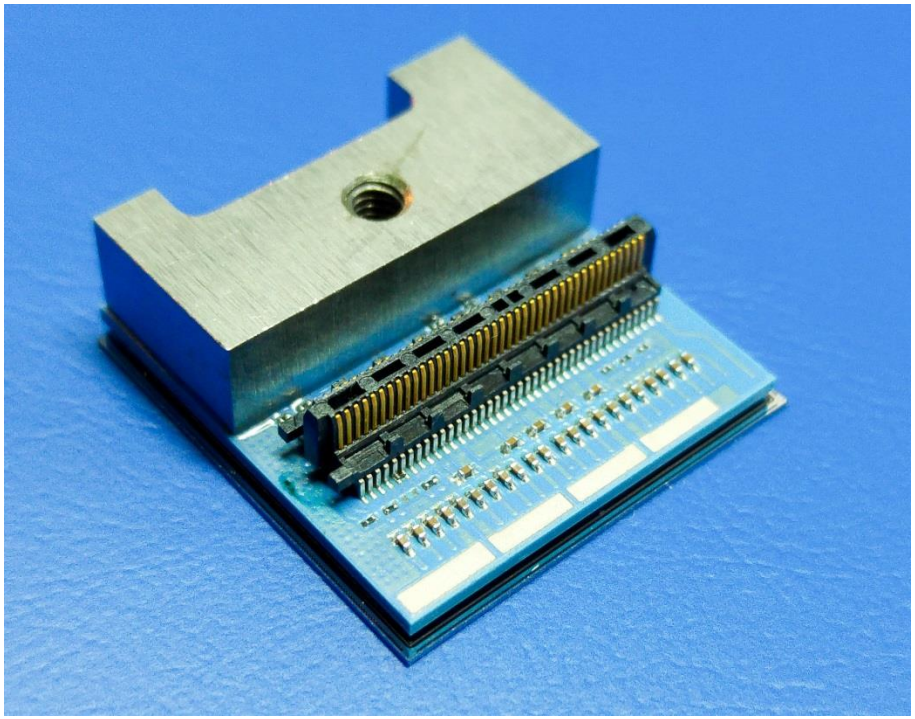
TSV – top and bottom view

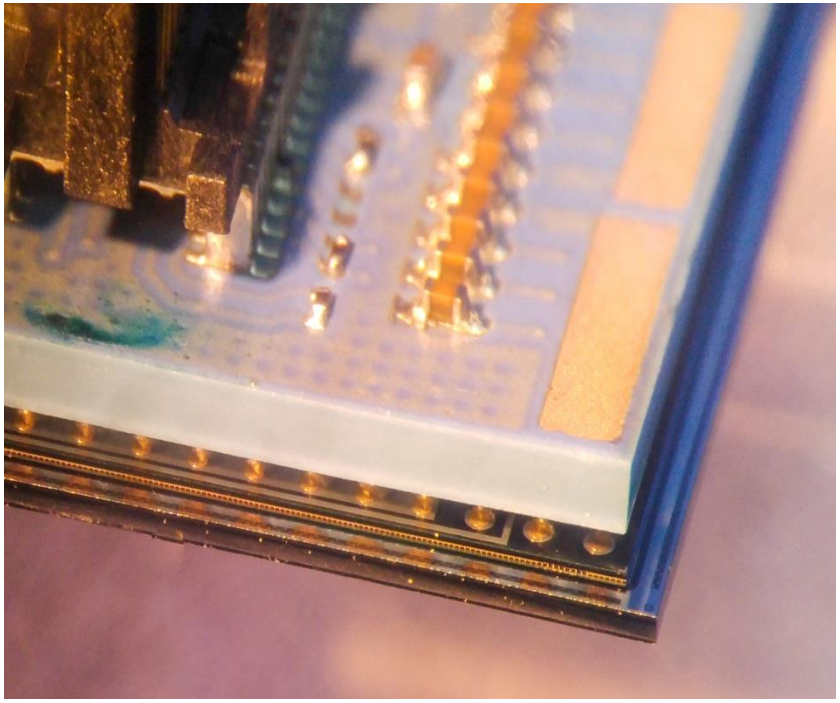






Progress in TSV processing





Modul with TSV.

Summary of UFX32k performance

comparison of counting pixel chips in submicron technology

COMPARISON OF COUNTING PIXEL CHIPS IN SUBMICRON TECHNOLOGY

Chip [ref]	Medipix 3RX [2, 19, 23]	PIXIE III [6]	PILATUS3 [20]	XPAD3S [3]	PXD18k [4]	Eiger [5]	UFXC32k this work
Process	130 nm	160 nm	250 nm	250 nm	180 nm	250 nm	130 nm
Chip area [mm^2]	15.9 ×14.1	25 ×32	10.5 ×17.5	10.4 ×17.4	9.6 ×20	19.3 ×20	9.6 ×20.1
Pixel matrix	256×256	402×512	60×97	80×120	96×192	256×256	128×256
Pixel size [µm^2]	55×55	62×62	172×172	130×130	100×100	75×75	75×75
Power/pix. [µW]	9	–	15*	40	23	–	26
Offset spread [e$^-$ rms rms]	37.5&	30	–	57	42	20–30	8.5
ENC [e$^-$ rms]	80	50	–	130	168	110 / 135 / 175	123 / 163 / 235
Dead time [ns]	400&	–	67	–	172	510 / 170 / 128	232 / 101 / 85
10% dead time loss input rate # [photons mm^{-2} s^{-1}]	0.87 × 10^8	–	0.53 × 10^8	–	0.61 × 10^8	1.46 × 10^8	2.20 × 10^8
Double threshold	Yes	Yes	No	No	Yes	No	Yes
Counters per pixel	2 ×12 bit	2 ×15 bit	1 × 20 bit	1 × 12 bit	2 ×16 bit	1 ×12 bit	2 ×14 bit
TSV option	Yes	No	No	No	No	No	Yes
Frame rate max [kHz] (readout bits)	–	0.5	0.5	0.5	7.1 (4-bits)	~23 (4-bits)	23 (2-bit)

*static PWR consumption.
&min. reported value – for details see [2, 19].
calculated using min. dead time and assuming $N_{OUT}/N_{IN} = 0.9$ – see formula (1).

P. Grybos, P. Kmon, P. Maj, R. Szczygiel, 32k channel readout IC for single photon counting pixel detectors with 75µm pitch, dead time of 85 ns, 9 e−rms offset spread and 2% rms gain spread, IEEE Transactions on Nuclear Science , 2016, vol. 63, p. 1155–1161,

3D technology

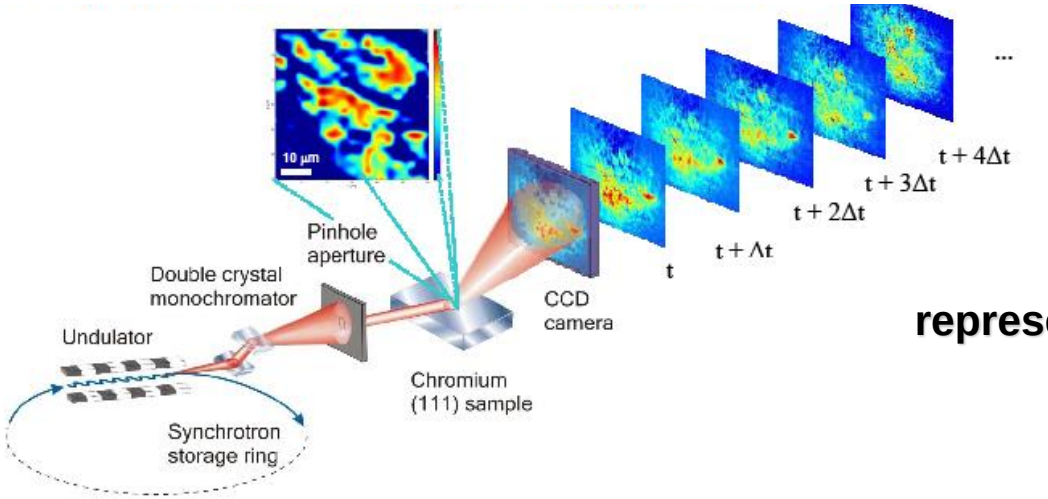
VIPIC IC - 3D Pixel Chip

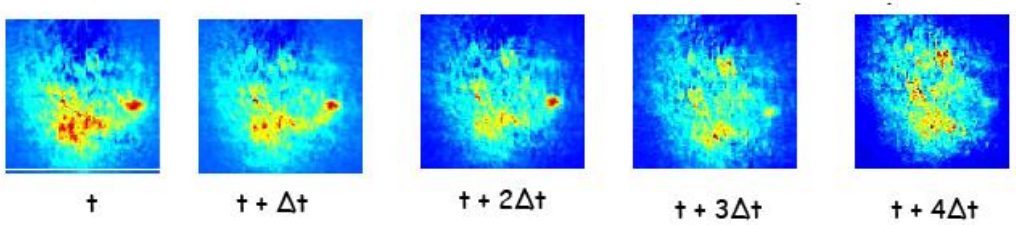
FNAL, USA

AGH UST, Poland

BNL, USA

Application: X-ray Photon Correlation Spectroscopy





O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

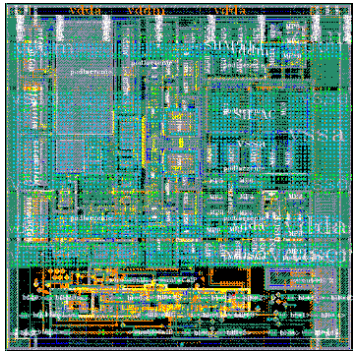
final results are not actual images but mathematical representation of autocorrelation series computed per spatial position

the speckle pattern changes

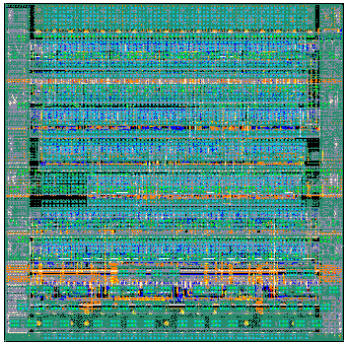
Example of 3-D CMOS

VIPIC chip: 5.1 x 5.1 mm^2 ,continuous readout (XPCS)

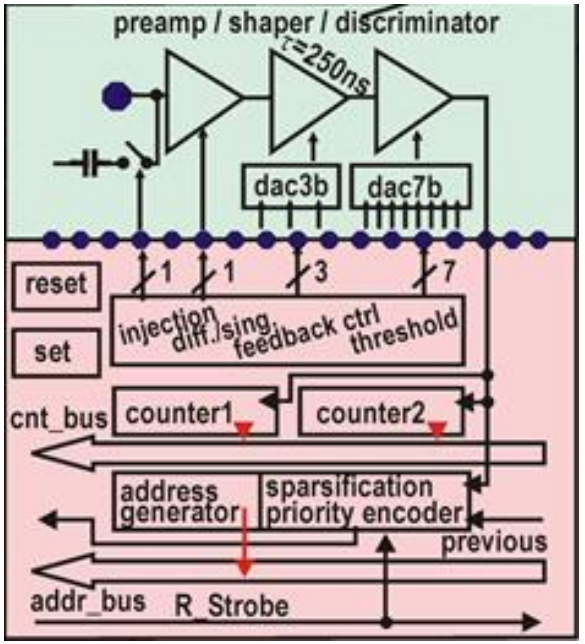
Pixel: 80 x 80 um^2 , matrix: 64 x 64,
2 layers face to face: CMOS 130 nm, TSV dia =1.3 μm
6 μm deep and 3.8 μm minimum



Analog part of pixel

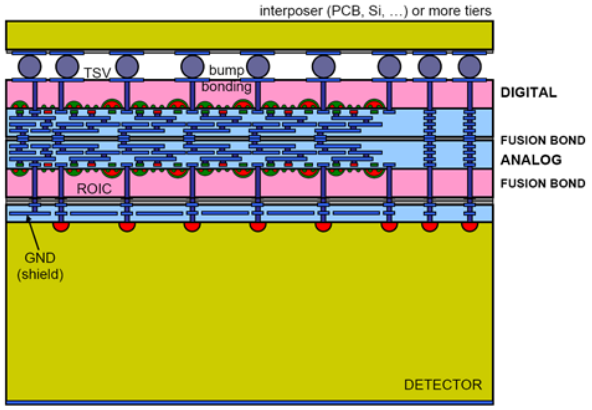


Digital part of pixel



MPW organized by FermiLab
(17 member groups: France, Italy, Germany, Poland, Canada, USA

2 layers face to face: GF 130 nm
TSV 1.3 μm in diameter,
6 μm deep and 3.8 μm minimum spacing is required



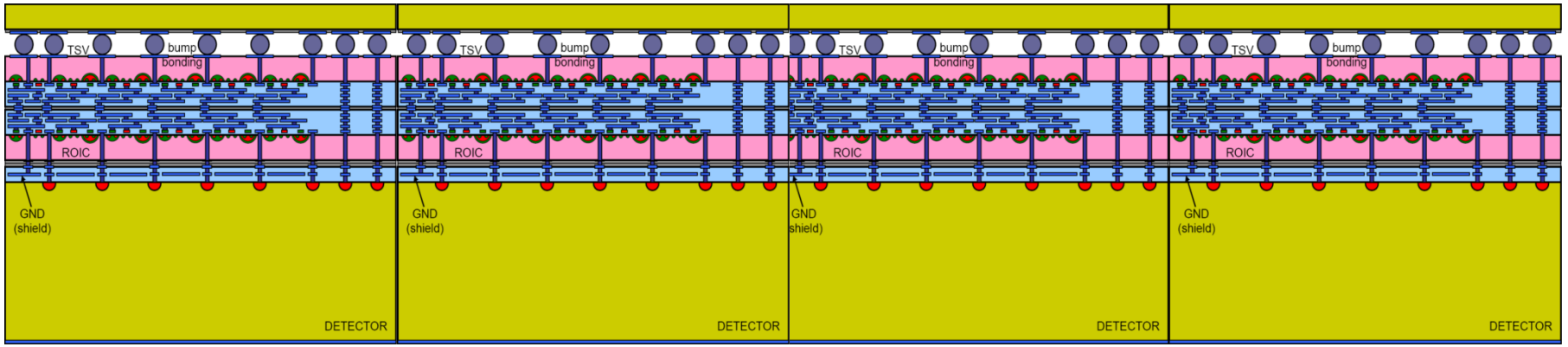
- 160 ns / hit pixel in sparsified mode
- 50×10^3 frame/s in imaging mode (5 bit counting)

G.Deptuch, M.Trimpl, R.Yarema, P.Siddons, G.Carini, P.Grybos, et al., "VIPIC IC - Design and test aspects of the 3D pixel chip", 2010 IEEE Nuclear Science Symposium Conference Record, Orlando, FL, USA, pp.1540-1543, 2010

G.Deptuch, M.Demarteau, J.Hoff, R.Lipton, A.Shenai, M.Trimpl, et al., "Vertically Integrated Circuits at Fermilab", IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 2178–2186, 2010

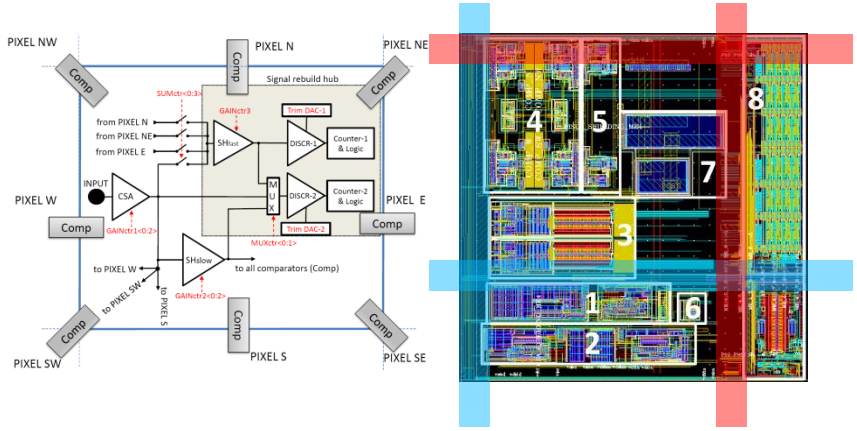
Advantages of 3D:

4-side buttable, dead-area-free detector structure without wire-bonding



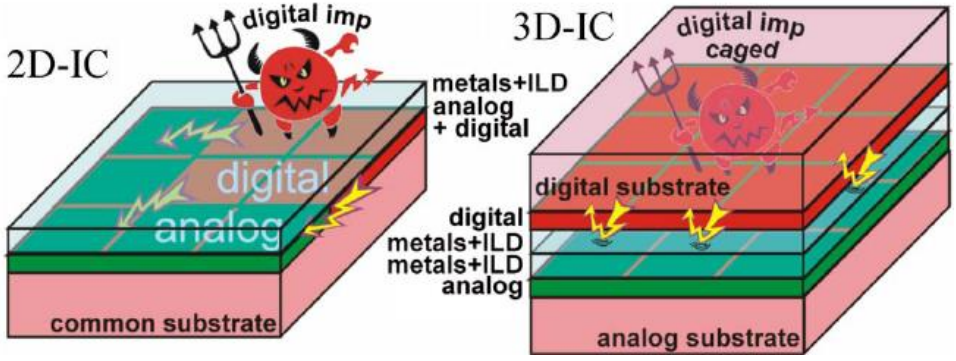
Crosstalk reduction

Interpixel communication – CMOS 40nm



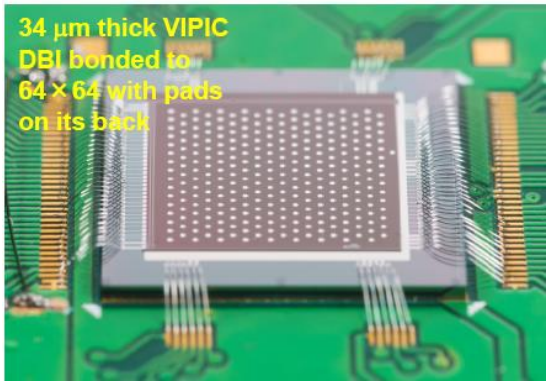
analog channels digital channels

P. Maj, P. Grybos, R. Szczygiel, P. Kmon, R. Kłeczek, A. Drozd, et al., "Measurements of matching and noise performance of a prototype readout chip in 40 nm CMOS process for hybrid pixel detectors", IEEE Trans. Nucl. Sci., vol. 62, 2015, pp. 359–36.



G.W.Deptuch, G.Carini, P.Gryboś, P.Kmon, P.Maj, M.Trimpl, D.P.Siddons, R.Szczygieł, R.Yarema, "Design and Tests of the Vertically Integrated Photon Imaging Chip", IEEE Trans. Nucl. Sci., vol. 61, no. 1, pp. 663-674, 2014

Test with the bump-bonded detector



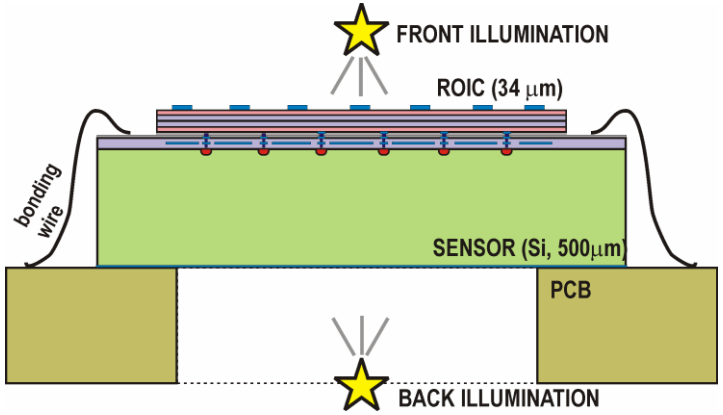
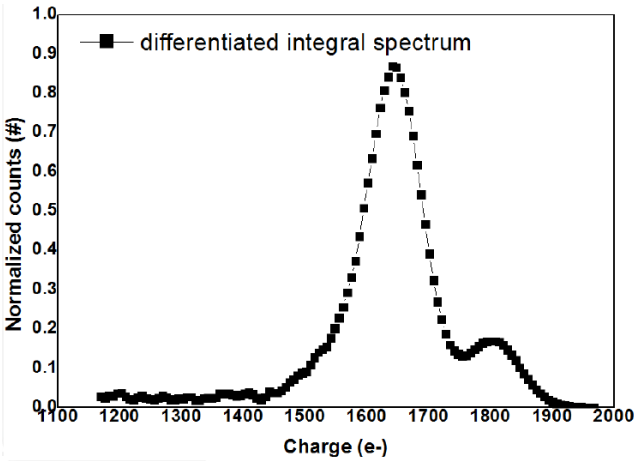


Illustration of how the front and back illuminations of the silicon sensor could be achieved.

Spectrum of ^{55}Fe obtained in front illuminations of the 500 μm fully depleted Si sensor



Ultra low noise = 36 el. rms

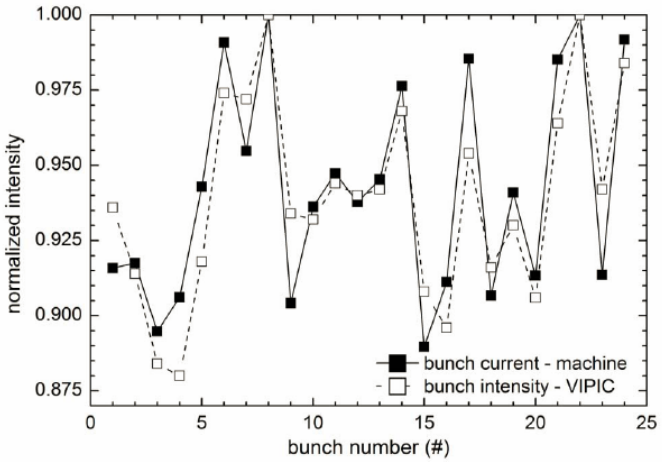


Fig. 10. X-ray intensity measurements of bunch-to-bunch electron beam current variations from the machine and from the VIPIC1 chip.

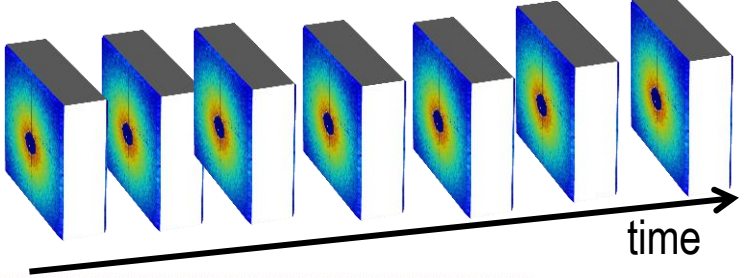
Data collected every 153 ns

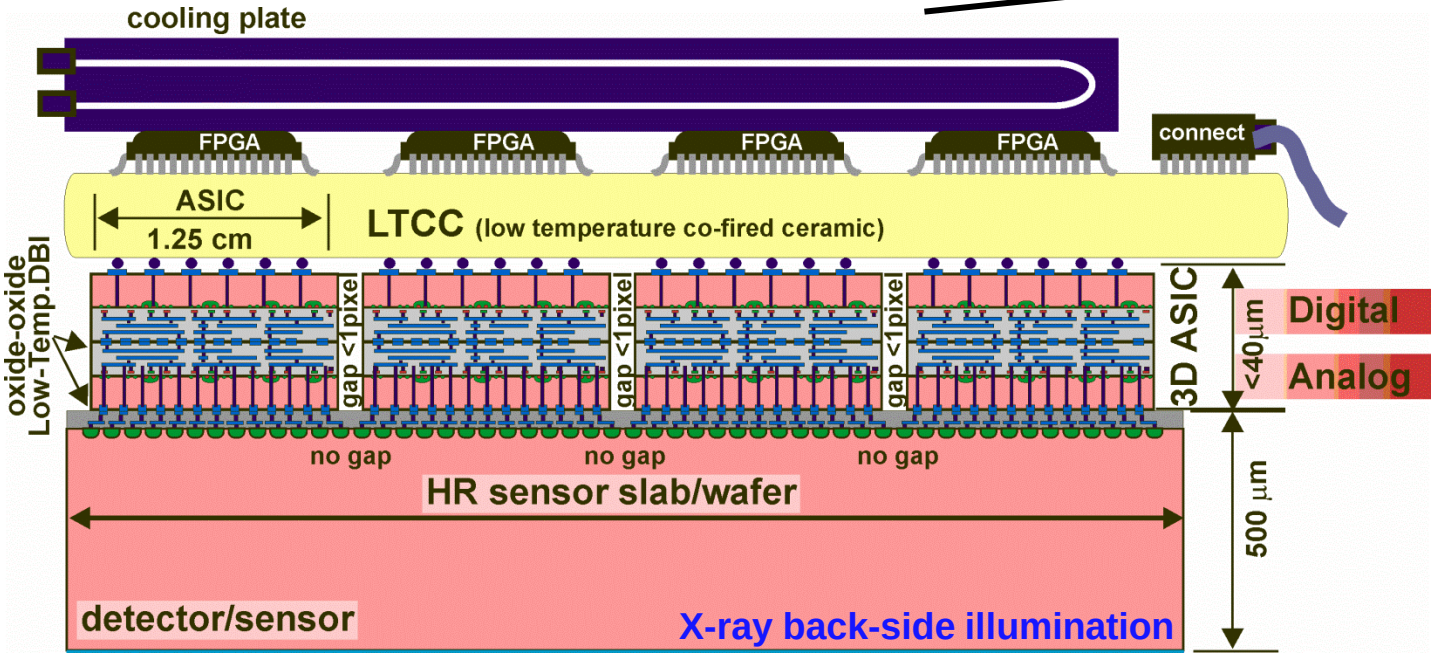
G. Deptuch, G. Carini, P. Enquist, P. Grybos, S. Holm, R. Lipton, et al., "Fully 3-D Integrated Pixel Detectors for X-Rays", IEEE Tran. Electron Devices, vol. 63, no. 1, 2016, pp. 205-214

NEXT step:

VIPIC-L camera (Fermilab, BNL, ANL, AGH)

Vertically-Integrated Photon Imaging Chip - Large





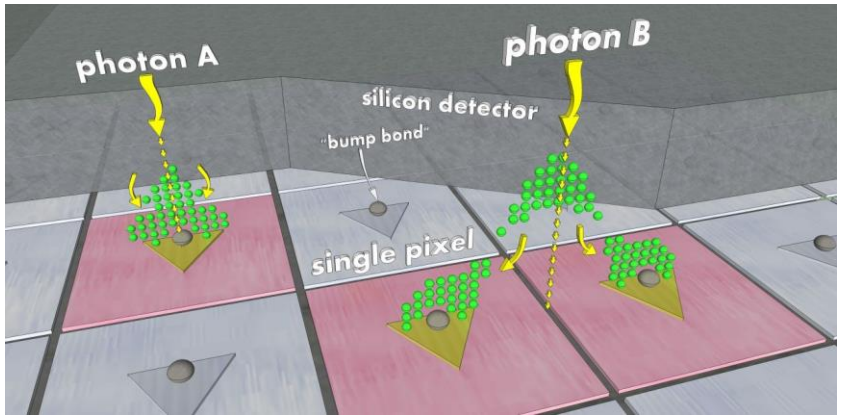
1.2M-pixel, single module camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays, Funded by DOE Office of Science Office of Basic Energy Sciences

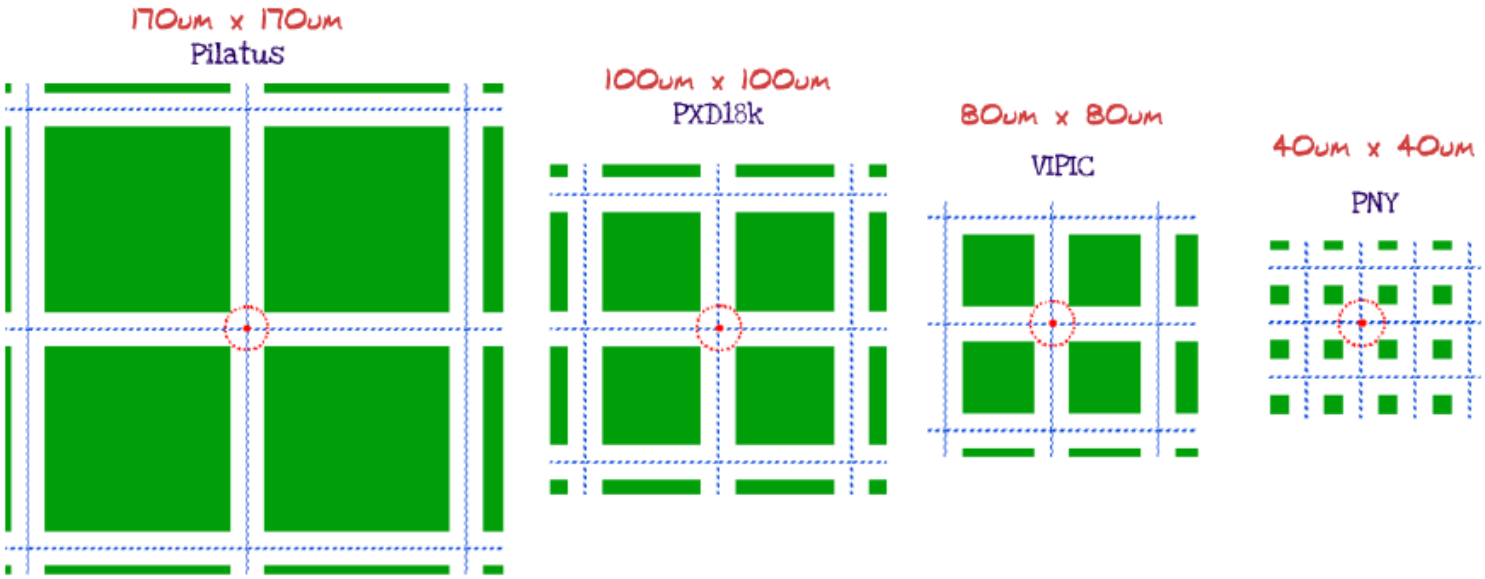
(Project started in Oct. 2014, completion planned for Sept. 2017)

- VIPIC-L ASIC is a two tier 3D ASIC 1.25 × 1.25 cm^2 with ~120M transistor (largest ASIC built by a US national lab) and 65μm pixel pitch and is configurable in sparsification or imaging mode (up to 78kfps)
- 1 Mpixel = 3 slabs of 2 × 6 VIPIC-L LTD-bonded directly to a Si sensor wafer
- 1FPGA per VIPIC-L (in its footprint) for on the fly data processing (up to 0.72 Tbps of raw data produced)
- Multi-layer (>20 routing layer LTCC) suports b-bonded detector structure

Step forward to colour X-ray imaging (technology CMOS 40 nm)

Charge sharing effect





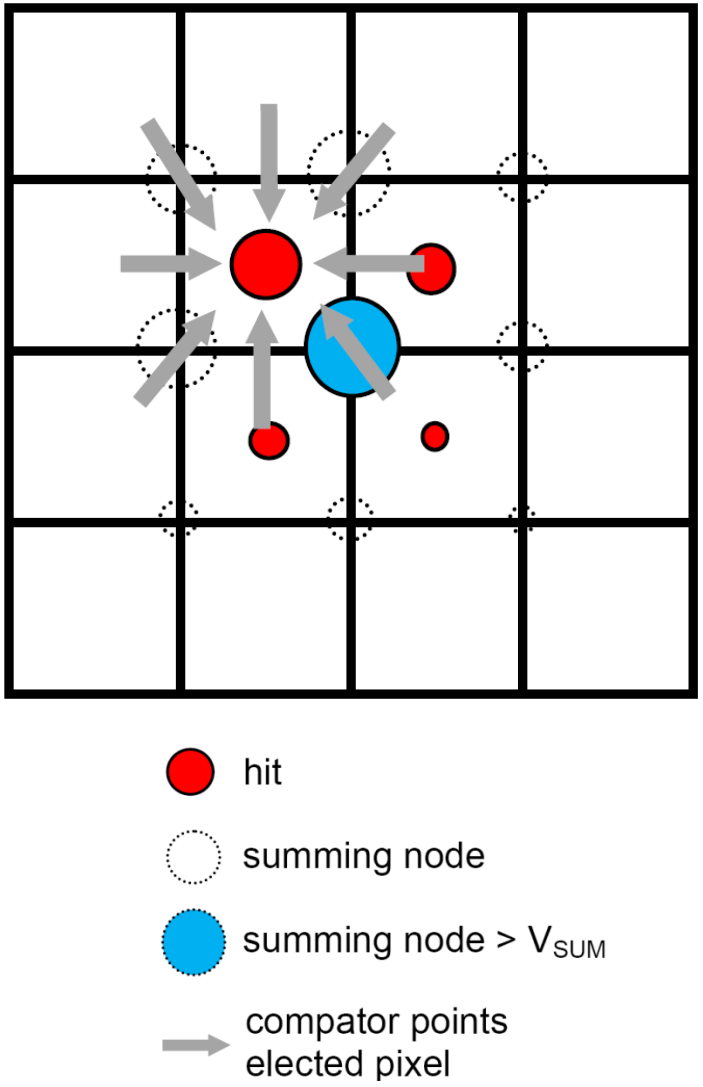
The first solution of this problem was proposed by CERN and consequently it was implemented in the Medipix III chip. However, due to pixel-to-pixel threshold dispersions and some imperfections of the simplified algorithm, the hit allocation was not functioning properly.

Hit position identification (C8P1)*

1) pulse at summing node is above a threshold

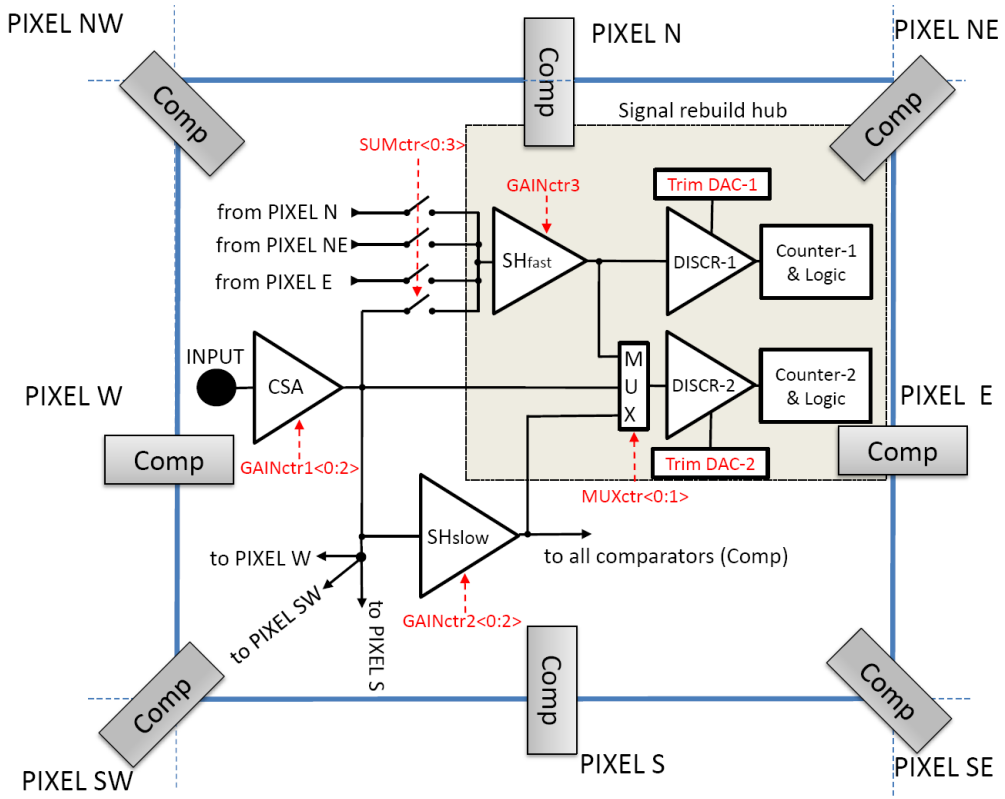
2) comparision of pulse amplitude in a single pixel with its 8 neighbours

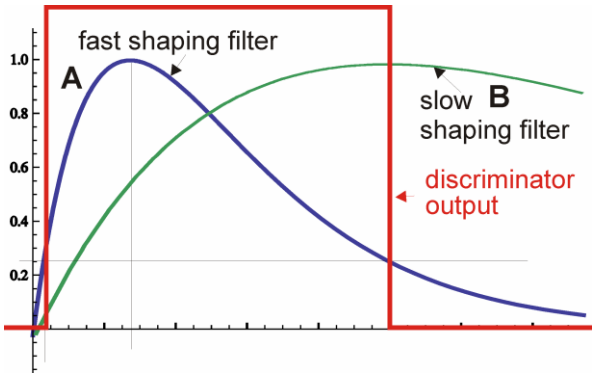
Selected pixel: one of its summing node is above the threshold AND all 8 comparators point out this pixel



*A. *Baumbaugh, G. Carini, G. Deptuch, P. Grybos, J. Hoff, P. Maj, P. Siddons, R. Szczygiel,M Trimpl, R. Yarema,* **Analysis of Full Charge Reconstruction Algorithms for X-Ray Pixelated Detectors, Proceedings of IEEE NSS 2011, Valencia, Spain,** Page(s): 660 – 667, Publication Year: 2011 ,

Matching and testability





MATCHING:

1) Shfast: 7-bit offset trim

2) Shslow: 3-bit gain tim

3) COMP: auto-zero correction trigged by DISCR output

4) Latching of COMP triggered by DISCR rising edge is controlled by timing curcuitry ; 5 bit trim

5) Additionally: **CSA** – 3-bit gain control

TEASTABILITY:

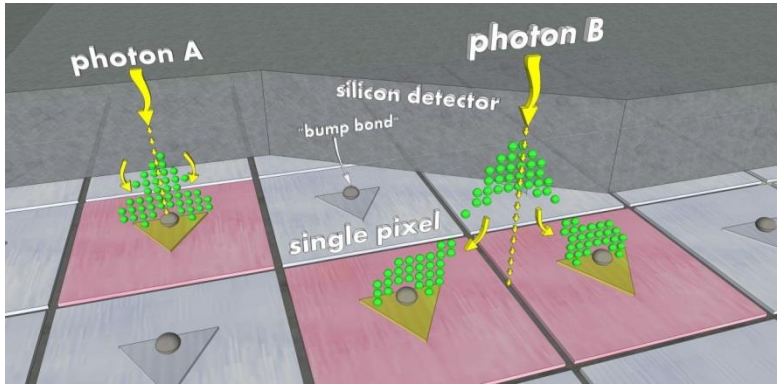
1) Test injection circuit: 4 difffrent charges can be injected to diffrent pixels at the same time

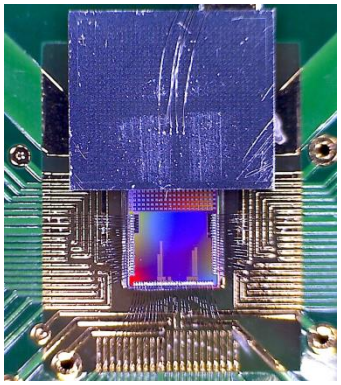
2) MUX: pulse can be counted at CSA, Shfast and Shslow outputs

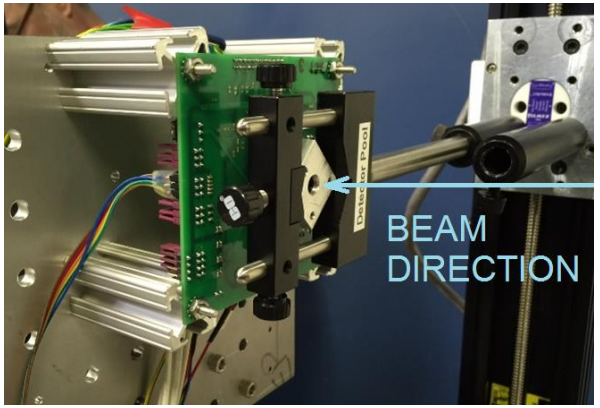
3) COMP: outputs can be redirected to counters

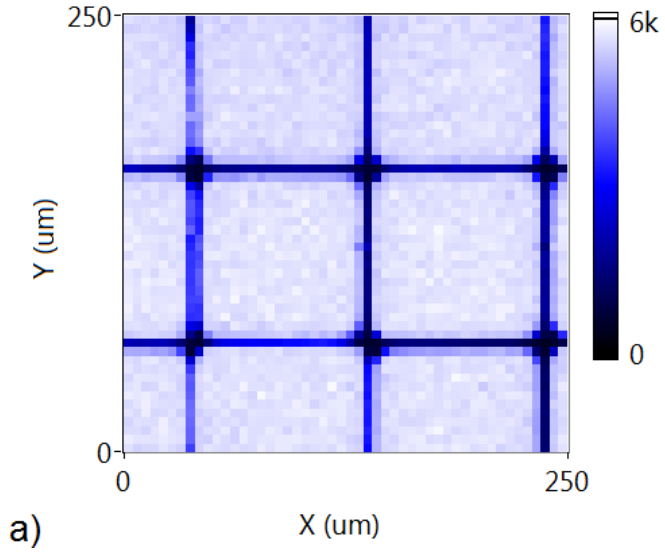
P. Maj, P. Grybos, R. Szczygiel, P. Kmon, R. Kłeczek, A. Drozd, et al., "Measurements of matching and noise performance of a prototype readout chip in 40 nm CMOS process for hybrid pixel detectors", IEEE Trans. Nucl. Sci., vol. 62, 2015, pp. 359–36.

Standard counting vs. C8P1
(X-Ray measurements)

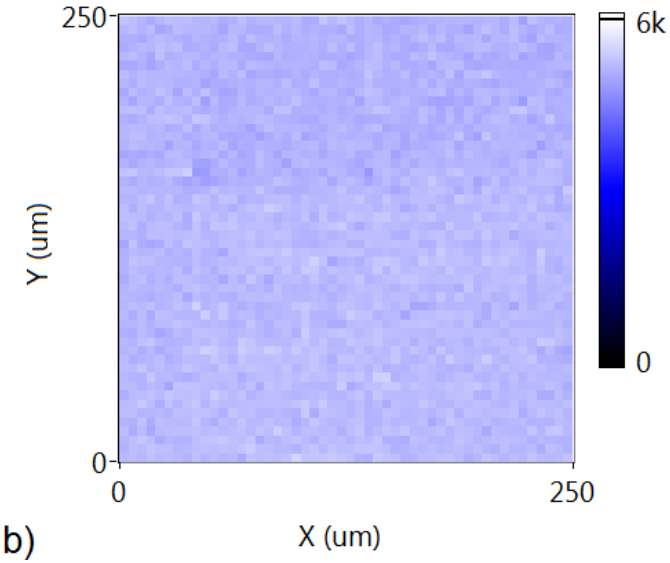








standard counting

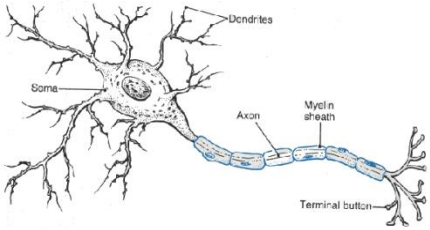


C8P1

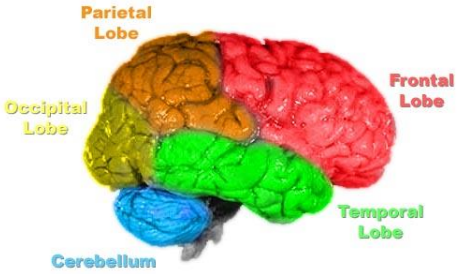
Neurobiology

Neural systems

SINGLE NEURON



BRAIN



Bibliographic Entry	Result (w/surrounding text)	Standardized Result
Glencoe Health 2nd Edition. Mission Hills: Glencoe Inc., 1989: 252.	"Weighing around three pounds (1.35kg), the brain contains nearly 100 billion cells."	100 billion
World Book 2001. Chicago: World Book Inc., 2001: 551.	"The human brain has from 10 billion to 100 billion neurons."	10 - 100 billion
Magill's Medical Guide Revised Edition. Salem Press, 1998: 221.	"It has been estimated that the adult brain has around one hundred billion neurons and an even larger number of glial cells."	100 billion
The Science Times Book of the brain. New York: The Lyons Press, 1987: 150.	"The human brain holds about 100 billion nerve cells."	100 billion
The Scientific American Book of the Brain. New York: Scientific American, 1999: 3.	"An adult human brain has more than 100 billion neurons"	> 100 billion

RETINA

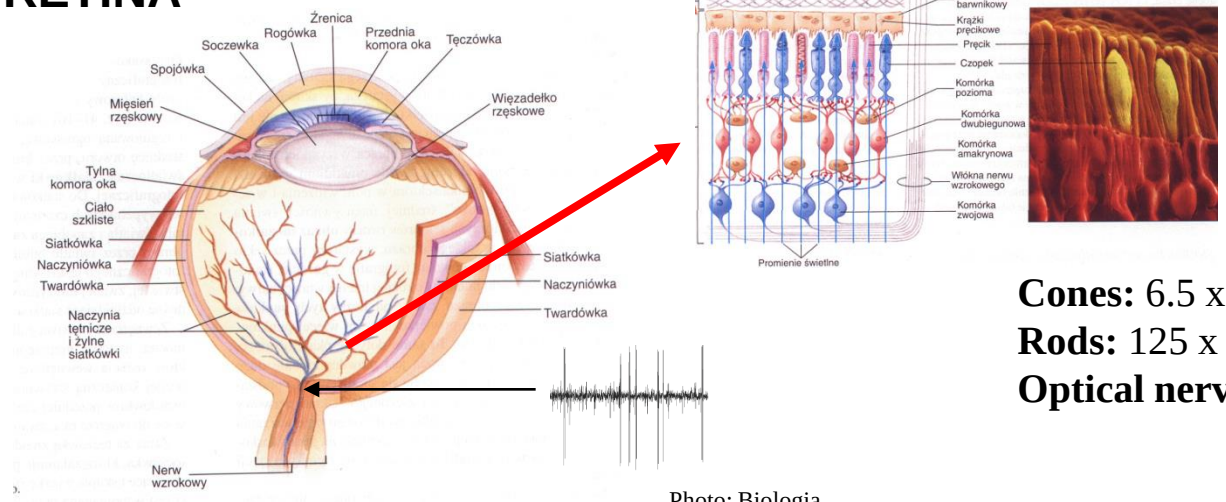


Photo: Biologia, PWN

Cones: 6.5 x 10^6 (colours)
Rods: 125 x 10^6 (move, shape)
Optical nerve: 1 x 10^6 fibers

AIM: to build an electronic interface

for recording/stimulation of neuronal system comprising several hundreds or thousands of electrodes

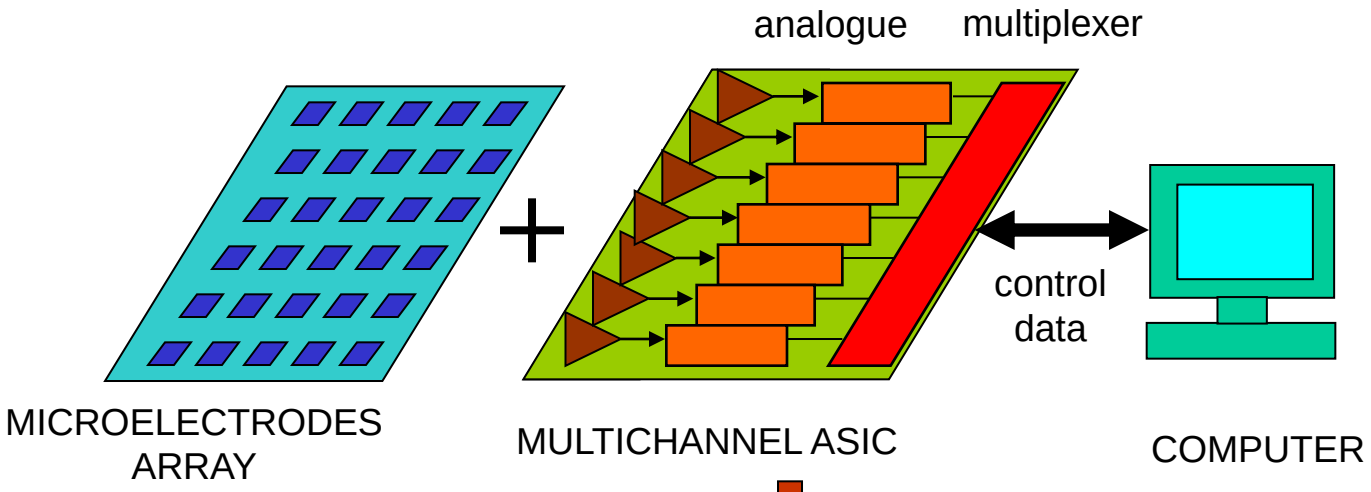
Motivation

1. Understand neuronal coding,
2. Biosensors
3. Neuronal prostheses

Components

1. Microelectrode array
2. Multichannel electronics

Multichannel neuribiological recording based on ASIC

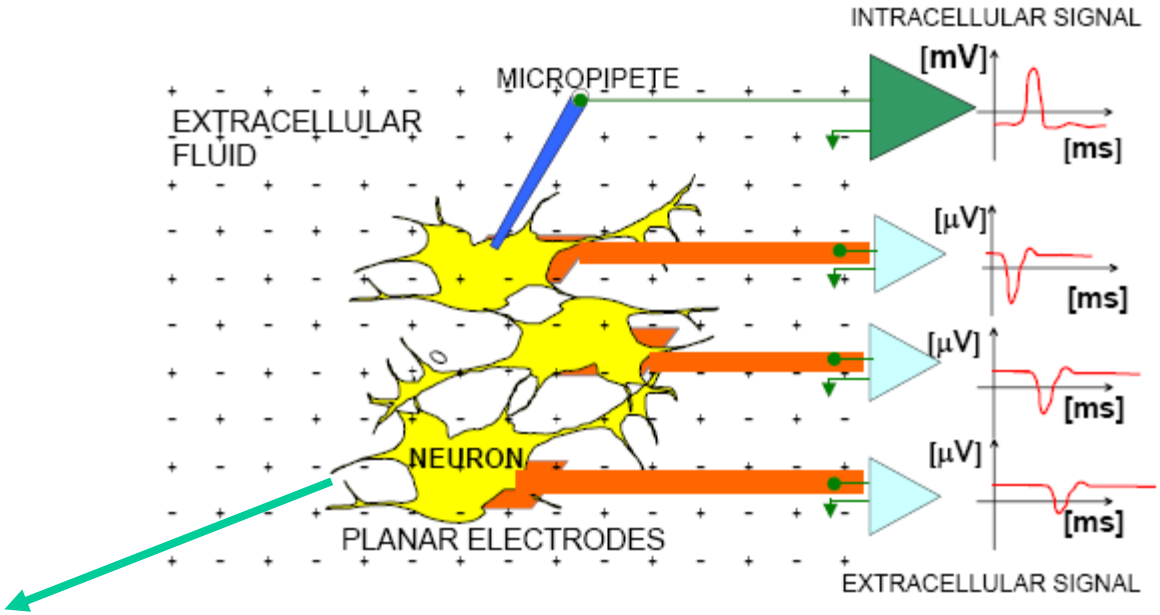


To design a multichannel
APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC),
which is able to cope with extracellular neuronal recording

system

- **to built recording system comprising several hundreds or thousands of electrodes**
- **miniaturization**

Extracellular recording – requirements for electronics



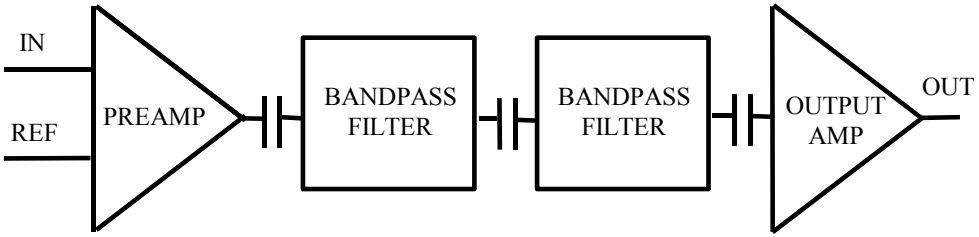
Signal source (e.g. retina tissue): V_{amp} = 50-500 μV, DC offsets,
$t_w \approx$ 1-2 ms, band: 20 -2000 Hz,

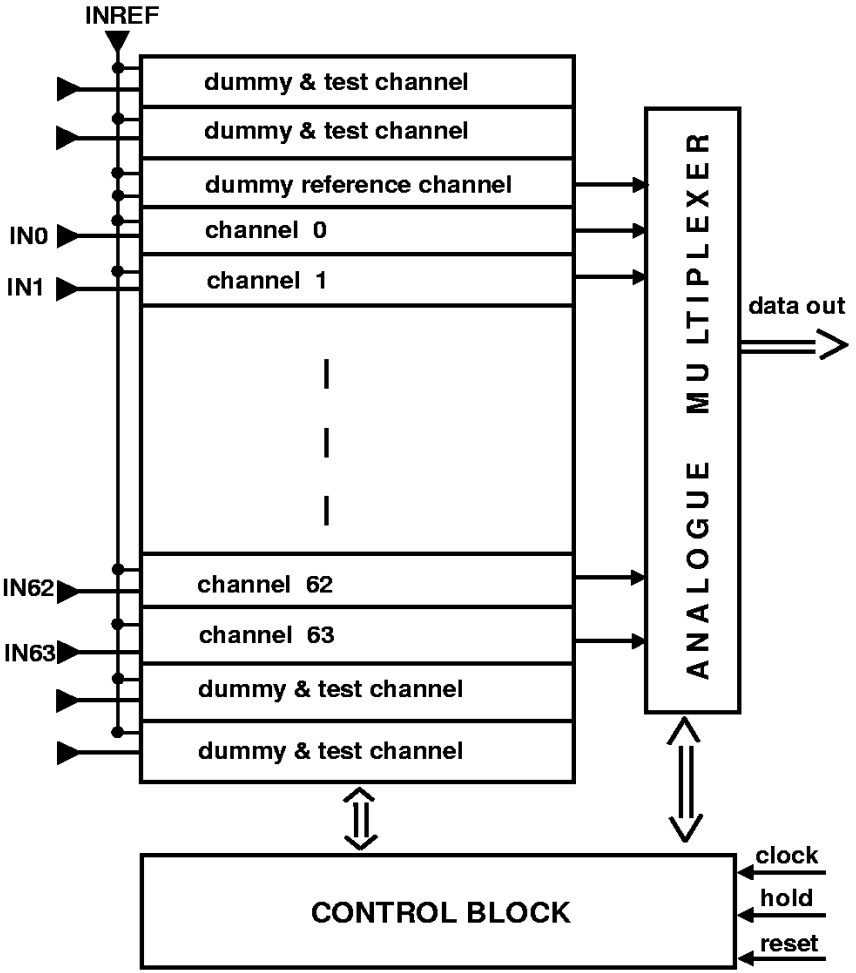
Requirements:

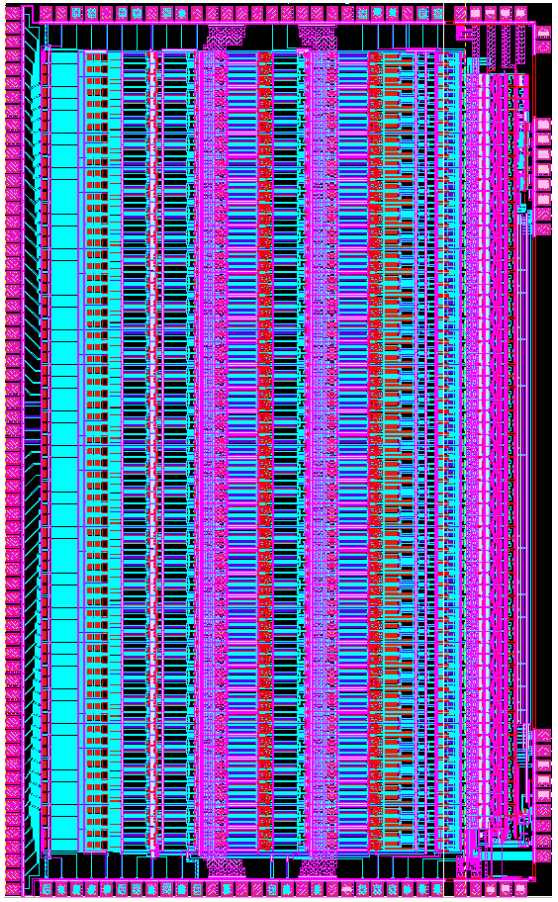
Low noise ~ 5 μV rms
Frequency band pass 20 Hz to 2000 Hz
AC coupled input cut-off frequency < 20 Hz

→ **MULTICHANNEL ARCHITECTURE**

NEURO64

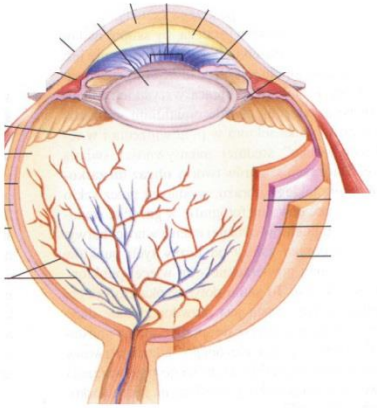


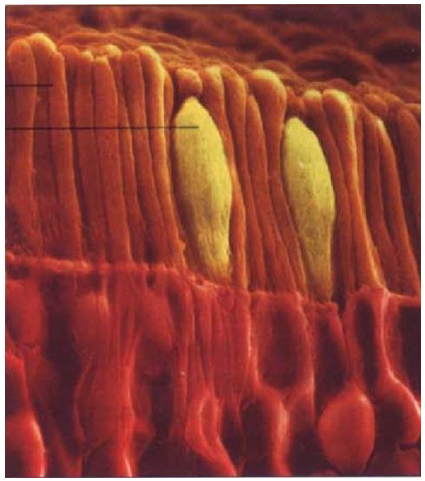


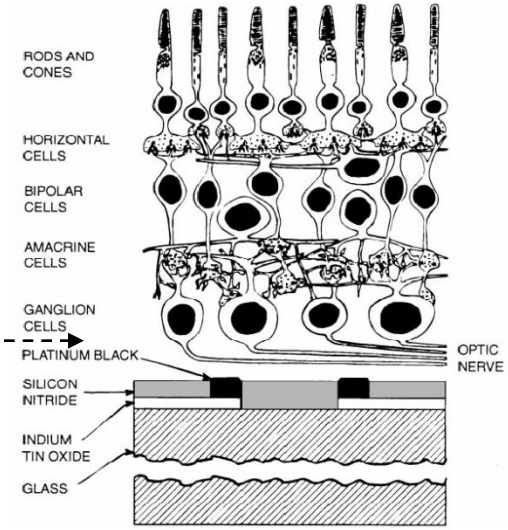


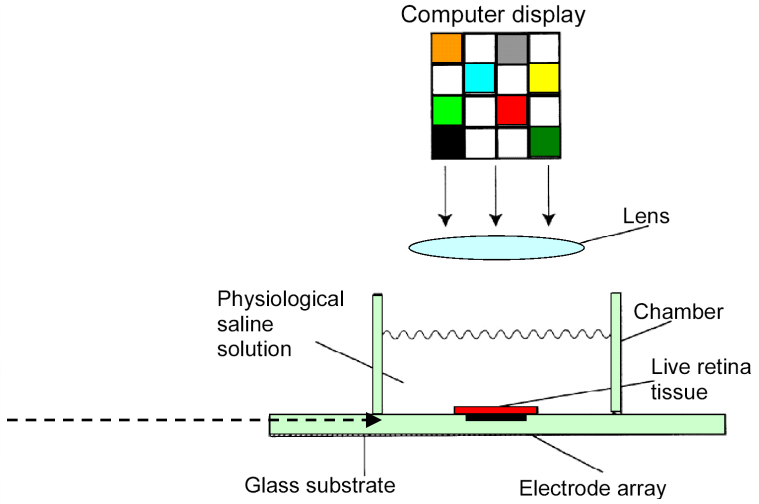
4000×6500 μm2

Example of application:
RETINAL READOUT SYSTEM









Four group of people from:
UC - Santa Cruz: data acquisition system & analysis
AGH UST - Krakow: IC design and testing
Univ. Glasgow – UK: microelectrode fabrication
Salk Institute - San Diego: neurobiology

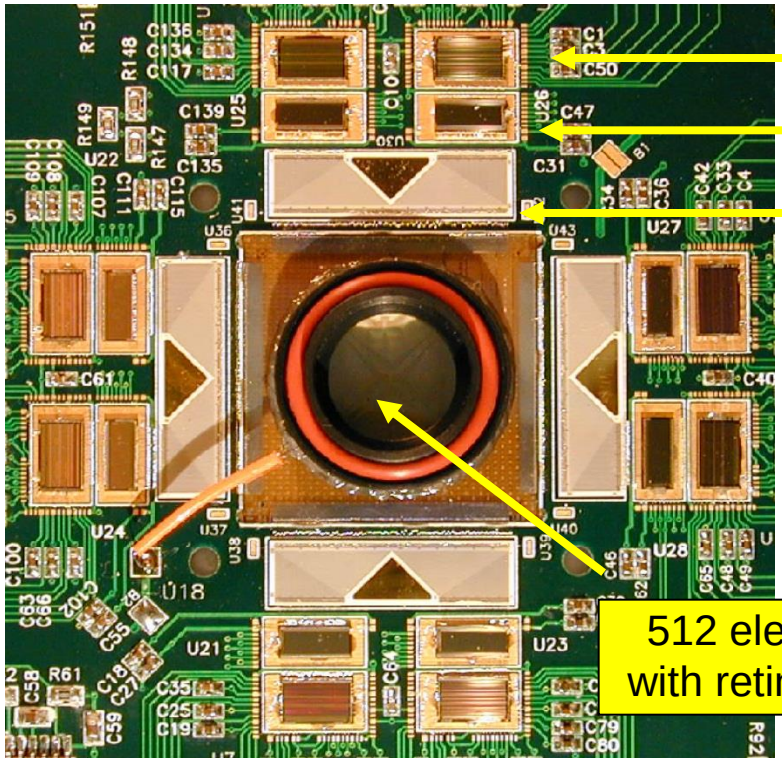
A movie is focused on the retina tissue

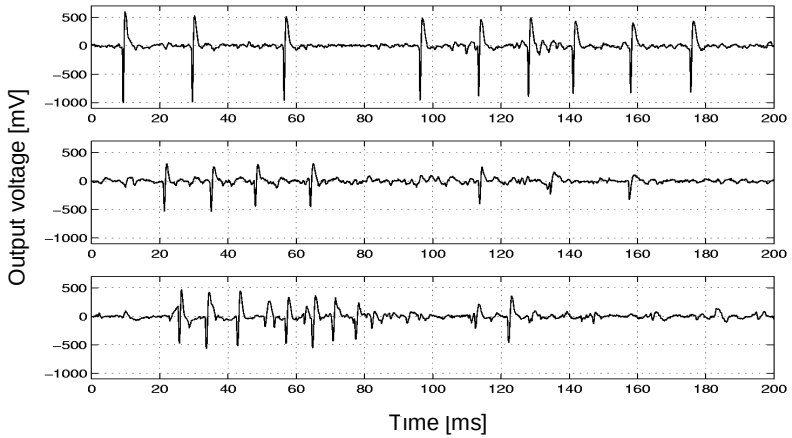
⇓

The patterns of electrical activity generated by hundreds of retinal output neurons are recorded

System of 512 readout channels

To understand how the retina processes and encodes dynamic visual image





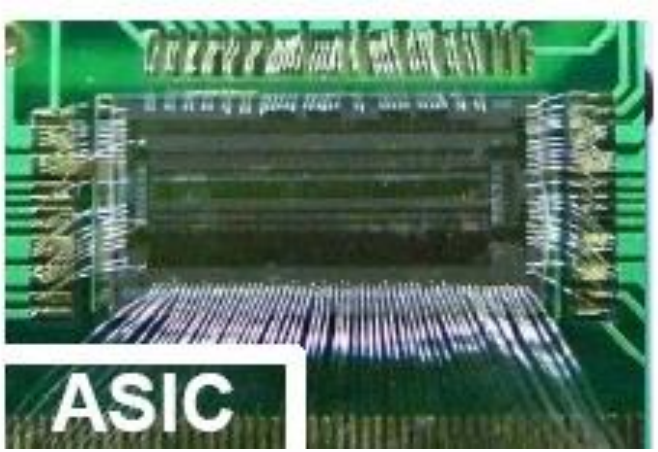
More about above system in ref:

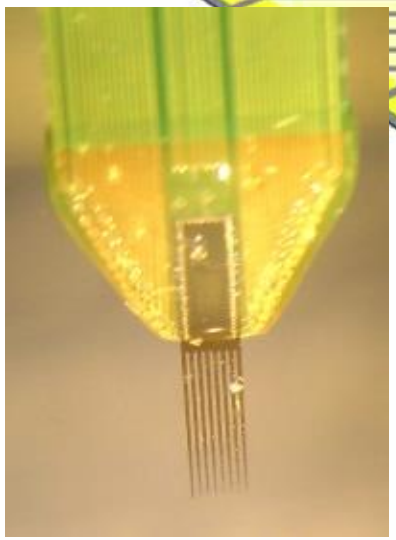
Litke AM, Bezayiff N, Chichilnisky EJ, Cunningham W, Dabrowski W, Grillo AA, Grivich M, Grybos P, Hottowy P, Kachiguine S, Kalmar RS, Mathieson K, Petrusca D, Rahman M, Sher A.

What does the eye tell the brain?: Development of a system for the large-scale recording of retinal output activity.

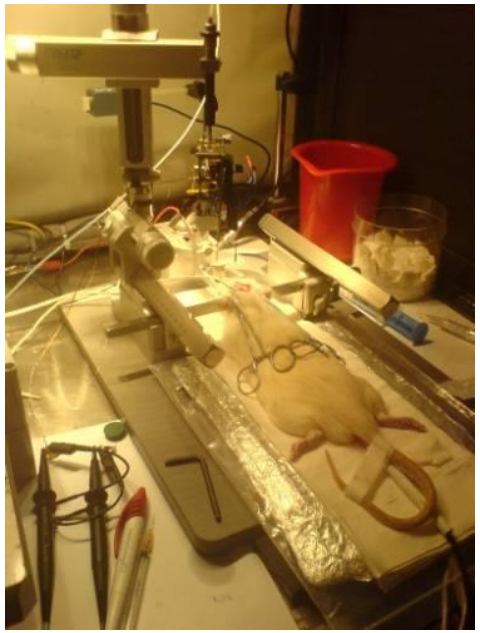
IEEE Transactions on Nuclear Science, vol.51, no.4, Aug. 2004, pp.1434-40.

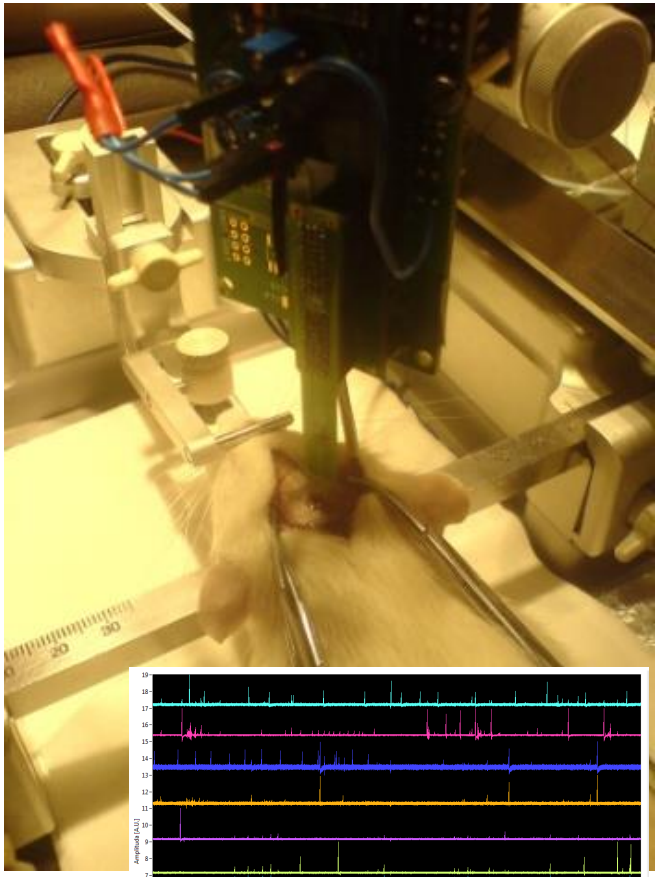
ASIC for vivo experiments + electrodes



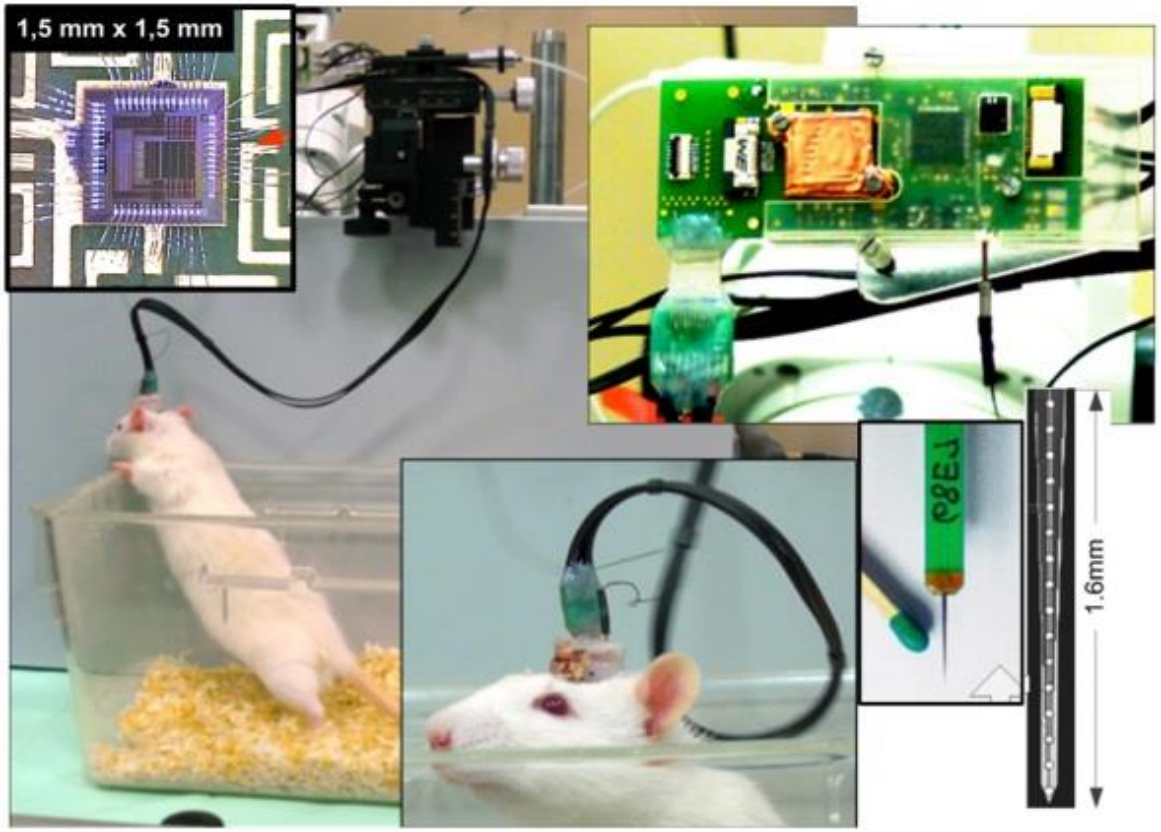


Neurobiological tests
cooperation with Jagiellonian University





Neurobiological tests
cooperation with Jagiellonian University



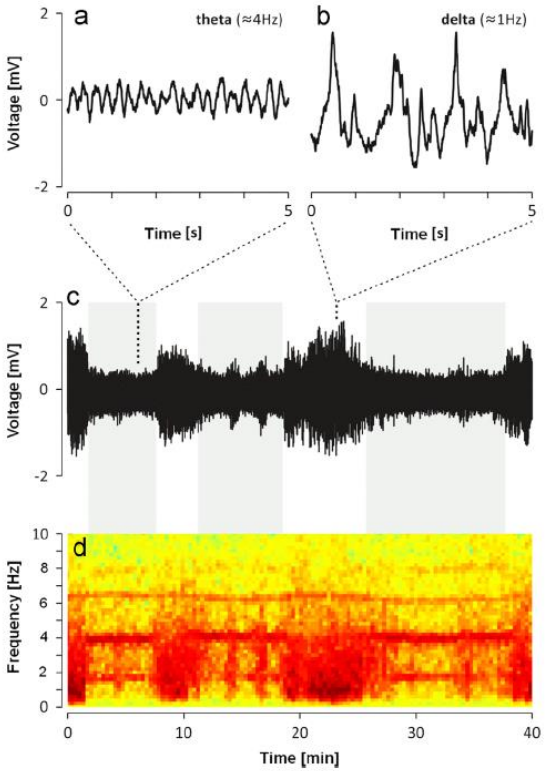
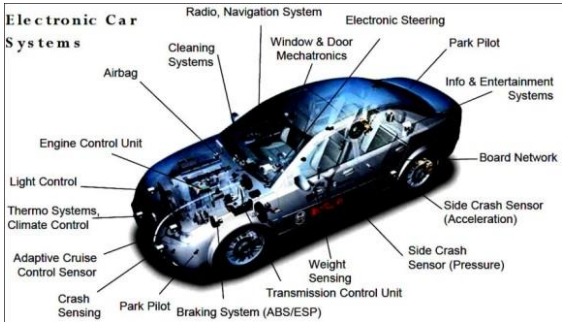
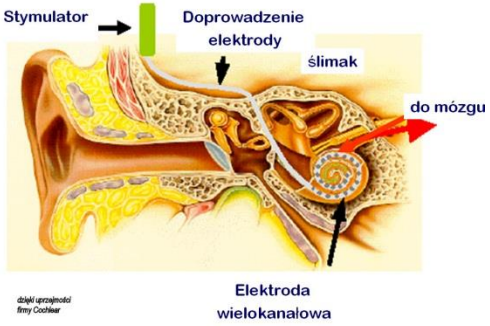


Fig. 14. An example showing the alternations of the dominant frequency of the local field potential (LFP) recorded in the nucleus incertus (NI) of the urethane anaesthetised rat. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

NEW COURSE!!! (BSc, MSc.)

Microelectronics in industry and medical applications





IEEE+Cadence+ New courses in microelectronics

1) hold meetings, seminars and short courses for the members, replay interesting tutorials and conference presentations,

2) **increase the quality and innovation factor in our IC designs**,

3) **invite distinguished lectures/researchers to Poland**,

4) strengthen the relations between different engineers from university and industry working on solid state circuits,

Acknowledgments:

1. ASIC Design Group
Dep. of Measurements and Electronics AGH UST.
http://www.kmet.agh.edu.pl/www/asics

2. FNAL US (G. Deptuch – 3D MPW, VIPIC)
BNL US (P. Siddons – synchrotron facility)
Rigaku Corporation, Japan

3. Department of Microelectronics and Computer Science, Lodz University of Technology
Institute of Microelectronics and Optoelectronics, Warsaw University of Technology

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2) National Science Center, Poland,

3) DOE Office of Science Office of Basic Energy Sciences , US