Multiple Trigger Requests Implementation in the GTS and Other Developments on Trigger Interface Cards

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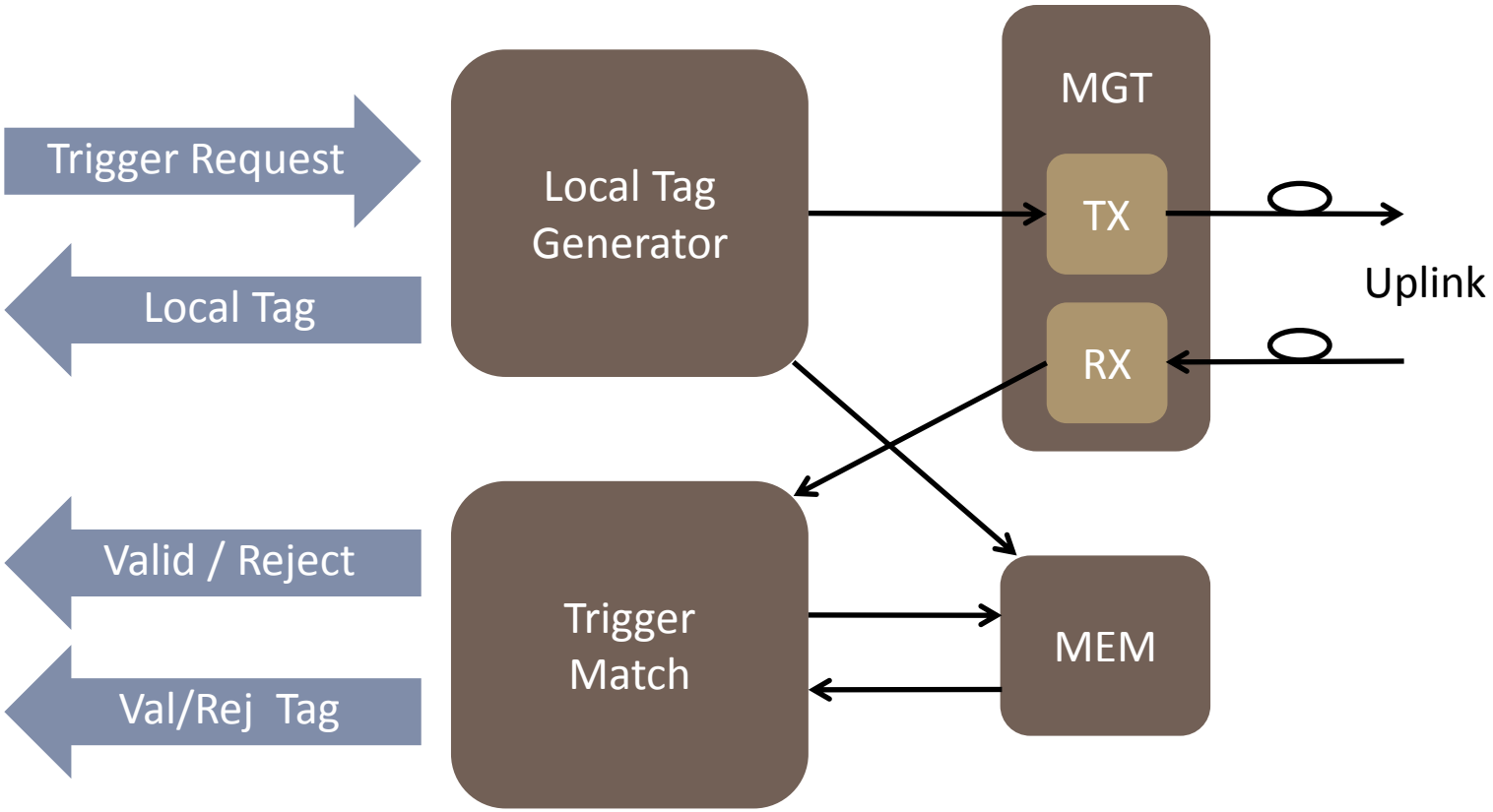
GTS Functionalities

- Common clock
- Global clock counter
- Global event counter
- Trigger requests
- Error reports

- Trigger controls:
  - Throttling of the L1 validation signal
  - Fast commands (fast reset, initialization, etc.)
  - Fast monitoring feedback from the crystals
  - Calibration and test trigger sequence commands
  - Monitor of dead time



Trigger Request Limit

- Serves just one trigger request

Interface for 16 (80ns latency!)

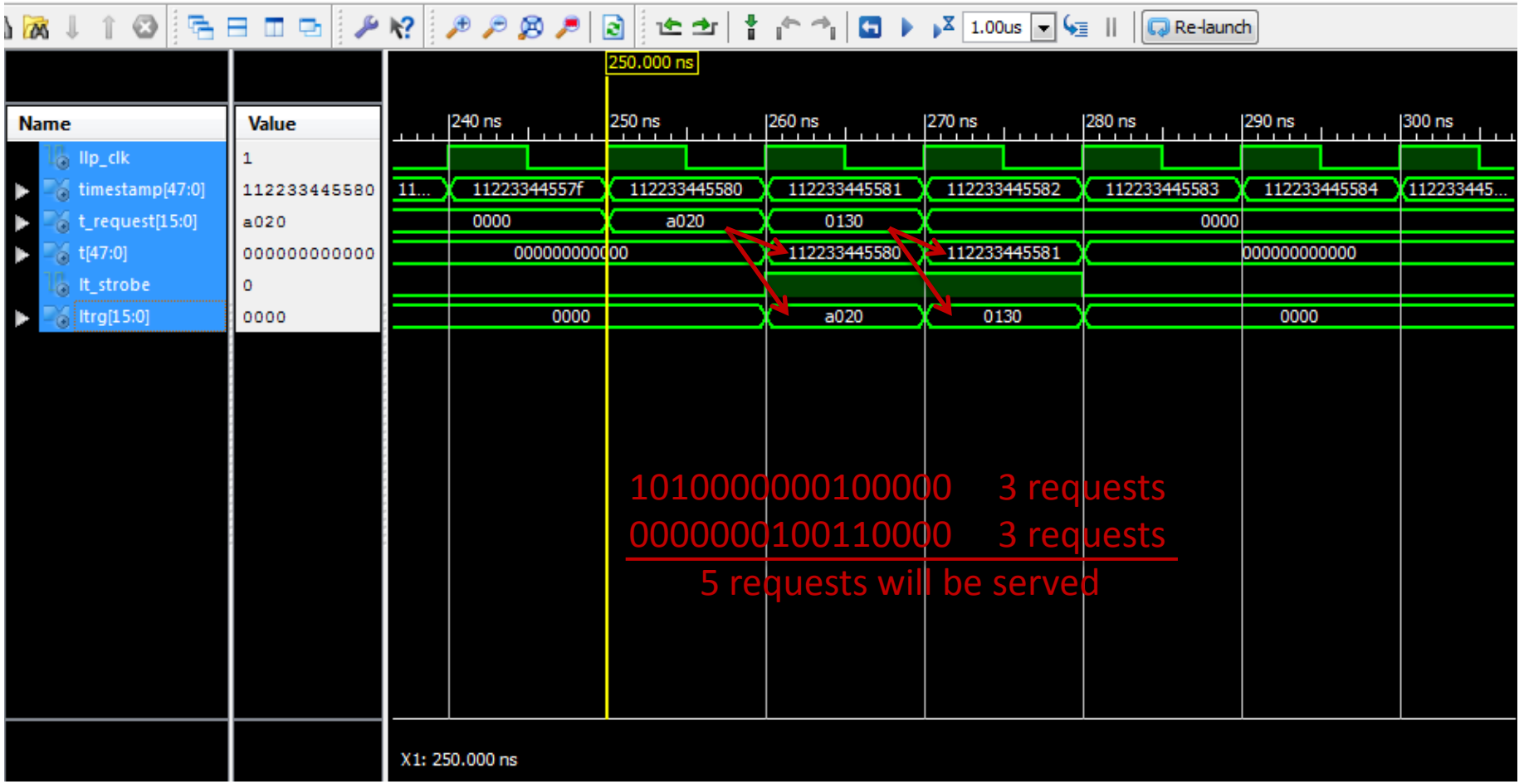
- Parallel bus (48 bit)
- Timestamp latch and timestamp assignment are pipelined

- Handles just one ID request

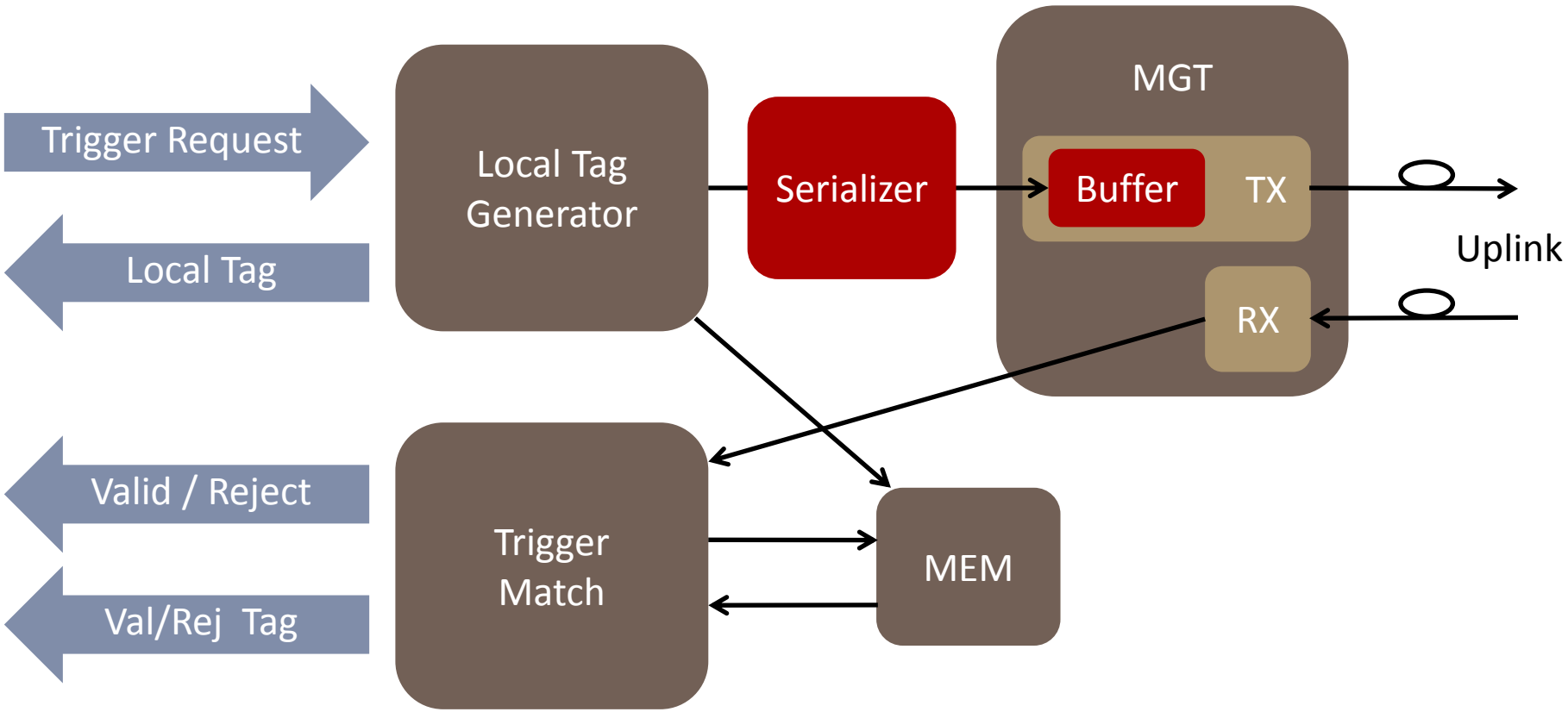
16 ID per GTS core

- Concurrent requests are serialized in order to be passed to command encoder
- Bufferized at the input of the command encoder in order to leave it the time of building the packet and to schedule the sending of the packets to the root node

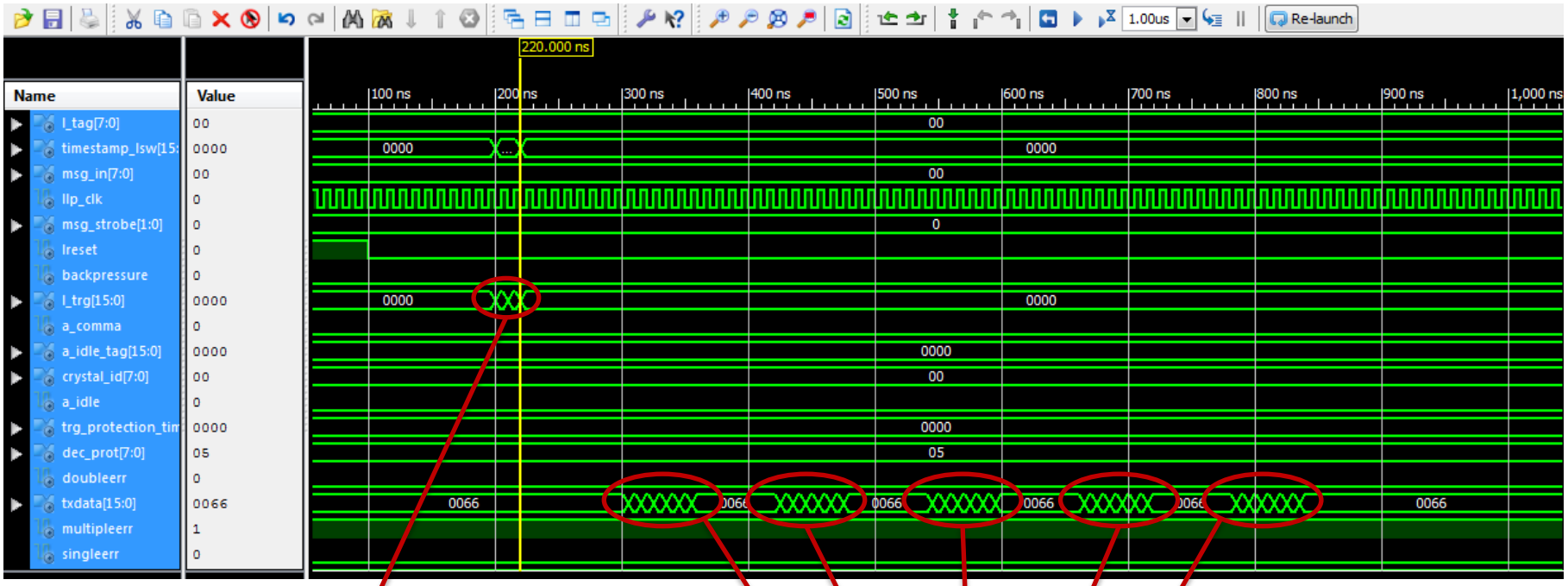
Requests Interface



Requests Serializing



Multiple ID Requests

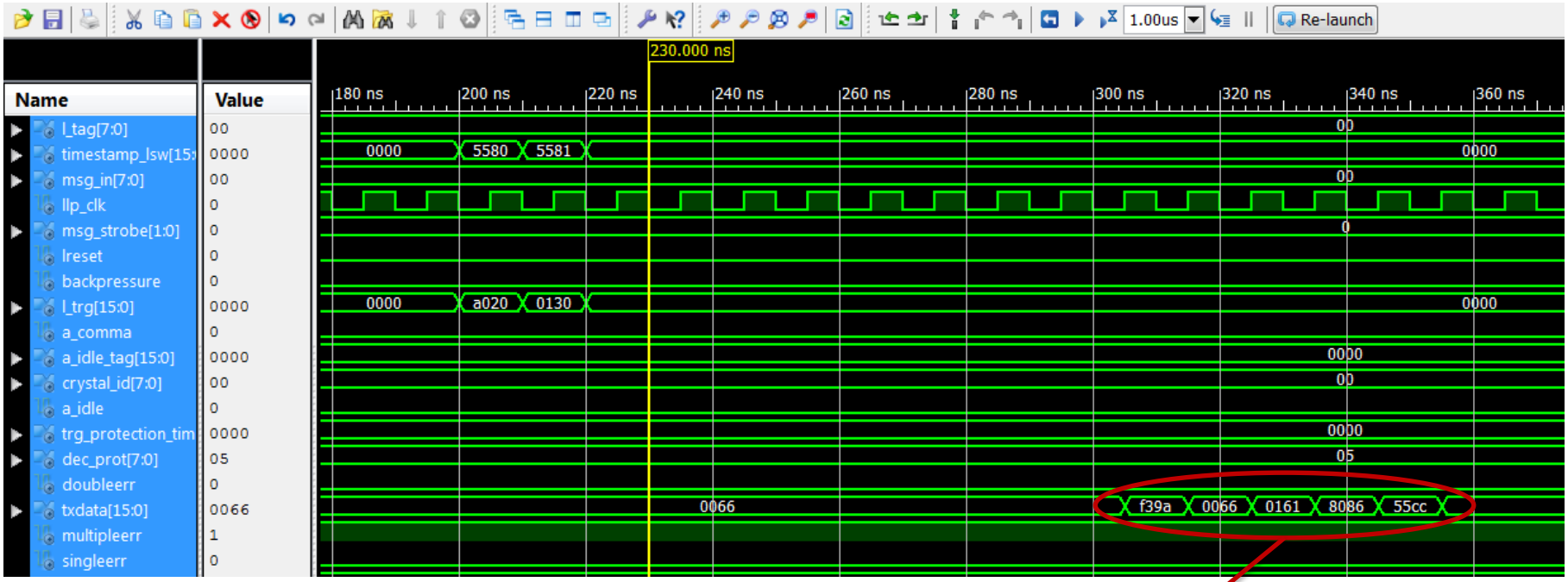


1010000000100000
0000000100110000

5 different IDs:
Channels:

1010000100110000
0123456789ABCDEF

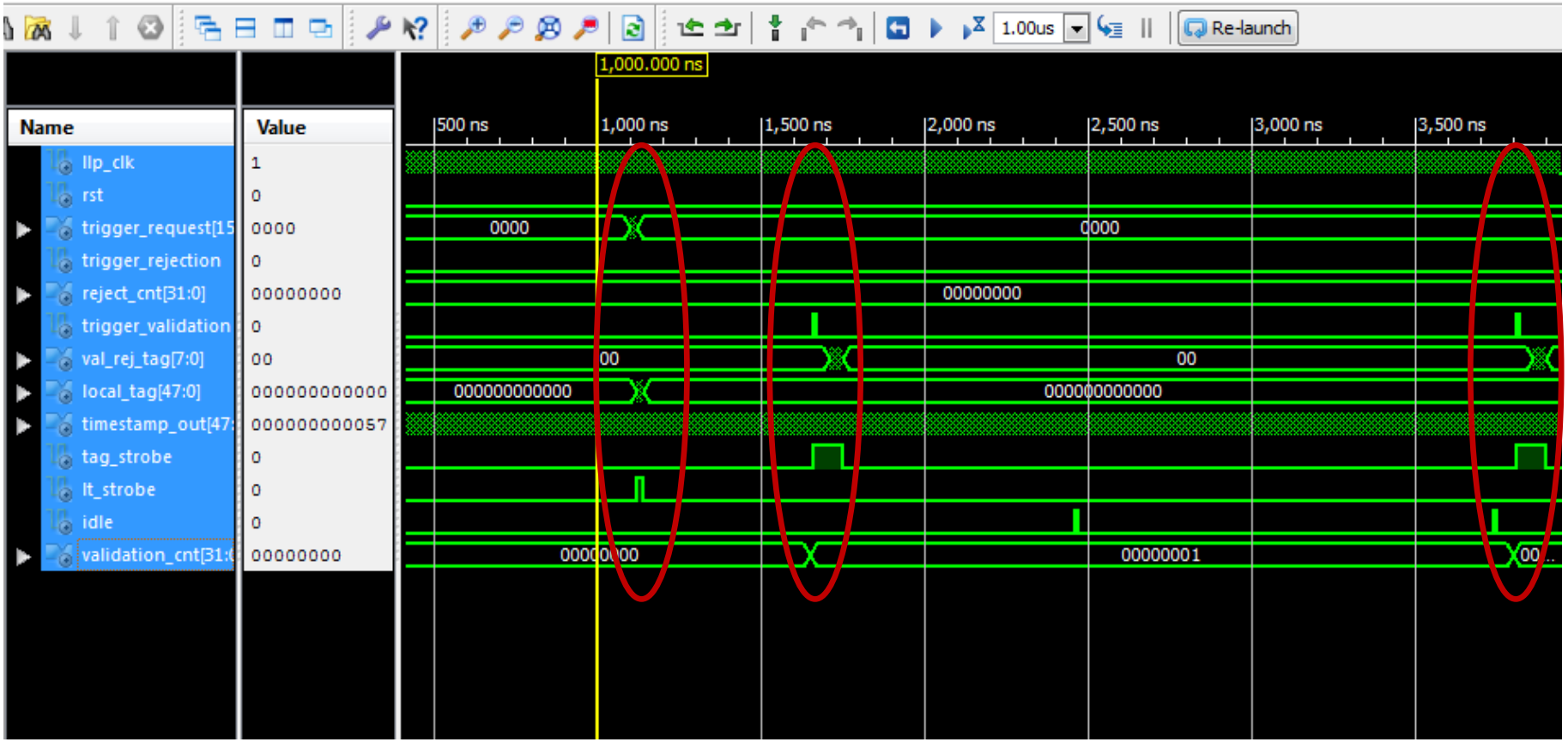
Multiple ID Requests – 1st Packet



F3 00 01 80 55

START | LENGTH | TRIGGER ID | COMMAND ID | LOCAL TAG (7:0) | LOCAL TAG (15:8)

Full Interface



Multiple Requests Limits

- Trigger IDs
  - 256 trigger IDs in triggerless mode (root node validates all)
  - Trigger processor limits the ID numbers to 40, but it could be increased
- Validations

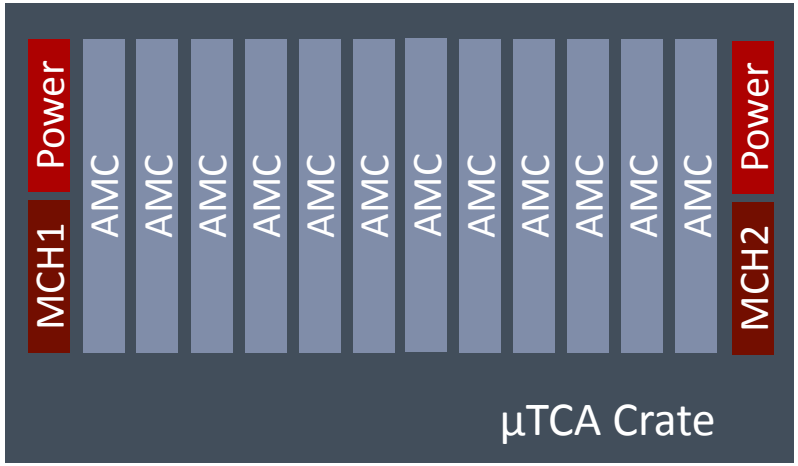
  The validation regards only local tag:
  - Many trigger requests with the same local tag but different ID generate only one validation/rejection
  - Complainant with the old GTS

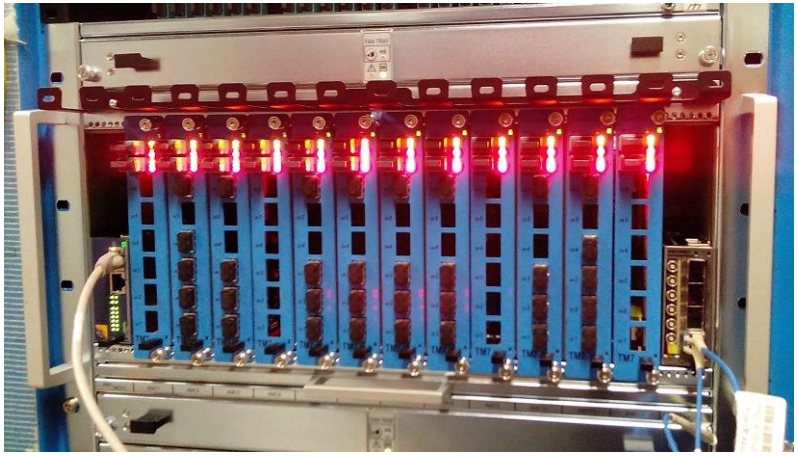
Hardware Development of a Trigger Concentrator

A µTCA Board

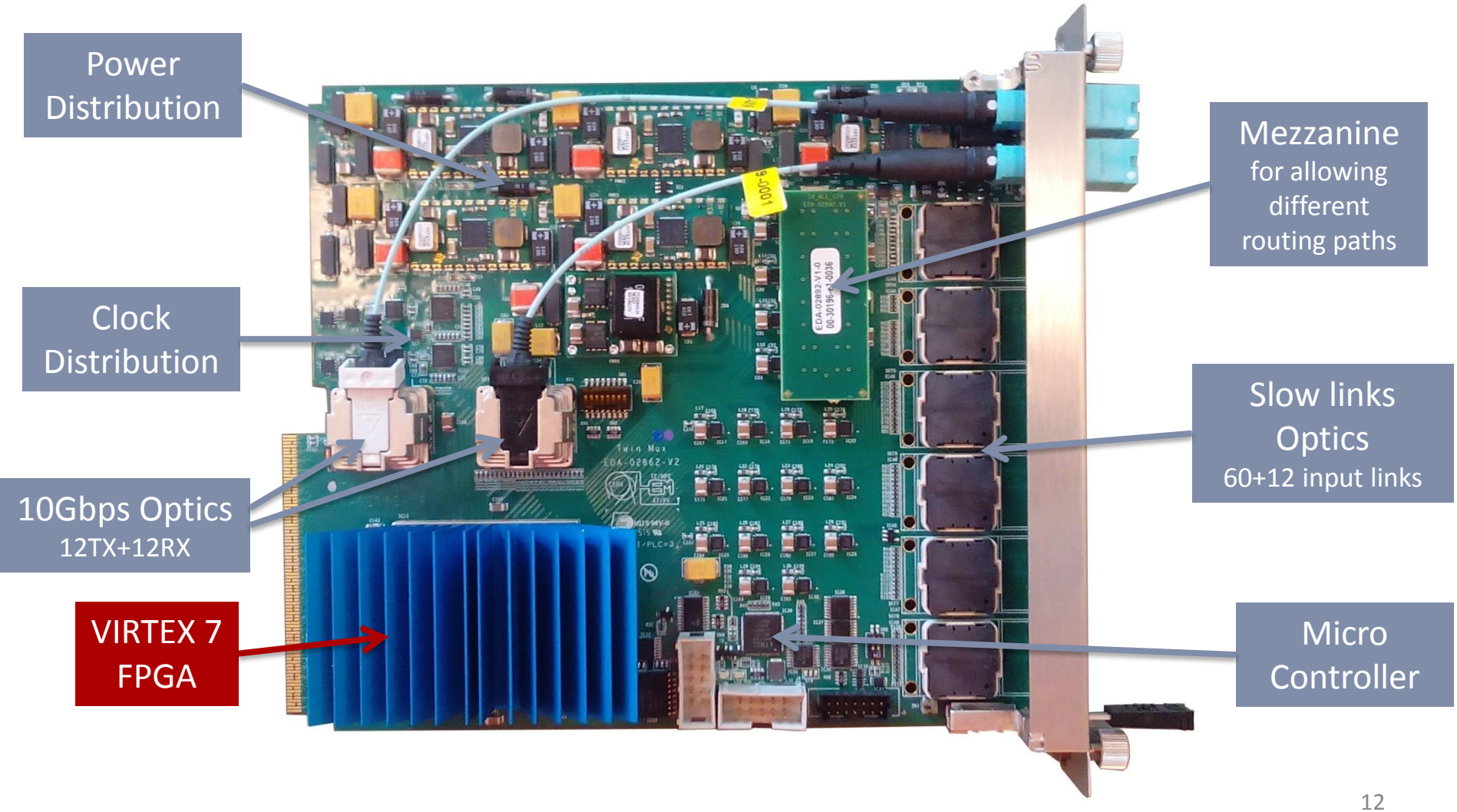
- 12 boards (AMCs) per crate
- Dual star topology
- Power redundancy
- 10GbE, PCIe, sRIO on the backplane
- Clock distribution
- IPMI management control

TwinMux is a trigger data concentrator that merges, arranges and fan-out slow optical links from the front end in faster links (10 Gbps) to the track finders

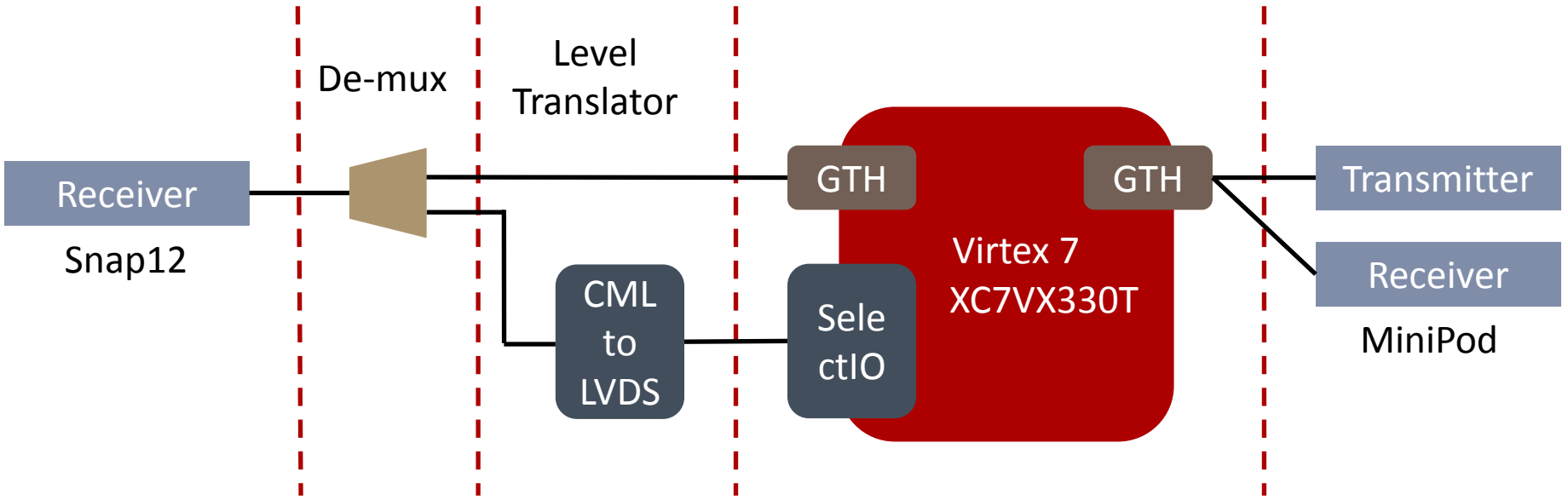




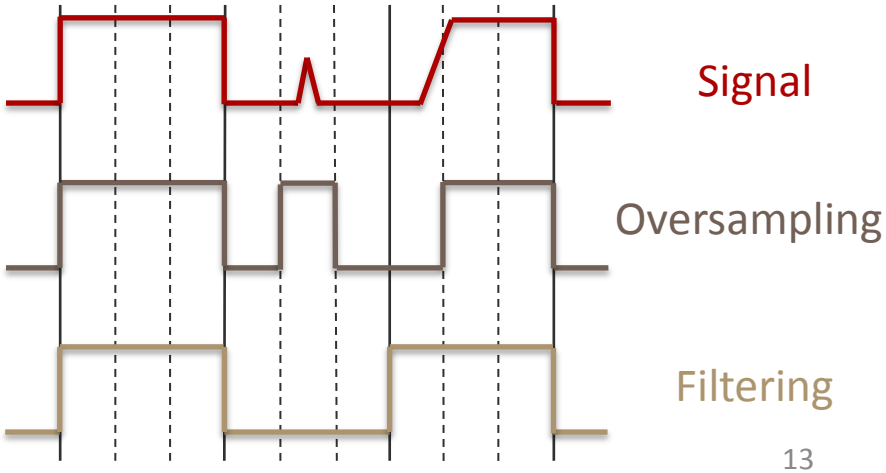
TwinMux Hardware



TwinMux Input

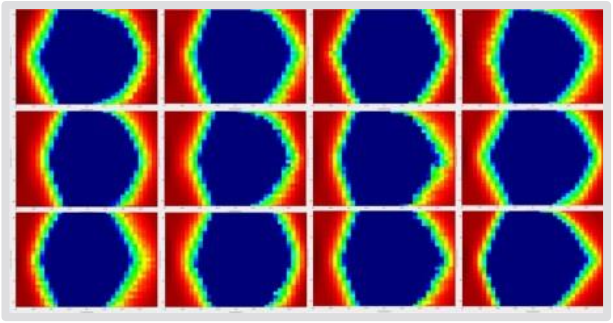


- DC unbalanced optical transmitter in the front end side at 480Mbps
- Virtex 7 SERDES works up to 1.6Gbps
- Oversampling x3 480Mbps → 1.44Gbps
- Digital filter on oversampled data (majority)

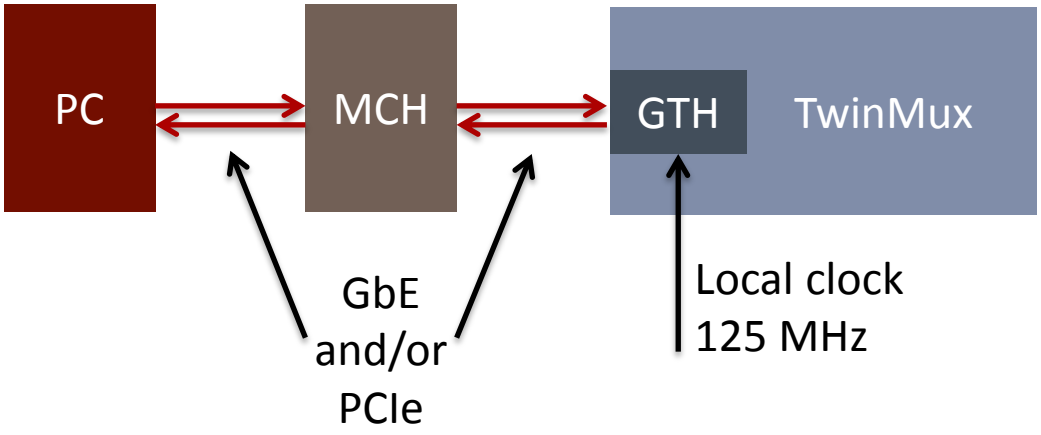


Hardware Validation

- Input/Output
  - Pseudo Random Pattern test on all the input and output lanes
  - No errors up to Bit Error Ratio of 10^{-15}
  - 50-60% eye opening at BER < 10^{-12}



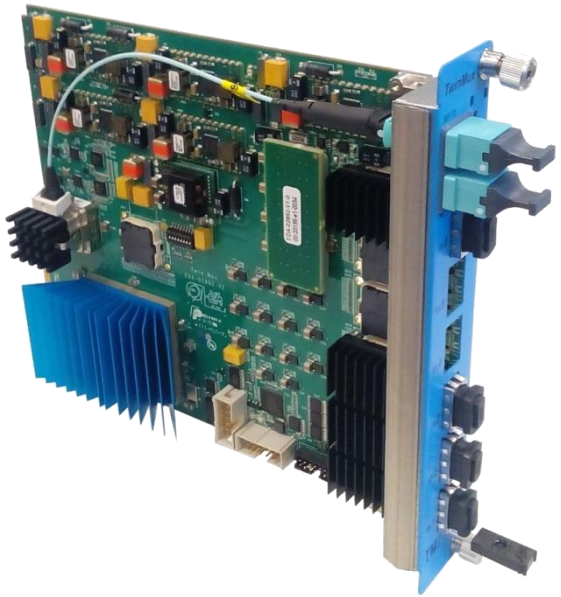
10Gbps Eye Diagrams



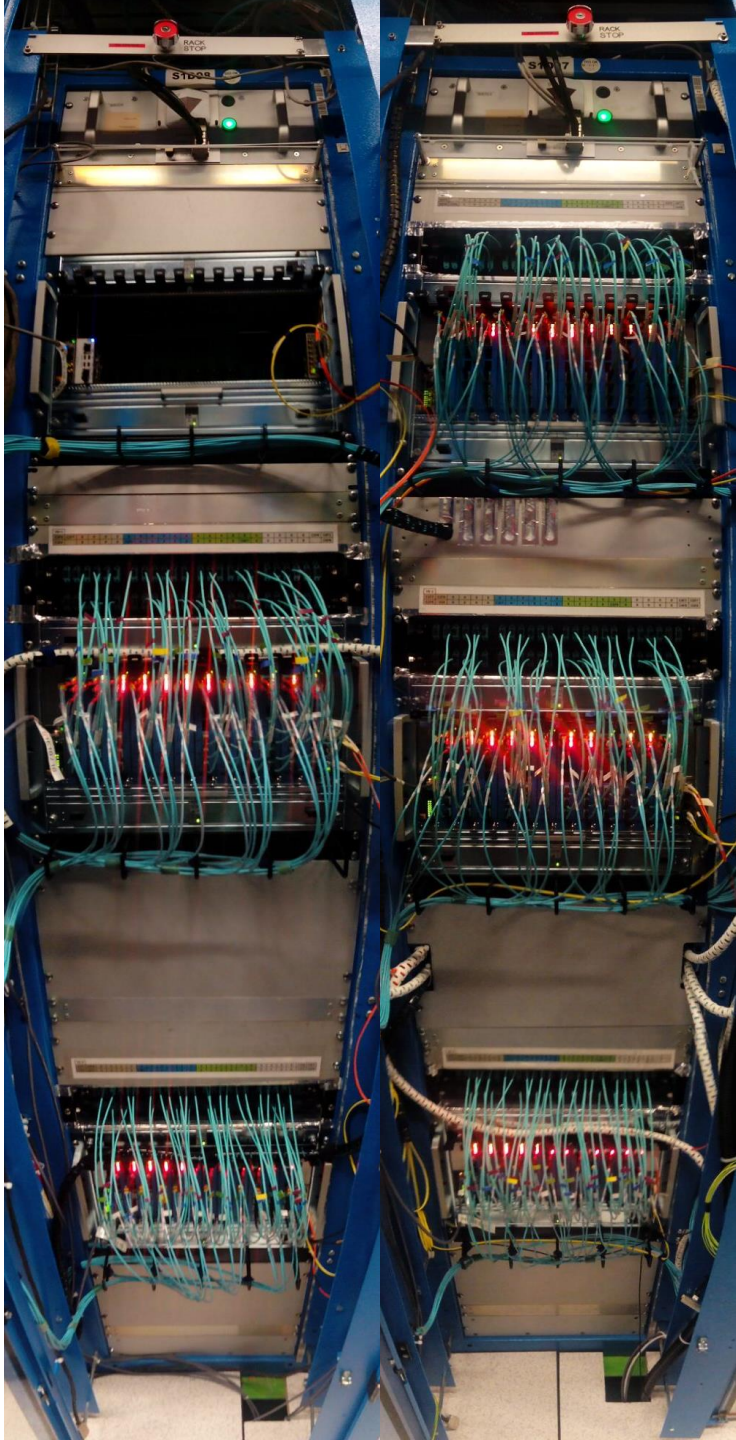
- Slow control & Monitoring
  - IPbus (gigabit Ethernet)
  - PCI Express Gen3 (no backplane clock)

Hardware Production and Installation

- Pre-series: 12 boards
  - No major issues found
  - 6 boards extensively tested in a slice test in parallel with data taking of the legacy system



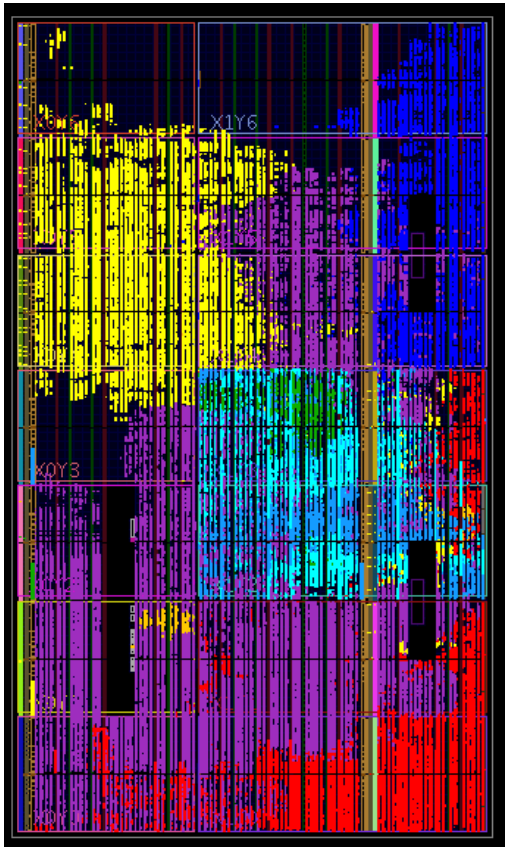
- Final production: 60 boards
  - Installed in 5 crates at the beginning of 2016
  - 2720+720 optical fibers
  - Fully operational in Run2 of CMS



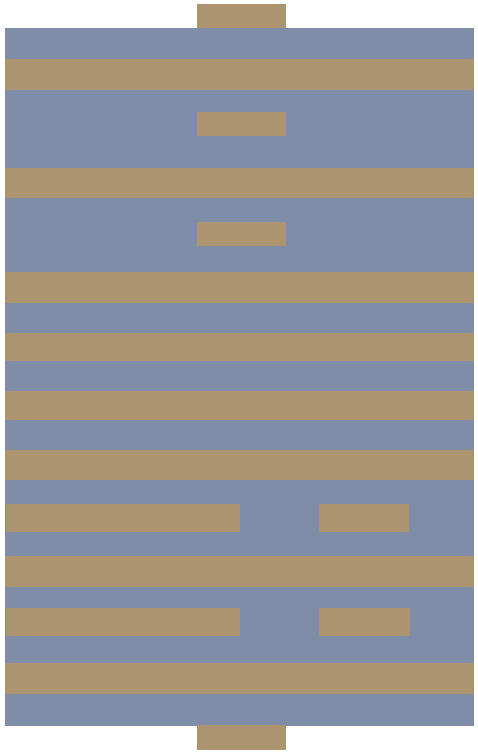
Backup

TwinMux Firmware

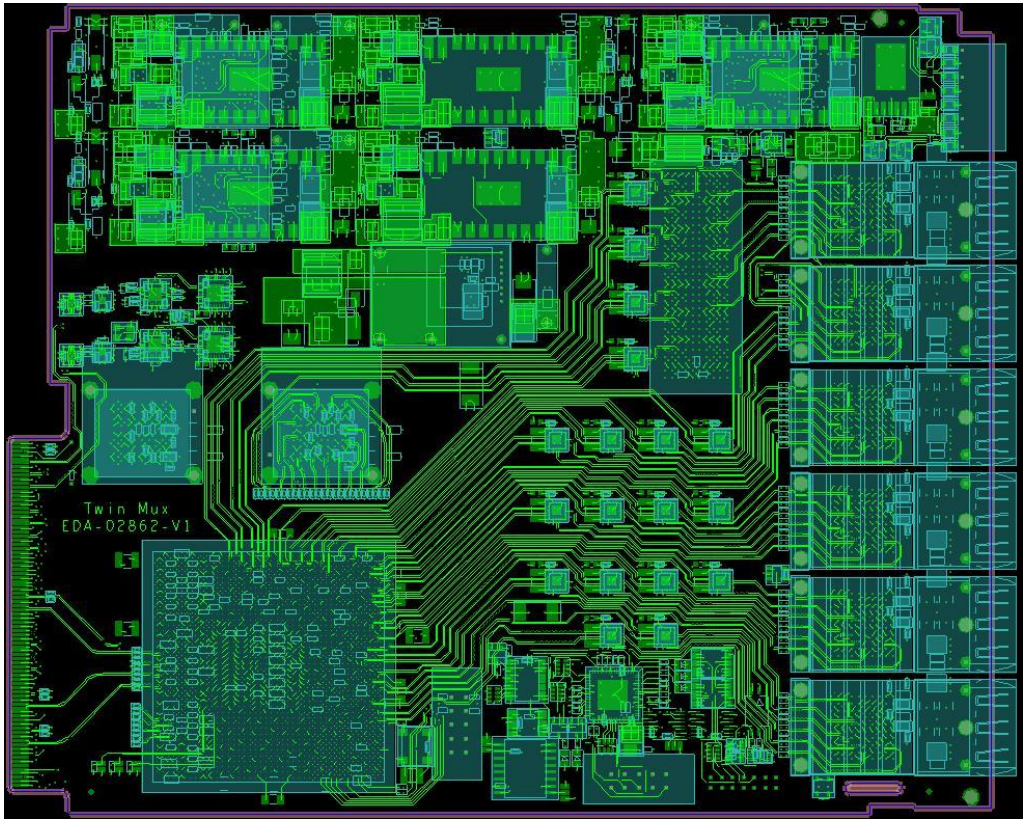
- DT Input
  - 40 input channels (1 sector)
  - Oversampling x3 480Mbps ⟶ 1.44Gbps
  - Digital filter on oversampled data
  - Automatic procedure for link locking
- RPC/HO Input
  - 5 input at 1.6 Gbps synchronous
  - Automatic links synchronization, alignment and monitoring
  - Clustering and coordinate conversion
- Output
  - 10Gbps asynchronous protocol
- Superprimitive
  - Bx-assignment via position-matching
  - Generation of RPC only primitive
- DAQ link
  - It sends to the cDAQ a window of data around a trigger
- Slow control: IPbus (gigabit Ethernet)



Stack-up



Top
Ground
GTH_1
Ground
GTH_2
Ground
Power
Power
Power
Split_1
Power
Split_2
Ground
Bottom



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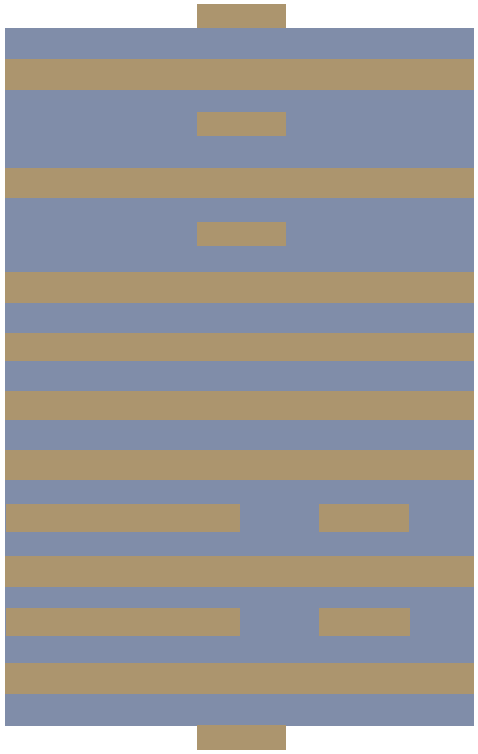
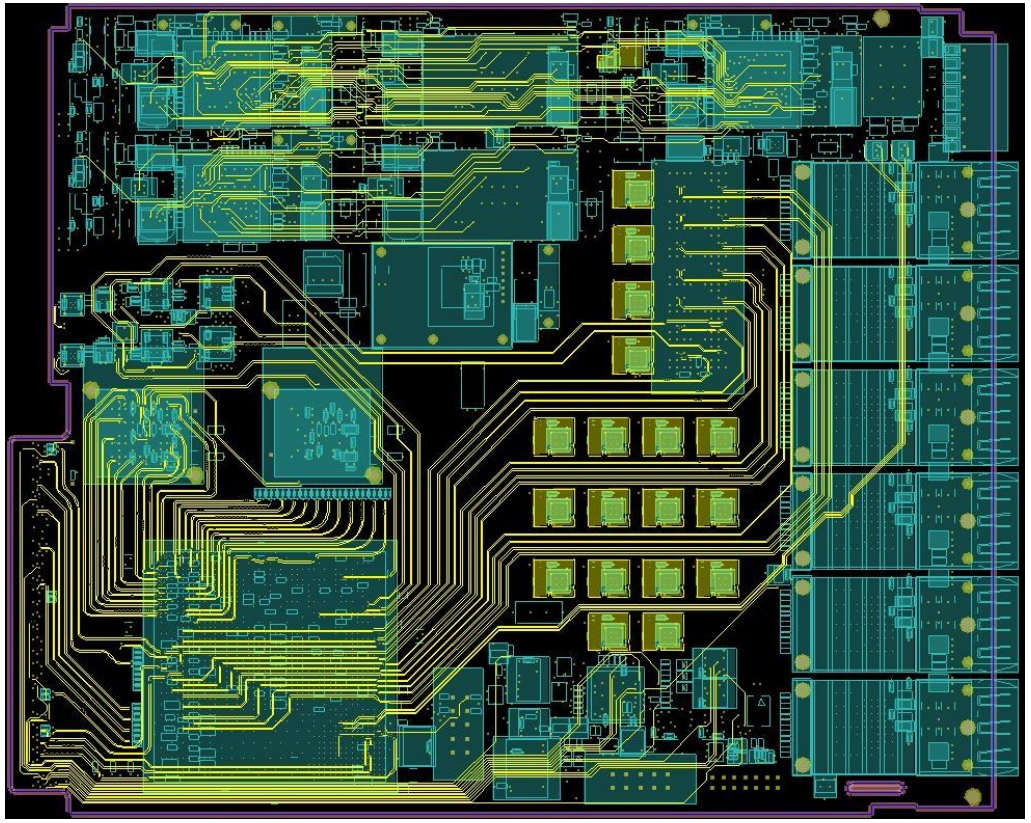


Top
Ground
GTH_1
Ground
GTH_2
Ground
Power
Power
Power
Split_1
Power
Split_2
Ground
Bottom



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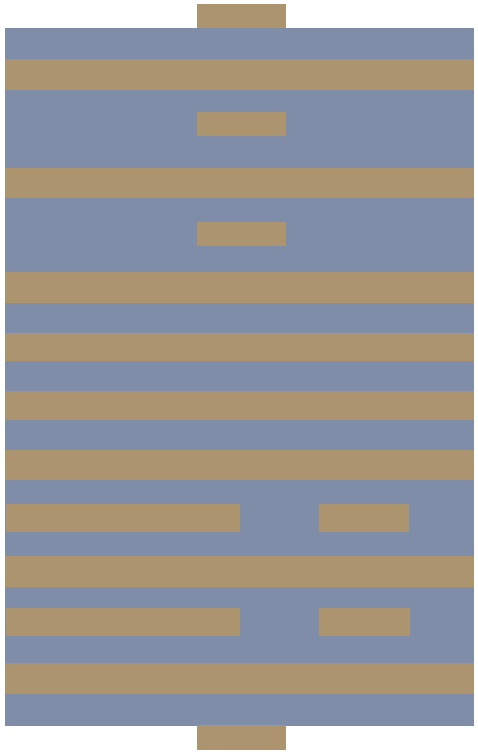
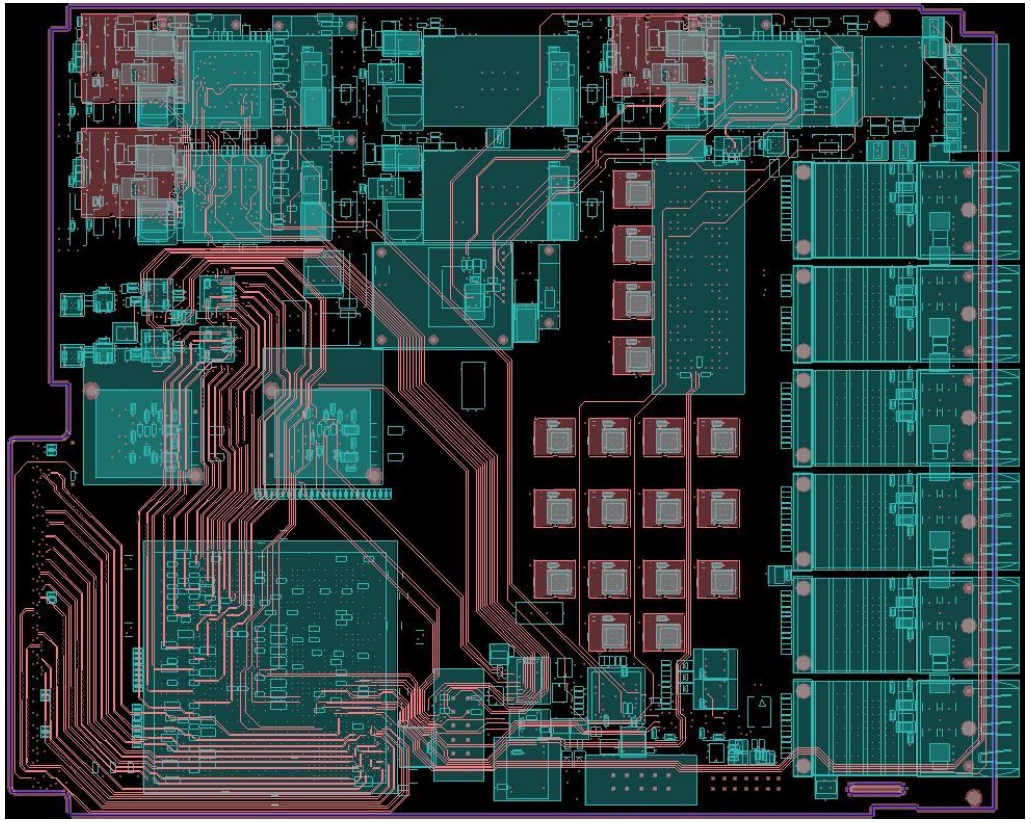


- Top
- Ground
- GTH_1
- Ground
- **GTH_2**
- Ground
- Power
- Power
- Power
- Split_1
- Power
- Split_2
- Ground
- Bottom



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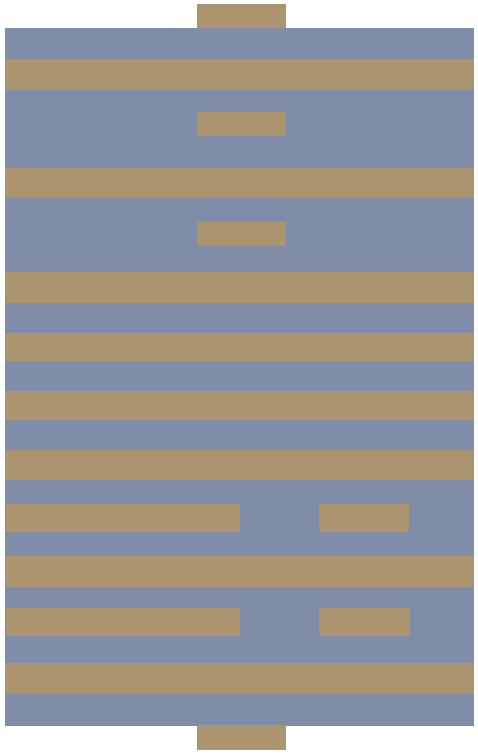
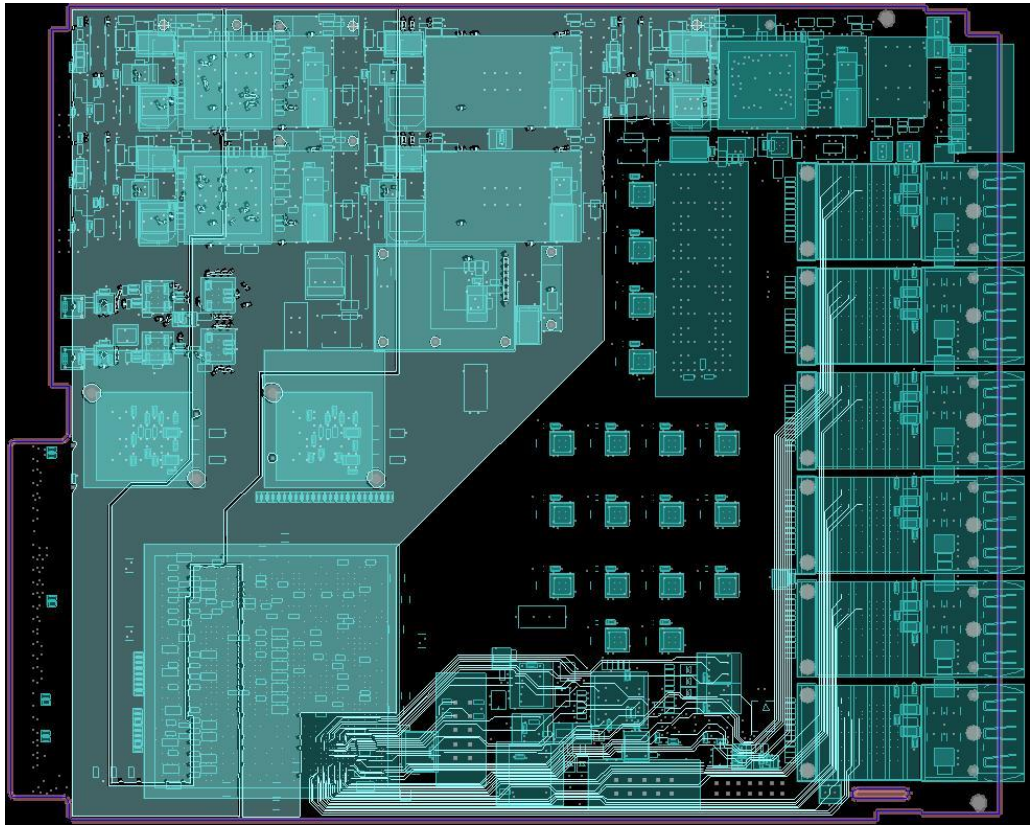


Top
Ground
GTH_1
Ground
GTH_2
Ground
Power
Power
Power
Split_1
Power
Split_2
Ground
Bottom



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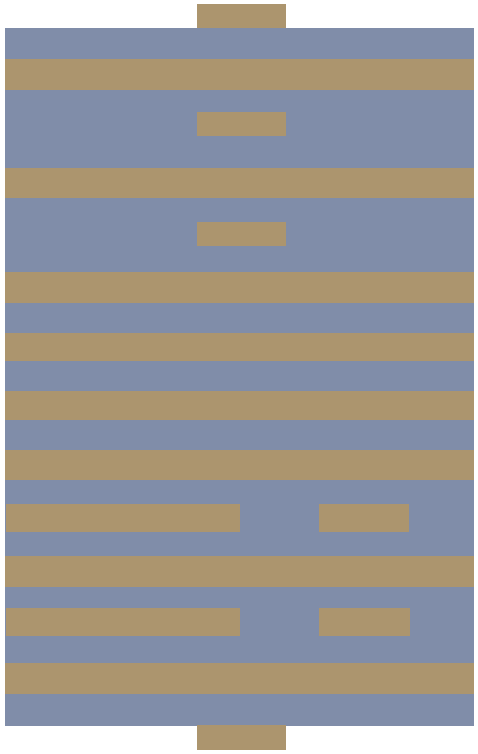

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Ground
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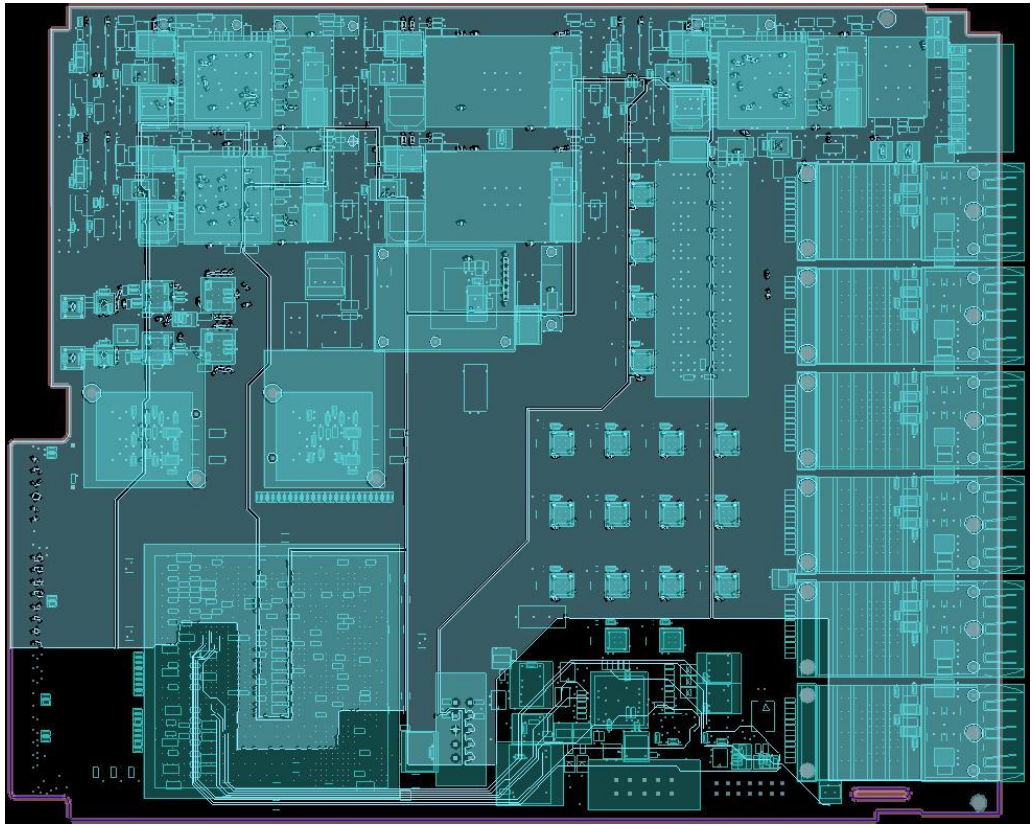

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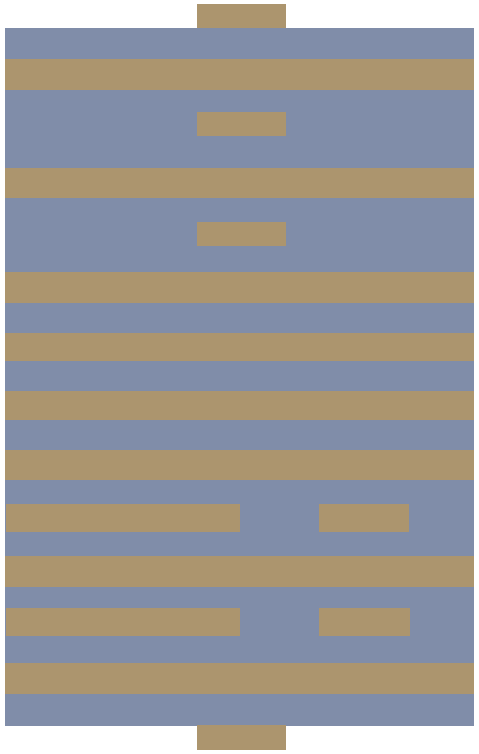

Top
Ground
GTH_1
Ground
GTH_2
Ground
Power
Power
Power
Split_1
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Split_2
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