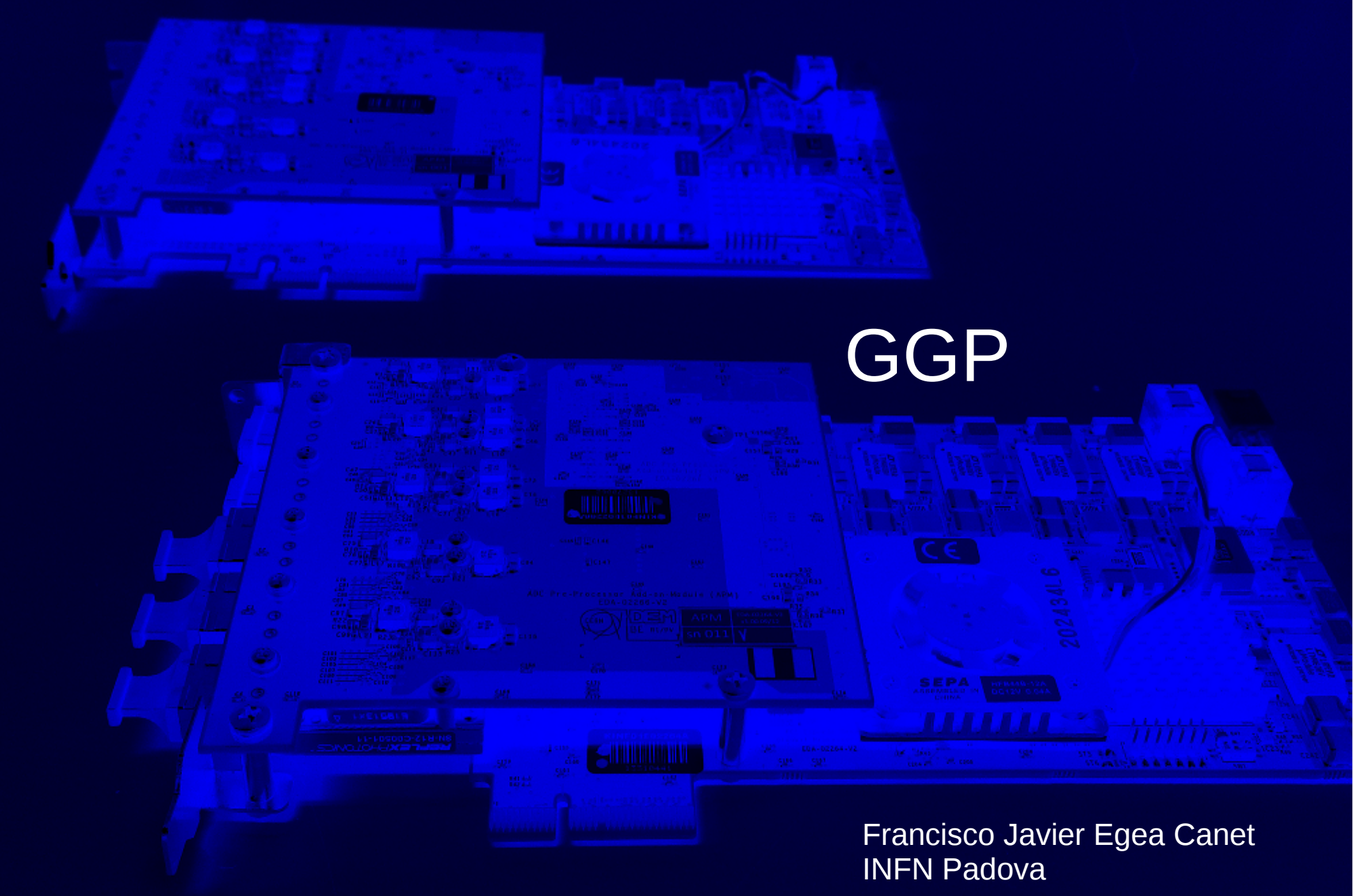

GGP

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INFN Padova

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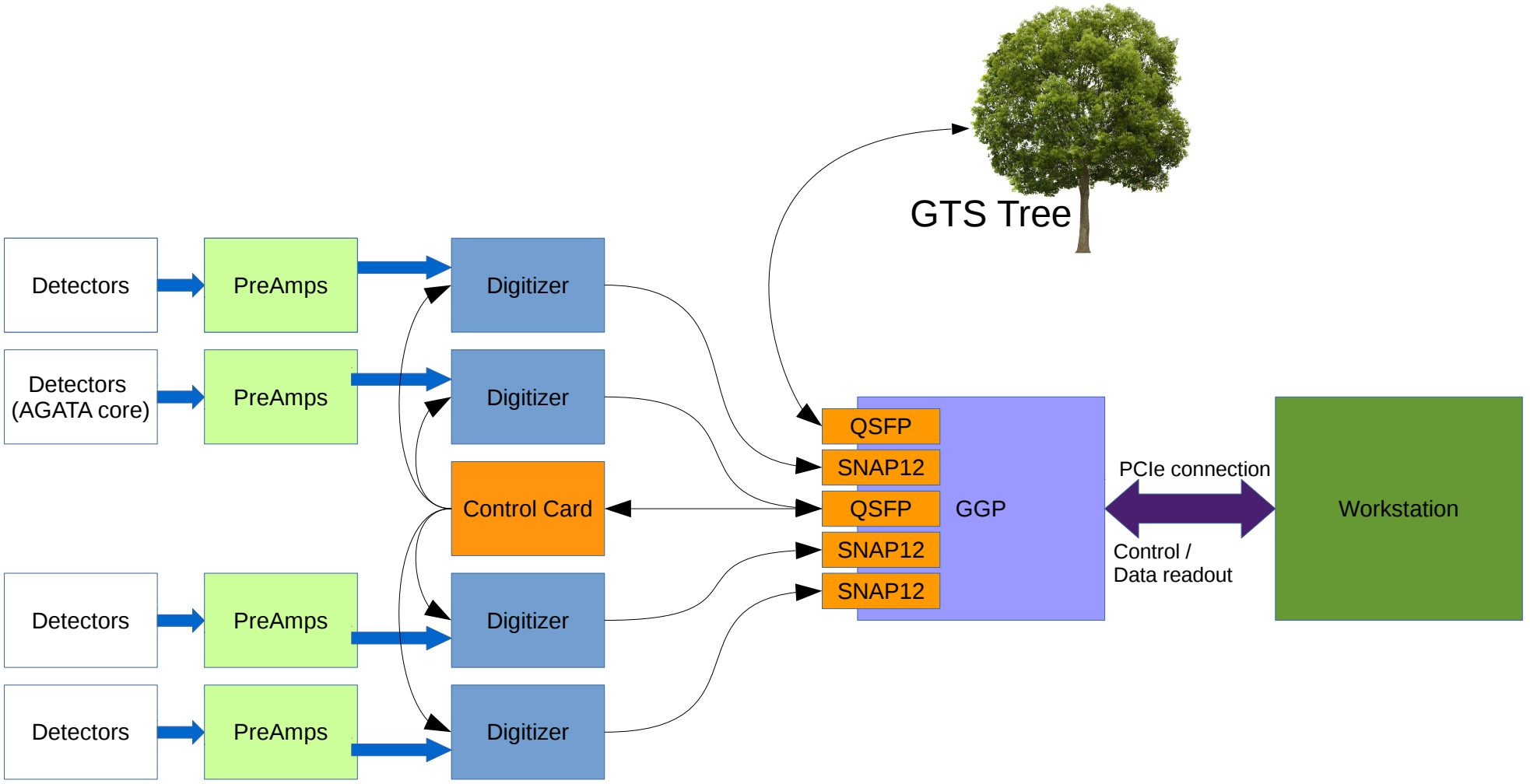
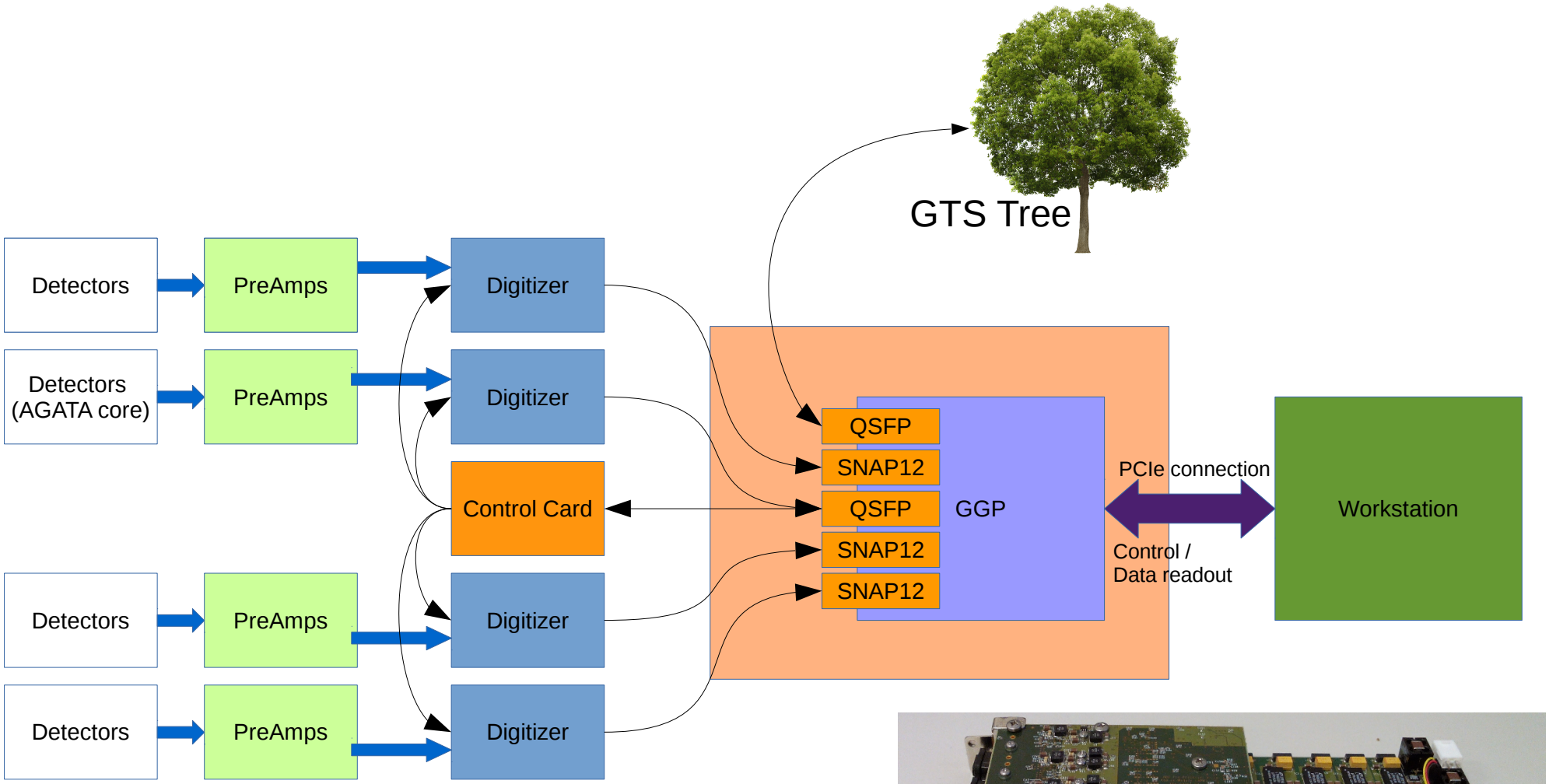
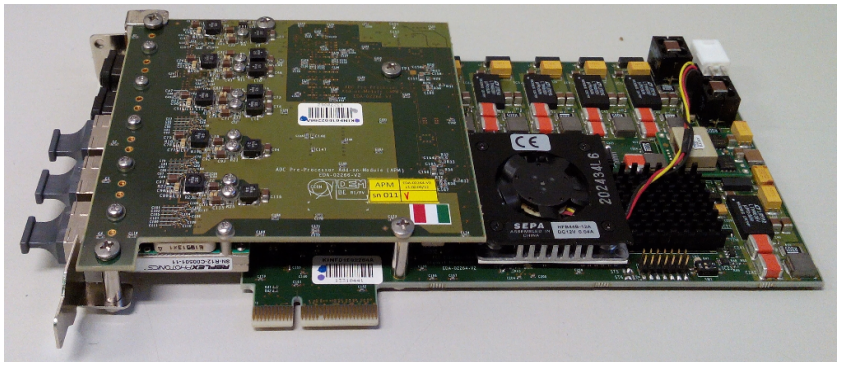
- GALILEO / AGATA Hardware and global electronics layout
- GGP Firmware block diagram
- Recent improvements in the GGP firmware
- IPBUS and GTS
- Status, improvements and TODO list

Global Electronics



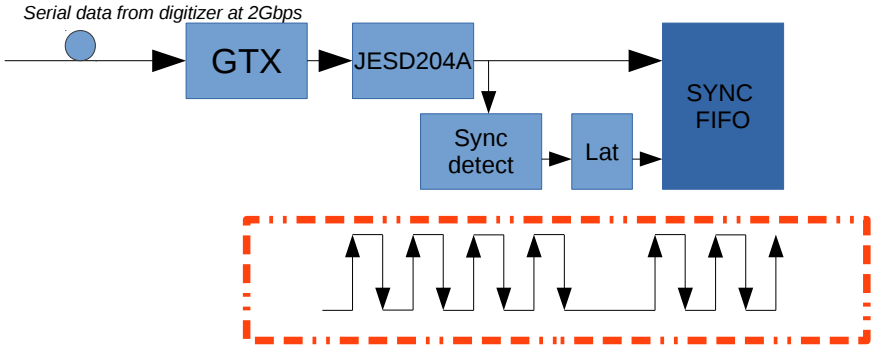
Global Electronics



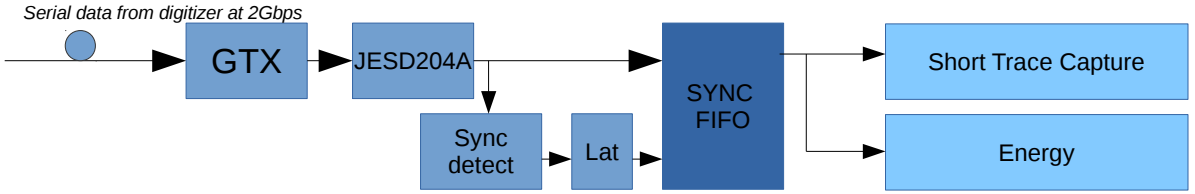


GGP Firmware

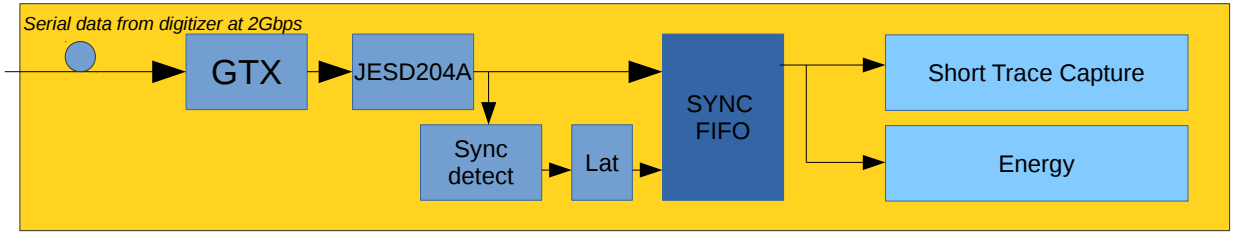
- *Data Reception from the ADCs*
- *100 MHz @ 14 bits per channel*
- *JESD204A ensures the data link protocol*



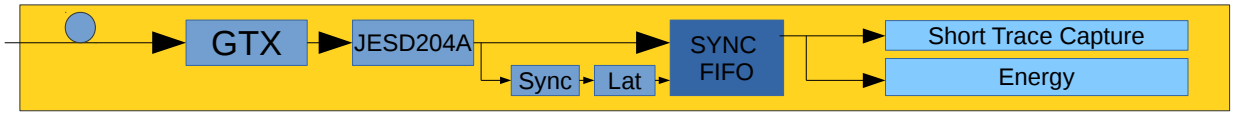
- *A switching pattern is sent to all ADCs.*
- *The pattern is digitized and sent back in order to detect the missing cycle.*
- *Detection of a syncrhonization pattern in order to align the channel-to-channel variations*



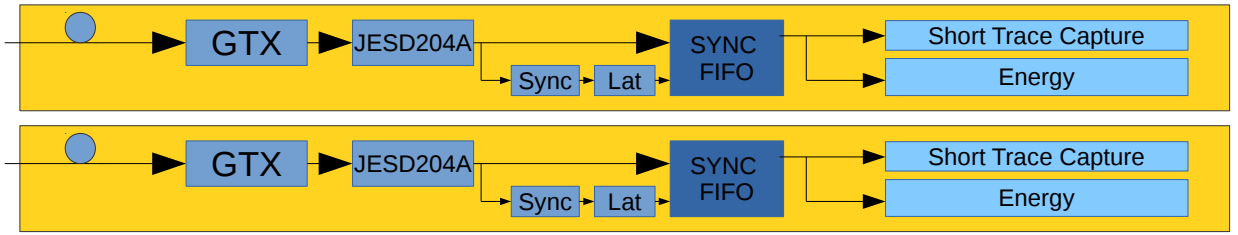
- *A set of 100 samples is stored every time a trigger occurs with some pre-trigger samples*
- *The energy comes after aplying a MWD and a trapezoidal filter (Shaping time)*



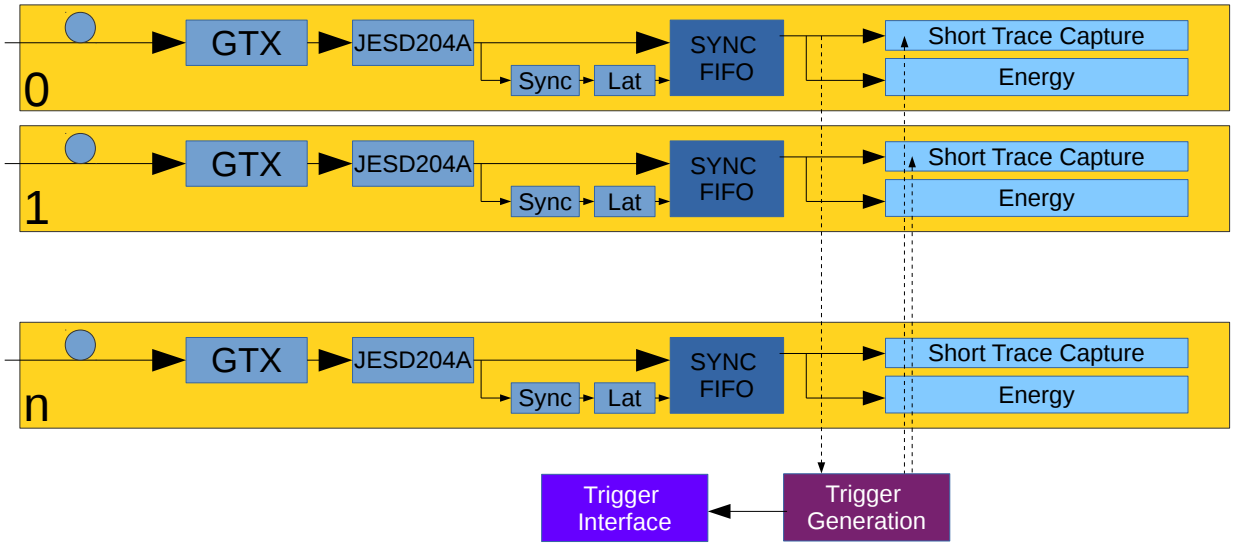
- *The logics involved in the deserialization, link stablishment, synchronization, trace capture and energy fits the functionality of a CHANNEL*



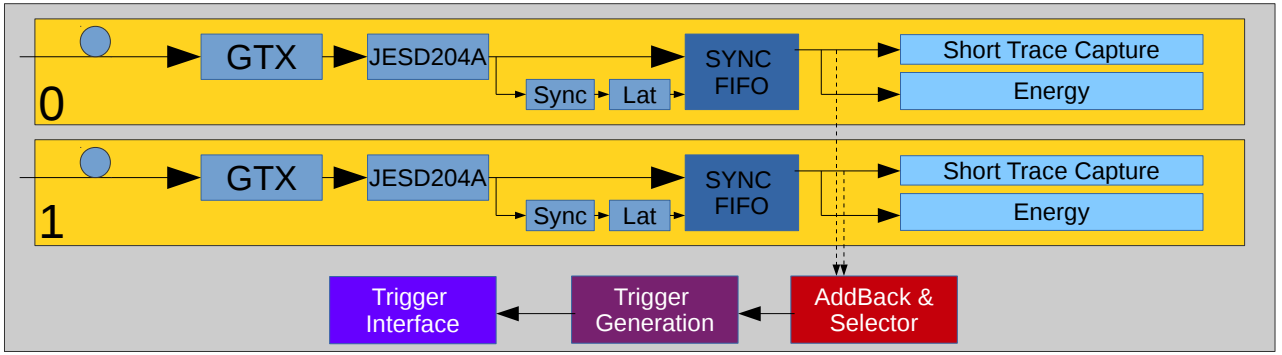
- *Let's fit it in a smaller space...*



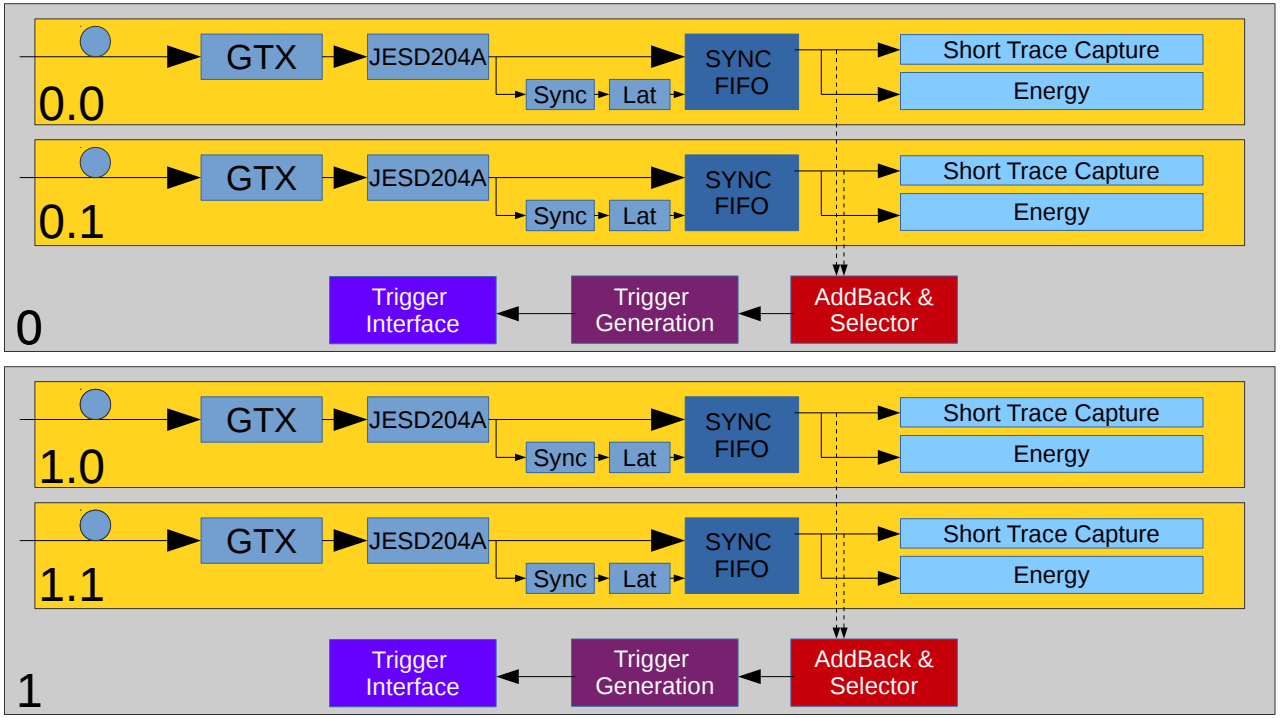
- *Obviously, the firmware can take more than a single channel...*



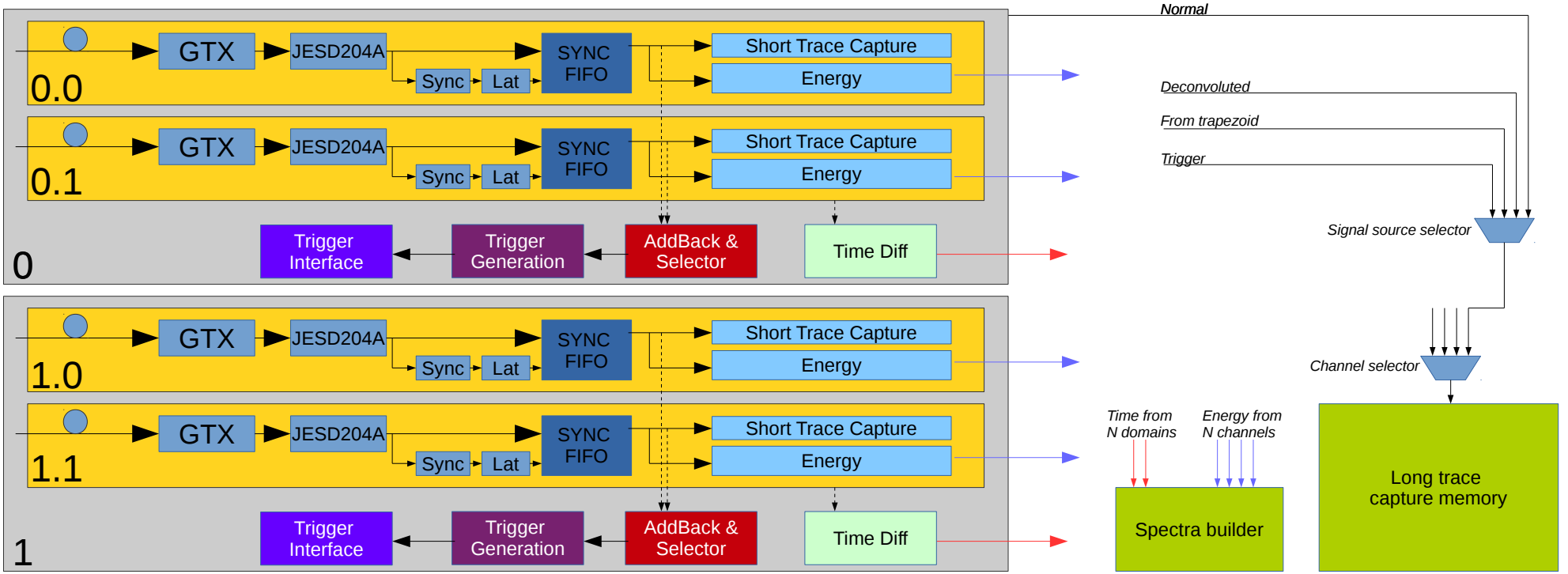
- *A pre-selected channel will generate the trigger request, using a small tringular shaper and a threshold*
- *Also, a trigger interface handles the requests to the GTS leaf*



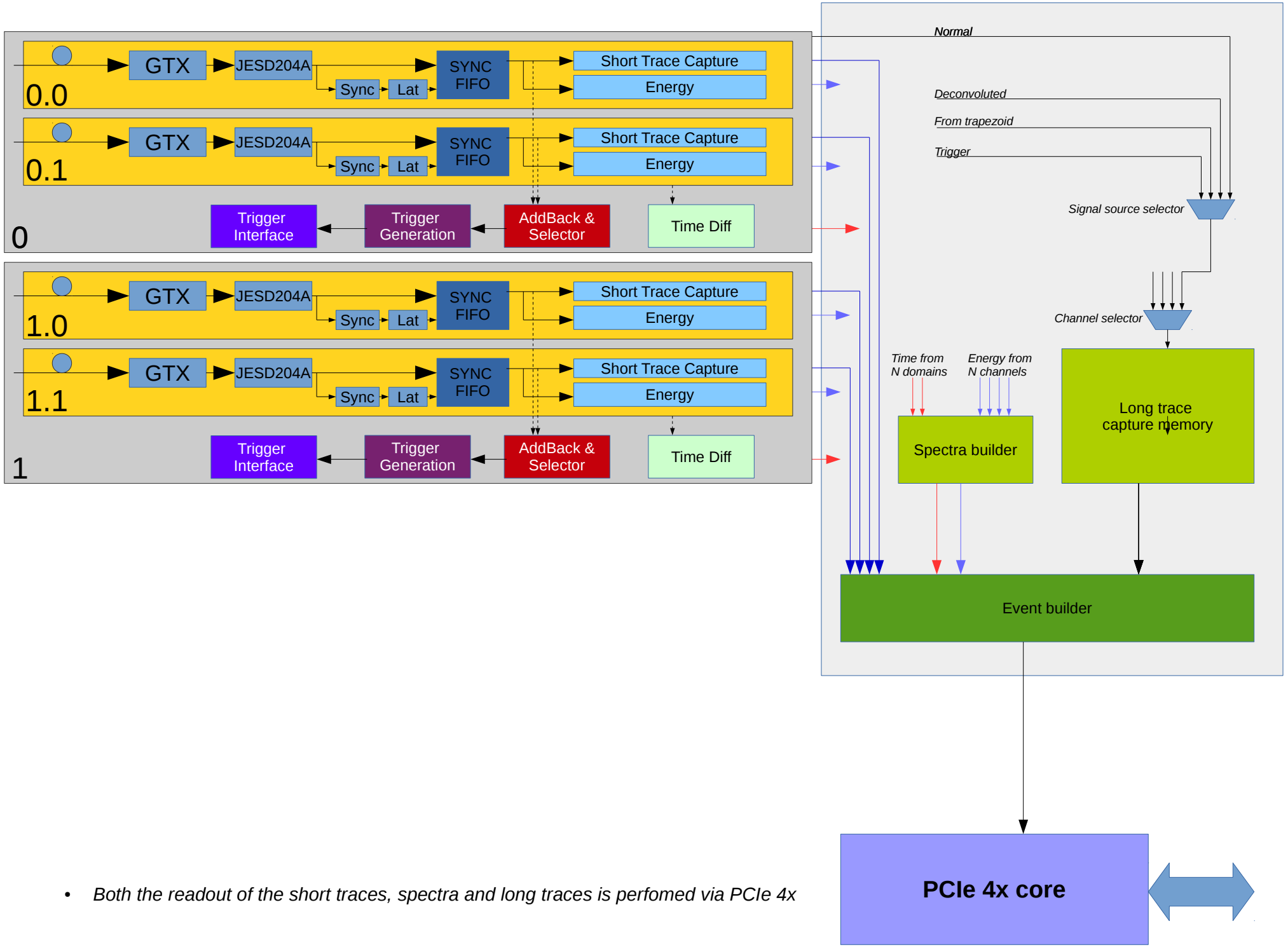
- *A group of channels plus the trigger logic is gathered in a DOMAIN.*
  - *GALILEO and EUCLIDES use domains with 2 channels*
  - *AGATA does the same with 38 channels*



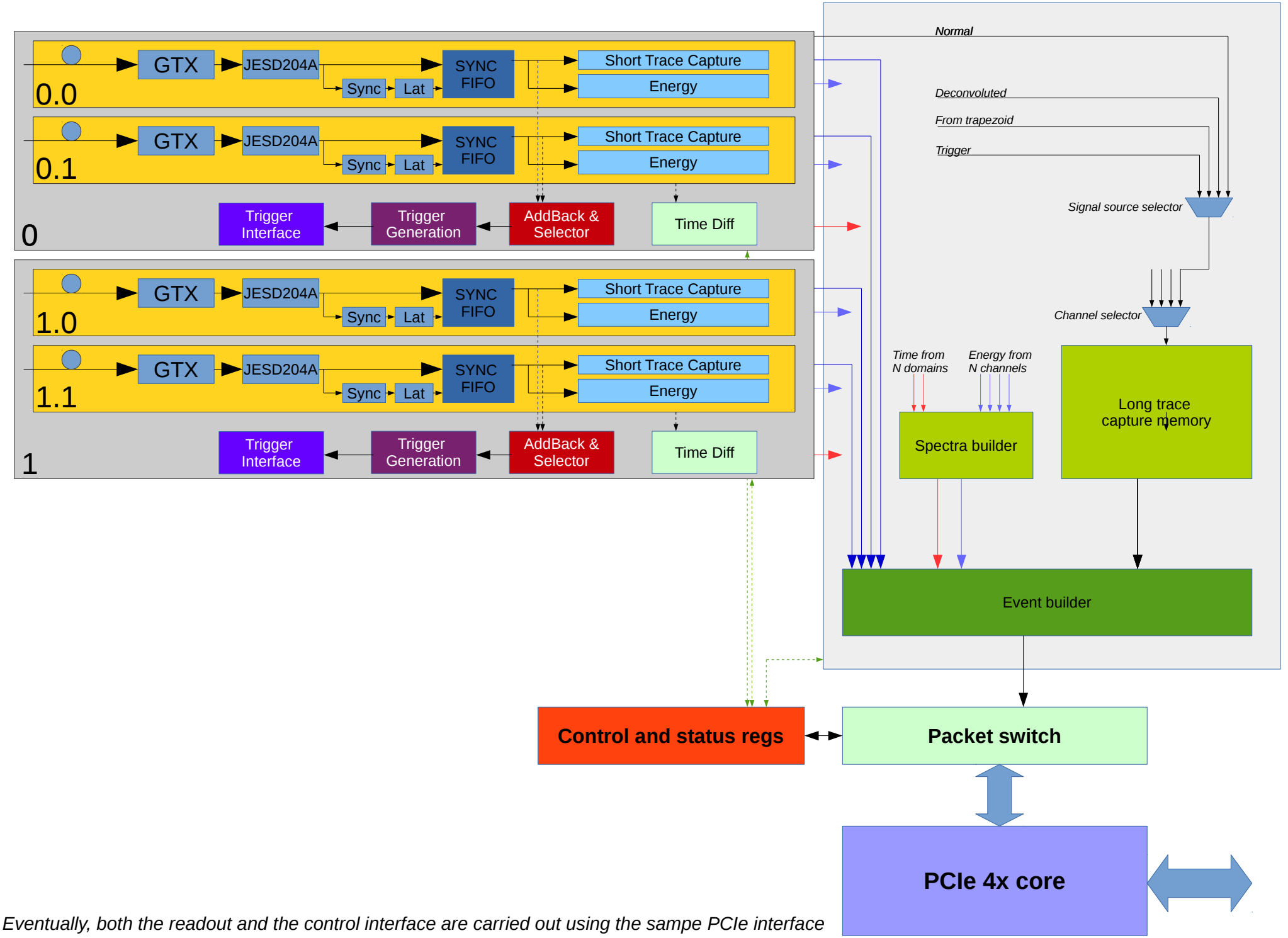
- *And in the same way, the FPGA can fit several domains...*



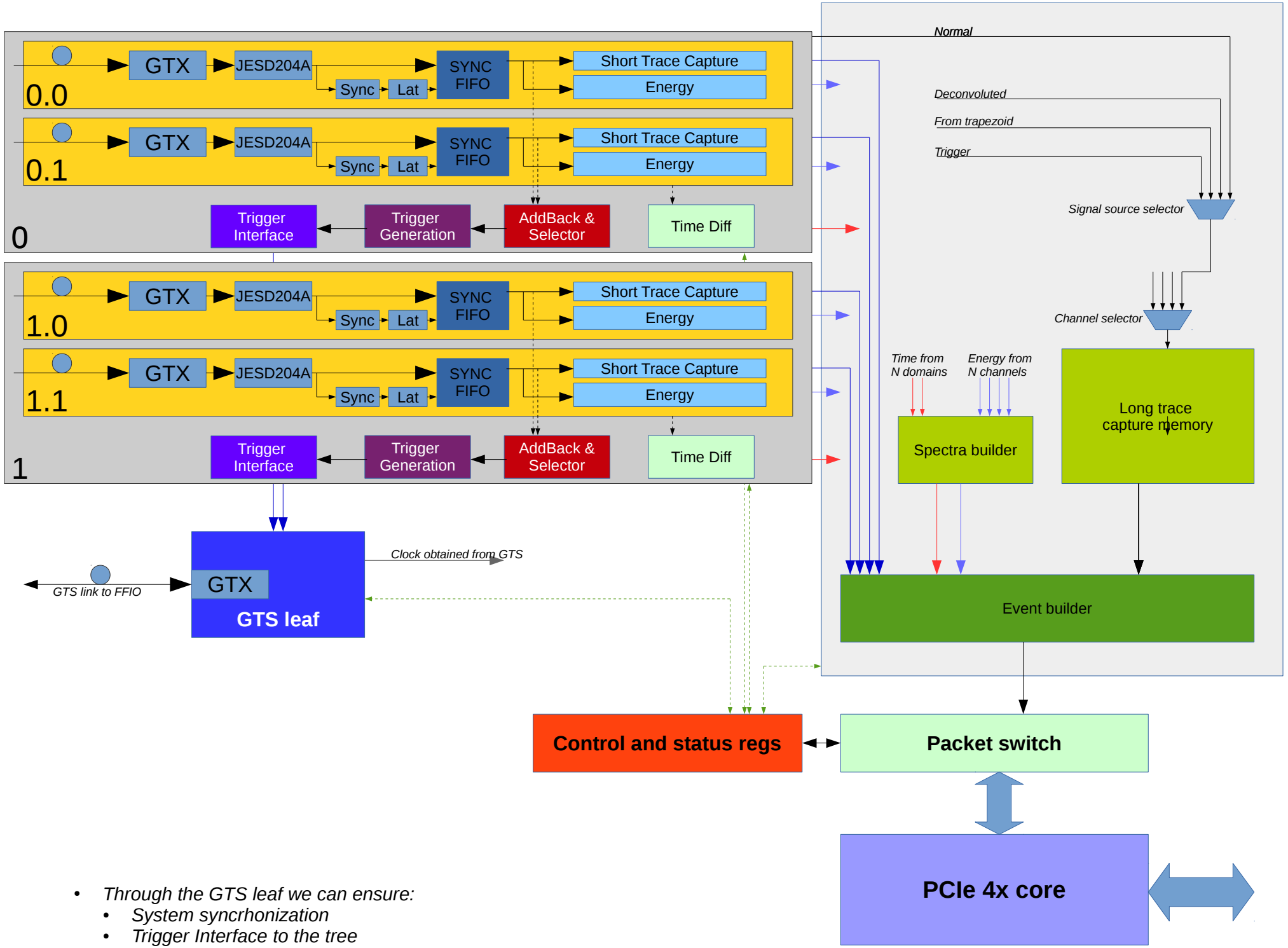
- *A large memory allows the capture of 100.000 samples for analysis*
- *Also, it is possible to get online energy spectra for all channels and time difference spectra in all domains*



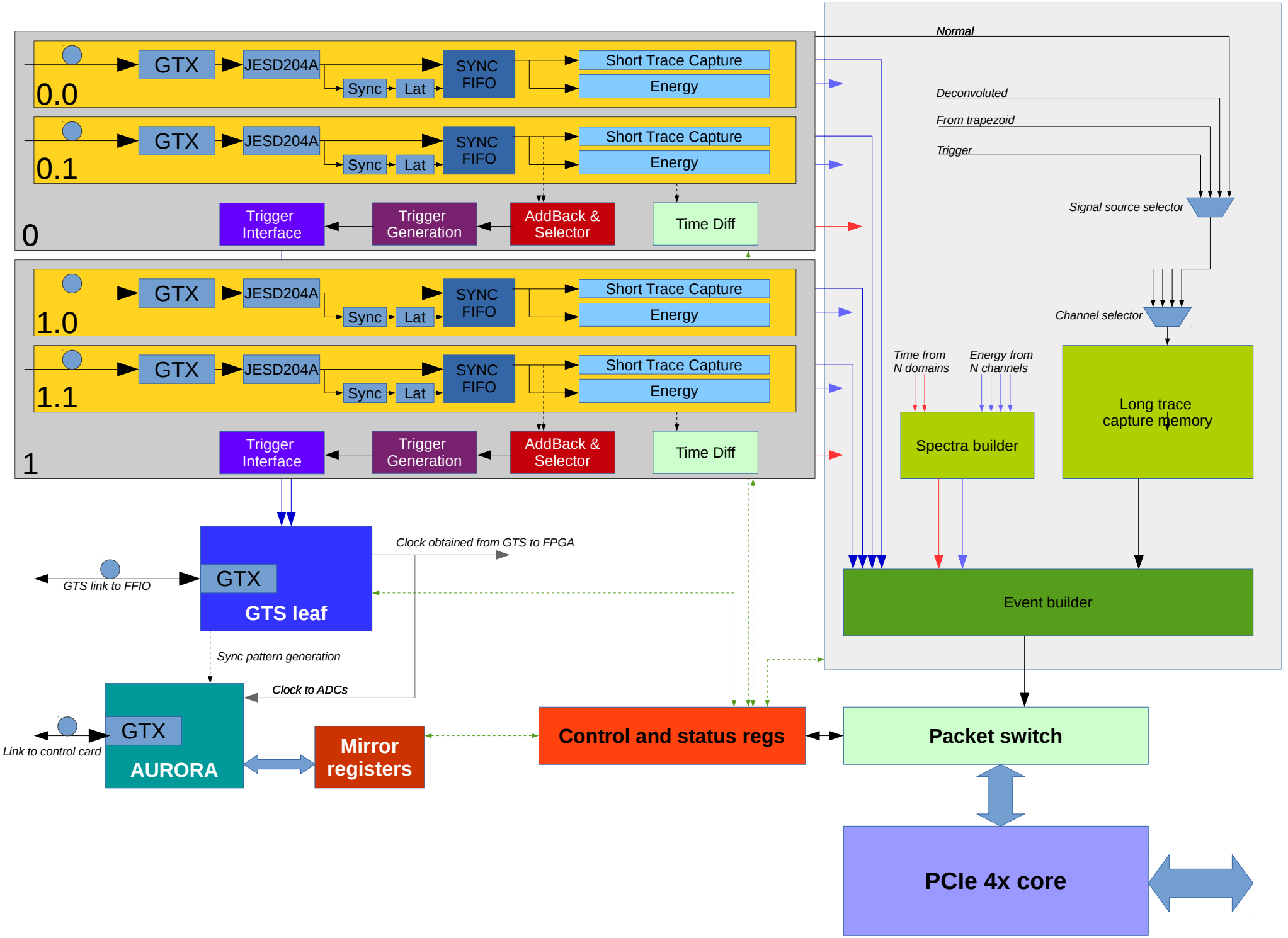
- *Both the readout of the short traces, spectra and long traces is perfomed via PCIe 4x*

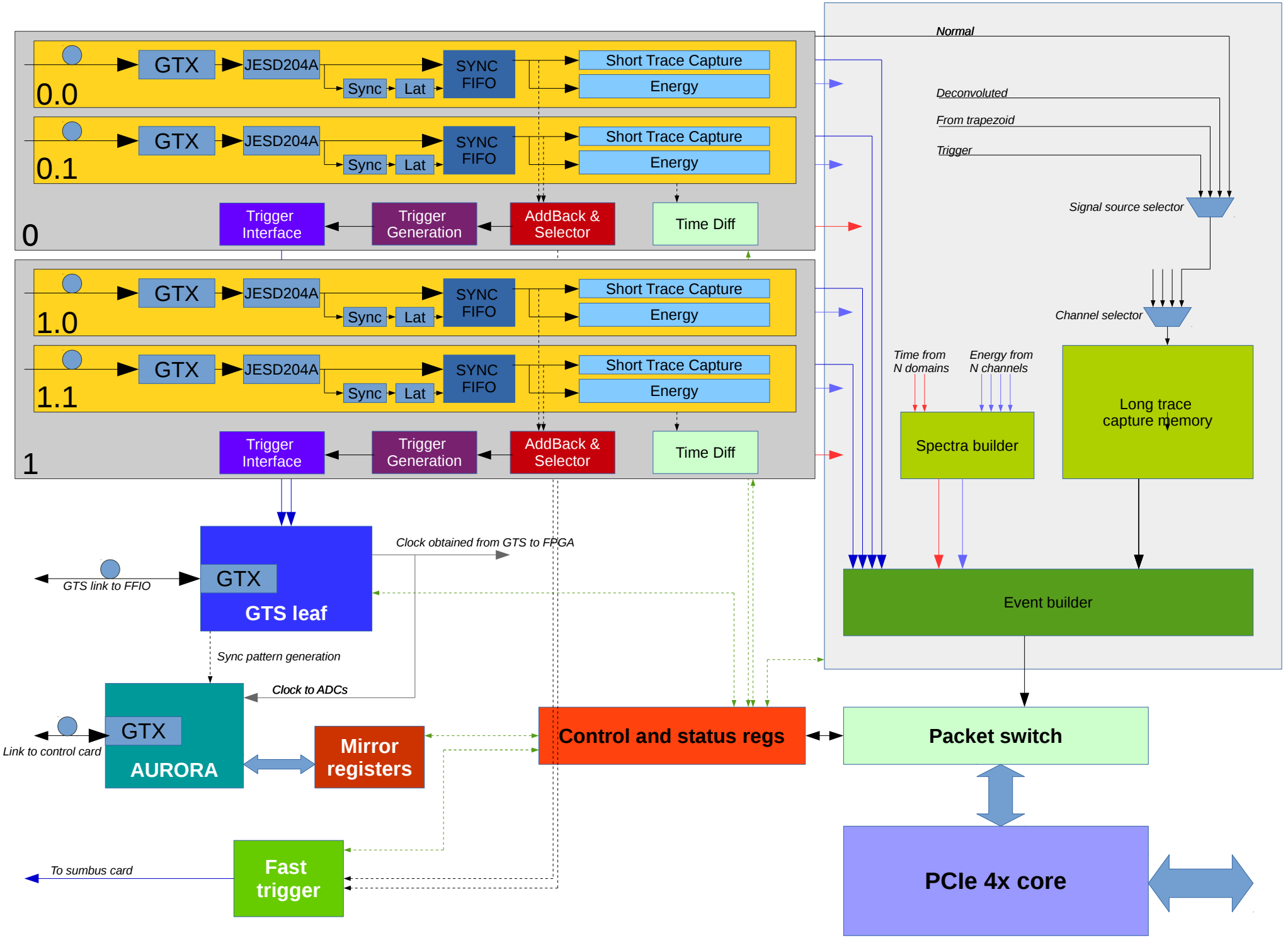


- *Eventually, both the readout and the control interface are carried out using the sampe PCIe interface*



- *Through the GTS leaf we can ensure:*
  - *System syncrhonization*
  - *Trigger Interface to the tree*
  - *Same timestamp in all nodes inside the tree*


0.0
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
0.1
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
0
Trigger Interface
Trigger Generation
AddBack & Selector
Time Diff
1.0
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
1.1
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
1
Trigger Interface
Trigger Generation
AddBack & Selector
Time Diff
Normal
Deconvoluted
From trapezoid
Trigger
Signal source selector
Channel selector
Time from N domains
Energy from N channels
Spectra builder
Long trace capture memory
Event builder
GTS link to FFIO
GTX
GTS leaf
Clock obtained from GTS to FPGA
Sync pattern generation
Clock to ADCs
Link to control card
GTX
AURORA
Mirror registers
Control and status regs
Packet switch
PCIe 4x core


0.0
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
0.1
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
0
Trigger Interface
Trigger Generation
AddBack & Selector
Time Diff
1.0
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
1.1
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
1
Trigger Interface
Trigger Generation
AddBack & Selector
Time Diff
Normal
Deconvoluted
From trapezoid
Trigger
Signal source selector
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Time from N domains
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Spectra builder
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GTX
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Mirror registers
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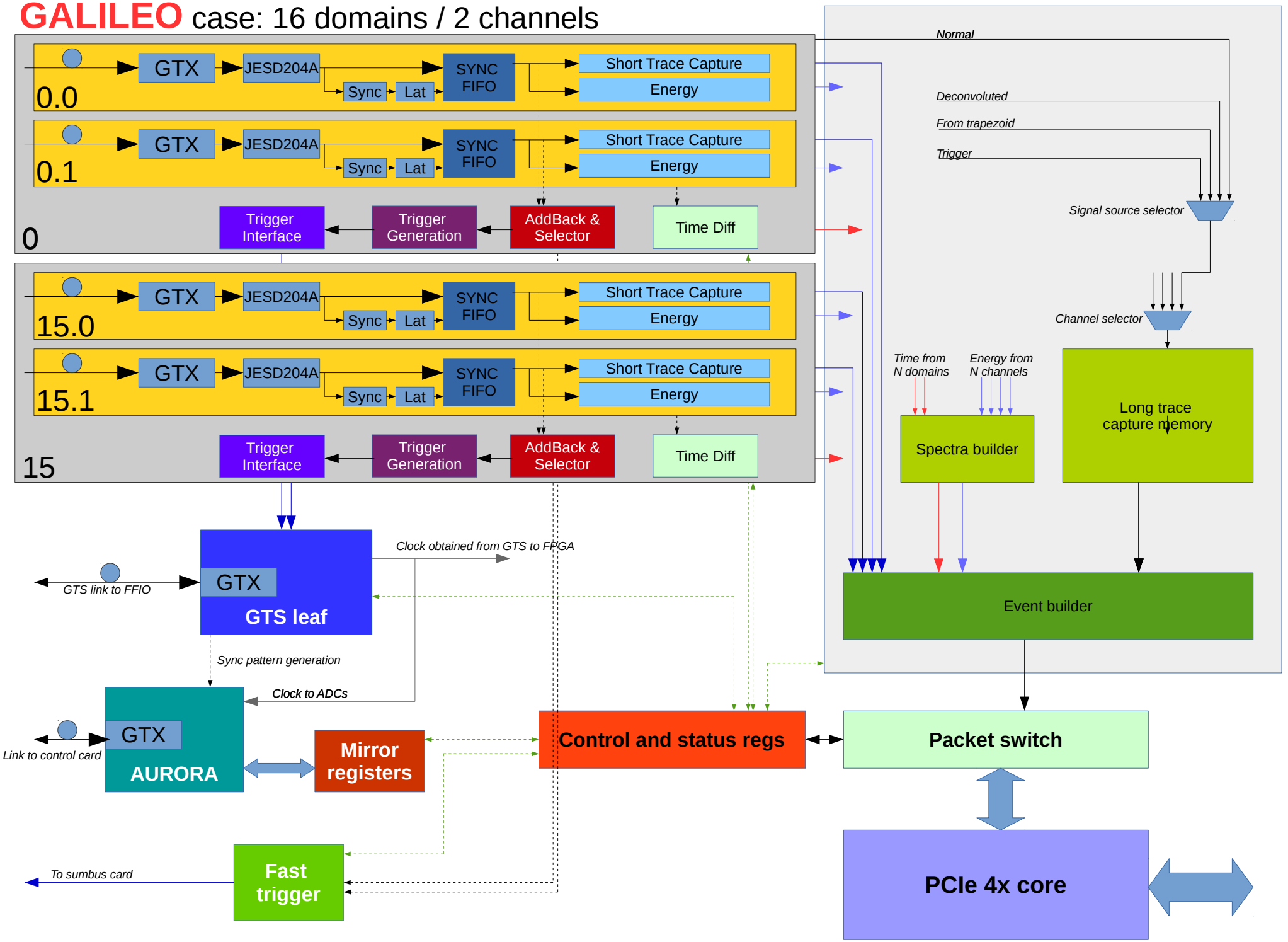
To sumbus card
Fast trigger
PCIe 4x core


GALILEO case: 16 domains / 2 channels
0.0
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
0.1
0
Trigger Interface
Trigger Generation
AddBack & Selector
Time Diff
15.0
15.1
15
Normal
Deconvoluted
From trapezoid
Trigger
Signal source selector
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Time from N domains
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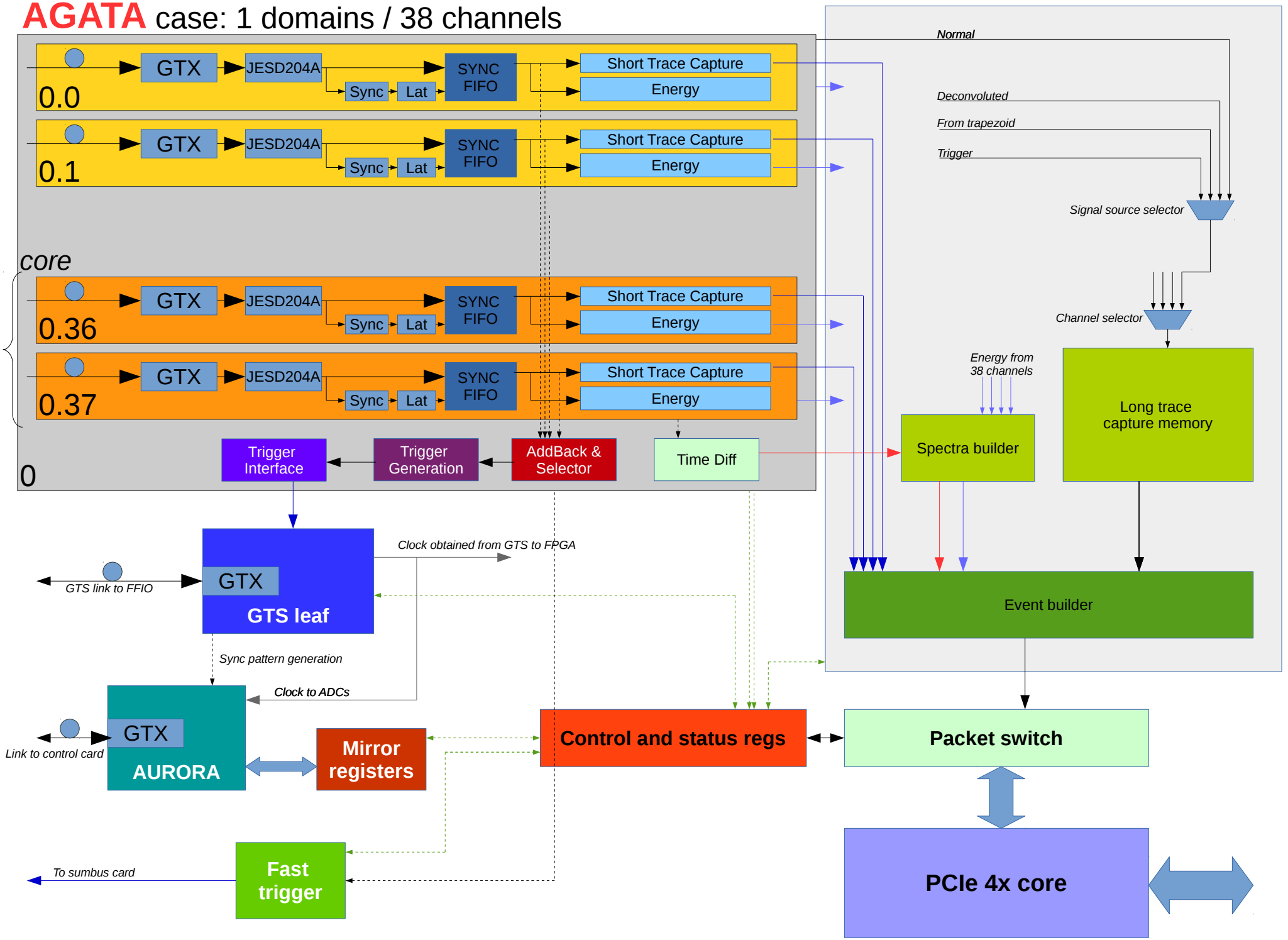
AGATA case: 1 domains / 38 channels
core
0
0.0
0.1
0.36
0.37
GTX
JESD204A
Sync
Lat
SYNC FIFO
Short Trace Capture
Energy
Trigger Interface
Trigger Generation
AddBack & Selector
Time Diff
Normal
Deconvoluted
From trapezoid
Trigger
Signal source selector
Channel selector
Energy from 38 channels
Spectra builder
Long trace capture memory
Event builder
GTS link to FFIO
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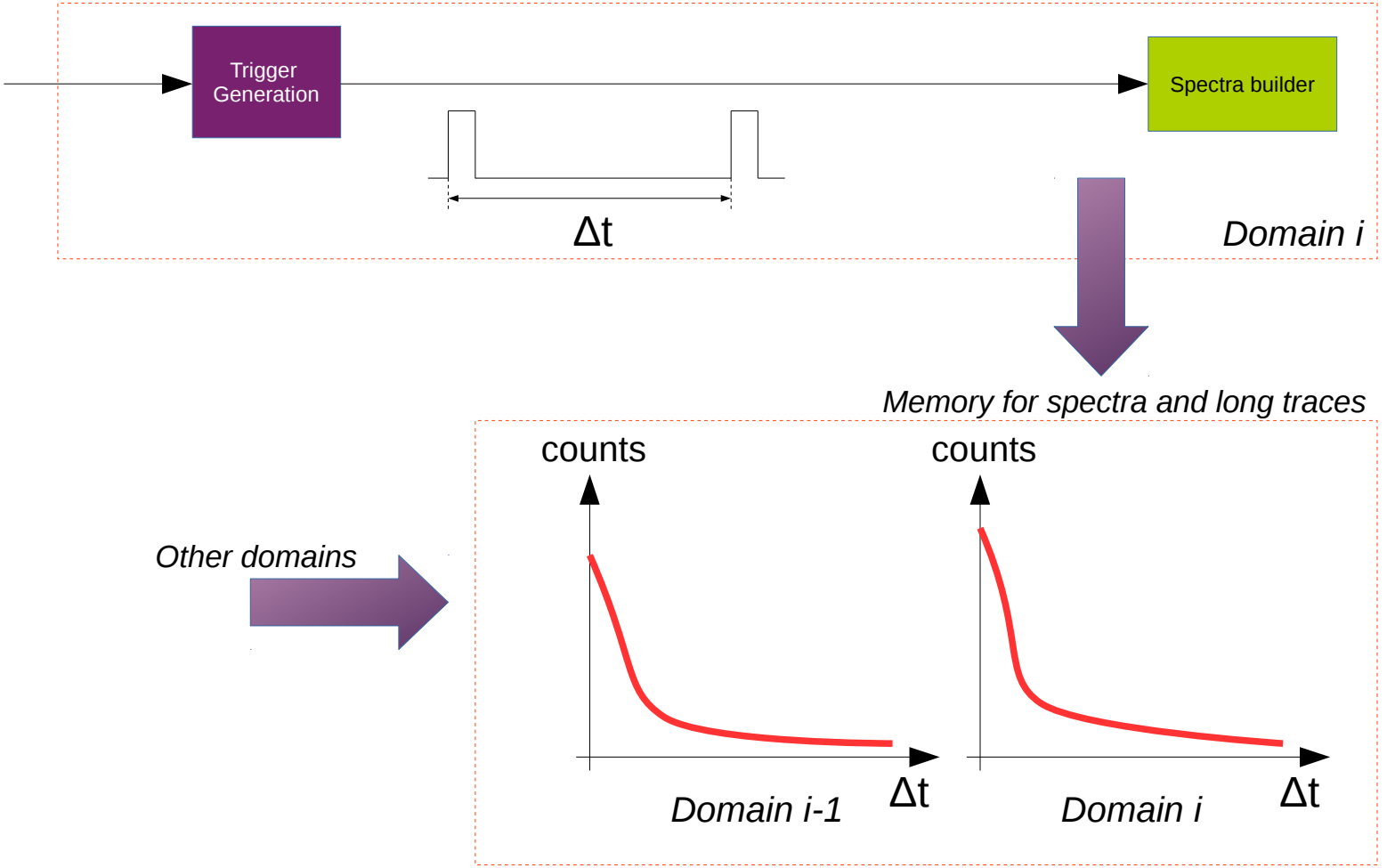
Link to control card
AURORA
Mirror registers
Control and status regs
Packet switch
To sumbus card
Fast trigger
PCIe 4x core

Time Difference Spectra

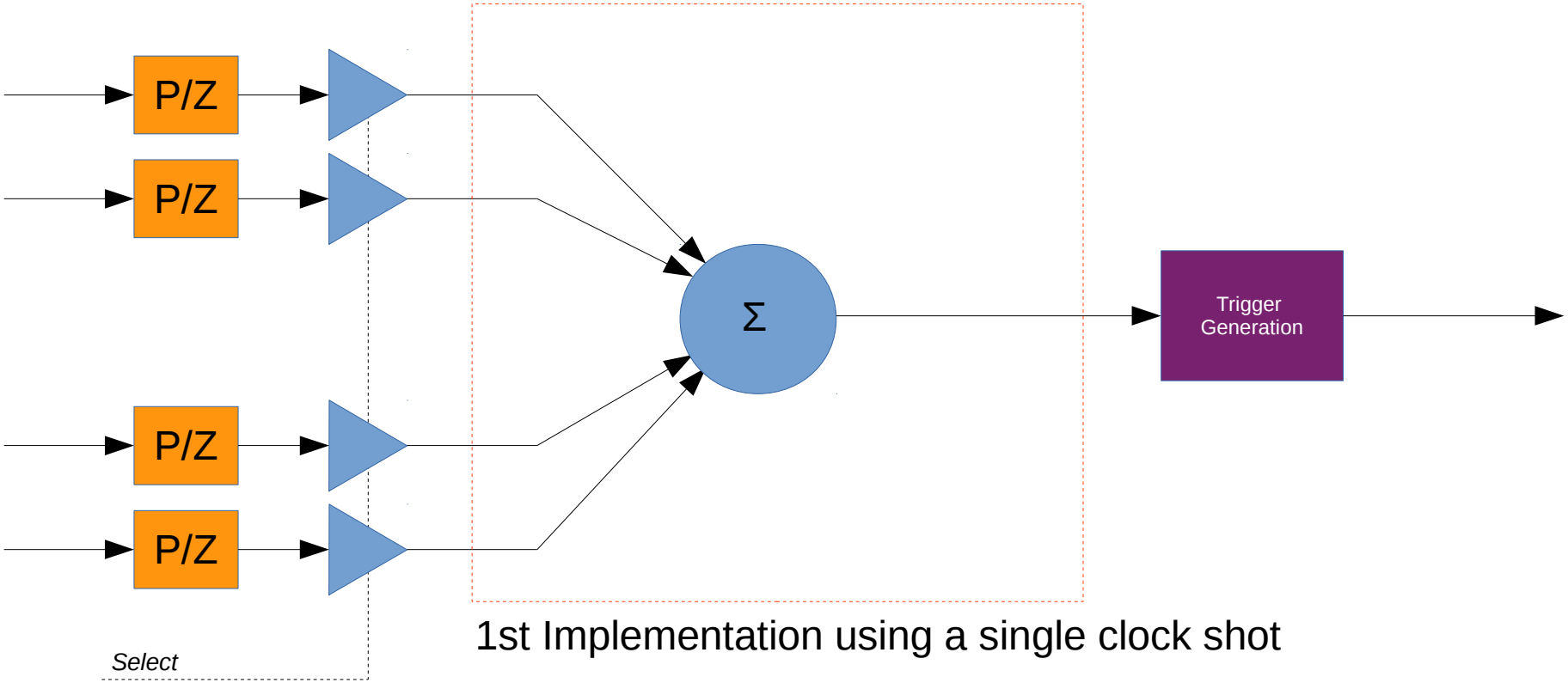
- Each domain allows to carry out time-difference spectra between consecutive events
- It can be used as an instantaneous rate-meter
- The time differences are calculated locally for every single trigger request (non-idle)



Add back and trigger selector

- Trigger functionality envisaged mainly for the GALILEO triple cluster

- Originally, a selectable single channel in a domain provided the triggering channel
- Now, with this mechanism, the trigger can be provided as the sum of several channels

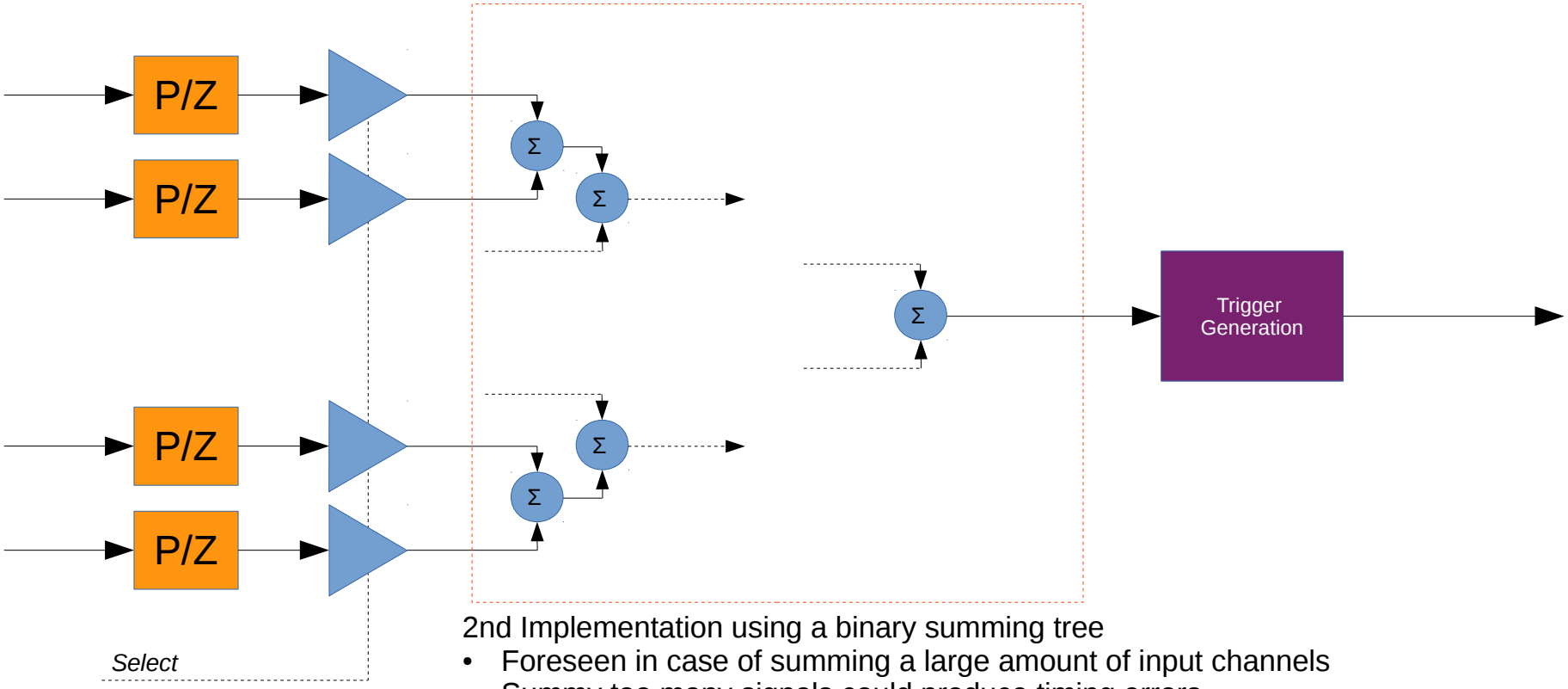


1st Implementation using a single clock shot

Add back and trigger selector

- Trigger functionality envisaged mainly for the GALILEO triple cluster

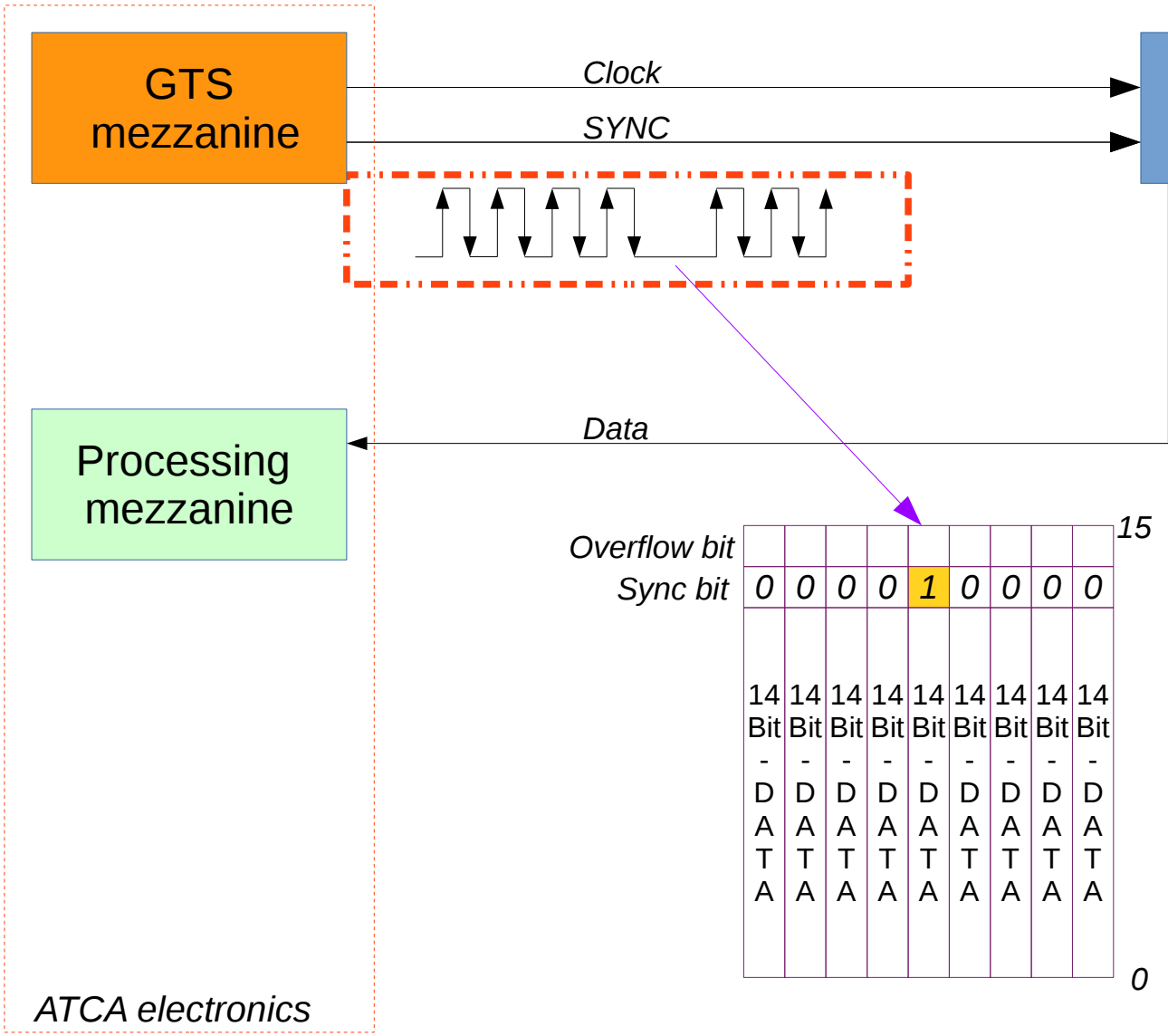
- Originally, a selectable single channel in a domain provided the triggering channel
- Now, with this mechanism, the trigger can be provided as the sum of several channels



2nd Implementation using a binary summing tree

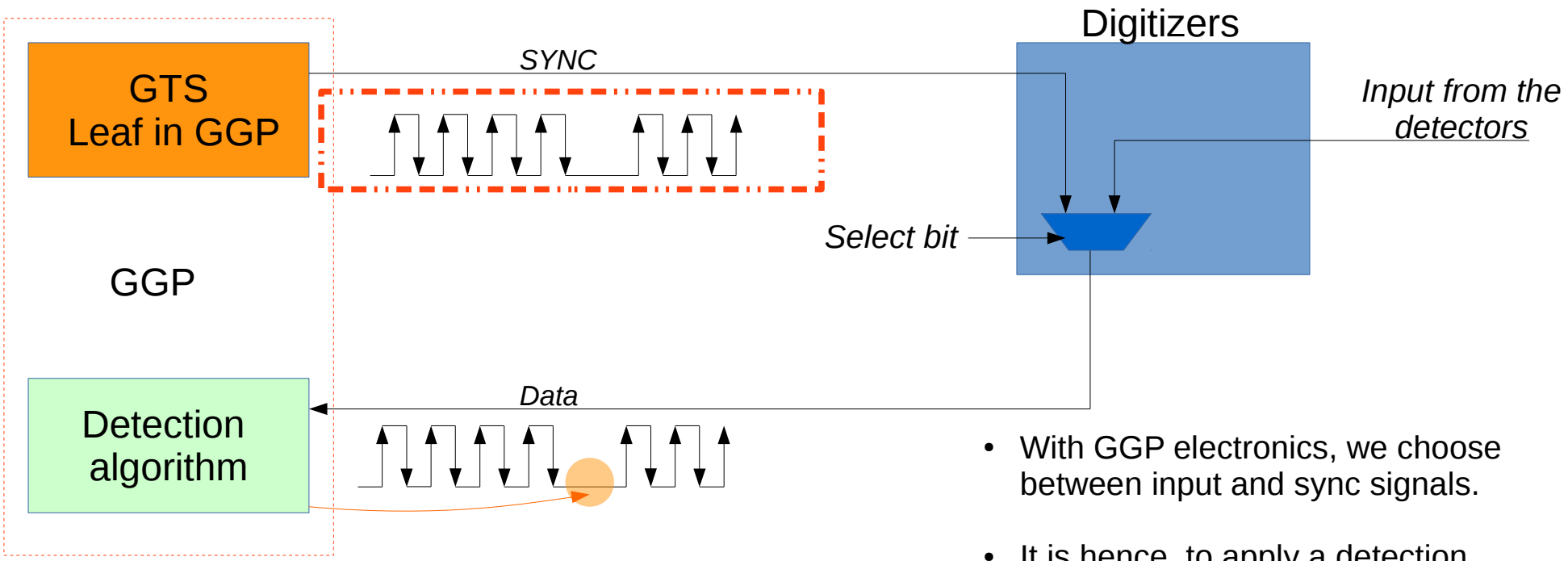
- Foreseen in case of summing a large amount of input channels
- Summy too many signals could produce timing errors
- Channels are summed up in pairs and delayed-aligned

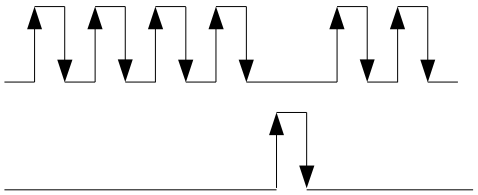
Sync mechanism (ATCA)



- With ATCA electronics, the missing cycle is detected in the digitizer board, adding a 1 on one of the spare data bits.
- This fact made possible the transmission of data and sync bits simultaneously
- The time difference between the missing cycle in the sync pattern and the sync detected bit is then used to compensate delays

Sync mechanism (GGP)



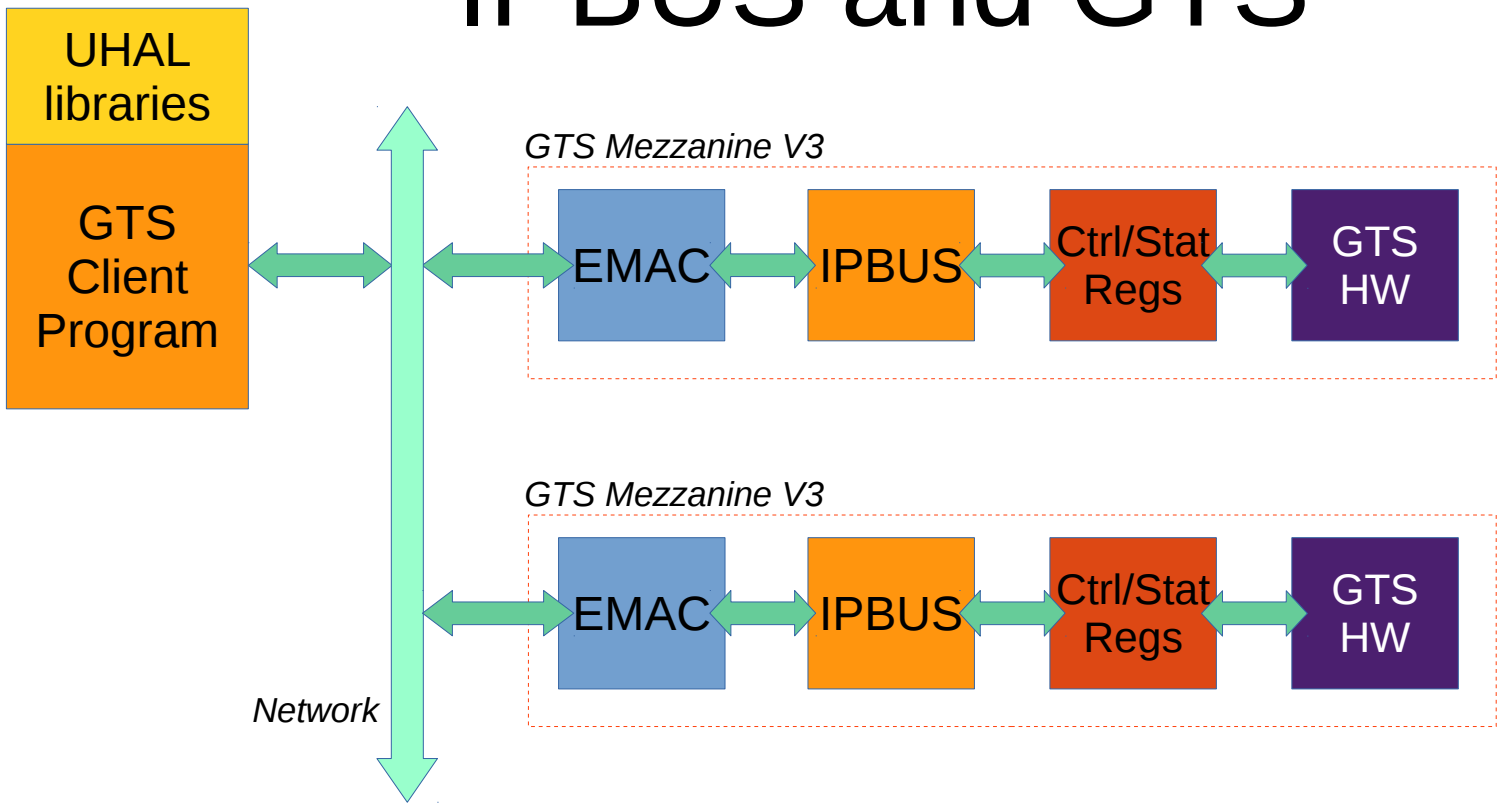


Sync pattern

Signal generated when the timestamp reaches a value equal to 2^N

- With GGP electronics, we choose between input and sync signals.
- It is hence, to apply a detection pattern algorithm over data in order to detect the missing cycle
- The time difference between the sent pattern and the detected missing cycle is used then to compensate the delays
- Enhanced robustness if using binary sub-multiples of the main frequency

IPBUS and GTS

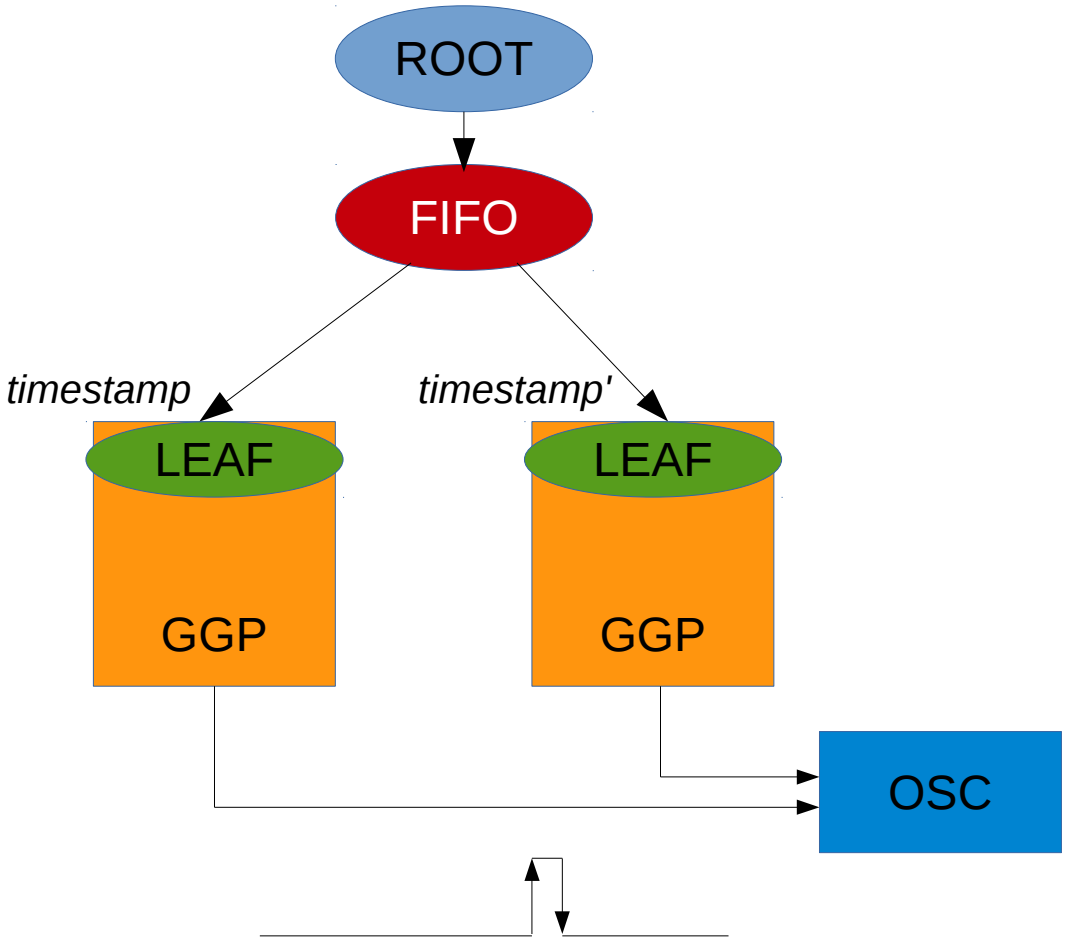


IPBUS solution proposed as an alternative to simplify the GTS control system.

- EPICS and VxWorks OS aren't used. Neither does the PowerPC processor.
- Therefore, a «GTS server» doesn't exist since there's not a program running on a processor.
- The client contains functions to read/write to/from the registers and act on the GTS HW

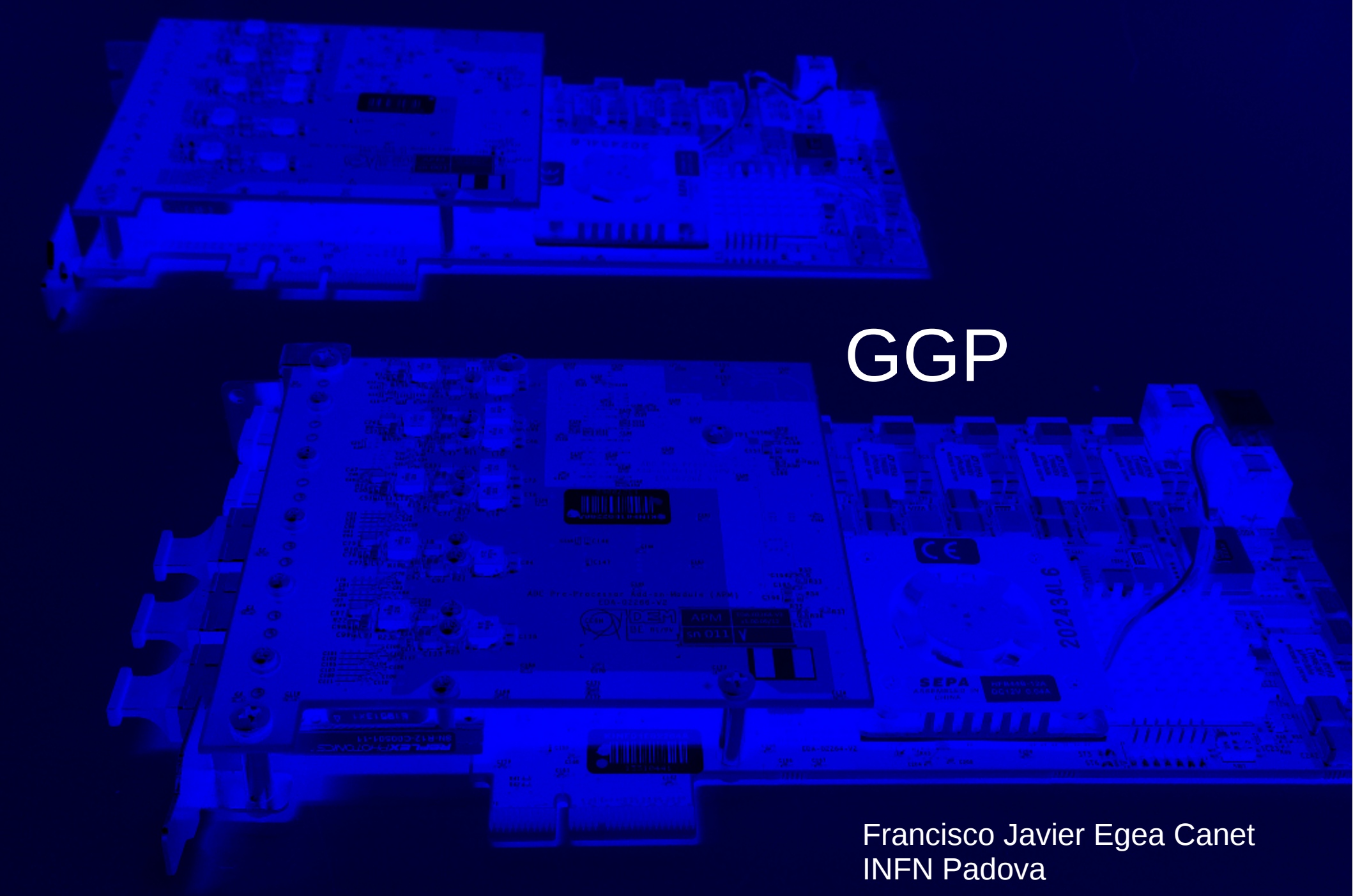
- Up to now, local tests have been carried out, being able to perform time measurements (both optical and with the MGTs).
- Still in a development stage.

GTS alignment problem



Monitoring the signal produced by the timestamp when generating the sync pattern using the sumbus interface

- In our setup in Legnaro, a misalignment has been seen using two GGPs.
- On our side, modifications have been made on the software side.
- The problem can be seen as a delay on the sync signals, indicating that the alignment wasn't carried out correctly.
- A test evidenced the origin of the problem in the GTS system as long as the local latency compensation with the digitizers was isolated.
- The consequence of this time misalignment is the delivery of different timestamps to different modules.
- Still, by now the problem hasn't been completely understood, and for this reason, the same setup must be compared using two VME leaf GTS cards.
- This might be relevant also for AGATA



GGP

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