VNIVERSITAT DE VALÈNCIA

R&D on electronics 2020
3rd Generation Electronics
PACE

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TeDRA - University of Valencia

2nd Generation Electronics

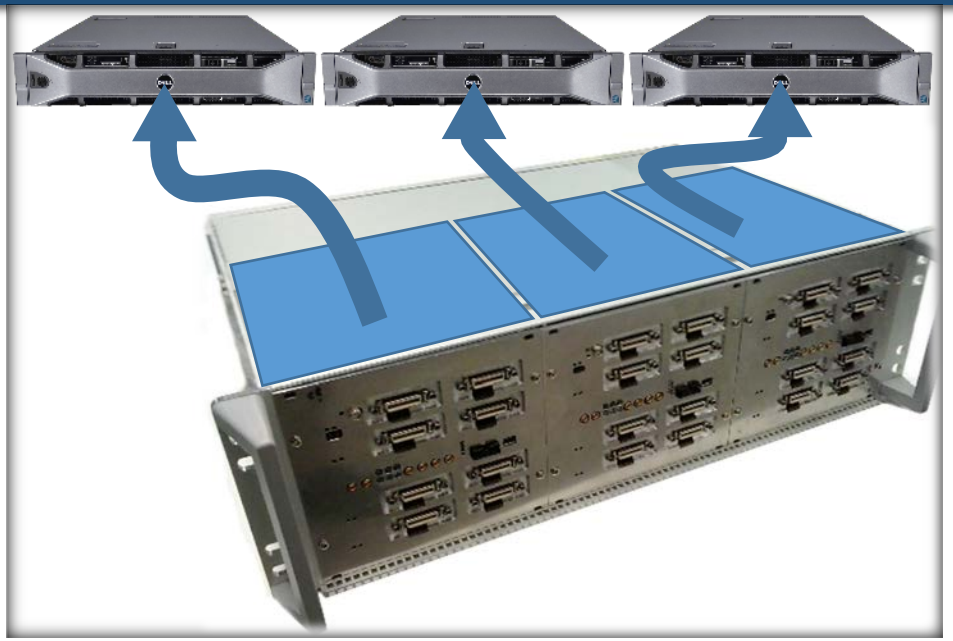
Digitizer
+
Slow Control
+
Preprocessing

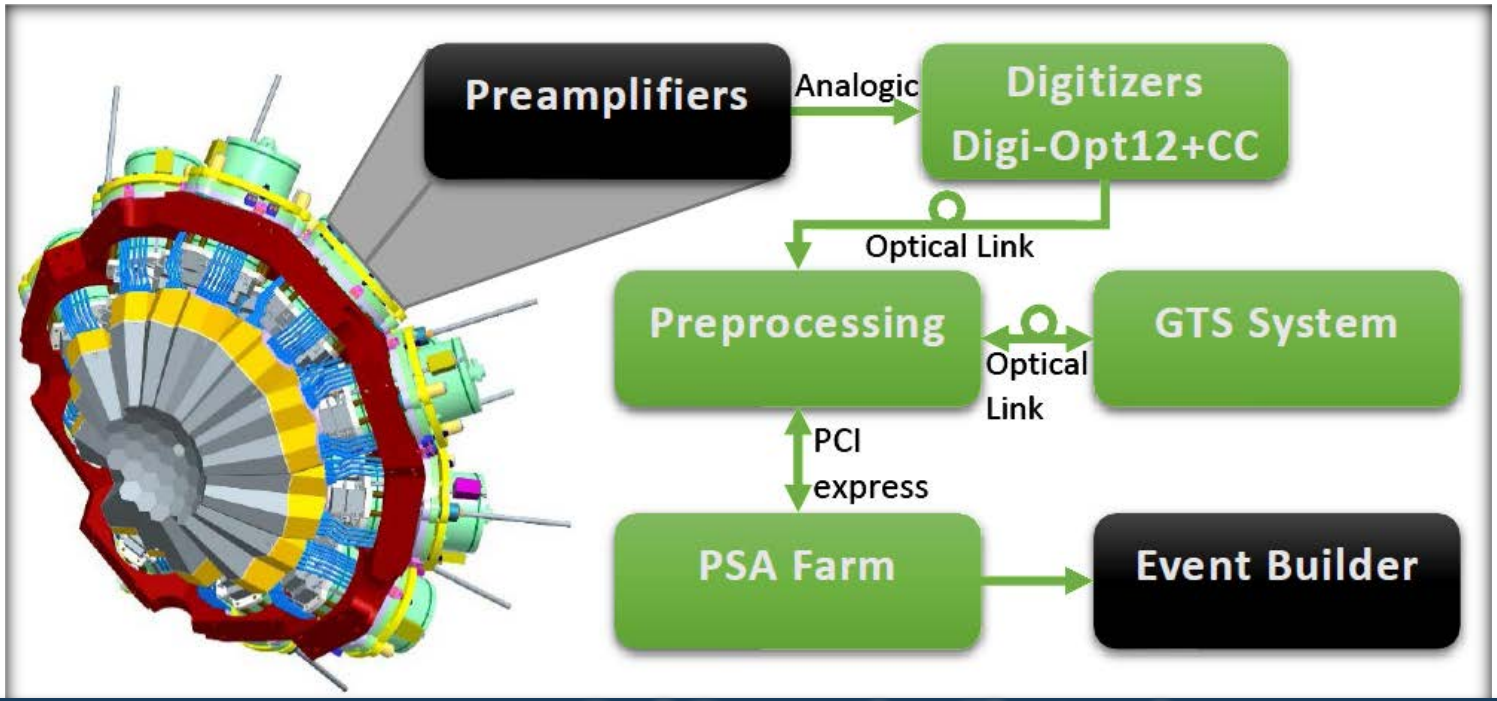
1 crystal

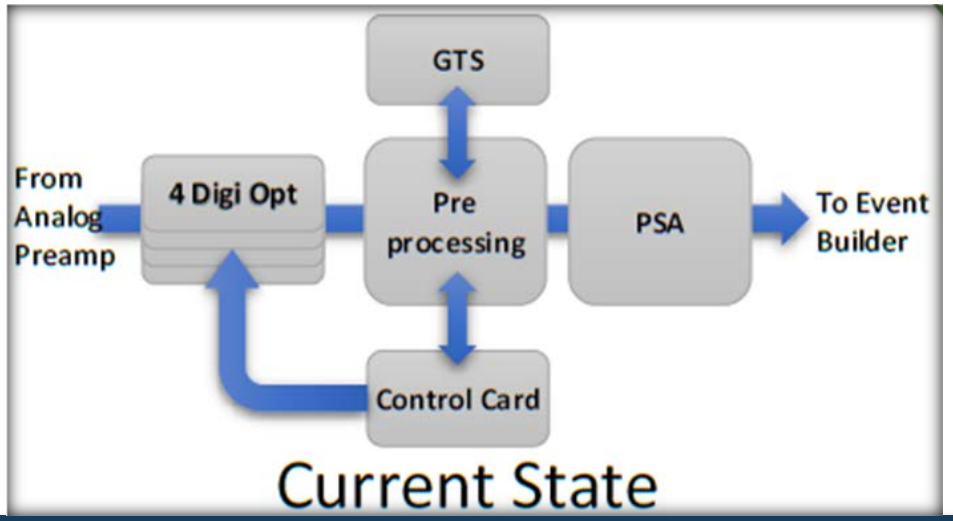
Optical Communication

PCI Express

PSA







Objectives

Preliminary Ideas

- Higher integration - less power consumption ASIC preamplifier
- Digitizer + Preamplifier
- Increase ENOB – 16 bit ADC
- Increase ENOB – Algorithm
- Control Card Integration
- Preprocessing – Full cluster
- Preprocessing near Digitizer
- Improve GTS number of Leafs
- Develop H&S of trigger processor
- Ethernet Acquisition
- No custom cards on processing farm
- Processing from FPGA to computing farm

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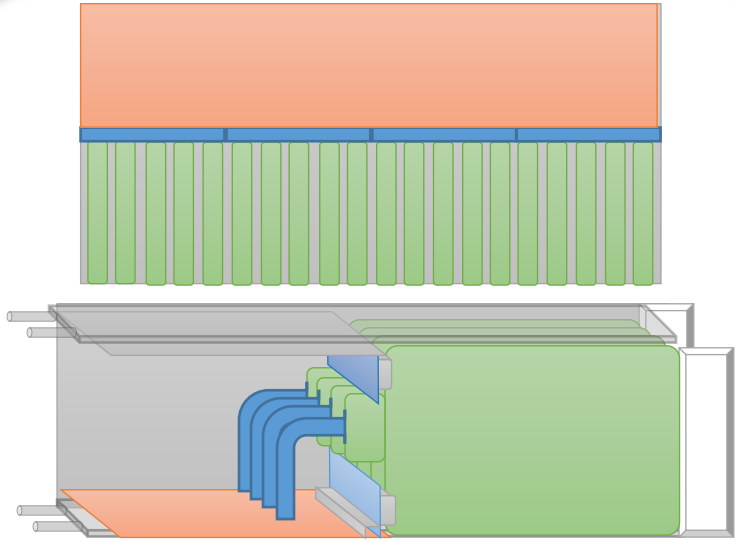
1. Increase de number of crystals processed per electronic device with associated electronic reduction.
2. Improve the computing and readout network.
3. Design compatibility and independence for previous electronics and future developments must be kept.



Objectives

- 1. Increase Capability
  - FPGA to process 3 crystals
  - Reduce the number of channels - TDM.
- 2. 40Gb Ethernet readout
  - No Point to Point
  - Less Optical fibres
  - Increase Data Rate
- 3. mezzanine approach design.
  - Independent Development and Update
  - Compatibility
- Modules:
  - IDM – Input Data Mezzanine
  - CAP – Control and Processing
  - STARE – Ethernet readout
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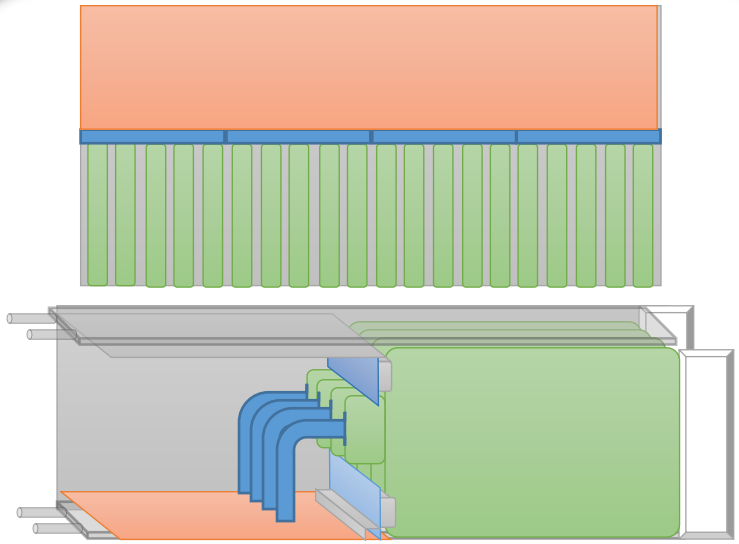

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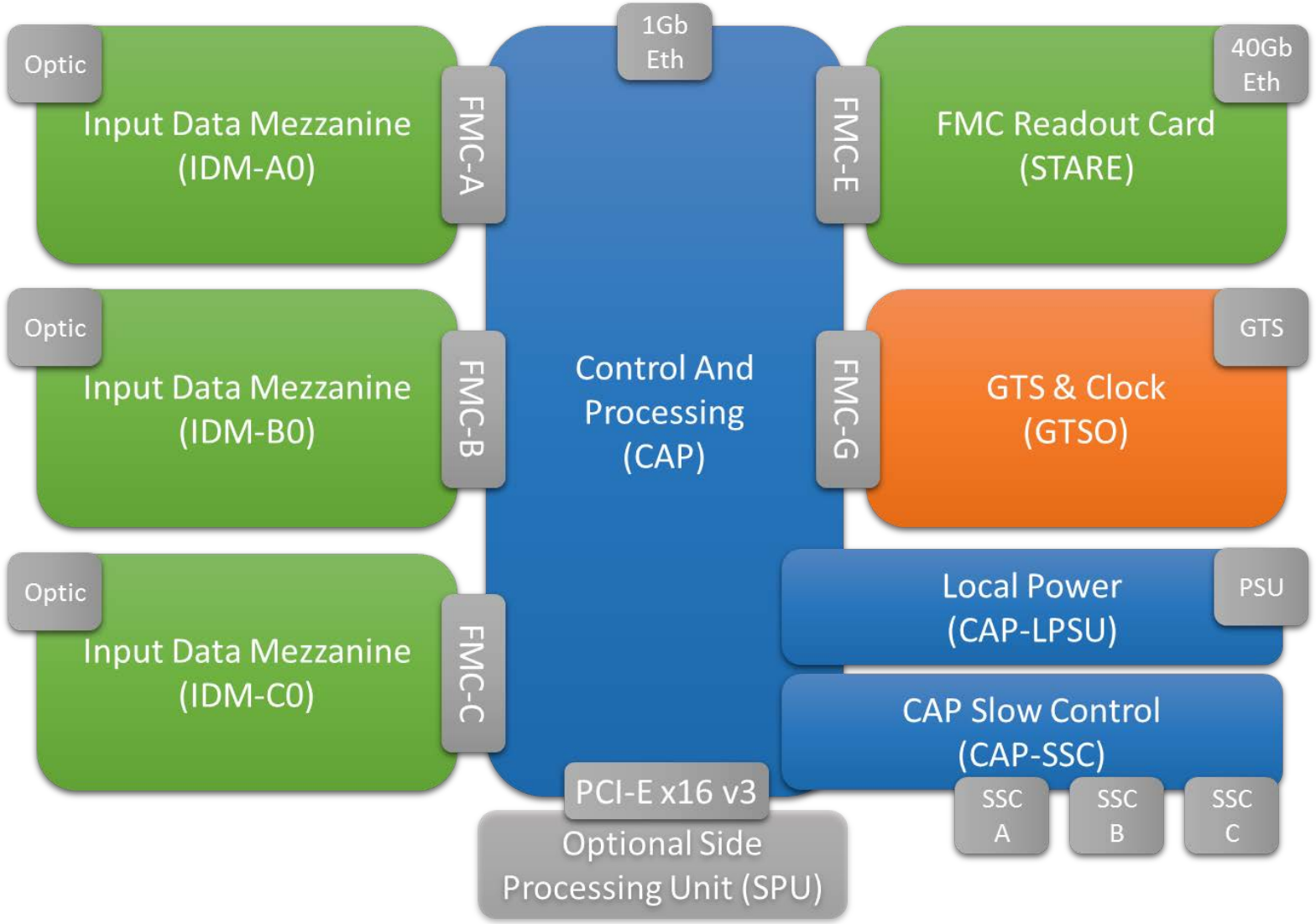
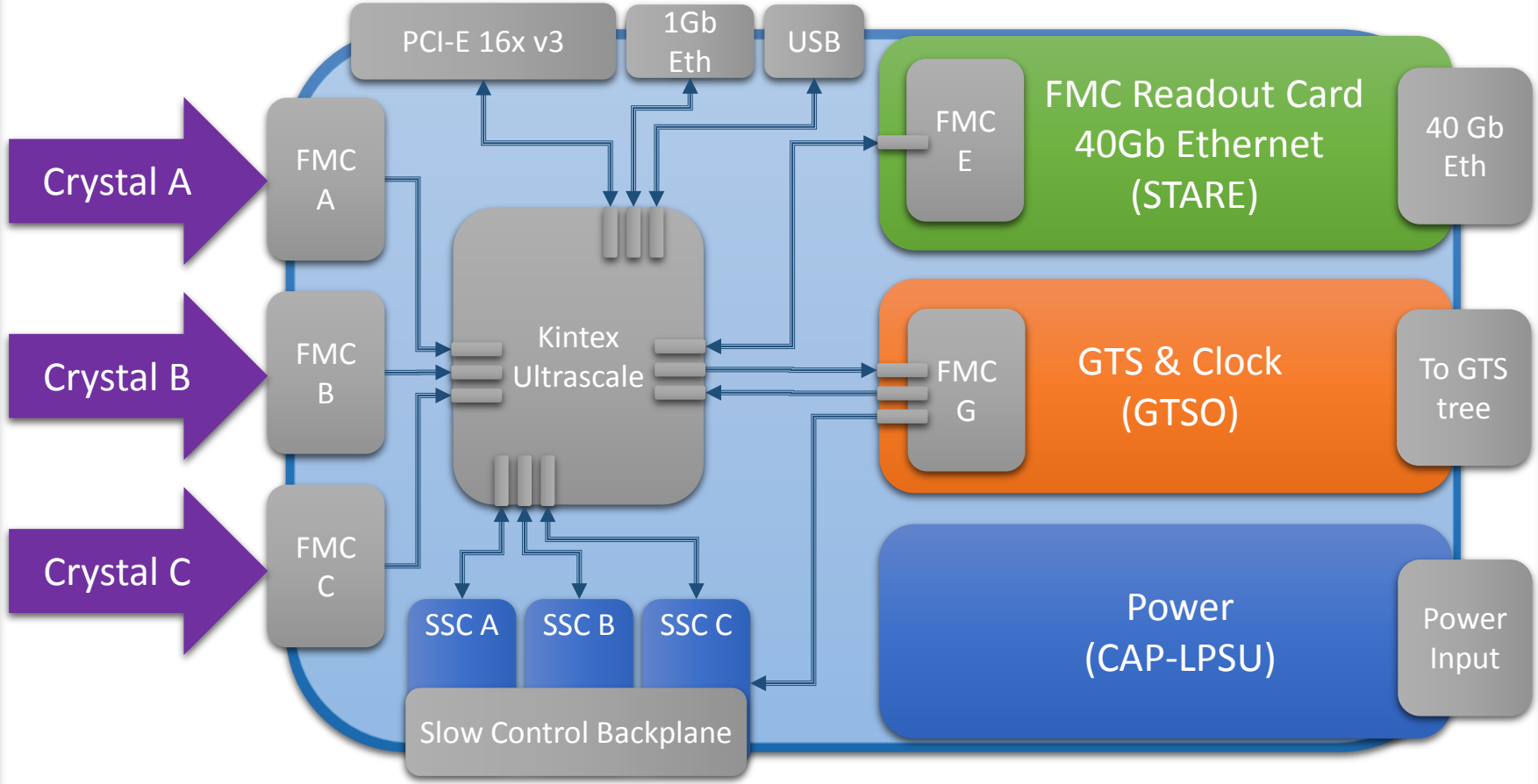


PACE: Control and Processing CAP

- Host up to five ANSI/VITA 57.1 Mezzanines
  - Ten 10Gbps Channels per mezzanine.
  - 3 Slots for IDM, 1 Slot for STARE, 1 for GTSO.
- Processing by Xilinx KintexUltrascaleXCKU115 FPGA.
  - Capable to process information from 3 crystal
  - 56 16,3Gbps transceiver. 30 for IDMs
- Slow control distribution
  - Autonomous initialization and maintenance.
  - User slow control from STARE communication.
- Provides power supply to all mezzanines



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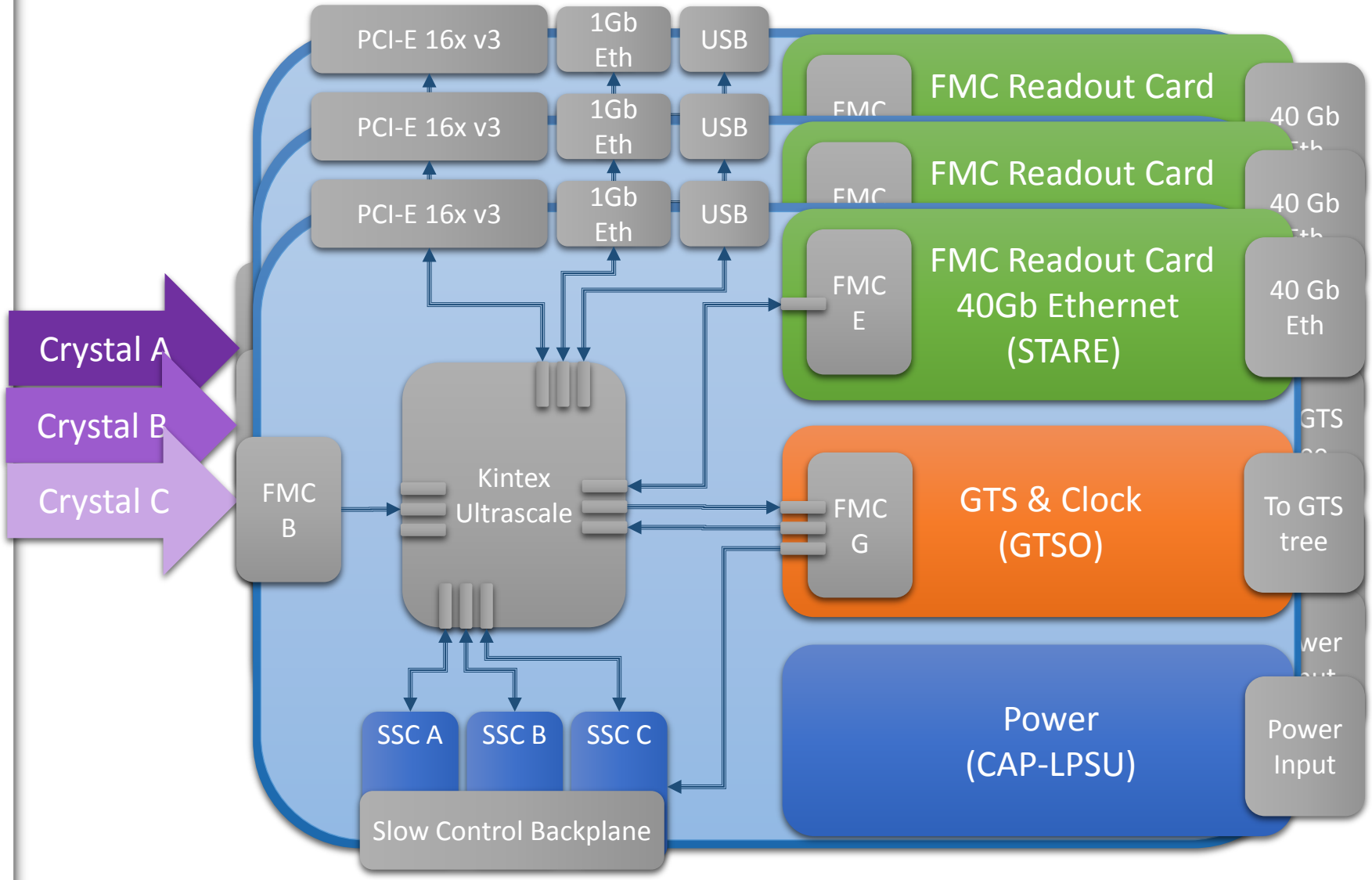

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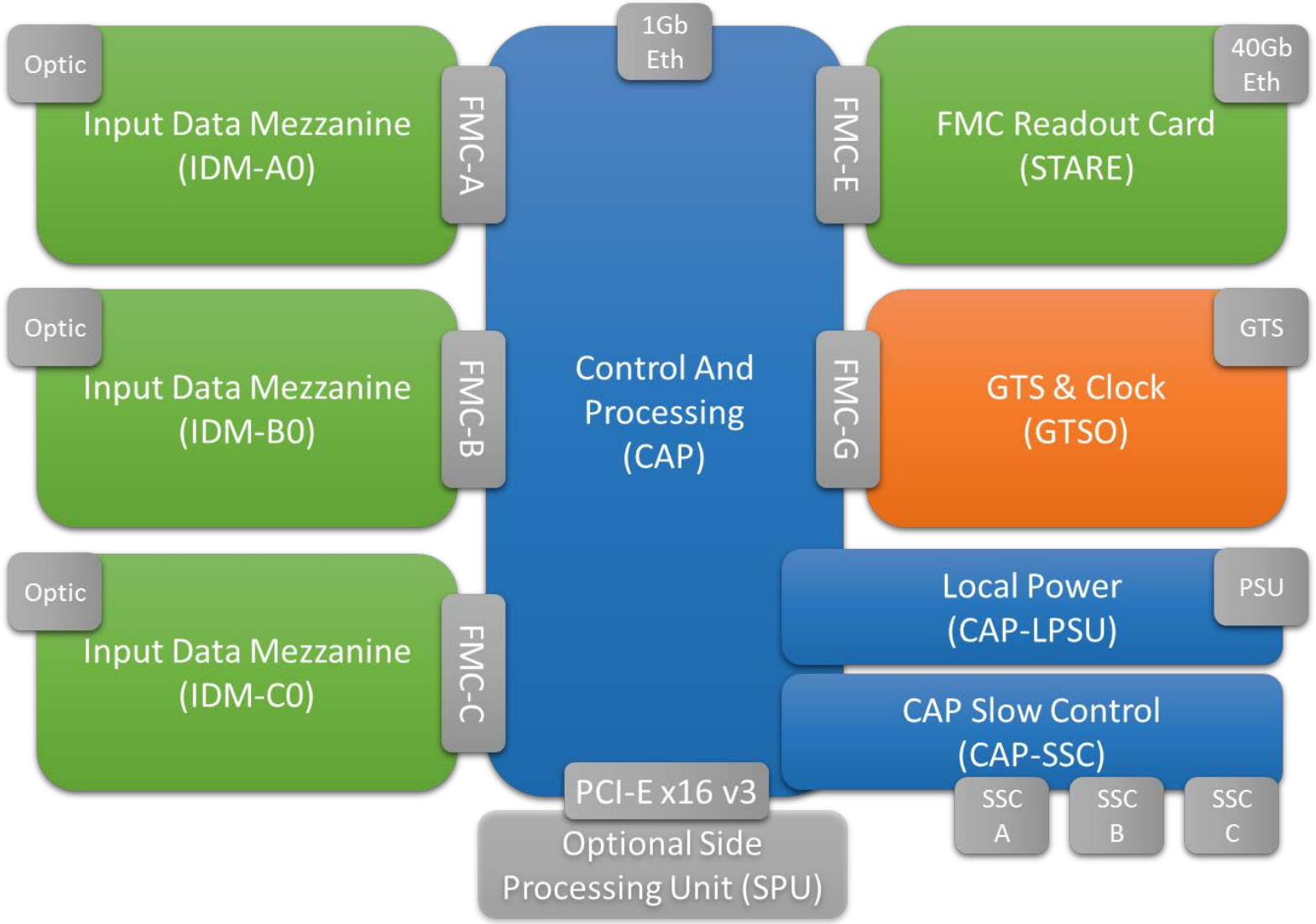
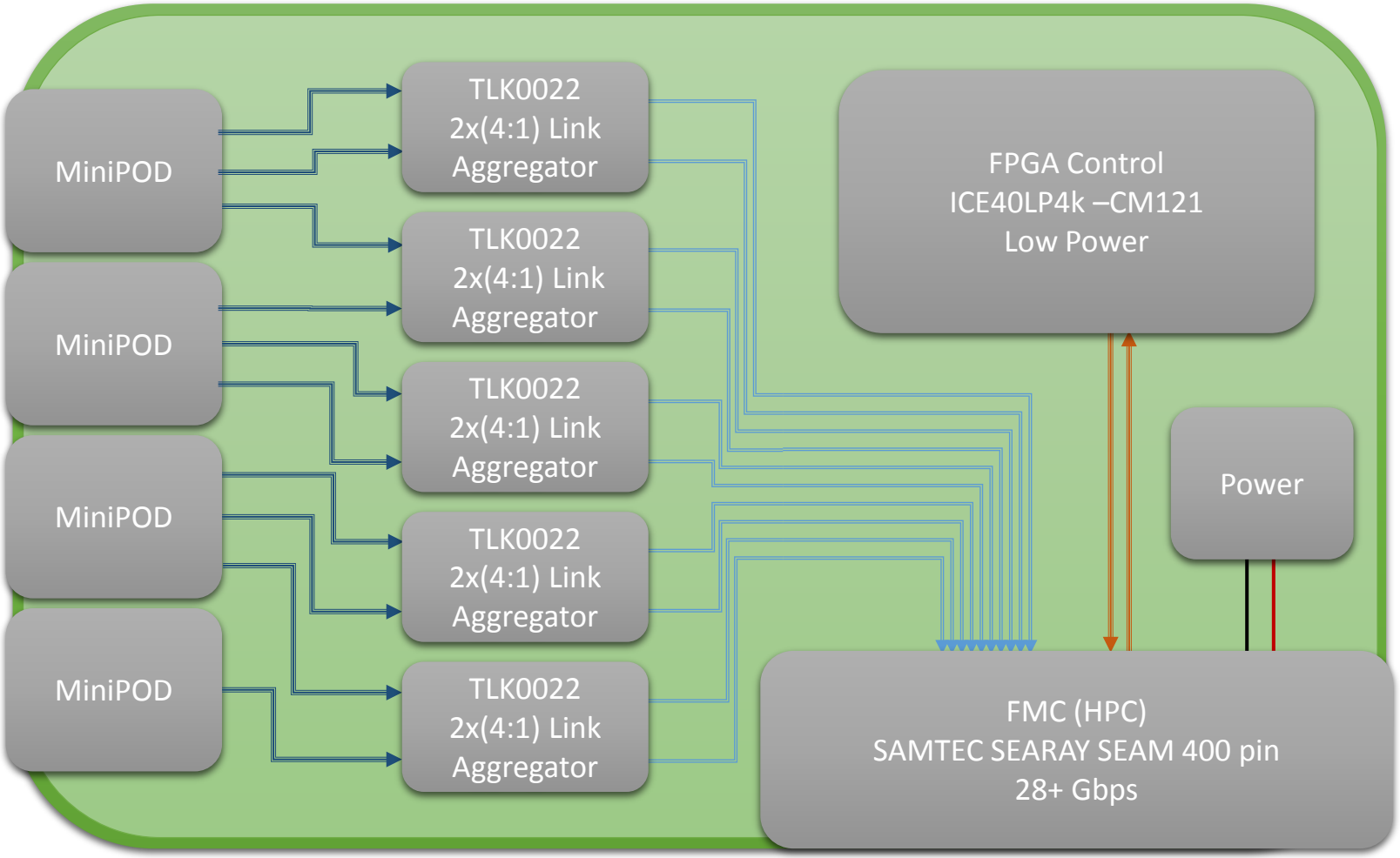


PACE: Input Data Mezzanine IDM

- Optical reception of 38 channels
  - Avago MiniPod
- Channel reduction by time division multiplexing.
  - 4:1 ratio from four 2Gbps signal inputs to one 8Gbps output. Total reduction 38 channels to 10
  - Compatible with JESD204A.
- Autonomous initialization and monitoring.
  - User slow control simple orders through CAP by I2C pair on FMC.
  - Alarm signals sent to CAP in case of failure.



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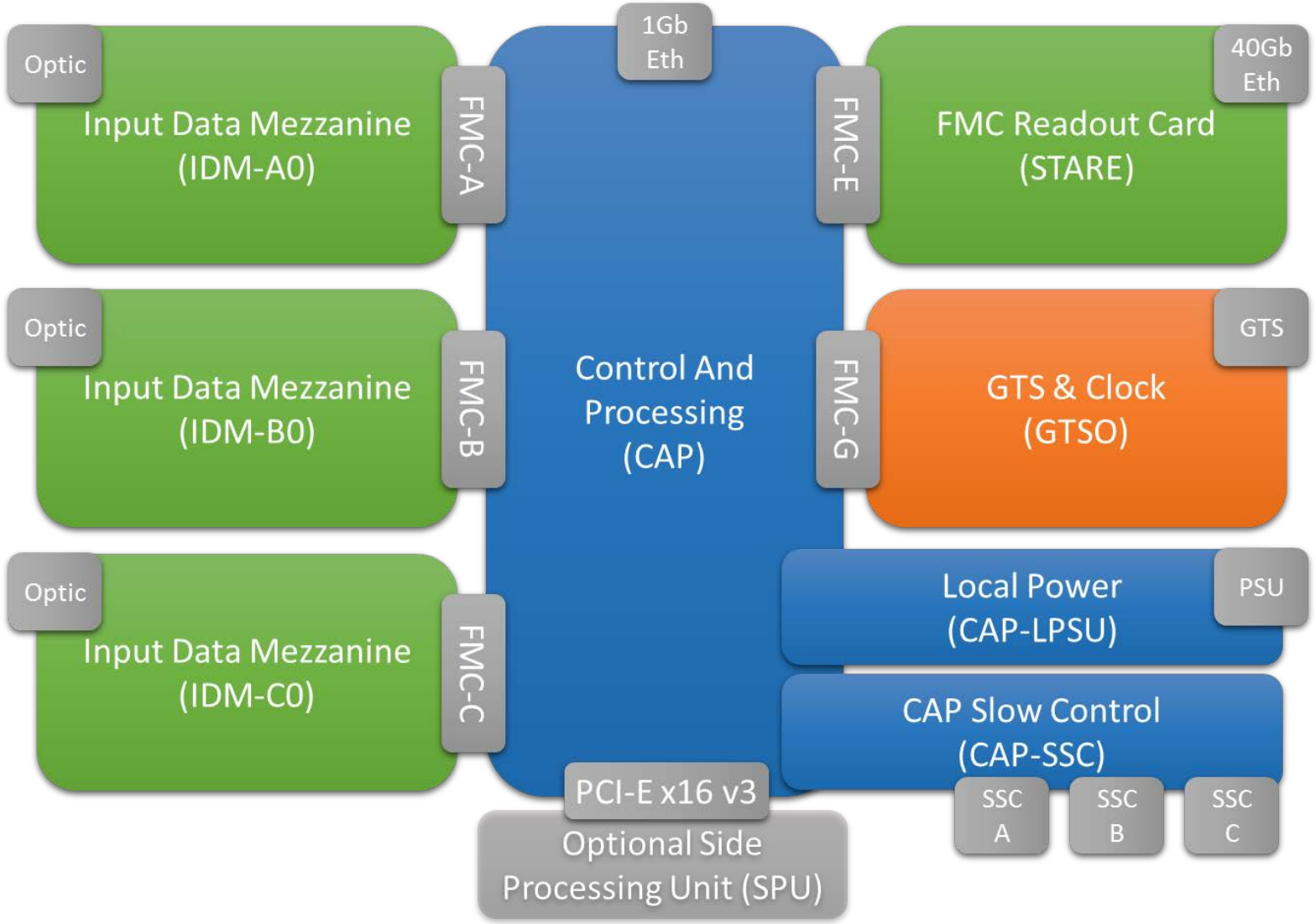
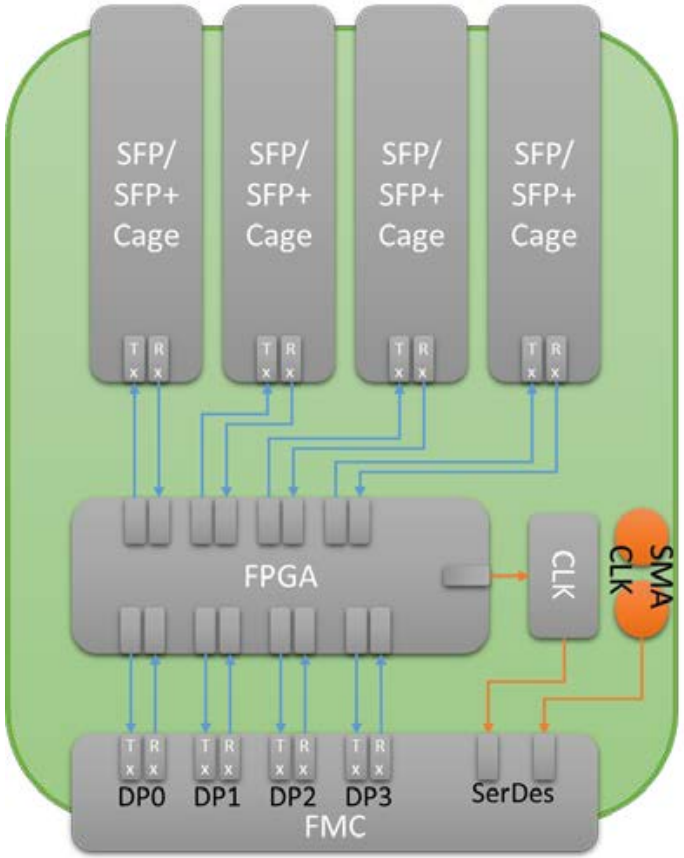
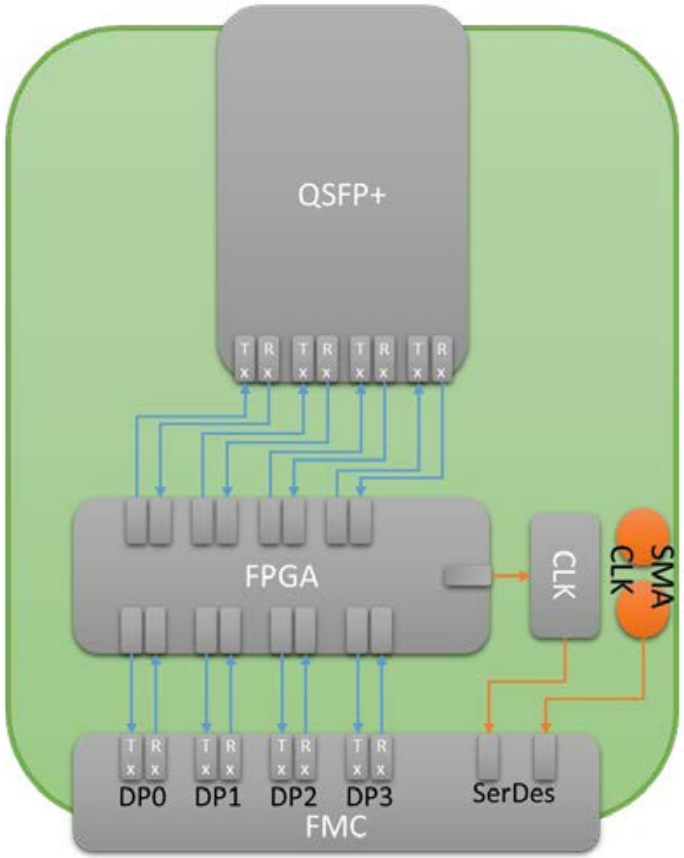


PACE: STARE

- Independent FPGA based 40 Gb communication module.
- Step by step design approach
- FPGA internal processor with embedded Linux OS for control.
- Slow Control: IPBus for PACE.
- Data Output:
  - The three crystal data will be transference relies on RATP protocol with UDP
  - Memories implemented on each side to avoid latency
  - Light packet control to ensure losing no data



V1: 4x10 Gb Ethernet Card



V2: 1x40 Gb Ethernet Card
V3: 100 Gb Ethernet Card with CFP

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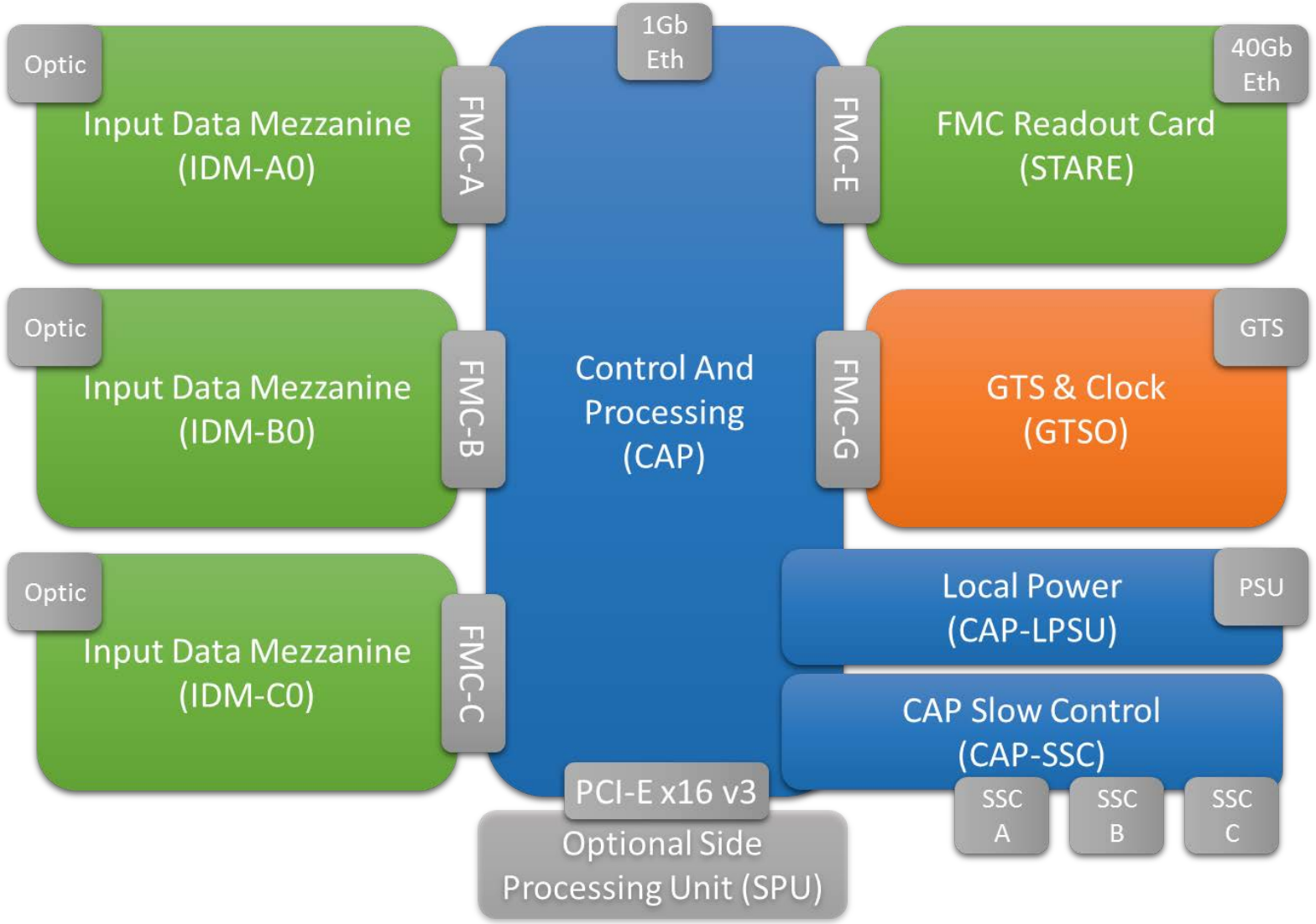
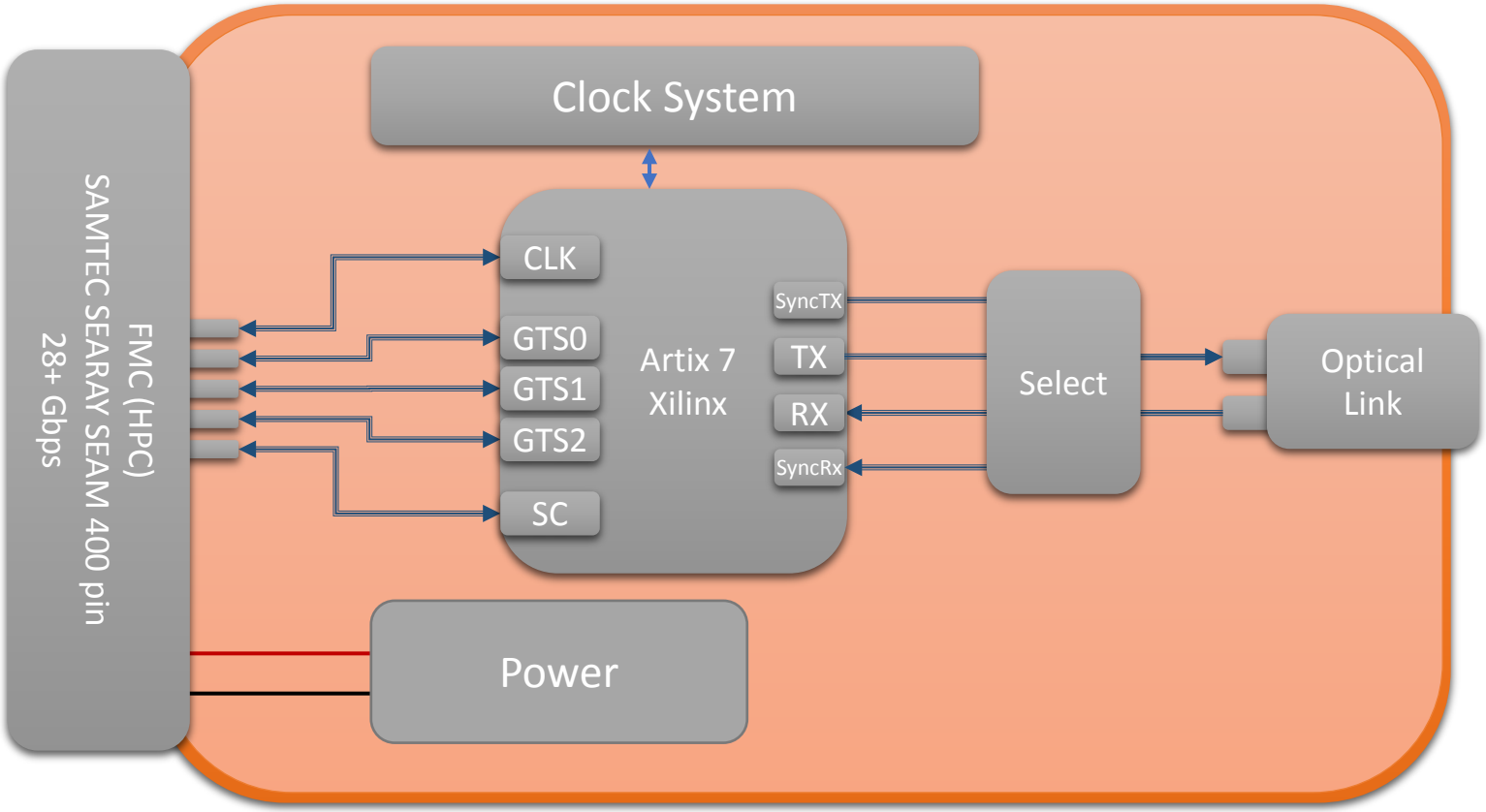


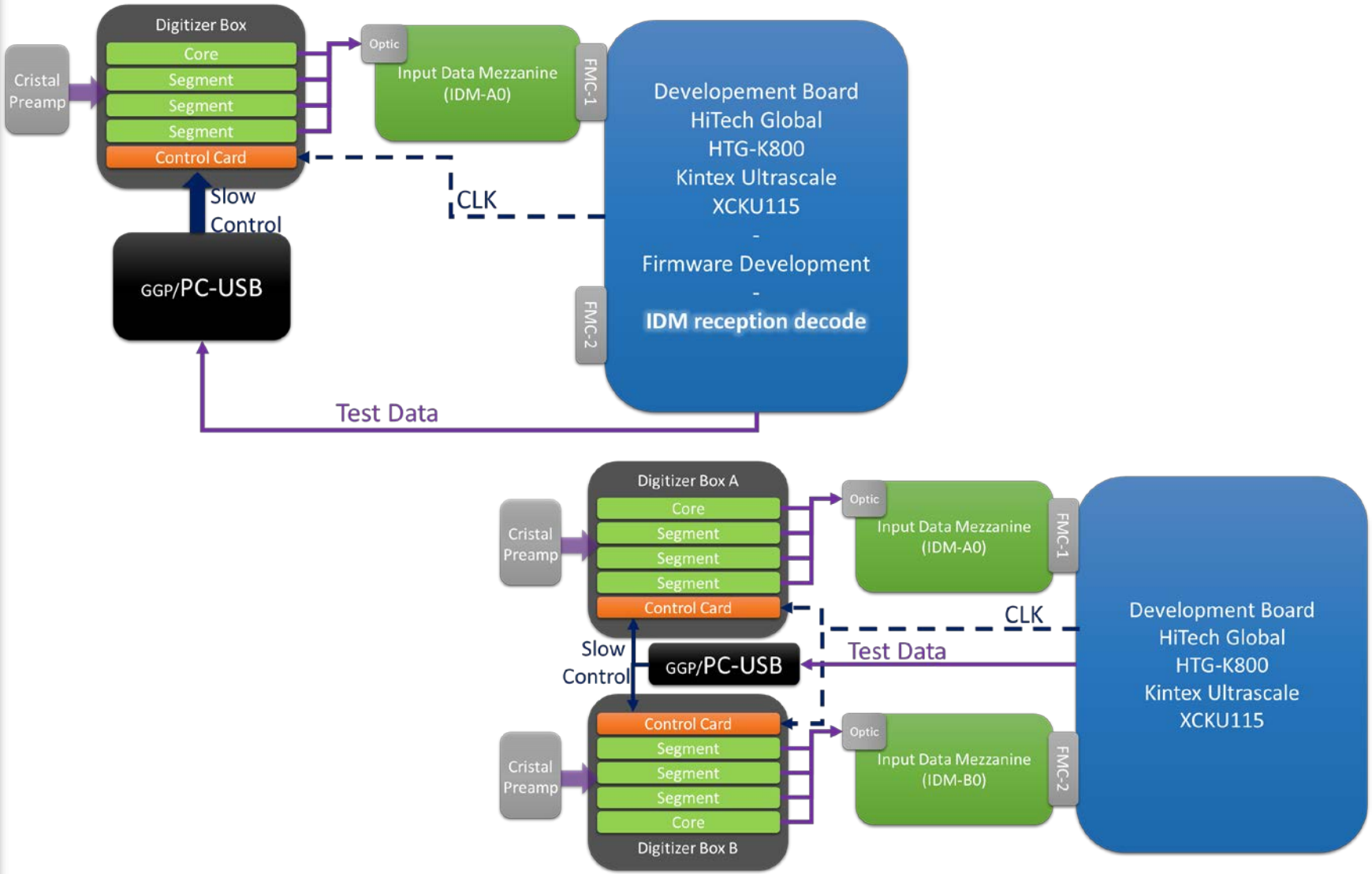
PACE: GTSO

- Interconnection with the rest of Global Trigger System (GTS) Tree
- Three possible GTS signals coming from CAP
- Processing power from Xilinx Artix7 XC100T FPGA.
- Clock Management for the PACE system.
  - Clock Generation or GTS clock input.



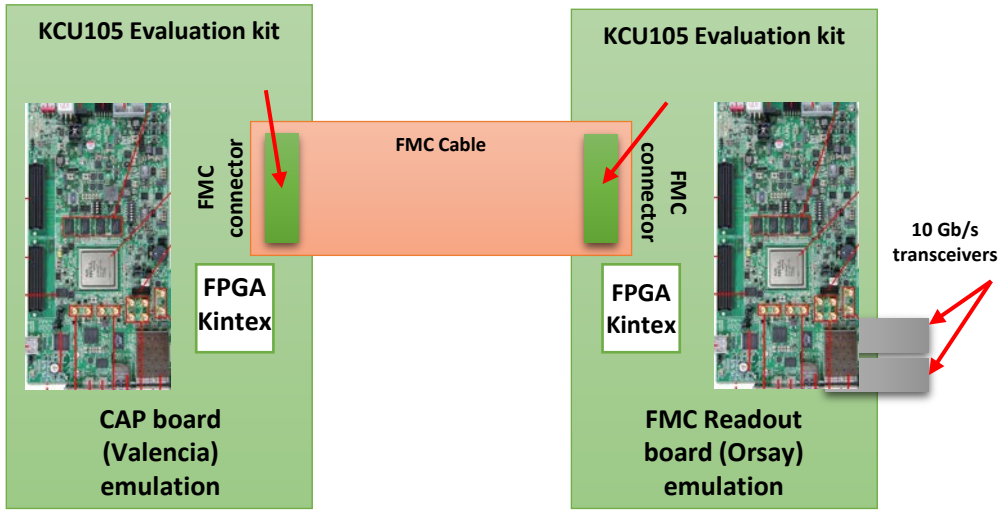
Validation: Data Receiving Test

- Validation of IDM: Link Aggregation concept with JESD204A.
- HiTech Global HTG-K800 Evaluation board emulates CAP with Firmware for Time domain multiplexing decrypt.
- Data from Digi-Opt12 stored on Memory and compared with the real data.
- A second test with two IDM and digitizer setup.



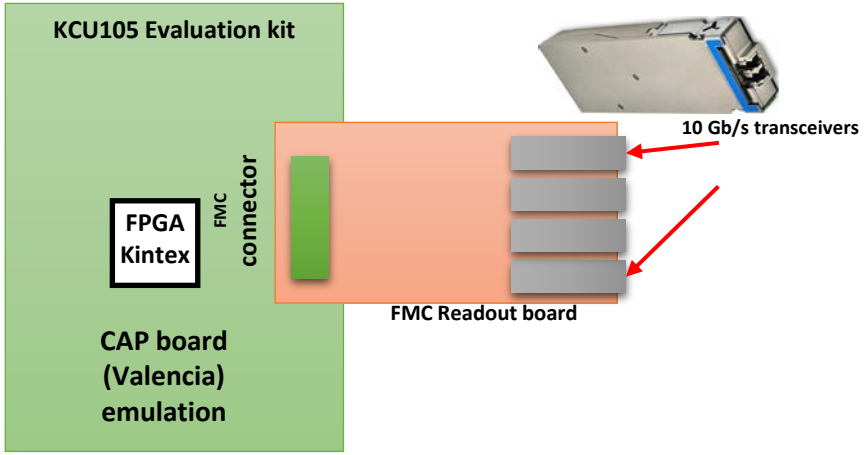
Validation: Ethernet Transmission Test

- Standalone communication for STARE with the 40Gb Network for data transmission.
- KCU105 evaluation board will emulate CAP on one side and another KCU105 emulates STARE.
- By the time STARE prototype is developed, one of the KCU105 will emulate CAP and will test the communication.



First Type Workbench

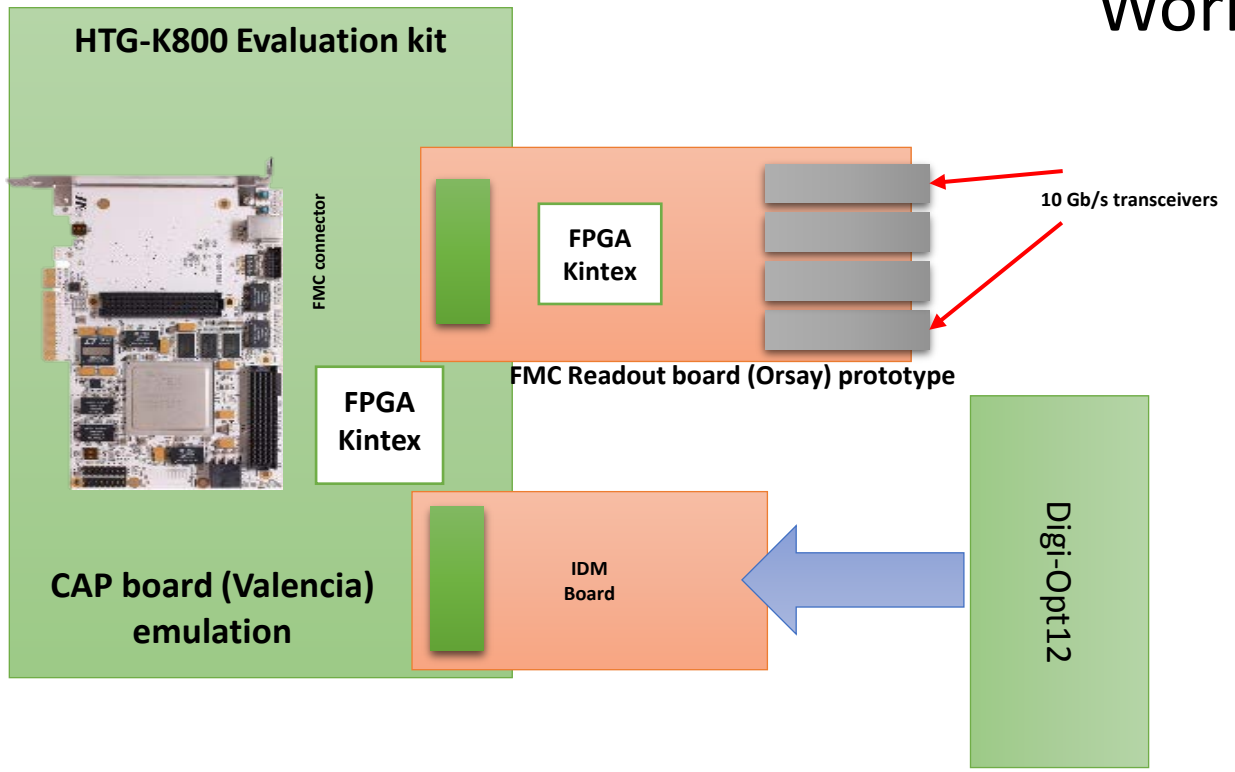
Second Type Workbench



Validation: Full System Test

- This test takes part after the two prototypes are developed and tested alone.
- STARE prototype and IDM prototype connected to the HTG-K800 development board as CAP.
- Digi-Opt12 data is sent to the network through PACE.

Final Step Workbench



Thank You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TRACKING ARRAY


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