FATALIC
in wrap up of June Test Beam activities

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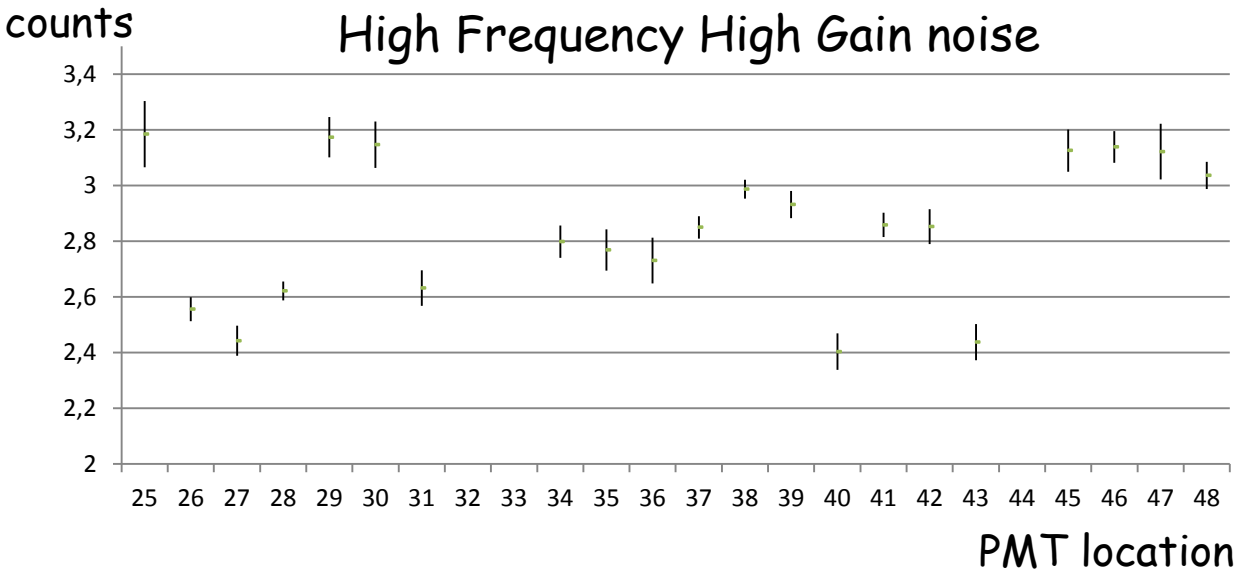
and the micro-electronics team
6 July 2016

- Short summary of performances and problems
- Tests during the next Expert Week
- Set-up for September
- Next actions

Short summary of performances and problems

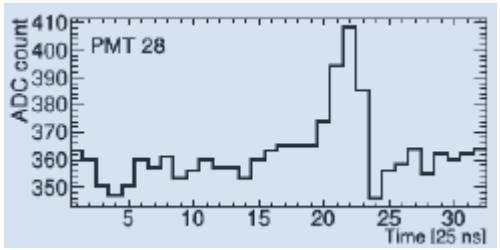
- **Set-up**
  - Assembly of complete Drawers 3 (10 PMTs) and 4 (11 PMTs) for a LB module, with Standard Main Boards, Daughter Boards and Remote HV system.
  - Insertion of Drawer 3 only (Drawer 4 for QIE).
  - Connection to the PPR.

- **Reference tests at LPC** on individual PMT Blocks connected one by one to the same channel of the MB Prototype (HV off) → Pedestals + electronic noise.



Mean noise over 21 PMTs:
2.80±0.05 counts
or 6.74±0.05 fC
with:
minimum: 5.77±0.16 fC
maximum: 7.64±0.29 fC

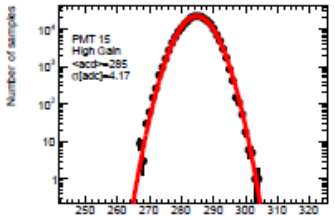
- **Measurements at CERN** using the Standard MB + DB + PPR + FLVPS and Remote HV on the Drawer 3 inside LB



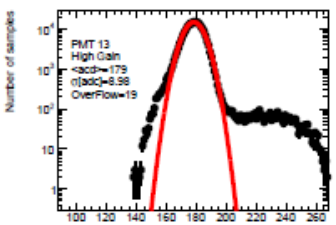
→ Good working of the whole MB-DB-PPR communication, despite the PPR spectra invert the time!

→ PMTS at their nominal gains.

→ Pathological aspects of some of the Pedestal spectra and/or increased width as far as the MB channel input is far from its FPGA! (See Back up slides)



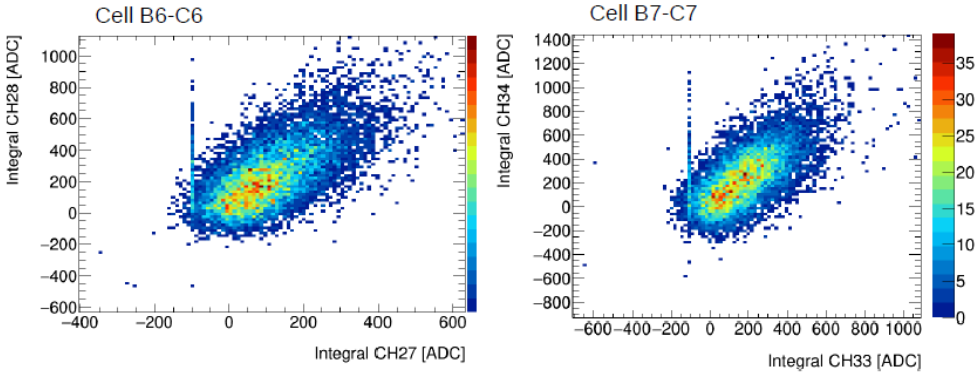
PMT30, close



PMT26, far

- Explanation: bad transmission of some bits from FATALIC to the FPGA's on the Main Board, because of the capacitance effect of tracks.
- How to cure it? To boost the digital information with a buffer on the All-in-One card (to validate) then inside FATALIC → New FATALIC5 specif.

→ PMT correlation on the same cell
- Rough calculation.
- Hadrons at 90°.



→ Other data taken after the official Test Beam period … not yet analyzed.

Tests during the next Expert Week

- First Cesium tests using the digital summation over 10 ms of HF data.
- Requests the access to the Drawer 3 in order to modify the FPGA firmware, and to the PPR data stream (in principle close to the Chicago one). (Wednesday 20 to Friday 22)

September Test Beam

- The same set-up as this one of June, but with the Drawers 3 and 4 on LB Module.
- The recorded data will be more significant on the channels close to their FPGA.
- Study of the Optimal Filtering.

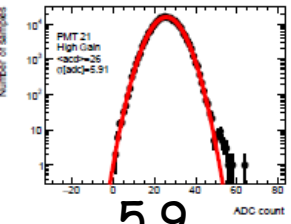
Next actions

- Validation of the buffer concept by using a modified All-in-One card.
- New simulations of FATALIC with an additional buffer inside ($\rightarrow$ FATALIC5).
- New studies of a complementary analog integrator for very low currents (Ilya's request): will be reported at the October TileCal week.
- It is urgent to coordinate the radiation studies $\leftarrow$ to quantify the requested funds.
- The dates of the 2017 Test Beam periods will condition the FATALIC5 availability.

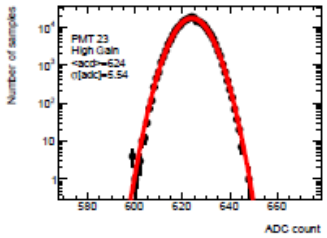
BACK UP

High Gain

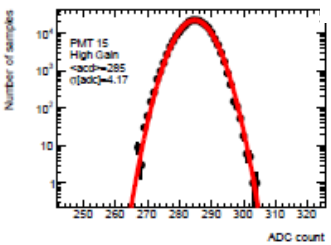
Pedestals, RMS and positions
(Straight line distances*)



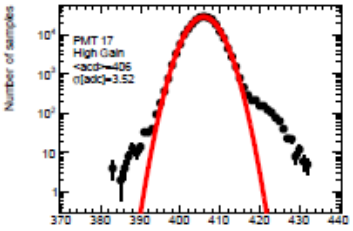
5.9



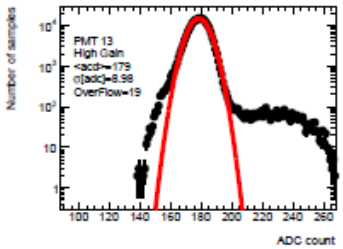
5.5



4.2

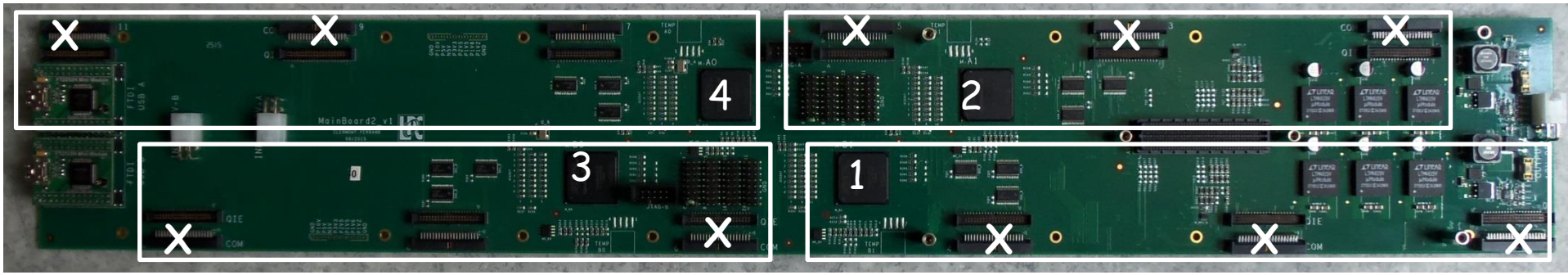


3.5

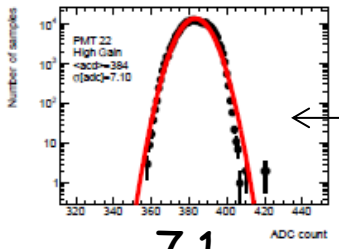


9.0

36(280mm) 34(175mm) 32(60 mm) 30(55 mm) 28(60 mm) 26(175 mm)

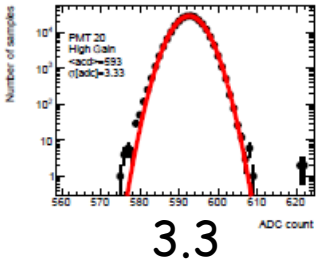


35(175 mm) 33(60 mm) 31(55 mm) 29(60 mm) 27(175 mm) 25(280 mm)



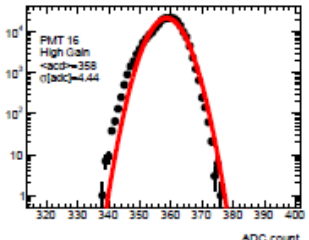
7.1

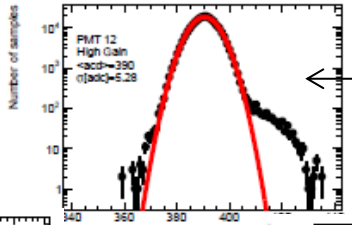
← Example: large



3.3

4.4

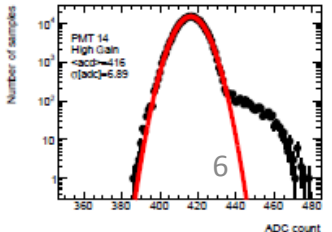




← Example: pathological

5.3

6.9



*Warning: Distances not taking into account the bending path in MB and the PMT Block connections.

Pedestal CERN/Pedestal LPC
Noise CERN/Noise LPC

PMT position (Straight line distance)

26/31
5.9/2.7

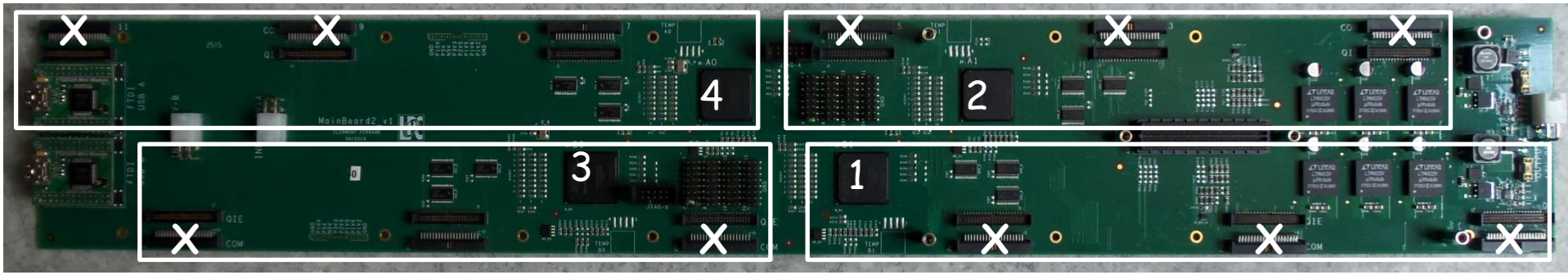
624/644
5.5/2.8

285/291
4.2/3.1

406/401
3.5/2.6

179/179
9.0/2.6

36(280mm) 34(175mm) 32(60 mm) 30(55 mm) 28(60 mm) 26(175 mm)



35(175 mm) 33(60 mm) 31(55 mm) 29(60 mm) 27(175 mm) 25(280 mm)

384/391
7.1/2.8

593/577
3.3/2.6

358/356
4.4/3.2

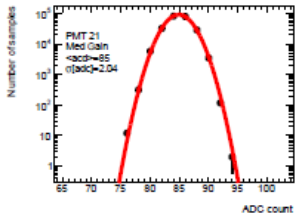
390/397
5.3/2.4

416/435
6.9/3.2

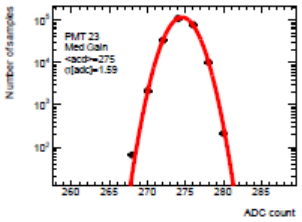
Medium Gain

Pedestals, RMS and positions

(Straight line distances*)

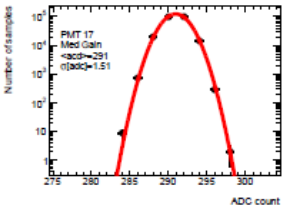


2.0

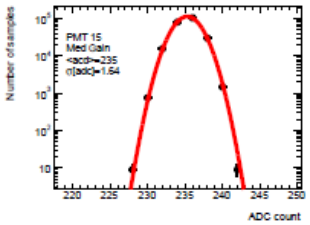


1.6

36(280mm) 34(175mm) 32(60 mm)

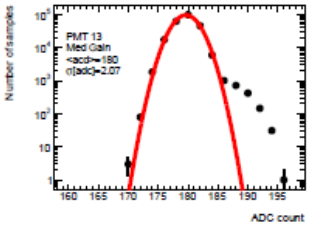


1.5



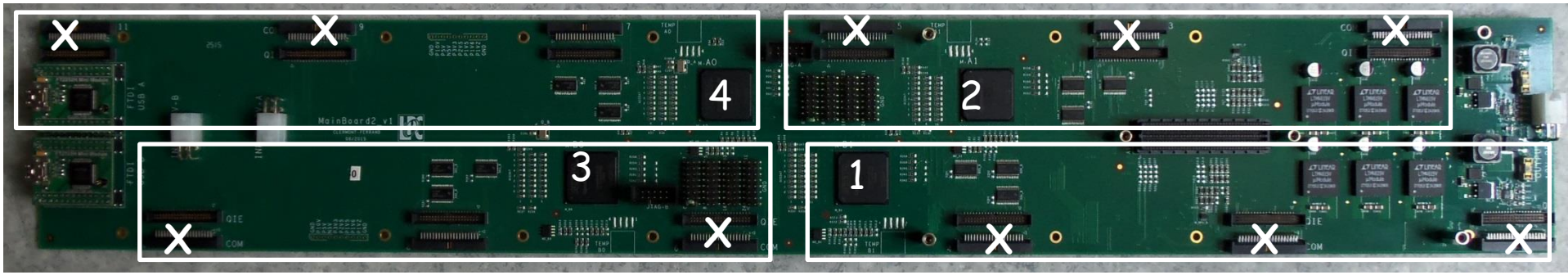
1.6

30(55 mm) 28(60 mm)



2.1

26(175 mm)



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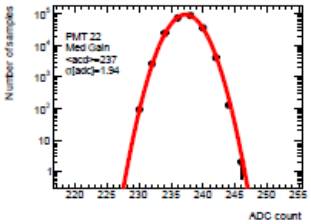
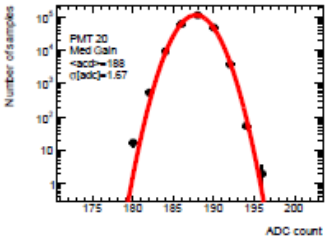
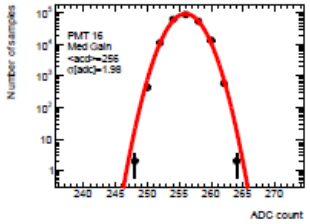


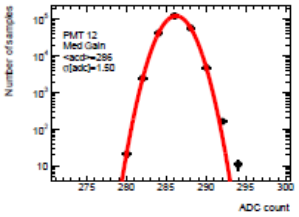
1.9



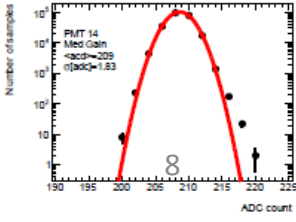
1.7



2.0



1.5



1.8

*Warning: Distances not taking into account
the bending path in MB and the PMT Block connections.

Pedestal CERN/Pedestal LPC
Noise CERN/Noise LPC

PMT position (Straight line distance)

85/82
2.0/1.6

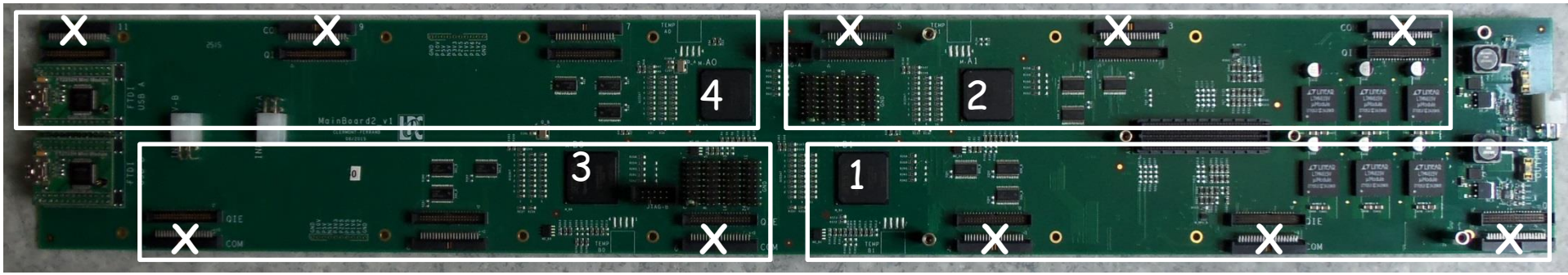
275/277
1.6/1.2

235/233
1.6/1.4

291/286
1.5/1.3

180/183
2.1/1.4

36(280mm) 34(175mm) 32(60 mm) 30(55 mm) 28(60 mm) 26(175 mm)



35(175 mm) 33(60 mm) 31(55 mm) 29(60 mm) 27(175 mm) 25(280 mm)

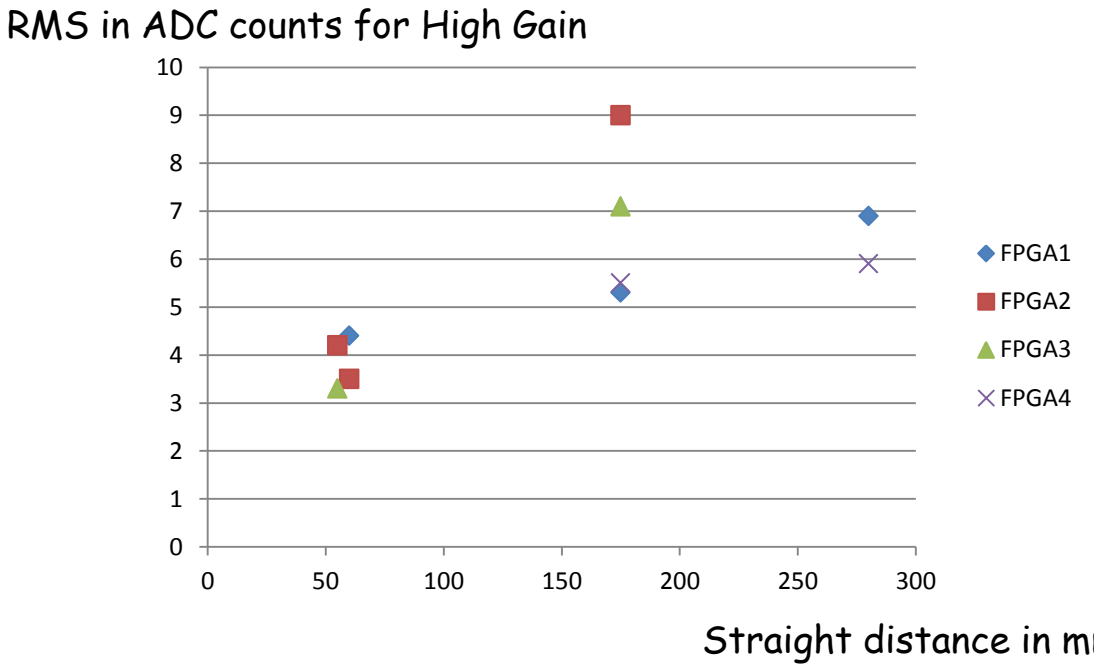
237/229
1.9/1.3

188/171
1.7/1.5

256/246
2.0/1.3

286/287
1.5/1.4

209/211
1.8/1.4



Conclusion:

- Pedestal peaks comparable to the individual results of PMT Blocks alone.
- Pedestal shapes and/or RMS values are better for channels close to their FPGA, and slightly above the individual RMS results:

Examples for HG: # 28: 3.5 (8.4 fC) instead of 2.6 counts (PMT Block alone)
31: 3.3 (7.9 fC) instead of 2.6 counts
30: 4.2(10.1 fC) instead of 3.1 counts
29: 4.4 (10.6 fC) instead of 3.2 counts

Comment: The set-up is more complete with respect to PMT Block alone.

- Pedestal shapes and/or RMS values worst for channels far from their FPGA.

Warning: this RMS should be better if we considered only High Frequency noise.