# ATLAS FastTracKer

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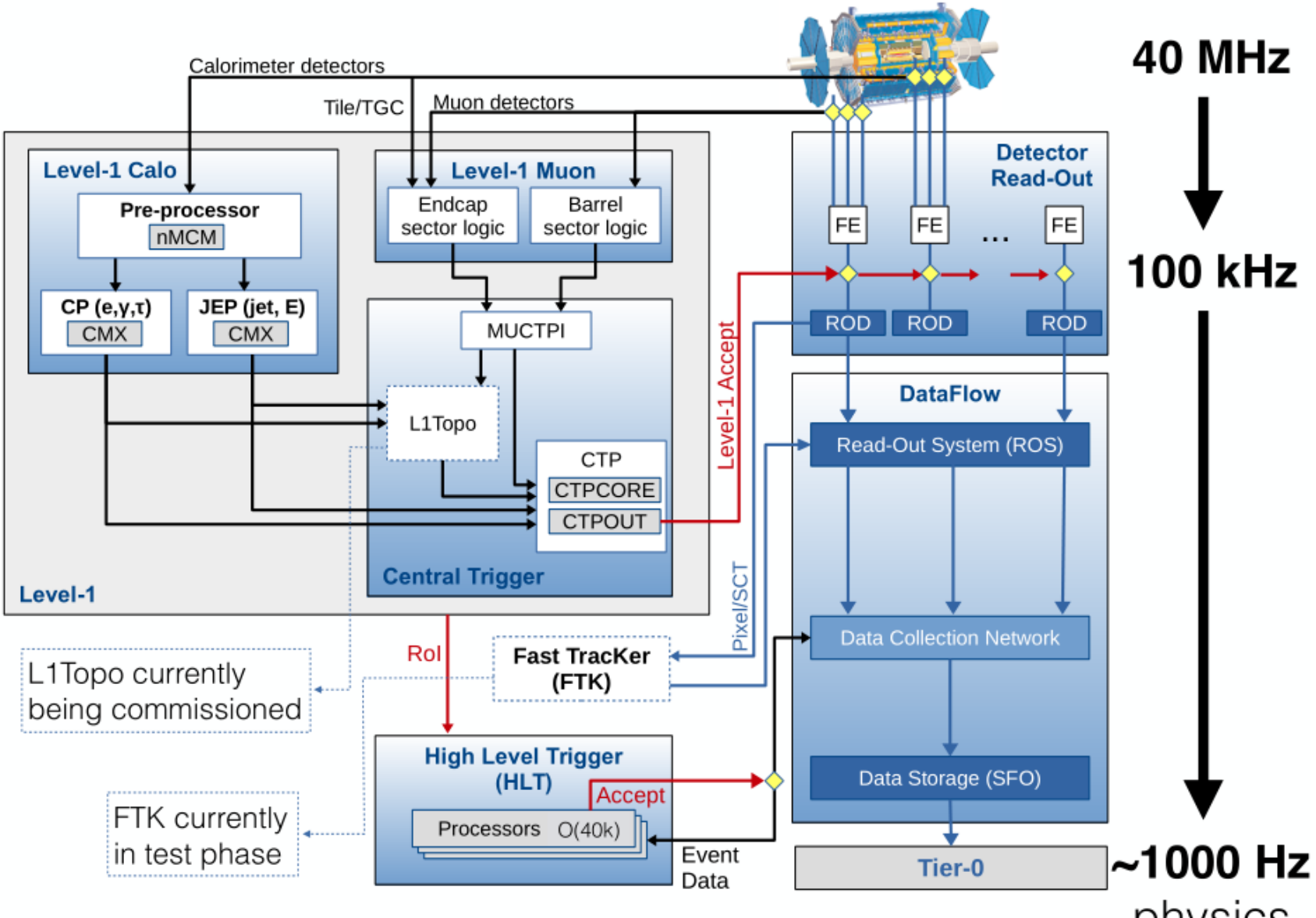
# ATLAS FastTracKer

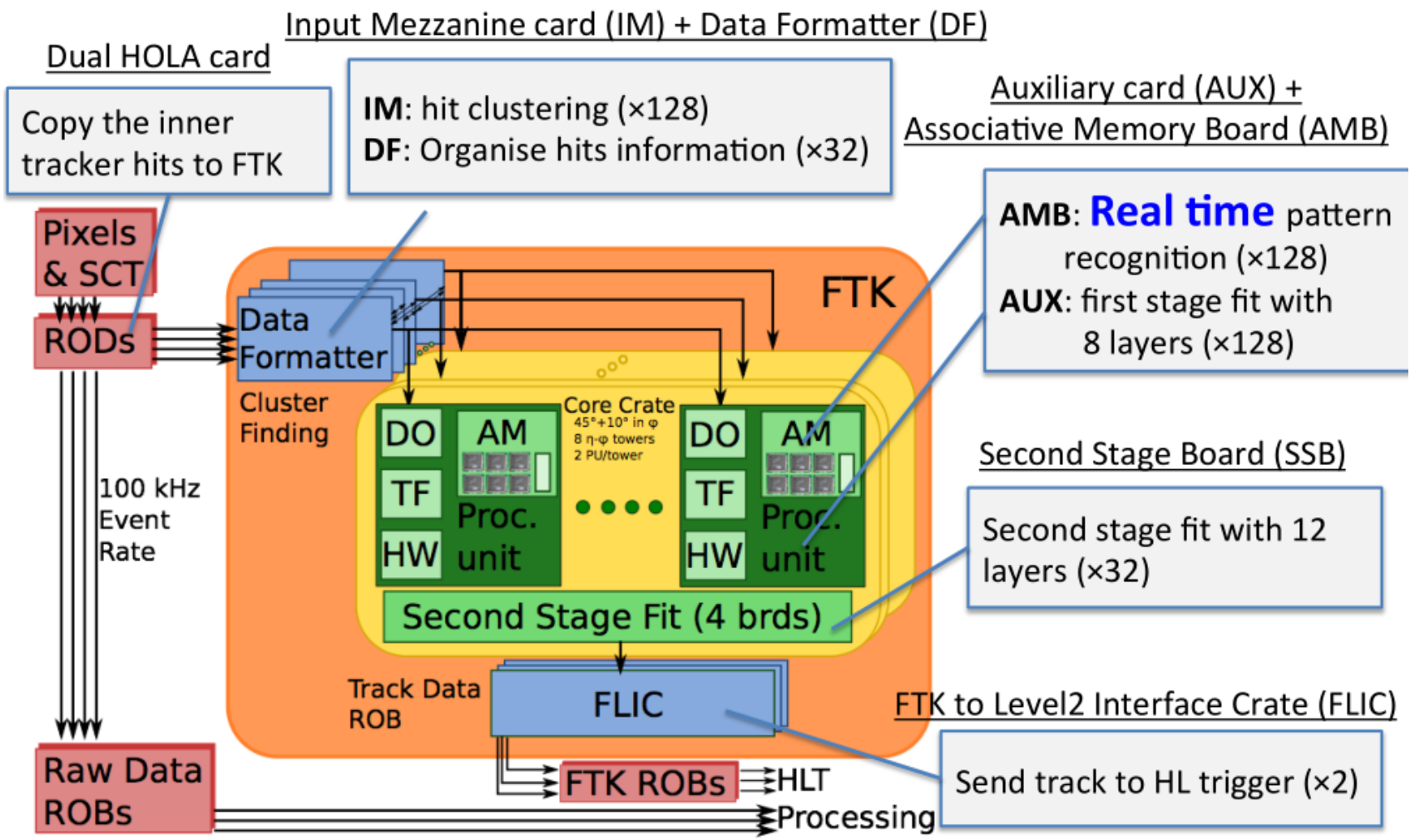
- Dedicated hardware (ASIC + FPGA)
- Full detector charged particles trajectory reconstruction (> 1 GeV)
- Data accepted by L1: 100 kHz event rate
- Real time: 100 $\mu s$ latency
- Tracks data feed to HLT for trigger decision (Vertexes, Bjet, MET, ...)

Staged installation: barrel-only in 2016 for commissioning → full detector 2017 50% power → full detector 2018 100% power

# Trigger structure - current

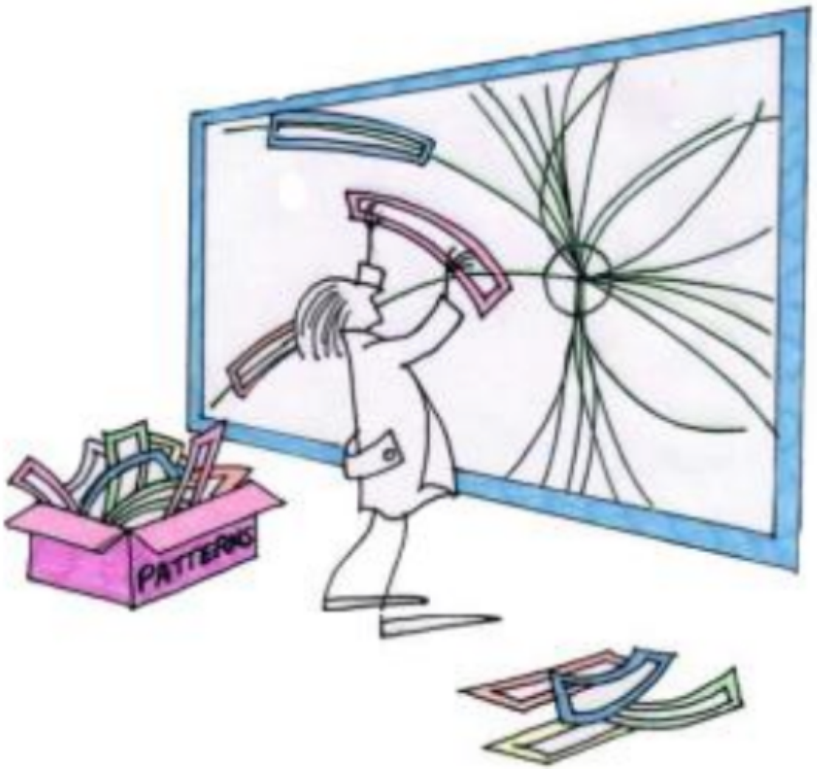


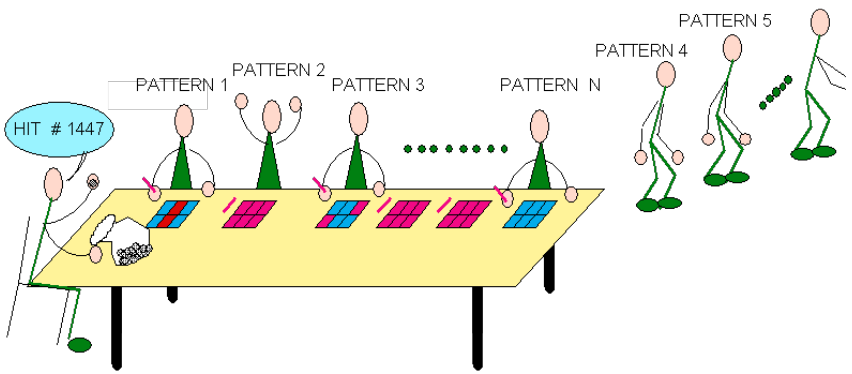
# FTK structure



# Associative memory

- Pattern recognition
- Finds correlation between event data (a collection of hits on N layers) and a pre-stored bank of trajectories (Ntuple of hits, one per layer)
- The search for patterns is done in real time during event readout
- Each stored pattern memory element has the logic to compare itself to the data and declare a match (like Bingo game)



# Bank production / optimization

- FTK efficiency depends on pattern bank quality
- Pattern banks must be optimized
  - LHC parameters (pile up events, beam spot, ...)
  - Bank size (how many AMchips are available in the system)
  - Number of linearized fits (how many fits/s can be done in the FPGA)
- Continuous effort to improve and adapt

Carlo Pandini, Louis D'Eramo

# AMchip06

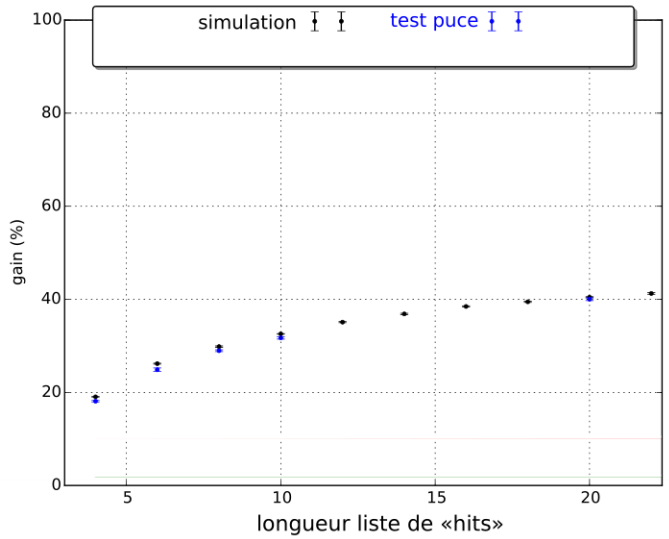

- Digital ASIC
  - 65 nm TSMC
  - 100 MHz
  - 168 $mm^2$
  - 128k 8x16 bit patterns
  - Flip-chip BGA
- Full-custom CAM cell
  - XORAM technology (original)
  - Optimized for low power
- Power consumption is related to data (avg 3 W)

**Design**: coordination, VHDL and final assembly LPNHE+INFN Milano.

**Testbench**: firmware, software done by LPNHE.
Main reference testbench at LPNHE.

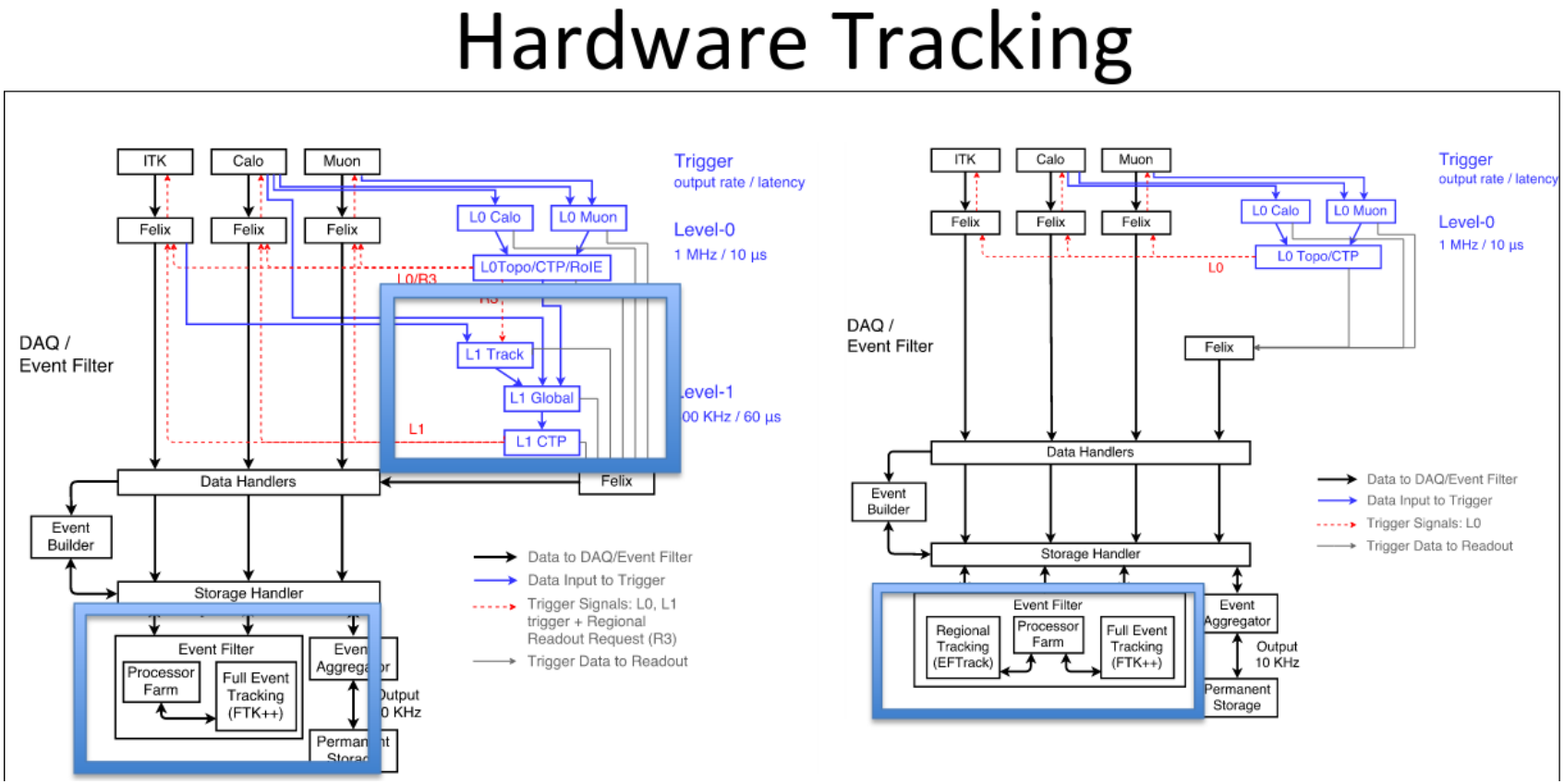
# Hits re-ordering

- Event hit data is streamed in the chip (one hit per clock cycle)
- Power consumption depends on Hamming Weight between subsequent hits
  - Peak consumption $\sim$ max Hamming Weight
  - Average consumptio $\sim$ avg Hamming Weight
- Idea: on the fly hit stream re-ordering to reduce Hamming Weight

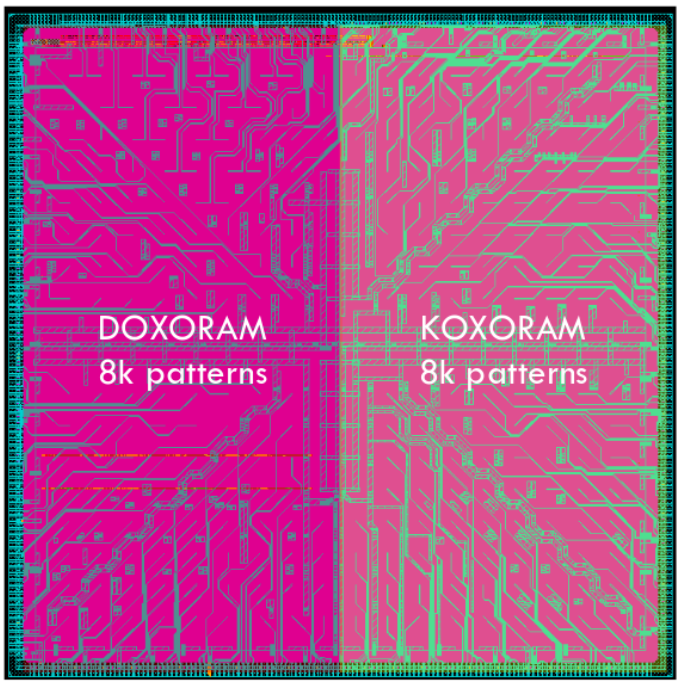



**Proof-of-concept**: Louis D'Eramo (qualification for ATLAS Authorship)
**FPGA Algorithm**: Olivier Le Dortz (algo ready, to be tested).

# Trigger structure - Phase-II



# AM07B

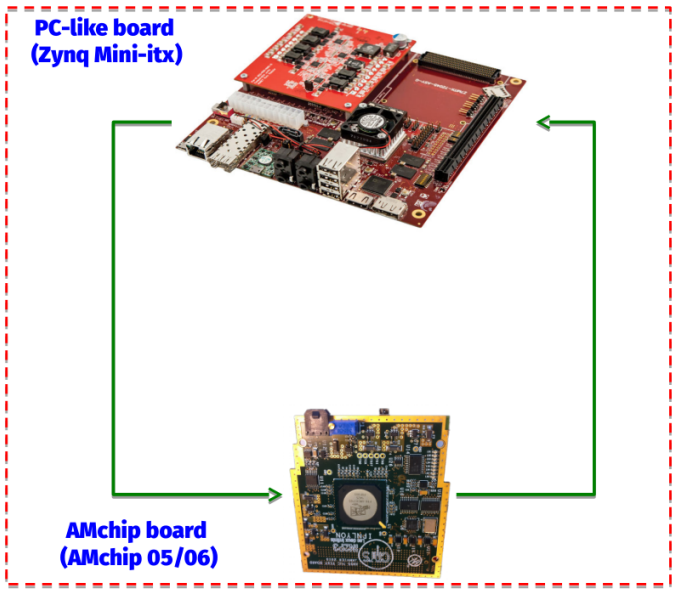



- 28 nm TSMC
- 200 MHz (next prototype will target 250 MHz or 500 MHz)
- 16k patterns with different CAM tech
  - KOXORAM (very low power, slower)
  - DOXORAM (low power, faster)
- Explore package options
  - Standard BGA
  - System-in-Package: AM+FPGA

**Coordination & funding**: AM07B is financed by ANR FastTrack
**Chip final assembly**: final timing closure of the chip done by LPNHE & INFN Milano like AM06

# AM-powered PC

- Zynq board
  - PC-like (video/keyboard/mouse/disk)
  - ARM CPU
  - Kintex-class FPGA
- FMC slot
  - AMchip card designed by IPNL (ANR FastTrack)
- Applications
  - **Genomics**
  - FTKsim acceleration
  - ...

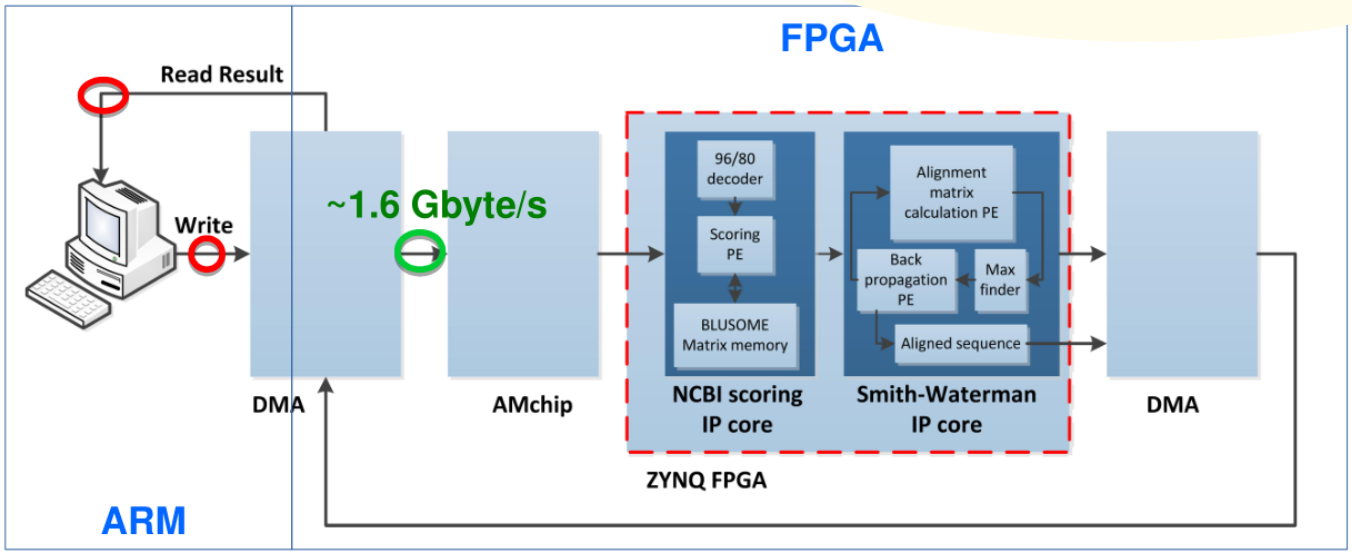



**Genomics**: M. A. Mirzaei et al., "A Novel Associative Memory Based Architecture for Sequence Alignment," 2016 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), Chicago, IL, 2016, pp. 473-478. doi: 10.1109/IPDPSW.2016.21

# AM-powered PC

FPGA Core for Genomics

30x30 sequence analysis with 68% of FPGA




**Optimization of data transfer**

| | GPIO | DMA | DMA |
|---|---|---|---|
| speed | 10 KByte/s | 250 MByte/s | **1.4 GByte/s** |
| library | | EasyDMA | Libganet |

V. Voisin and A. Mirzaei

# Conclusions

- ATLAS FastTracKer is an upcoming upgrade for the ATLAS trigger
- LPNHE is present in this effort
  - Key element: Associative Memory
  - Pattern bank studies
  - FPGA/boards contribution
- It is a great opportunity for students (qualification task, operations, performance, ...)
- Technological program stretching up to LHC Phase-II
  - Associative Memory will be in the Phase-II trigger of ATLAS (and CMS?)
  - Very challenging program
- Opportunities for applications beyond LHC and beyond physics