ATLAS Group LPNHE

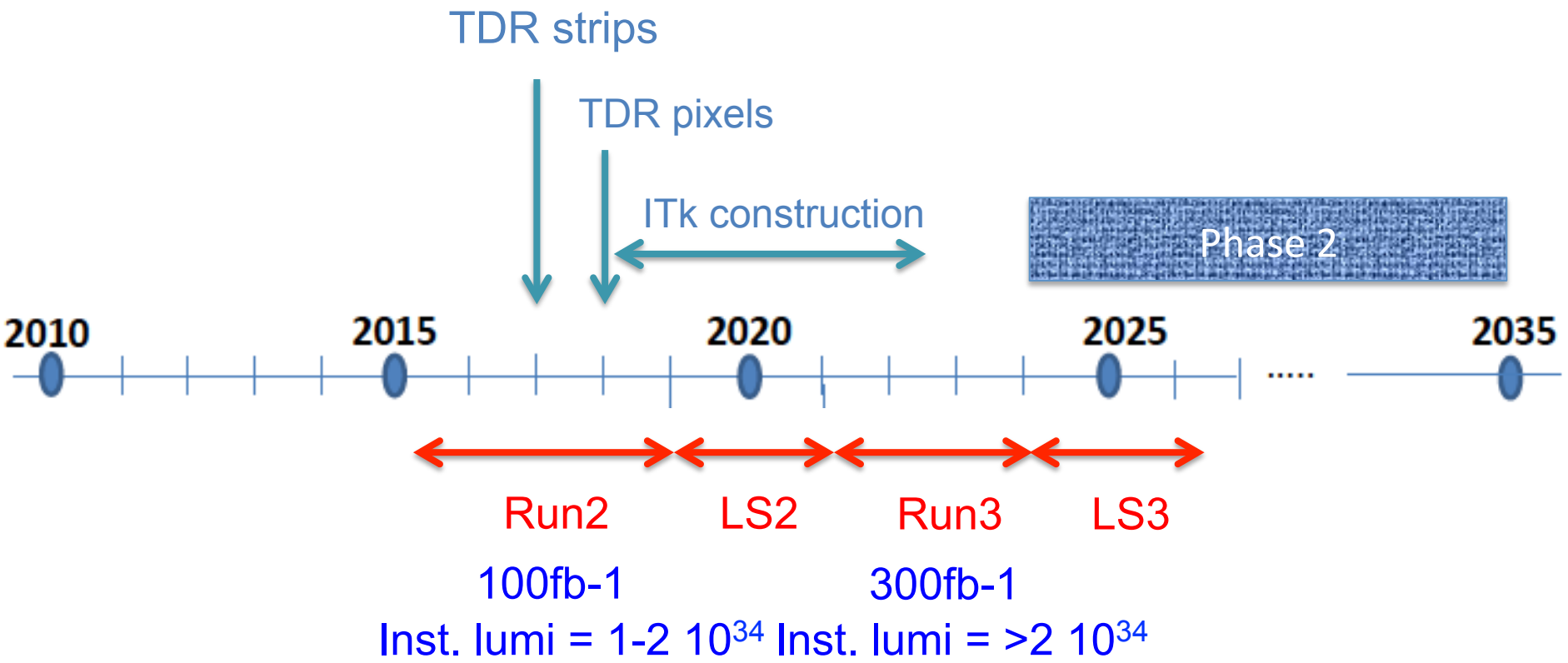
ATLAS upgrade activities

Biennale du LPNHE
Tirrenia (Pise)

4-7/10/2016

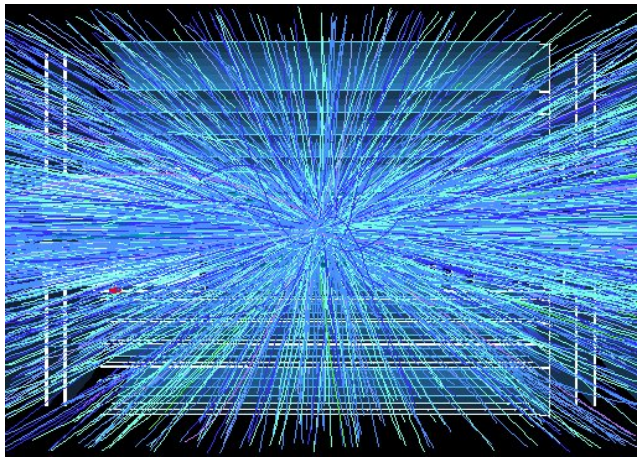
LPNHE
PARIS

The ATLAS roadmap in the LHC upgrade



High luminosity consequences for the ATLAS tracker

After Run 2-3 the present detector would not be adequate any more



Instantaneous dose

- pileup and high event rate
- increased occupancy

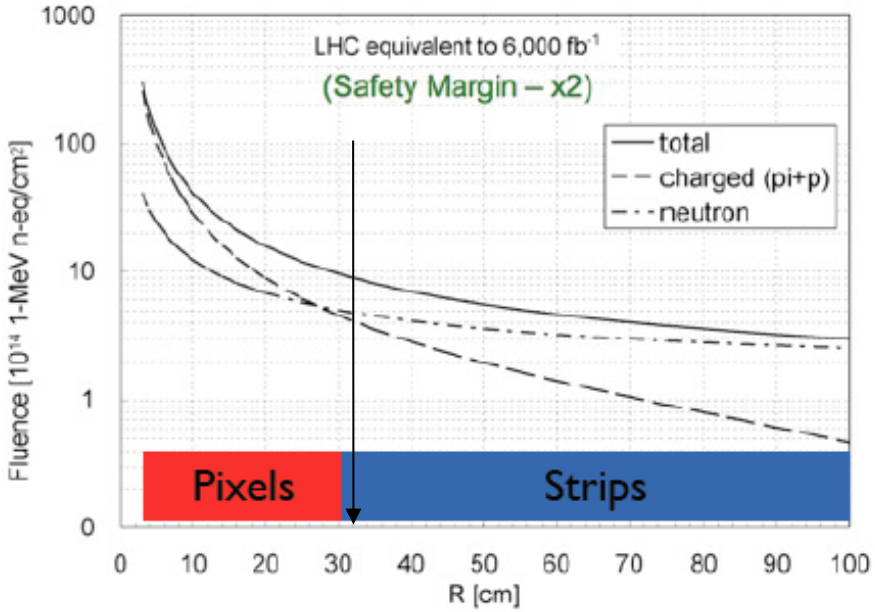
- higher granularity sensor
- SEU-robust chip

Integrated dose

- leakage current
- change in operation voltage
- reduced charge collection

- rad-hard components

fluence for the innermost pixel layer:
1-2 x 10^{16} n_{eq}/cm^2 (3 ab^{-1})



ATLAS LPNHE group activities

Sensors

- Simulations
- Active edge sensors
- More test of earlier productions
- Status of production 2016: FBK-AE3
- Sensors/measurements for HGTD

Electronics

- RD53
- FastTrack (+genomics)

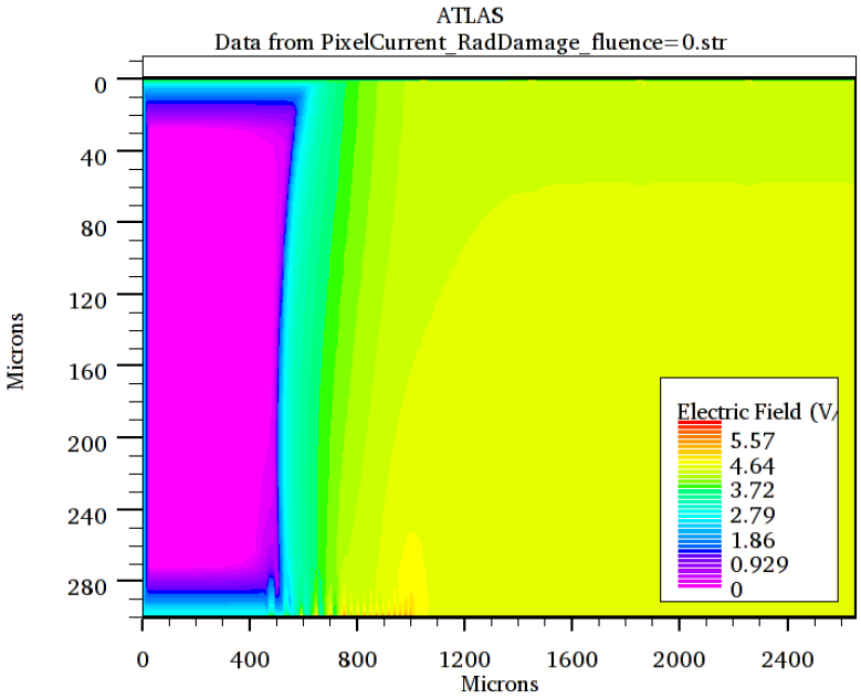
Mechanics

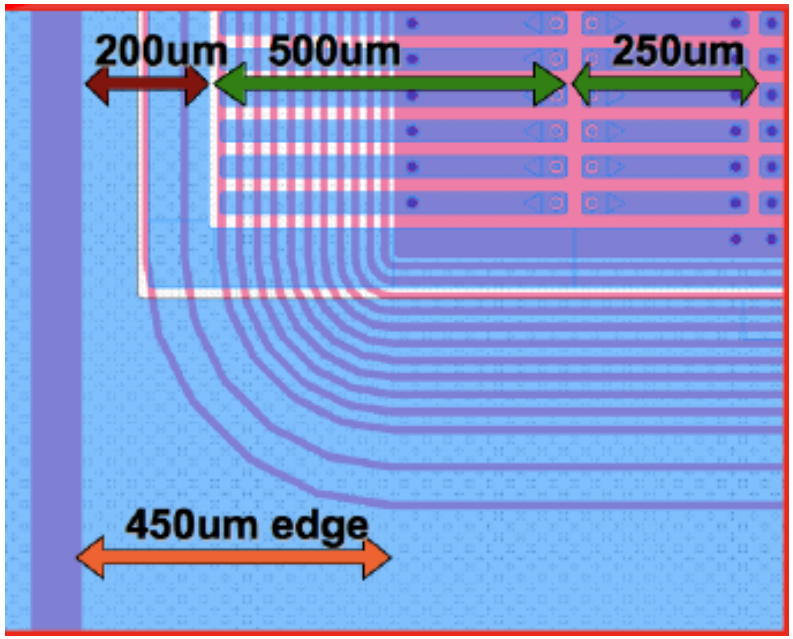
- Micro-channels
- AIDA-2020

ITk upgrade construction

Simulations

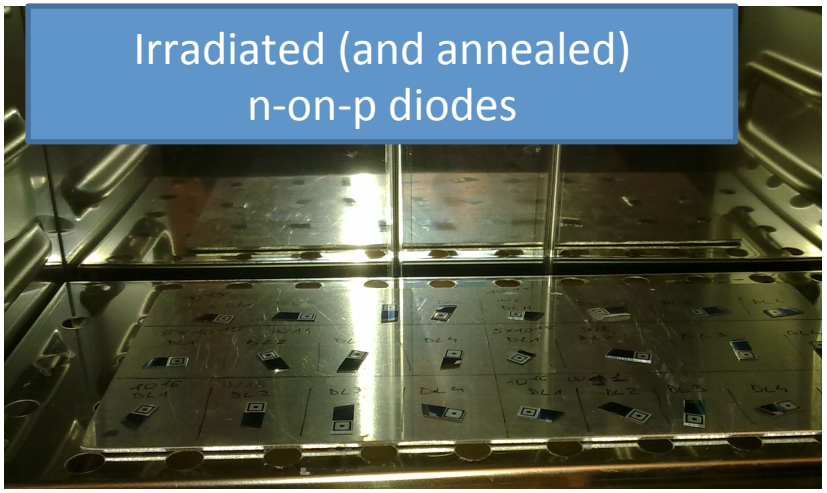
Critical tool to optimize the sensor production before sending the layout to the foundry

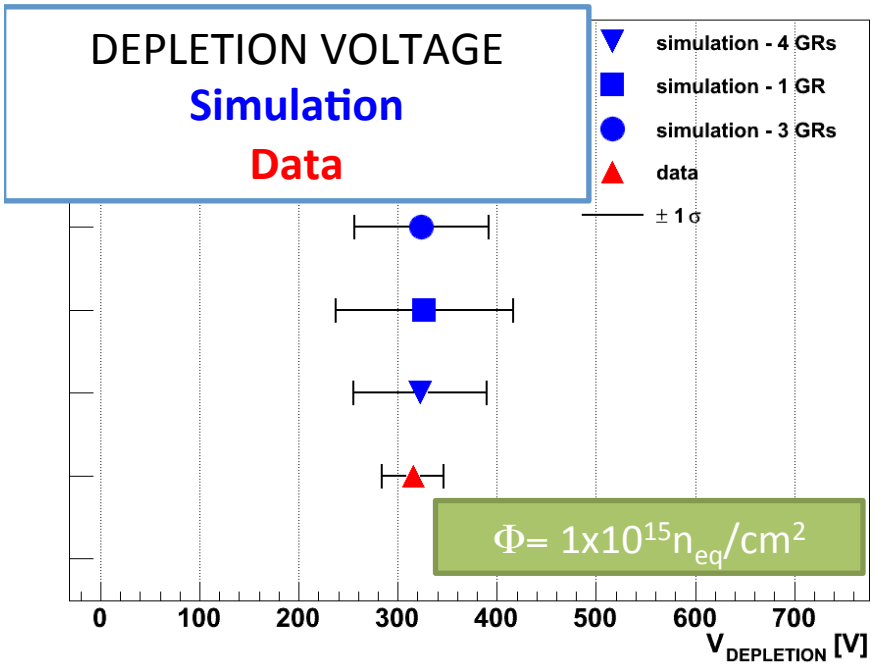


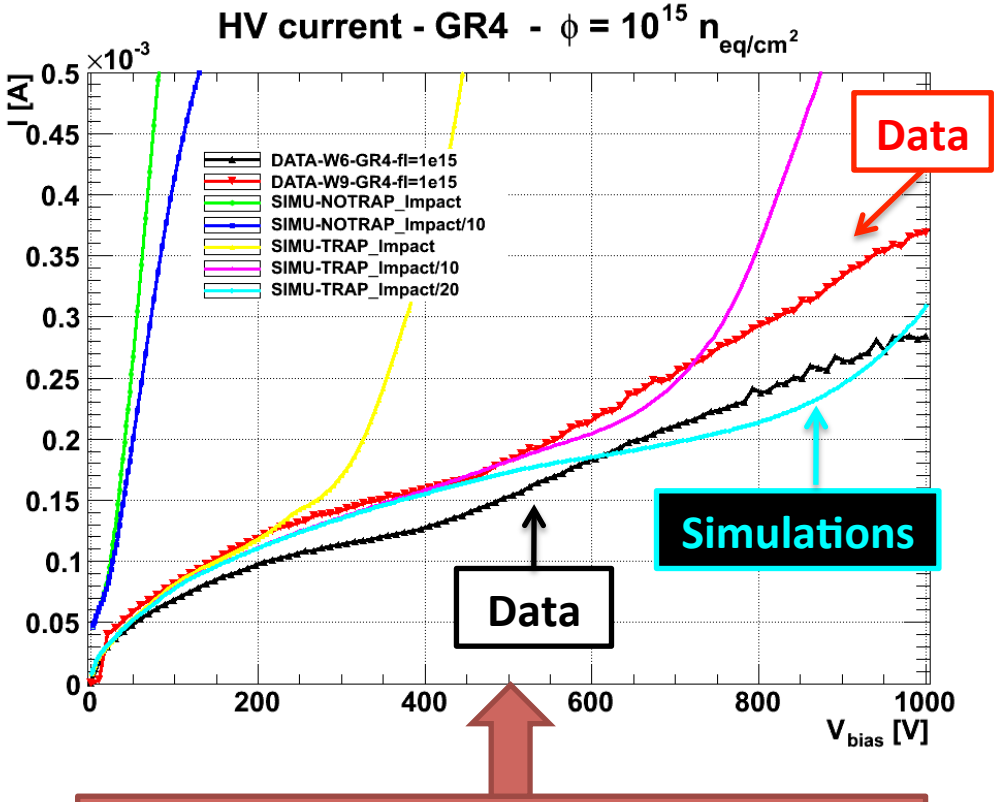


For instance for the IBL we used simulation to demonstrate that pixels could be pushed below the guard ring region.
It was done and we recovered almost 1mm of dead region

Simulations and model development







A lot of work for impact ionization models and interface traps and charges

On going effort with RD50, PSI, Uni PG, Uni TS, CNM & FBK

6

https://indico.in2p3.fr/e/simdet2016

SIMDET 2016

2e Ecole de simulation de détecteurs silicium

LPNHE - Paris

du 05 au 07 septembre 2016

Comité scientifique

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CALDERINI Giovanni LPNHE Paris
CLEMENS Jean-Claude CPPM Marseille
LAVERGNE Laurence LPNHE Paris
LIMOUSIN Olivier CEA/IRFU Saclay
LOUNIS Abdenour LAL Orsay
MARCHIORI Giovanni LPNHE Paris
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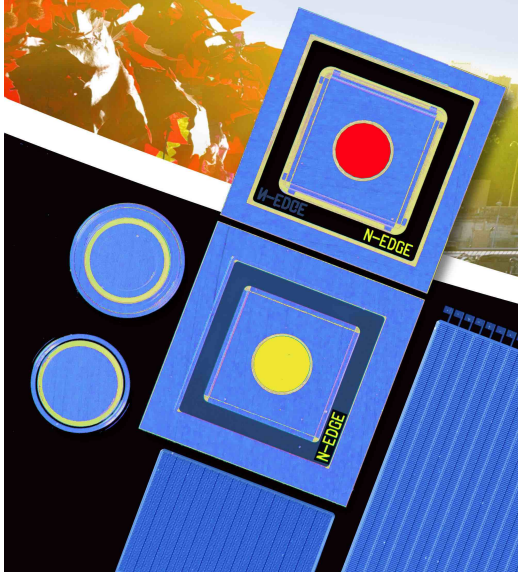
MARQUET Laurence
MARCHIORI Giovanni
MENDOZA Victor

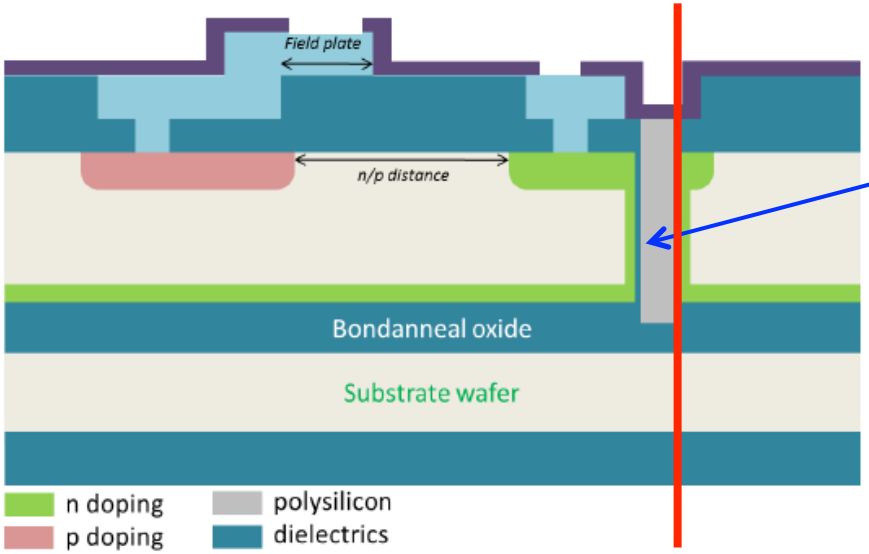


simdet2016@lpnhe.in2p3.fr

Bruno Mazoyer - LAL Orsay 2016

Sensors: active-edge concept

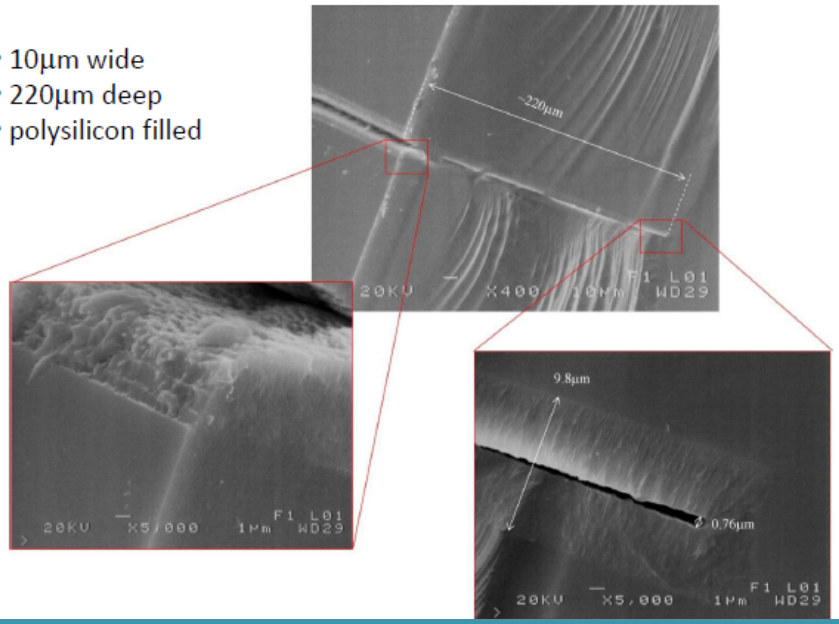
FBK(Trento)/LPNHE collaboration for active-edge detectors



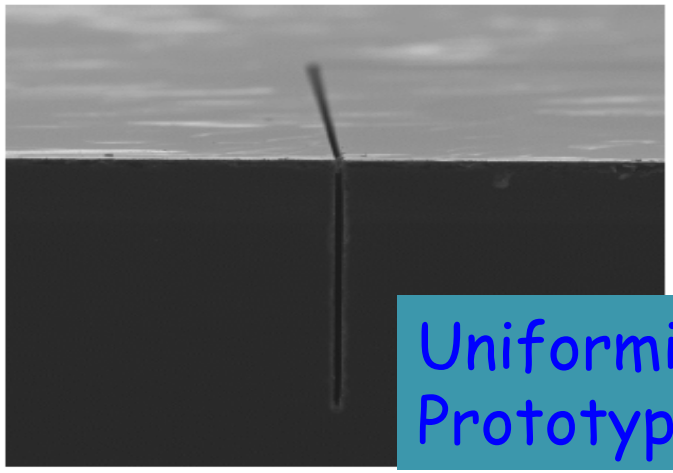
Deep trench diffusion (to prevent electrical field on the damaged cut)

Cut line

- 10µm wide
- 220µm deep
- polysilicon filled



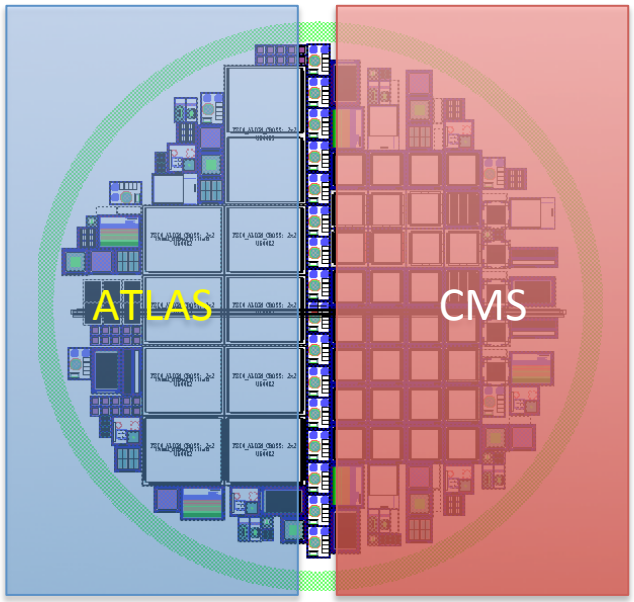
4,5µm wide
220µm deep

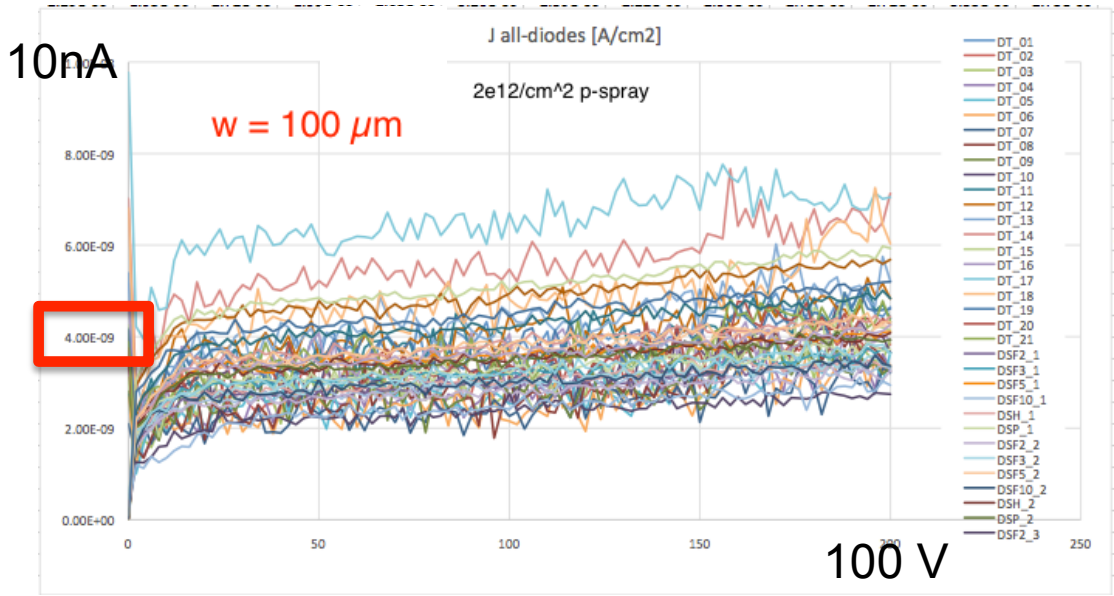


Uniformity of trench filling is critical.
Prototypes production under way, good results

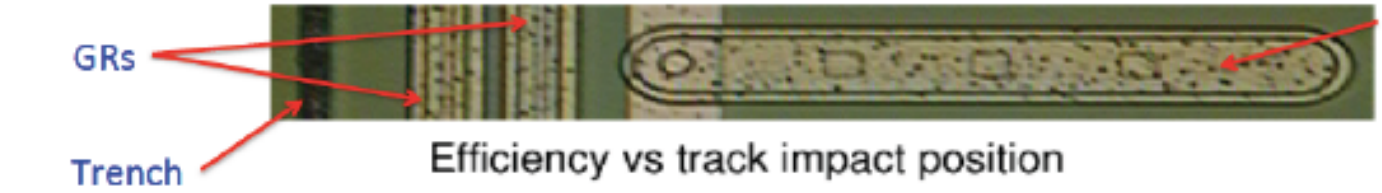
Earliest productions: FBK 2015

- Joint FBK-INFN-LPNHE production at FBK
- 2015: exploratory planar production at FBK on 6" Silicon on Silicon (SiSi) wafers.
- Sensor wafer thicknesses: 100 µm and 130 µm
- Shared ATLAS and CMS production
  - 10 FEI4 (ATLAS) + 30 PSI46 (CMS); and many test structures`



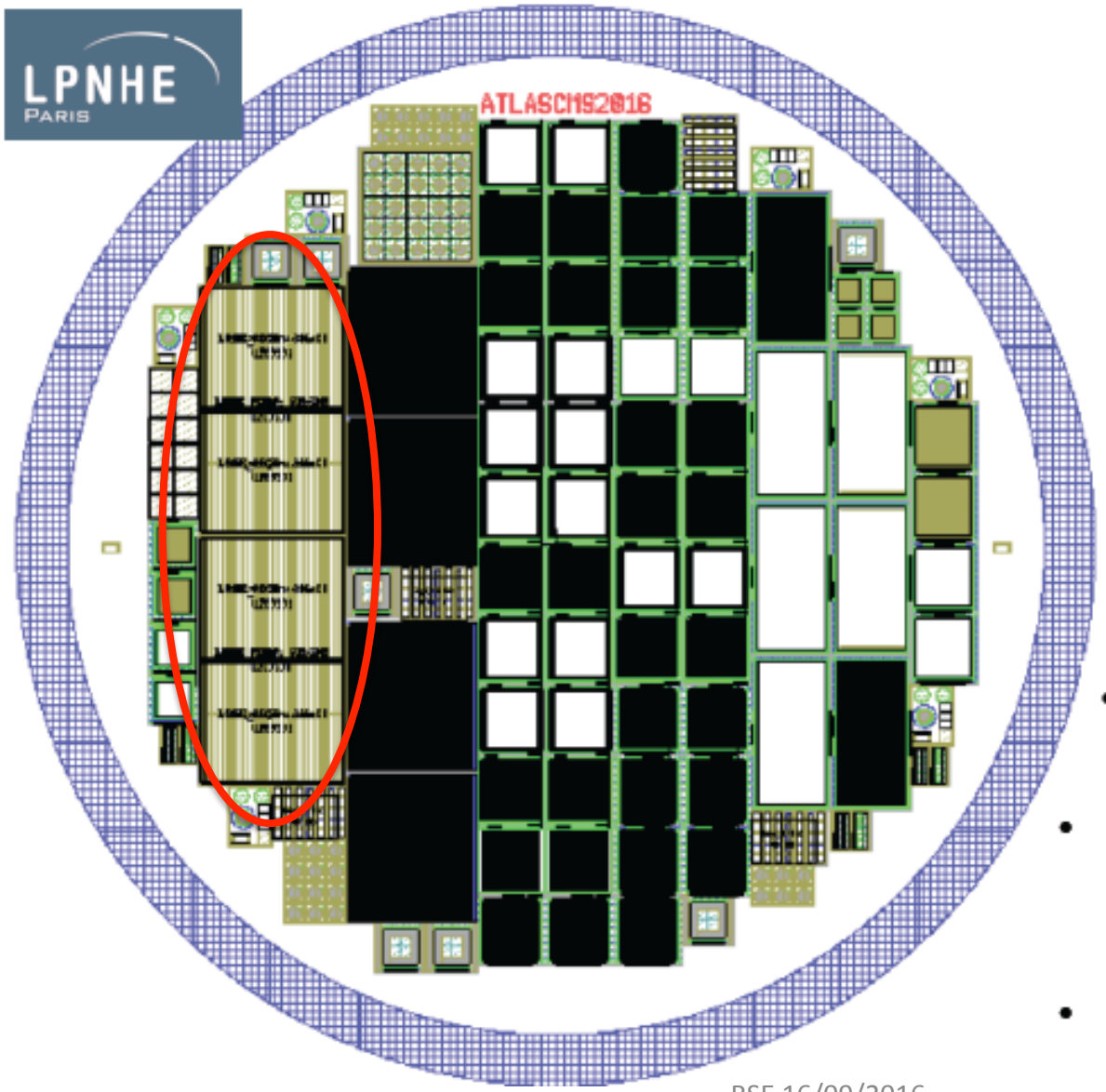


Results from ITk testbeam 2016



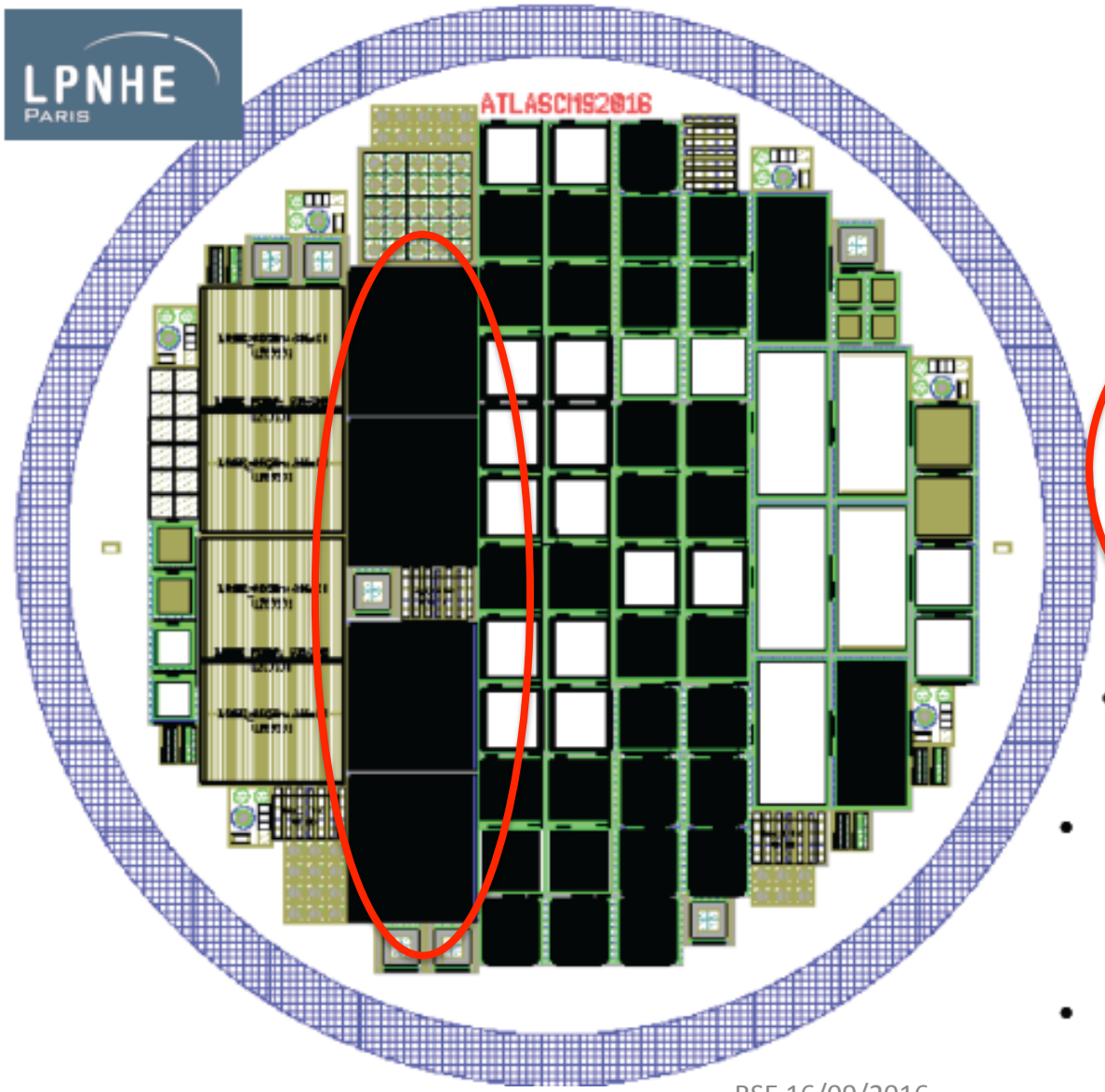
- ITK test-beam at CERN-SPS
- Active edge processing at FBK
- 200 um thickness
- 2 floating guard rings

Production 2016 in FBK 6" active edge



- 6" planar Si-Si production
- 100 and 130 µm thin sensors
- Active edge technique
- Shared Atlas-CMS
- 2 Alpines
- 4 FEI4B sensors
  - 2x 50 µm pixel-to-trench, 0 GRs
  - 1x 75 µm pixel-to-trench, 0 GRs
  - 1x 75 µm pixel-to-trench, 1 GR
- 7 RD53A compatible sensors
  - 50x50 and 25x100 µm²
- Etching trials completed on test-wafers for the new geometry of staggered trenches
- End of the production: October

Production 2016 in FBK 6" active edge



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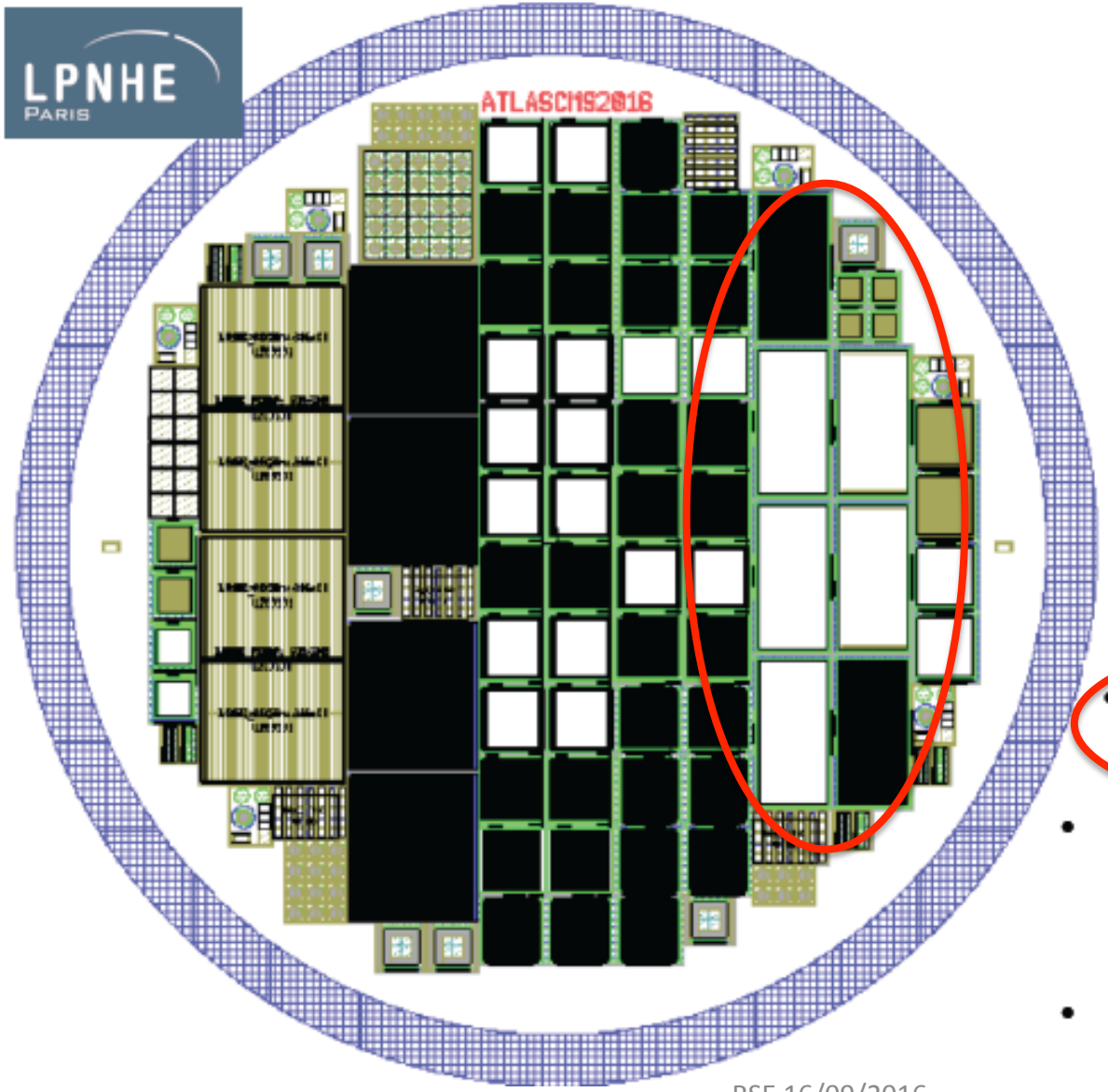

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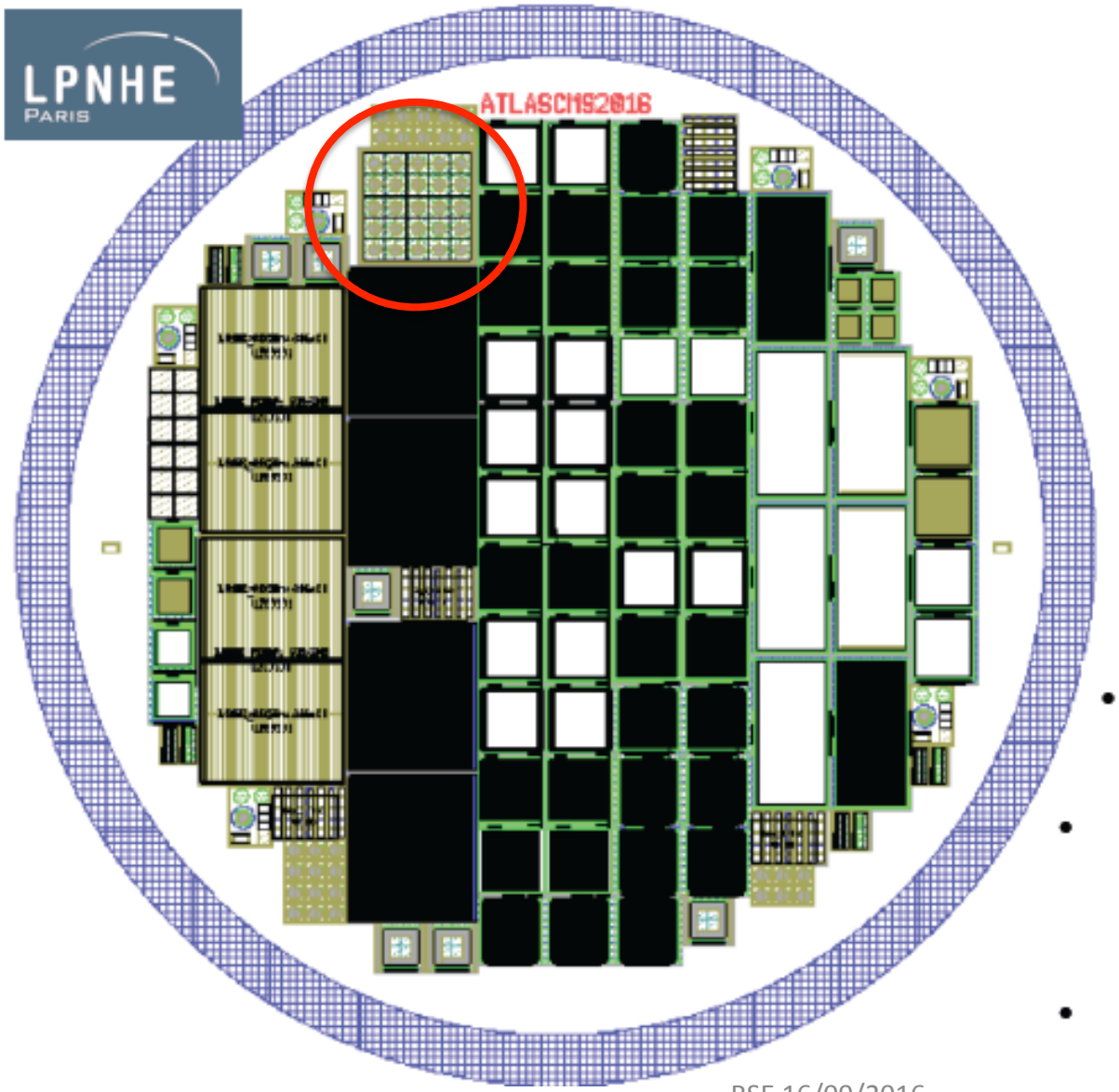

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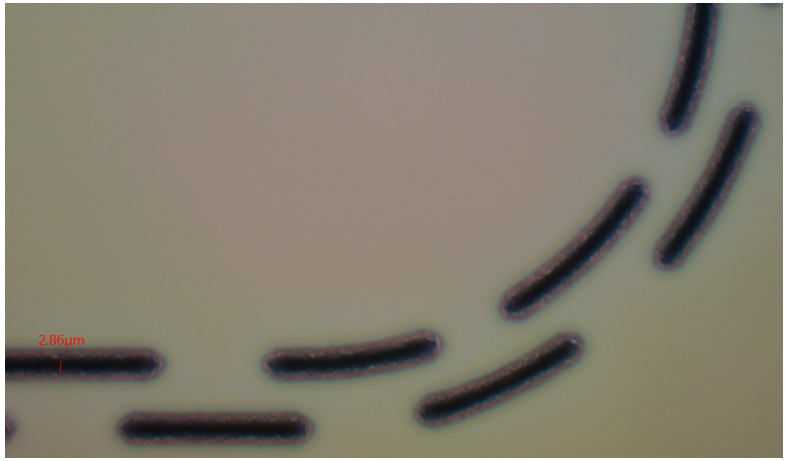
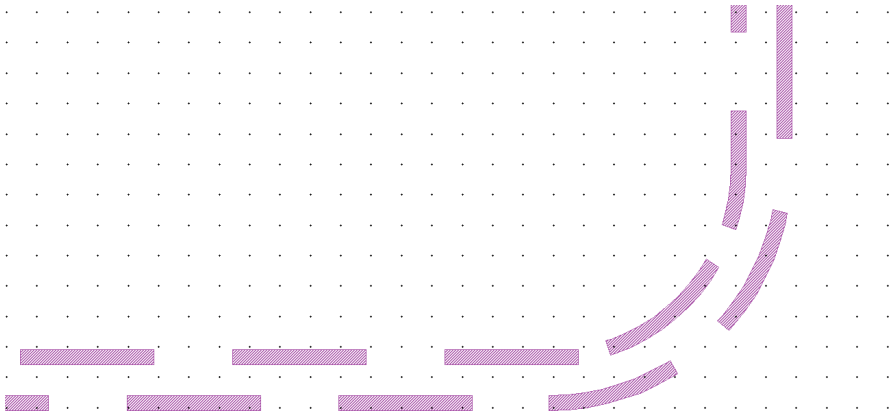
- End of the production: October

One specific feature

Dashed deep trench





This allows sensors to remain connected to wafers even if we back-thin support

Electrical properties unaffected

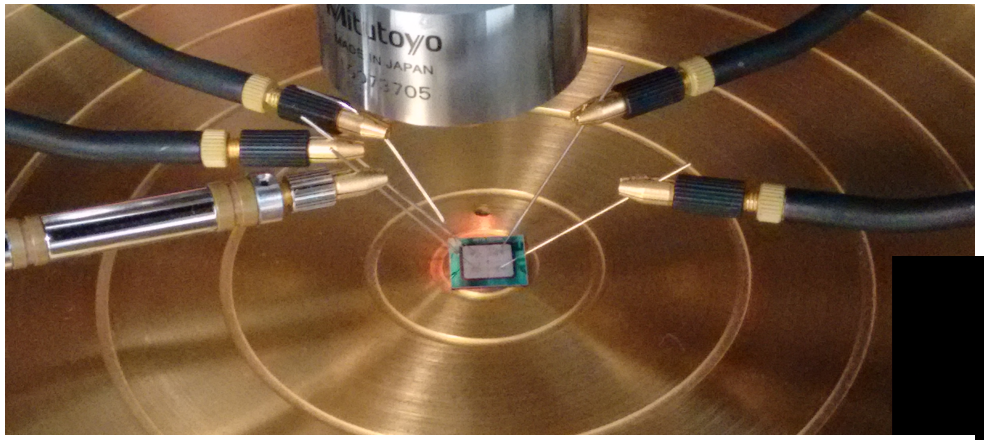
Production expected in October

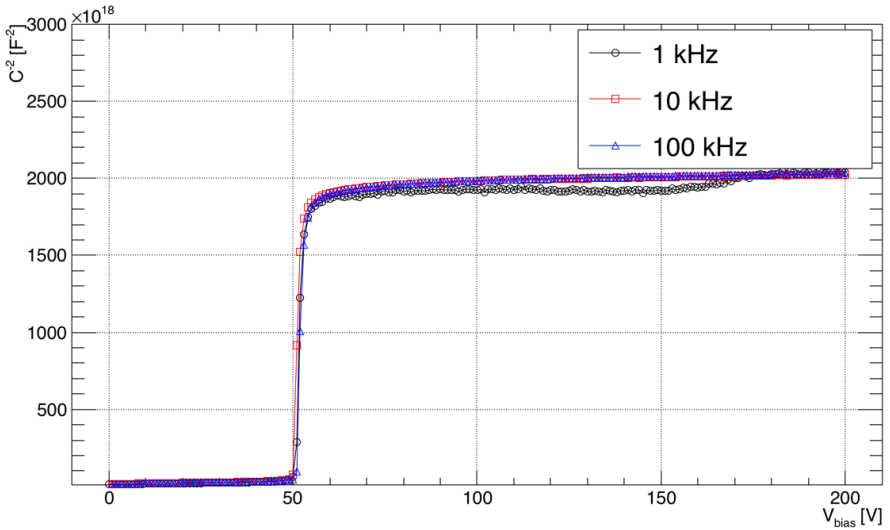
Sensors for HGTD

FBK Trento production (already shown)

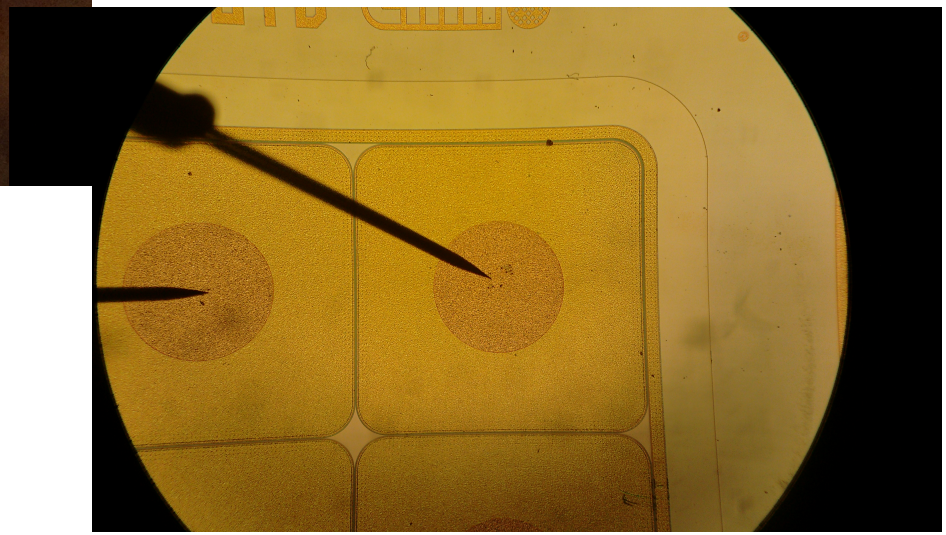
CNM (Barcelona) production (LGAD)

Tested at LPNHE





Different structures
- LGADs
- PIN diodes



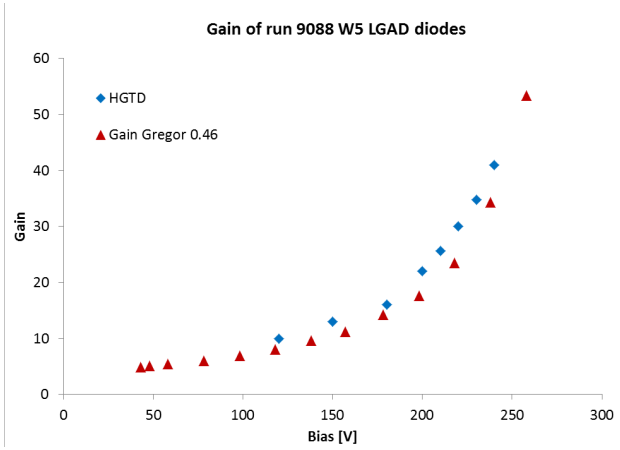
Example: Pads 2x2,
9 mm^2 50 um thick

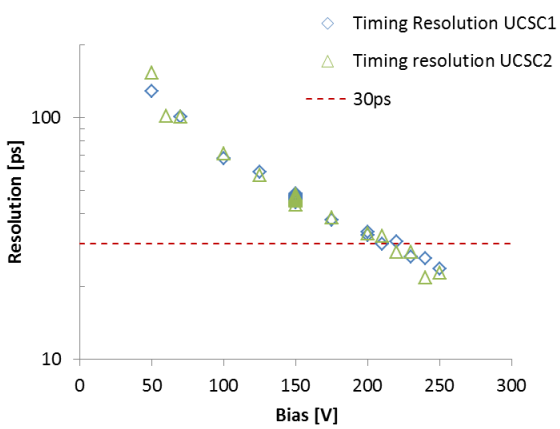
HGTD Sensor Status

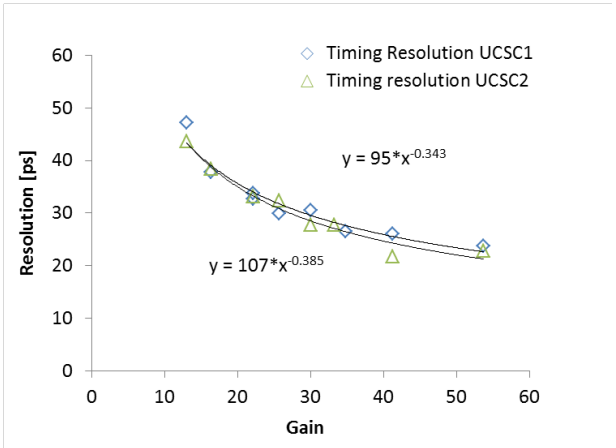
- The 45 µm sensors produced by CNM in the RD50 sponsored Run #9088 validate the principle of thin LGAD as timing detector.
- Timing resolutions of below 30ps were measured in two beam tests with 1.2mm LGAD (single pads).
- A stack of 3 UFSD reached a timing resolution of 15ps. https://arxiv.org/ftp/arxiv/papers/1608/1608.08681.pdf
- LGAD of 1.2mm (single pads) and 3.2mm (2x2 arrays) were produced.
- The stability of operation for small pads is good up to a gain of about 40.
- Testing was done by CNM, LPNHE, UCSC, IFAE, Ljubljana, INFN Torino

Gain M = Collected Charge/0.46fC

Good matching of 1mm LGAD
Timing resolution ~ $M^{-0.36}$







Electronics

RD53: common chip in 65nm for ATLAS and CMS pixels

- Design underway; LPNHE is contributing in Digital Design and I/O groups
- Transmission protocol Aurora 64b66b (VHDL code)

The chip will also be used to characterize the next sensors productions

FastTrack: track trigger for ATLAS; LPNHE and Milan responsible of AM design (Amchip06, 65nm)

- A small quantity of AMchip06 has been **produced and tested and delivered** to be mounted on AMB boards. These boards are under test in Pisa and at CERN (Lab4 & P1)
- The full characterization of AMchip06 is in the final stage: we collected all the data requested in the last Production Readiness Review and we are waiting for the OK to launch the production (15k chips)
- This last step is fundamental to be able to install the full system for data taking in 2017

We produced 9 wafers of AMchip06:
- Produce the first 64 LAMBs for FTK commissioning
- Characterize the chip to verify usage and stability

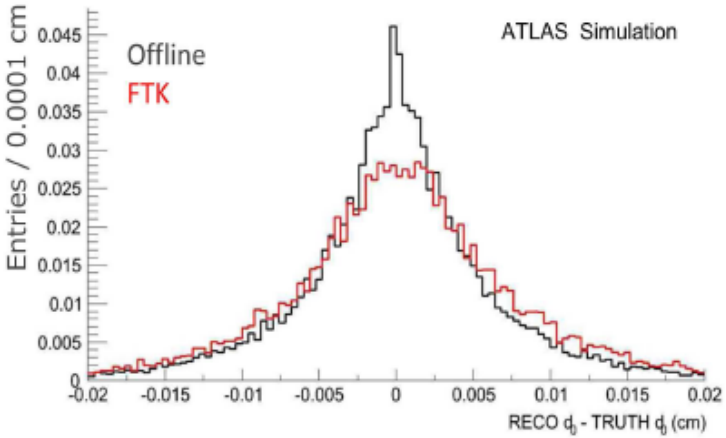
Track trigger (FTK)

Increase in luminosity will oblige to improve trigger performance, by using track information to select certain topologies (ex. impact parameter). Has to be fast, not enough time for pattern recognition

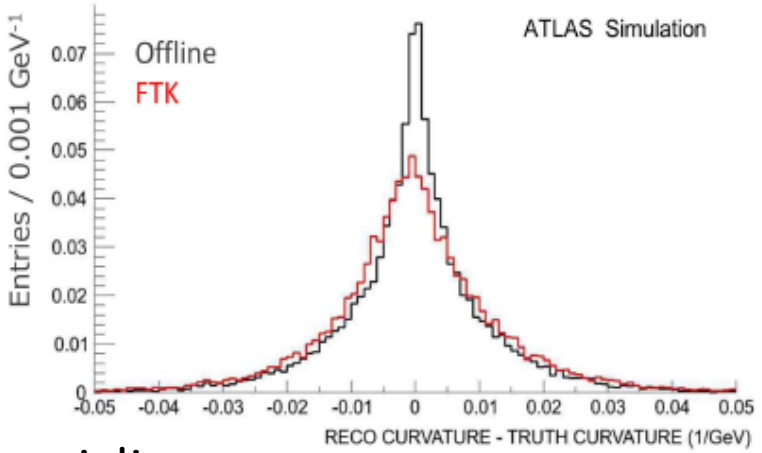
Solution is to use Associative Memories to pre-store patterns of hits. LPNHE responsible of AM chip design (with Milan).

65nm (IMEC) -> 28nm

Impact parameter resolution (FTK vs offline)

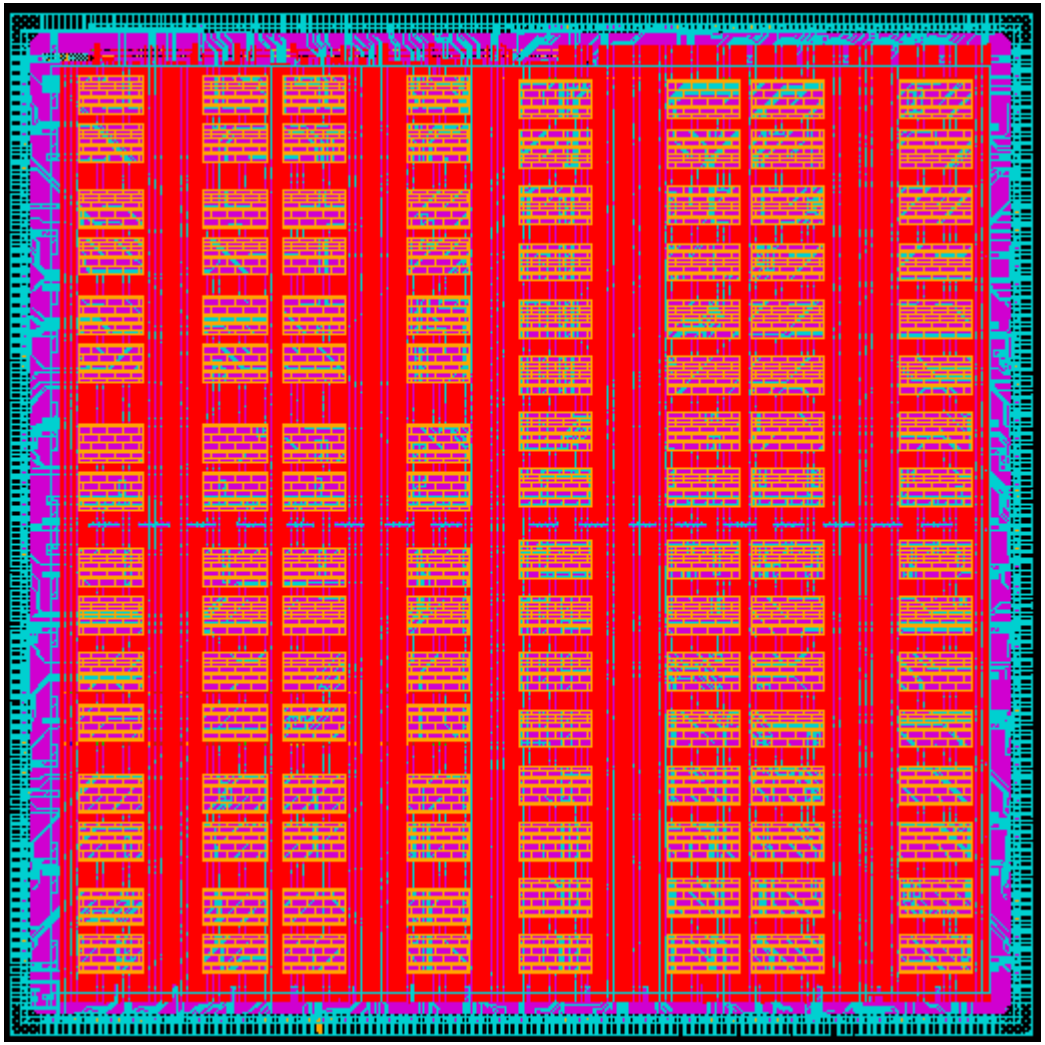


Curvature resolution (FTK vs offline)



See next talk by F. Crescioli

AMchip07 - 28nm



AM07B (INFN + IN2P3)

10 mm2 @ TSMC 28 nm

16k patterns (2 new design by INFN Milano):
- DOXORAM
- KOXORAM

200 MHz matching

7x 18 bit busses single ended
1x 9 bit bus LVDS (DDR → 18 bit)

LVDS pad designed by INFN Pavia

The design is finalized. We are completing the timing closure. Submission exp. End of September 2016.

AM-only package Jan 2017 – AM+FPGA package Spring 2017

Genomics application (HiCOMB 2016, Chicago)

A Novel Associative Memory Based Architecture for Sequence Alignment

M. Ali Mirzaei, Francesco Crescioli,
Giovanni Marchiori, Giovani Calderini
ATLAS group
LPNHE, IN2P3, CNRS, UPMC
4 Place Jussieu, Paris 75005, France
Email: mmirzaei@lpnhe.in2p3.fr

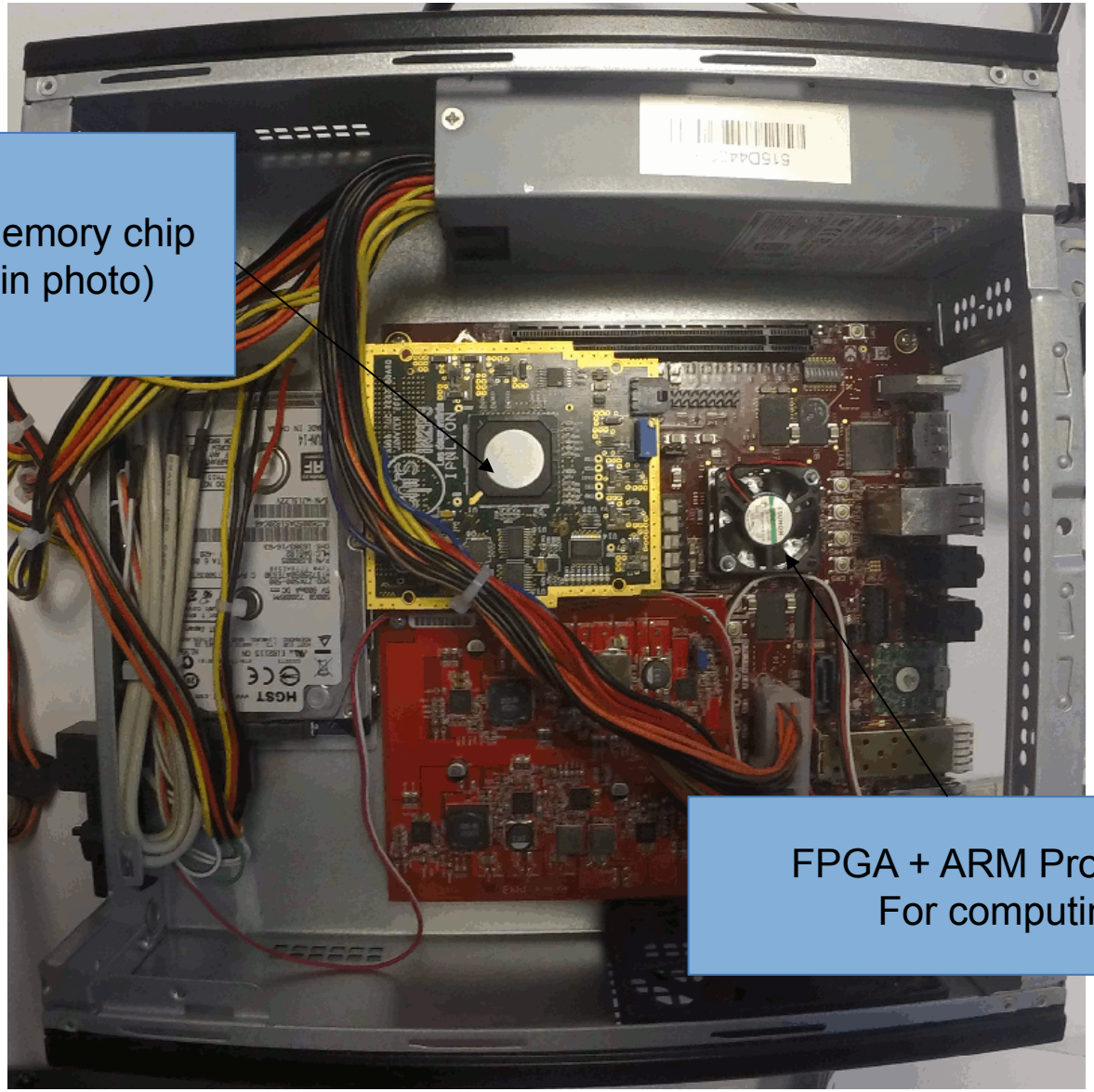
Sebastien Viret, William Tromeur,
Guillaume Baulieu, Geoffrey Galbit
CMS group
IPNL, IN2P3, CNRS, UCBL
4, Rue Enrico Fermi, 69622 Villeurbanne, France
Email: viret@in2p3.fr

***Abstract*—this paper presents a novel hardware architecture based on Associative Memory technology for sequence alignment. The Associative Memory chip (AMchip) architecture employs a huge amount of parallelization to perform real time combinatorial pattern matching. It can be used to perform very**

However, it is also a generic computing element that can be applied into other domains such as image processing [7] and of course bioinformatics, as shown in this document. In bioinformatics, global/local sequence alignment algorithms are comparing biological sequences such as amino

- We are currently implementing a full processing chain (ARM CPU → FPGA → AMchip) using a Zynq board and the Amchip05/06 card developed by IPNL Lyon
  - A fast data transfer system ARM → FPGA is under development
  - The scoring algoritm is under development, integrating the comments received at HiCOMB
  - We target to submit the new work to a conference by the end of the year

ANR FastTrack WP3 System

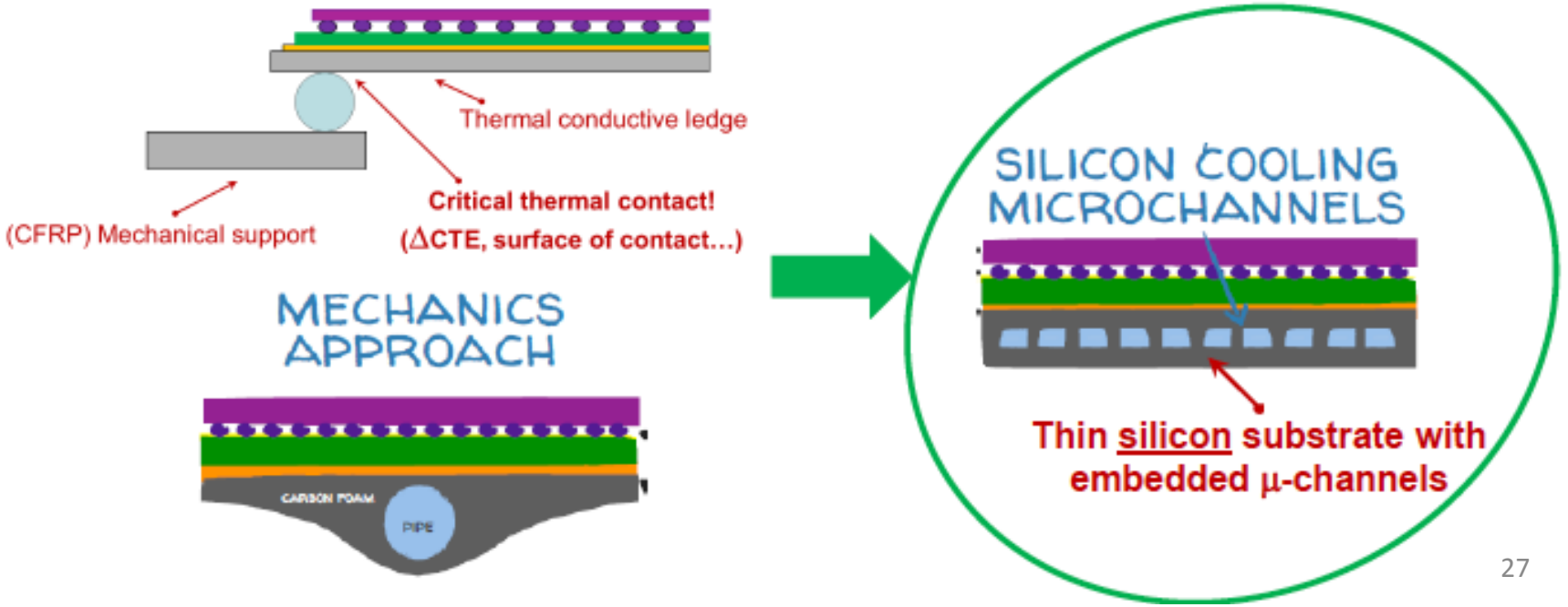


Mechanics

Micro-channels and CO2 cooling

This is progressing significantly

- REFLECS / REFLECS2 (porteur: Bomben)
- GC responsible for u-channel task of WP9 (AIDA-2) and LPNHE beneficiary with the CERN



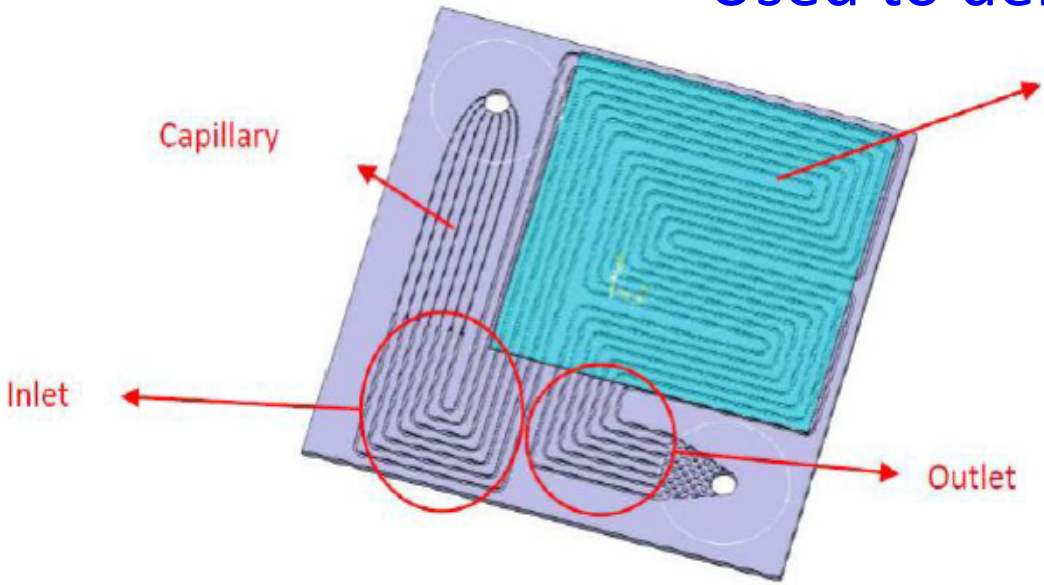
AIDA-2020 WP9: a new Network

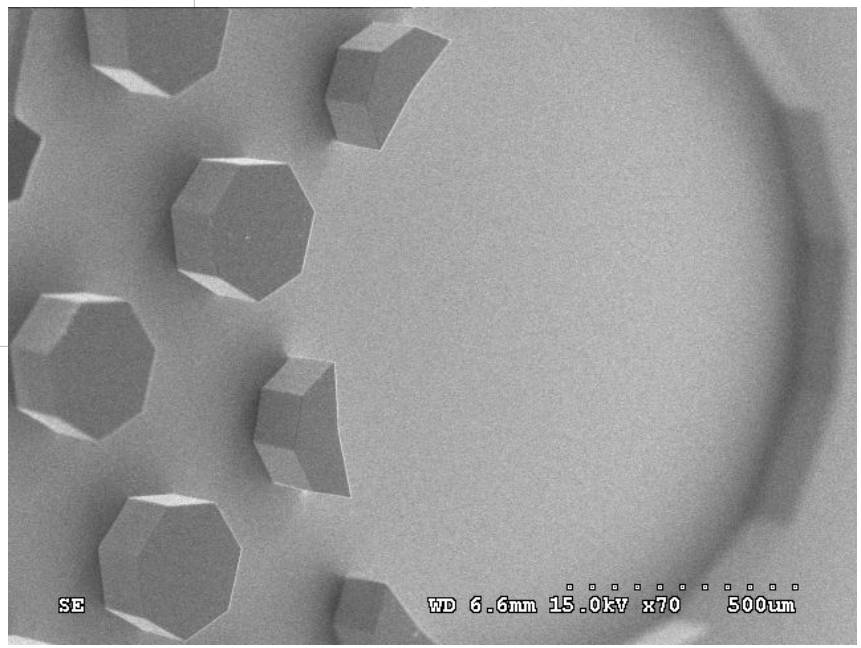
AIDA 2020 WP9 T9.2 Beneficiaries (and friends...)

- **CERN**
  - INFN-Milano (INFN beneficiary in WP 4, 6, 7, 13, 14, 15)
  - UNIMAN (beneficiary in WP 3, 7)
  - University of Twente (external collaborator)
- **CNRS-LPNHE**
  - FBK (beneficiary in WP 7)
  - University of Goettingen (external collaborator)
  - CNRS-LAL Orsay (CNRS beneficiary in WP 1, 2, 3, 4, 6, 8, 9, 13, 14)
  - MPG-MPP Munich (MPG-MPP beneficiary in WP 4, 7, 13, 14)
  - INFN-Pisa (INFN beneficiary in WP 4, 6, 7, 13, 14, 15)
  - University of Padova (external collaborator)
- **CSIC-IFIC**
  - MPG-HLL Munich (external collaborator)
  - UBONN (beneficiary in WP 4, 6)

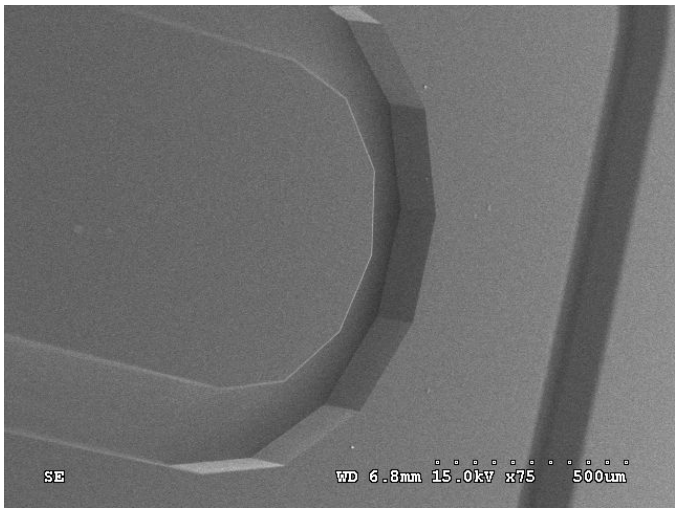
Collaboration with IEF Orsay and FBK Trento

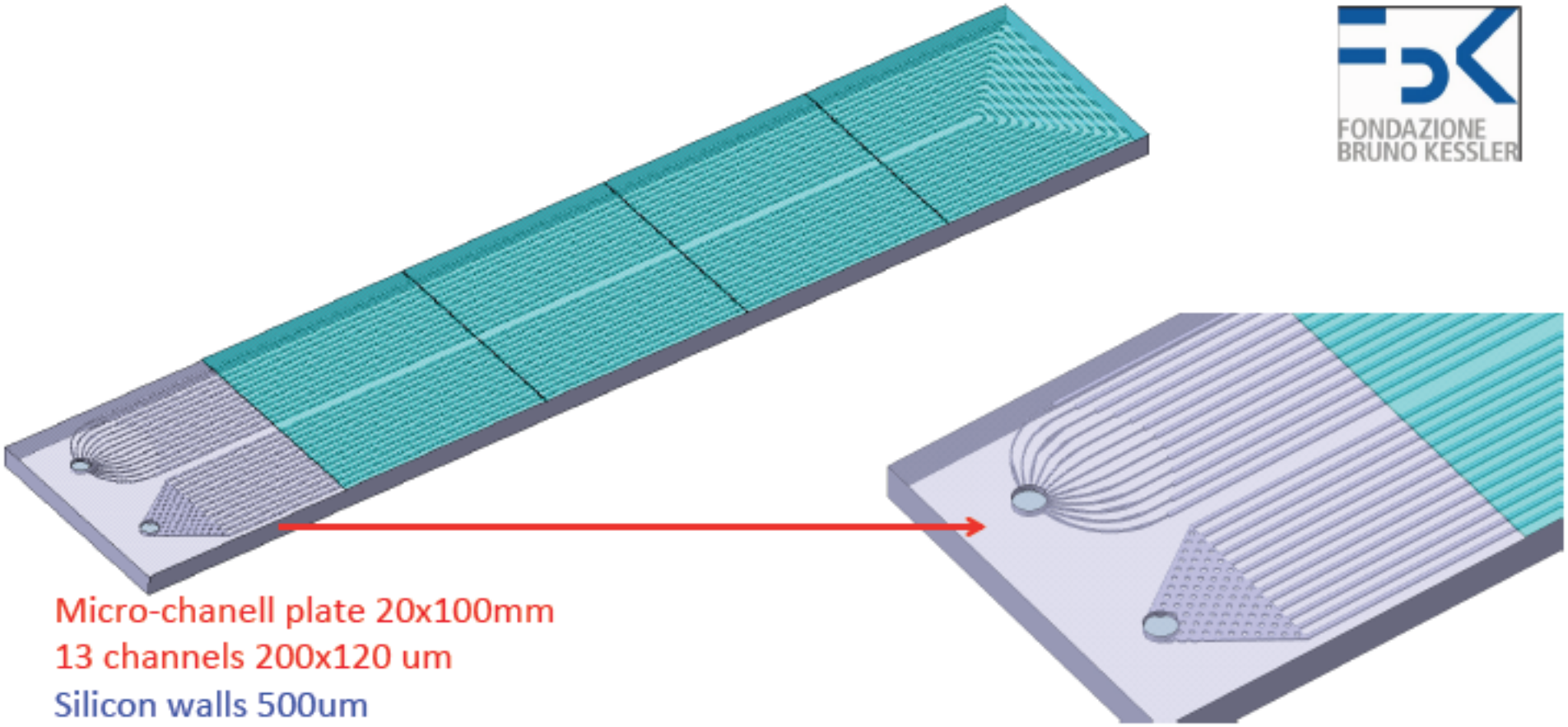
Used to demonstrate module cooling





Detail of outlet region





Micro-chanell plate 20x100mm

13 channels 200x120 um

Silicon walls 500um

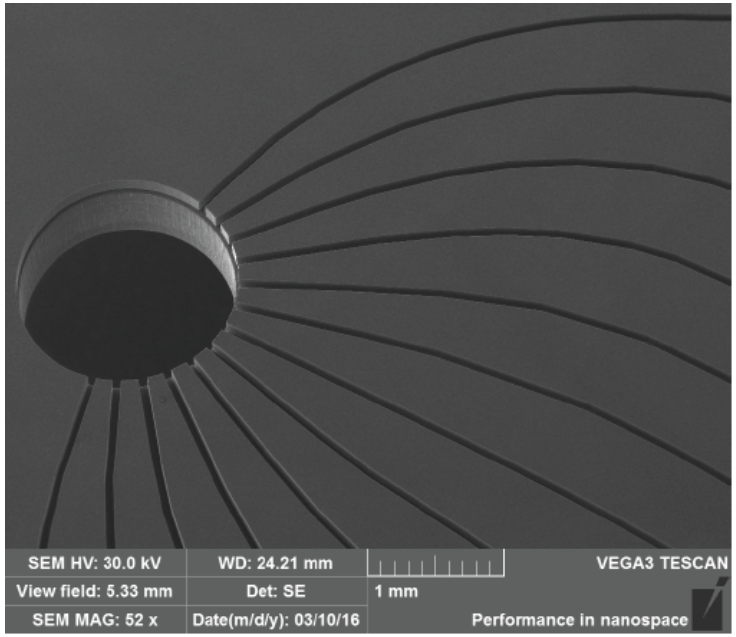
Inlet restrictions 60x120um: same lenght 6mm for all

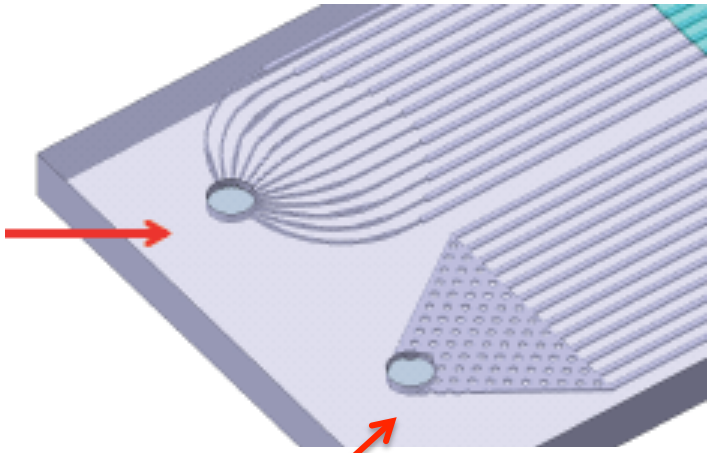
Inlet outlet holes 1.6 mm diameter

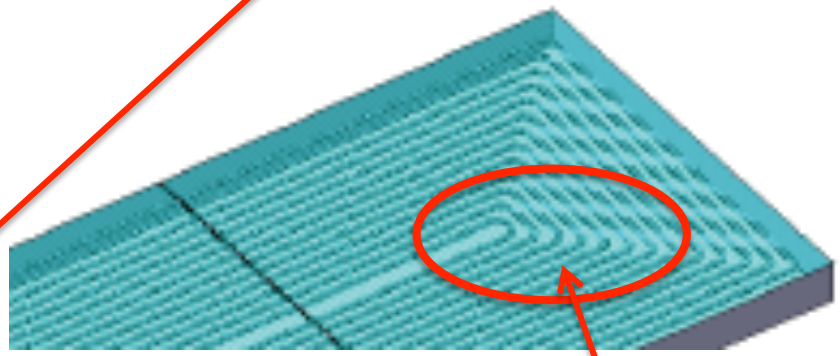
Pillars in the outlet: 350um diameter

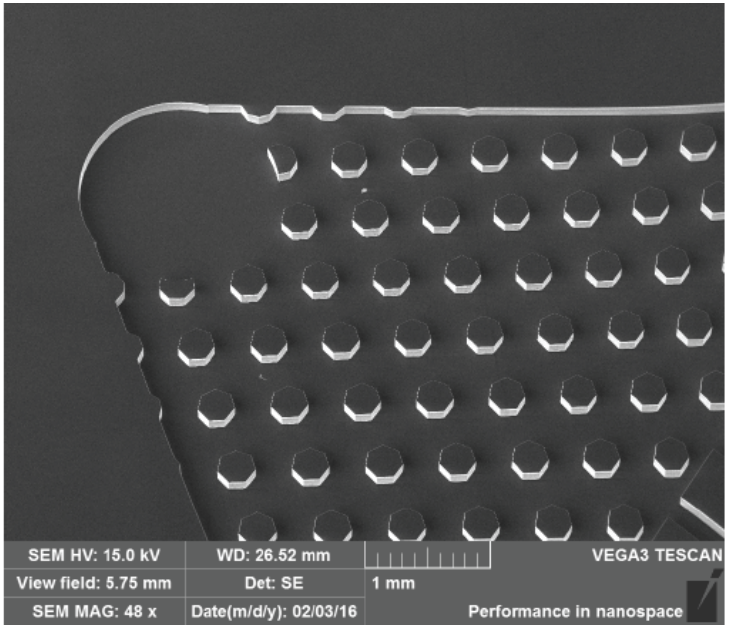
Shortest channel: 165 mm

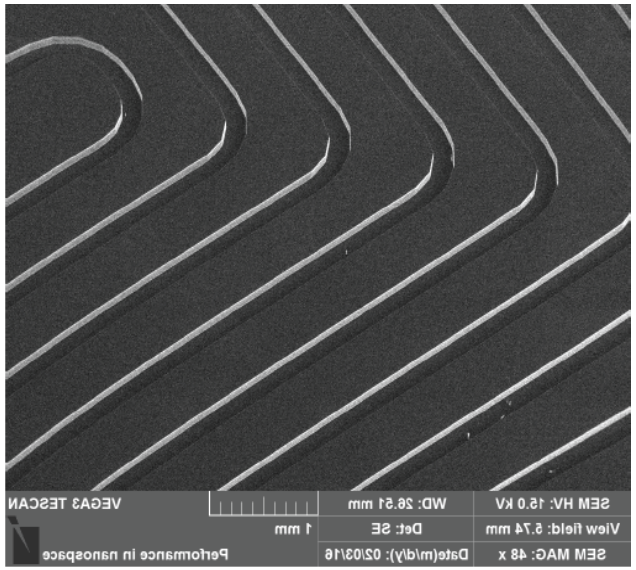
Longest channel: 199 mm


SEM HV: 30.0 kV
WD: 24.21 mm
VEGA3 TESCAN
View field: 5.33 mm
Det: SE
1 mm
SEM MAG: 52 x
Date(m/d/y): 03/10/16
Performance in nanospace






SEM HV: 15.0 kV
WD: 26.52 mm
VEGA3 TESCAN
View field: 5.75 mm
Det: SE
1 mm
SEM MAG: 48 x
Date(m/d/y): 02/03/16
Performance in nanospace



Plans for the Inner Tracker construction

Starting Oct 2016, I'm ATLAS upgrade coordinator of IN2P3 institutions in the tracker upgrade

Involved: CPPM, LAL, LAPP, LPSC, LPNHE

This will require a strong level of integration among the institutions, starting from the construction proposal

The plan for France could be to have:

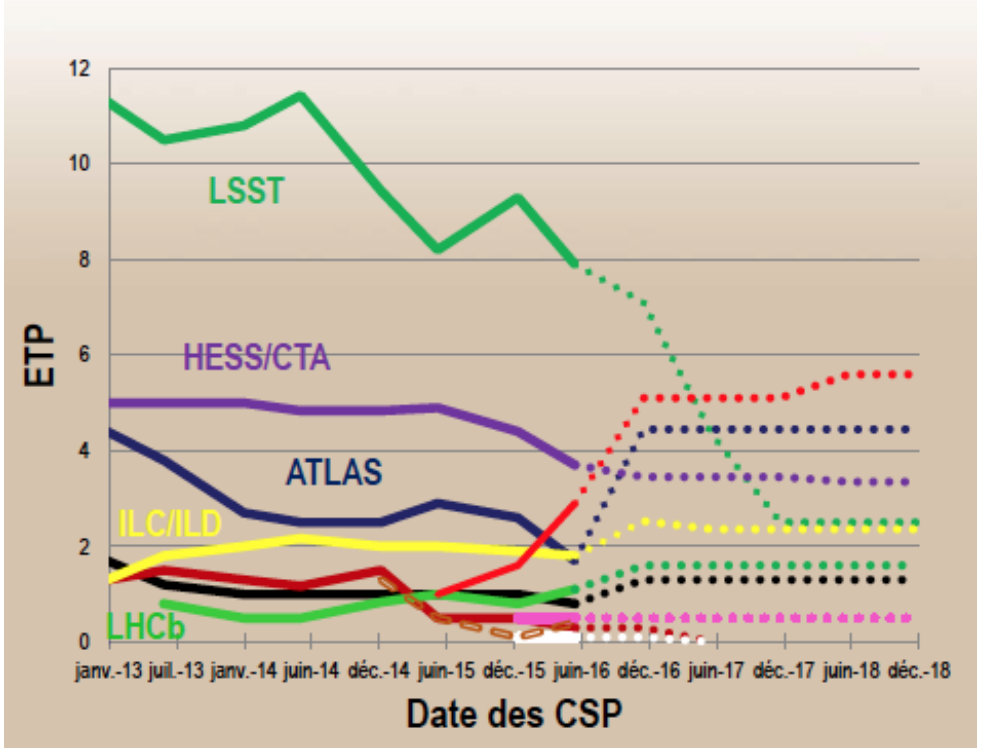
A module construction site in the Paris region (IRFU+LAL+LPNHE)

A stave loading site (at CPPM? With satellite activities at LPSC and LAPP)

Conclusions

The group of ATLAS at LPNHE is involved in many critical R&D activities for the PHASE-II upgrade of the ATLAS Tracker, with very high visibility.

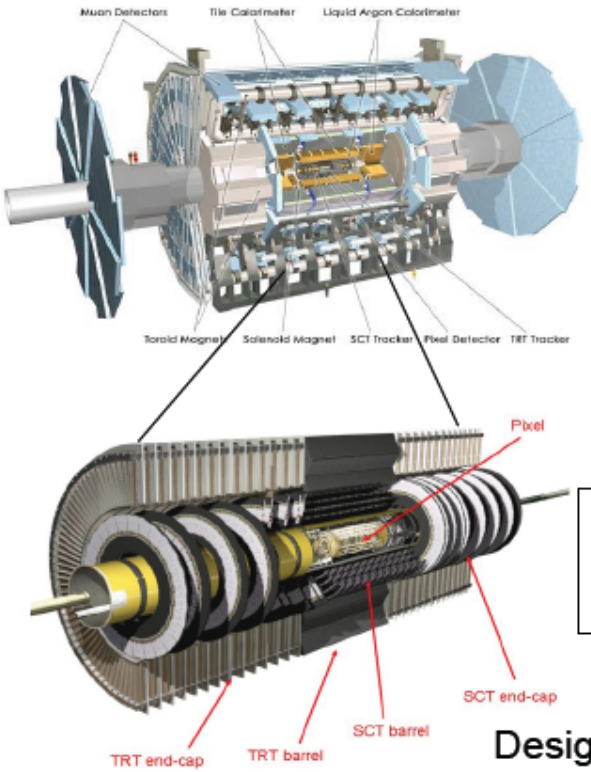
This follows a tradition started many years ago

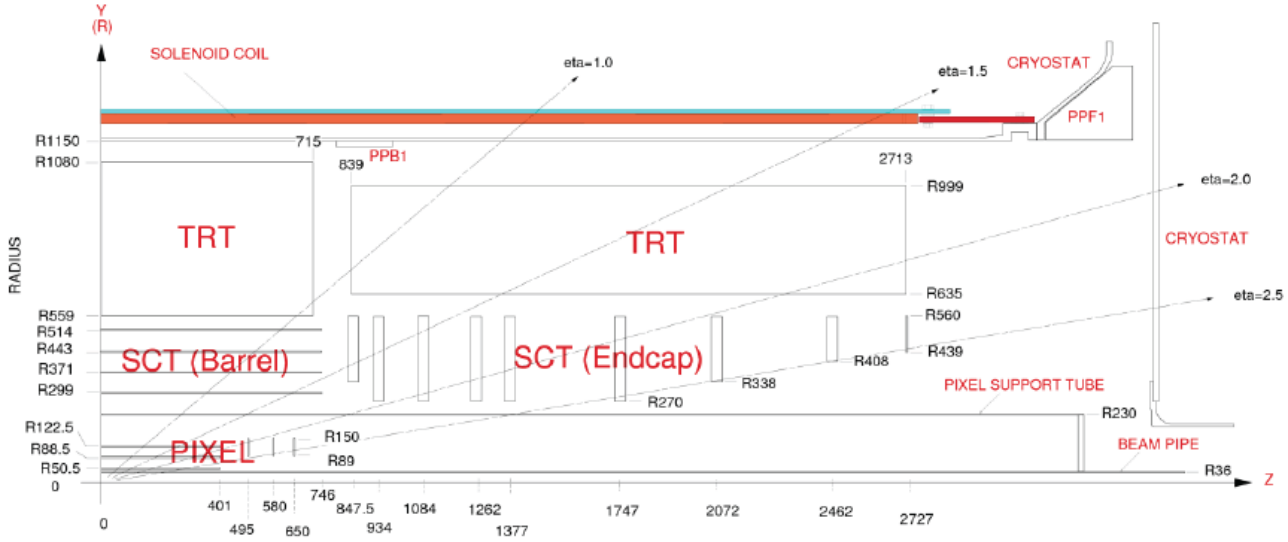


In the next few years the role in the ITk construction will require a support in ITA by the laboratory much larger of the ~2 ETP given so far. (in comparison of a group of 18 permanents).

Backup

Just a reminder of the present Silicon Tracker

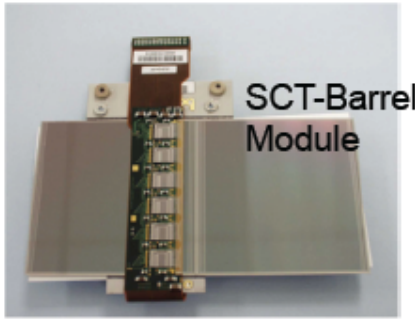




Pixel	(n+-on-n sensor)	: 3 barrels + 2x3 discs (5 < R < 15cm)
Strip (SCT)	(p+-on-n sensor)	: 4 layers + 2x9 discs (30 < R < 51cm)
TRT	(straw drift tubes)	: Barrel + Wheel (55 < R < 105cm)

Designed for fluences of :

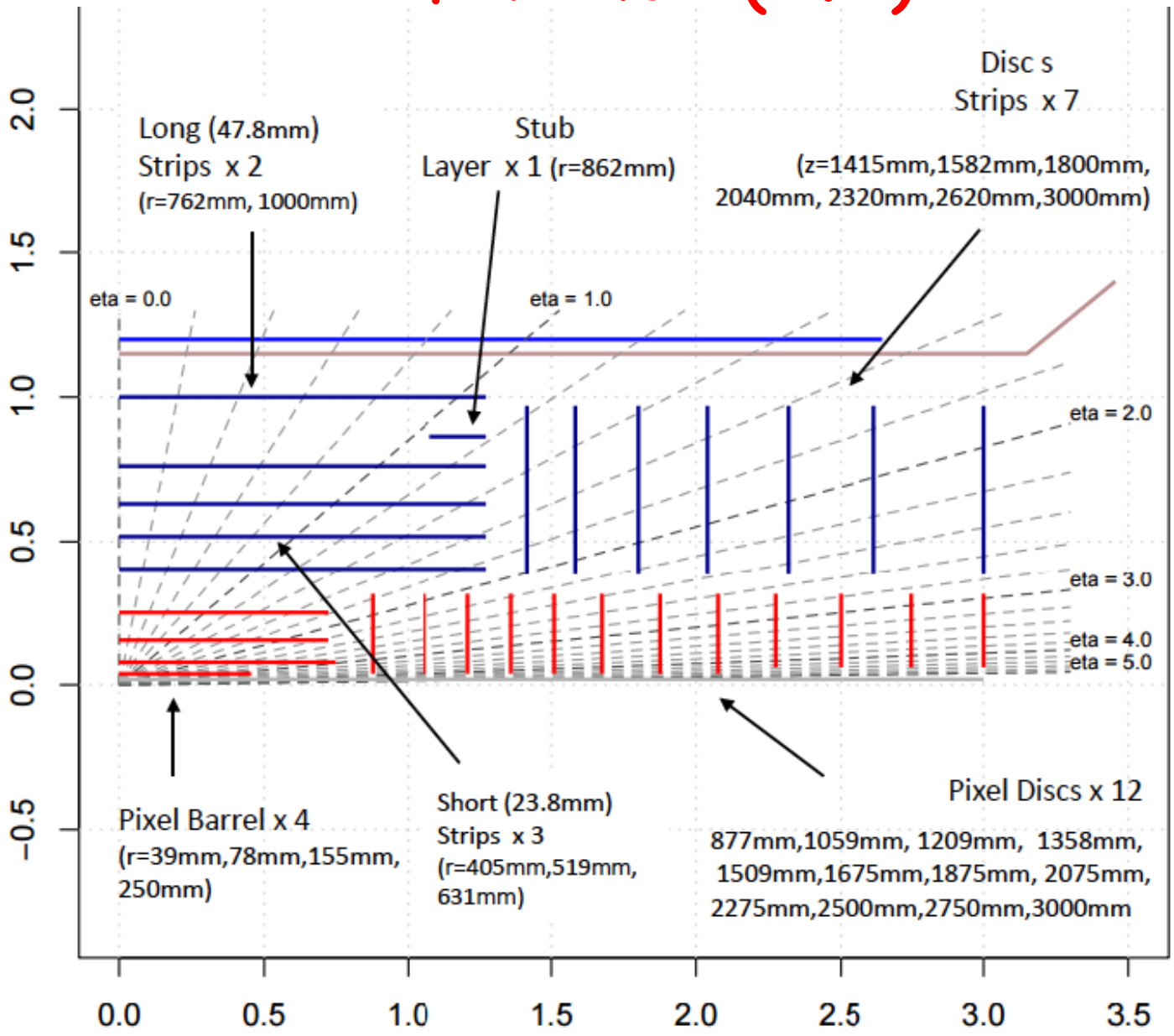
- Pixel B-layer : 1 x 10^{15} 1MeV n_{eq}/cm^2
- SCT layer 1 : 2 x 10^{14} 1MeV n_{eq}/cm^2
- TRT outer rad : 3 x 10^{13} 1MeV n_{eq}/cm^2



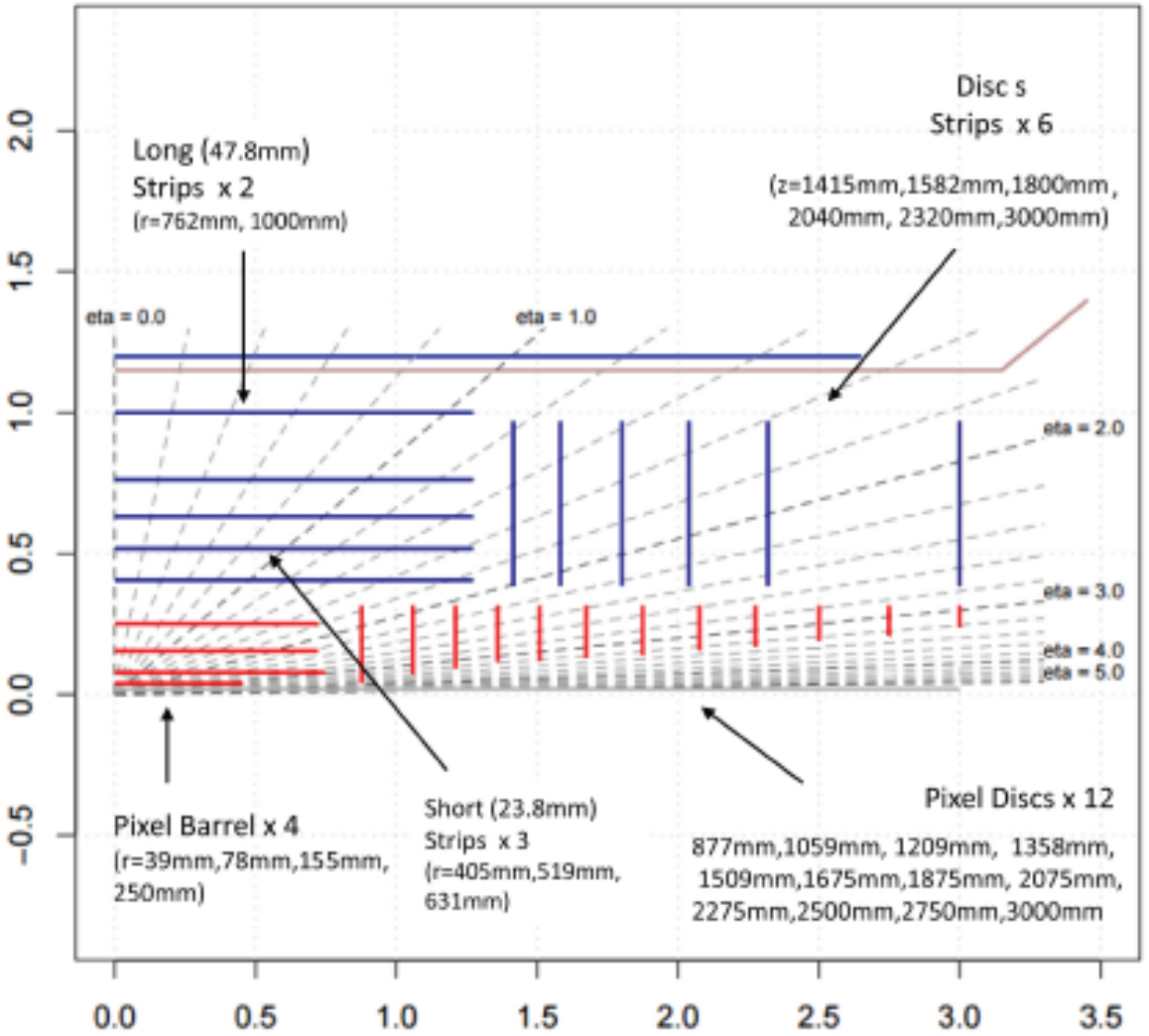
~ 50 Mrads !

- 80M channels
- Temperature: T=-5 / -13 C by evaporative (C3F8) cooling

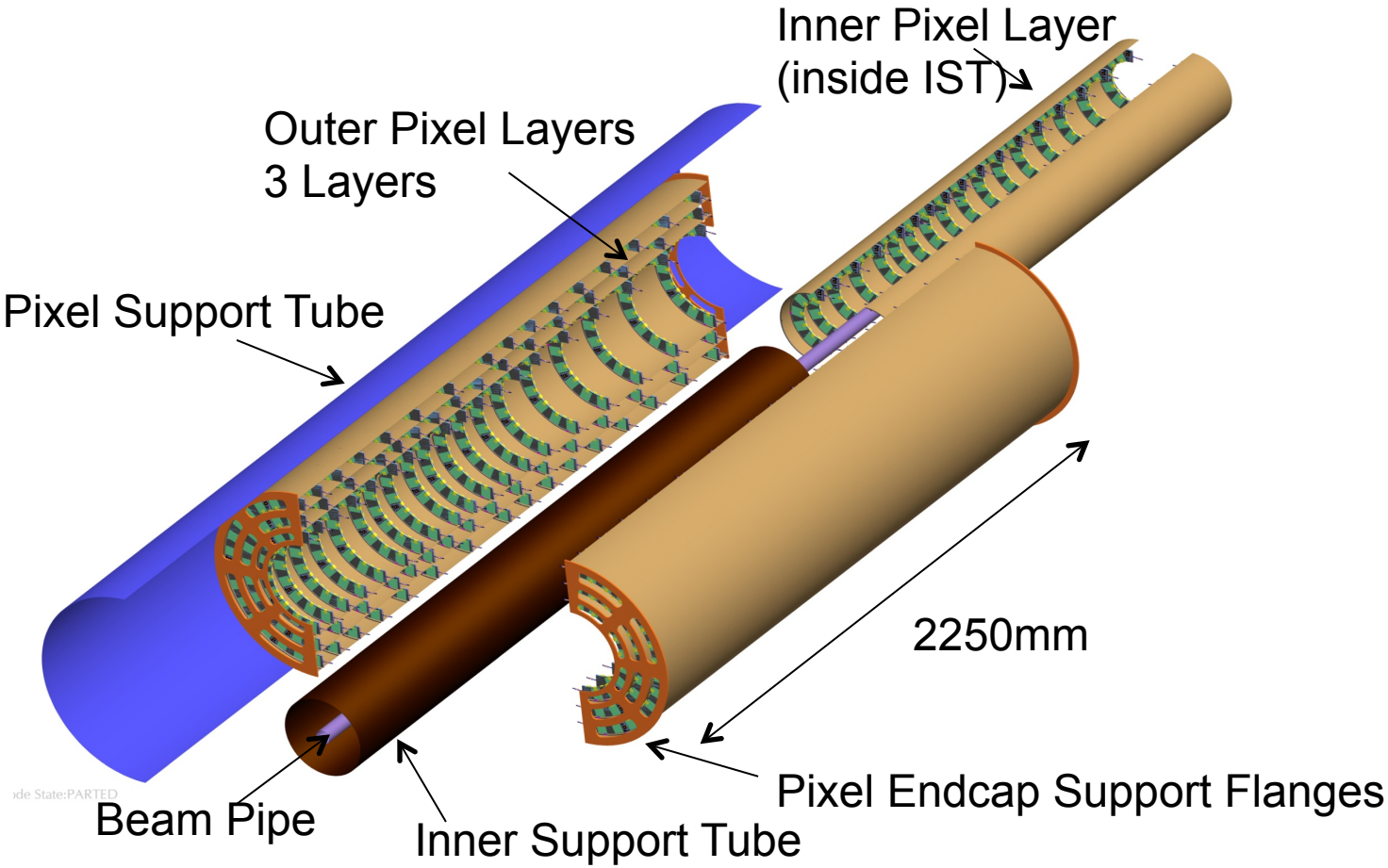
Reference (4.0)



Middle (3.2)

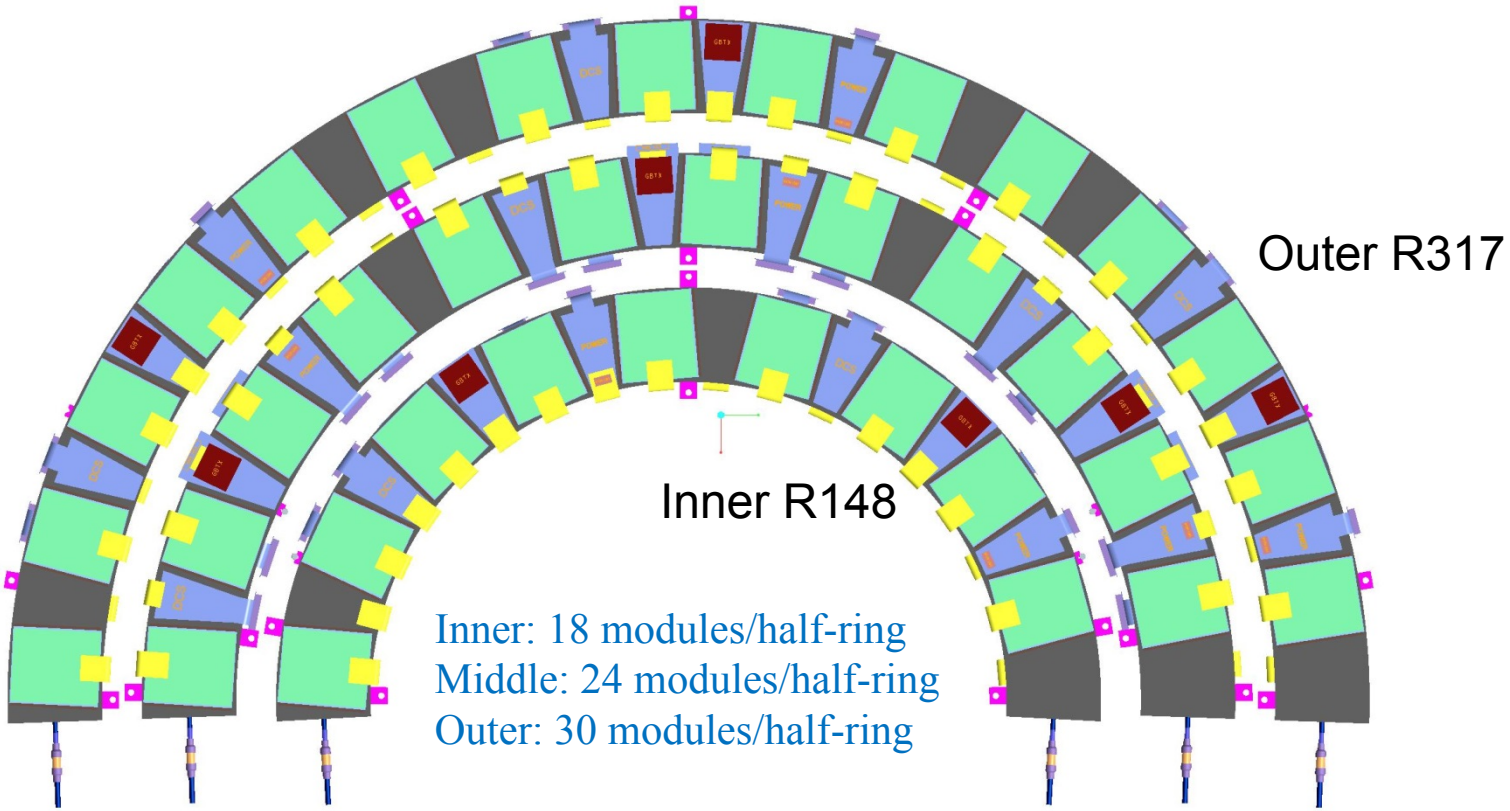

Long (47.8mm)
Strips x 2
(r=762mm, 1000mm)
Disc s
Strips x 6
(z=1415mm,1582mm,1800mm,
2040mm, 2320mm,3000mm)
eta = 0.0
eta = 1.0
eta = 2.0
eta = 3.0
eta = 4.0
eta = 5.0
Pixel Barrel x 4
(r=39mm,78mm,155mm,
250mm)
Short (23.8mm)
Strips x 3
(r=405mm,519mm,
631mm)
Pixel Discs x 12
877mm,1059mm, 1209mm, 1358mm,
1509mm,1675mm,1875mm, 2075mm,
2275mm,2500mm,2750mm,3000mm
2.0
1.5
1.0
0.5
0.0
−0.5
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5

A figure of merit



19 Inner Rings
16 Middle Rings
16 Outer Rings

Pixel endcap half-rings



- The half-rings will be assembled into a complete end-cap.
- Here, I am concerned with timescales for mounting pixel quad modules onto half-rings and testing of the assembled half-rings
- How long will it take ? Does it fit the schedule?

From Richard Bates, UK cluster

Numbers of modules to mount: example, take one Outer Endcap

- 19 inner 16 middle and 16 outer rings
  36, 48, 60 quads/ring respectively

- The natural sub-unit for assembly discussions is the **half-ring**:
- 38 inner 32 middle and 32 outer half-rings
  18, 24, 30 quads/half-ring respectively

- The total for OE is 684 inner, 768 middle, 960 outer = **2412** modules
- Add spare half-rings: 1 inner, 2 middle, 2 outer = **2538** modules

- **Most naïve assumption:**
- 1 hr to mount a module, say 35 hr/week
- 73 weeks, close to **1 year 9 months** (44 working weeks/year)

Realistic that the assembly site would likely have at least one physicist and 2 technicians, full time, working normal 8 hour days.

But then there is the test!...

From Richard Bates, UK cluster

AMchip06

- AMchip06, chip to be installed in FTK in 2015
  coordination of the project: F. Crescioli & A. Stabile
  - Design finished, post-layout simulation almost completed
  - Submitted in a few days from now
  - More transistors (>300M) than

    Intel Core 2 Duo 2006, 65nm, same area

144 mm^2
TSMC 65 nm

128k pattern
11 lignes haut débit
8 input → 2 Gbps
2 input → 2.4 Gbps
1 output → 2.4 Gbps
Clock 100 MHz
1.8 Petabit/s comparisons
~3 W (for FTK)

~8000 chip pour FTK
~1 milliard pattern