“An important point of computing for CMS”*

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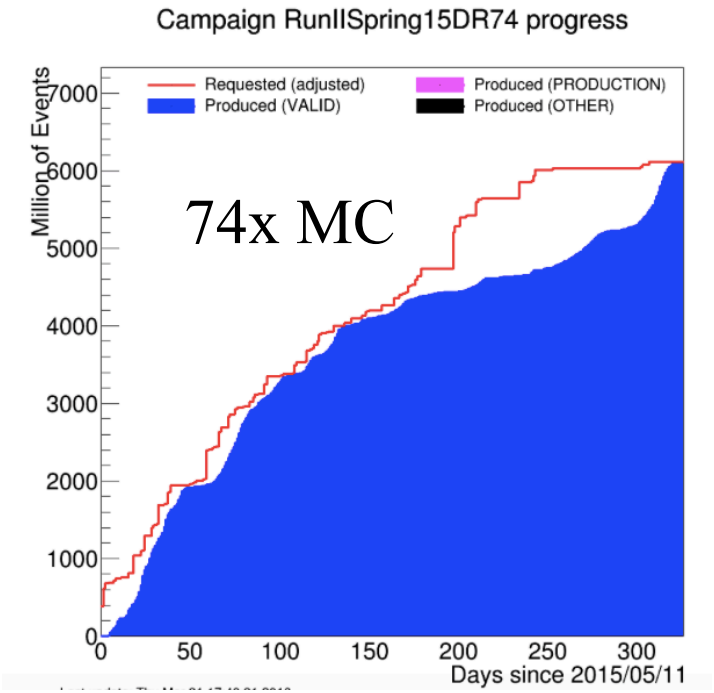
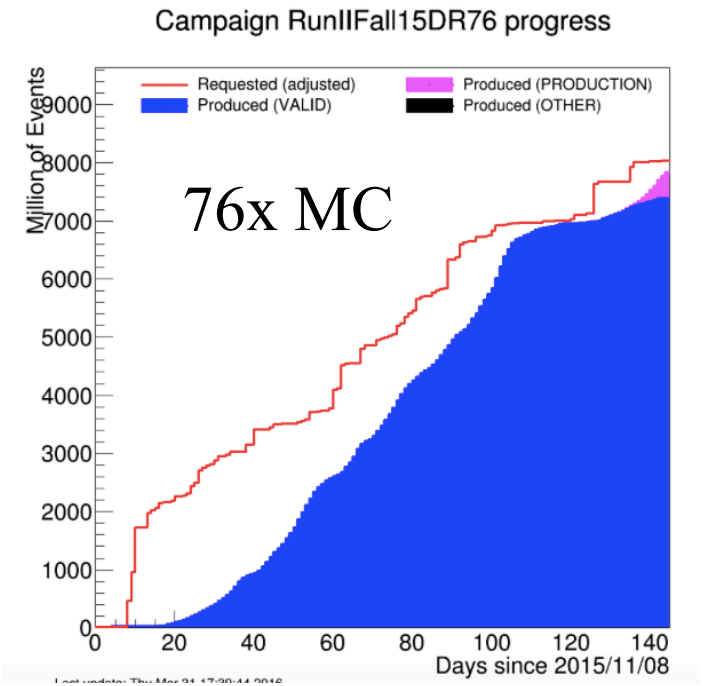
*More accurately: News from CMS offline and computing week

Production in 2015

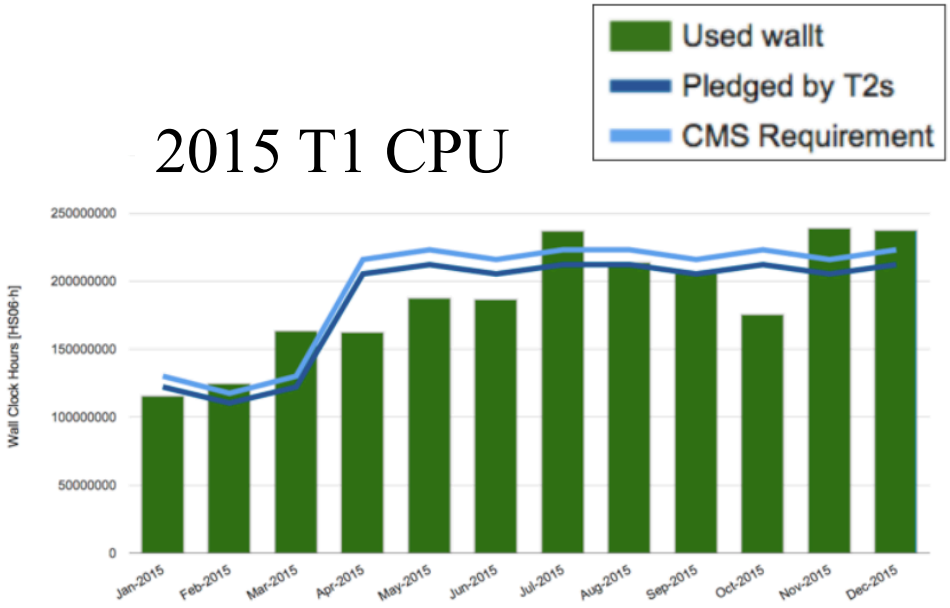




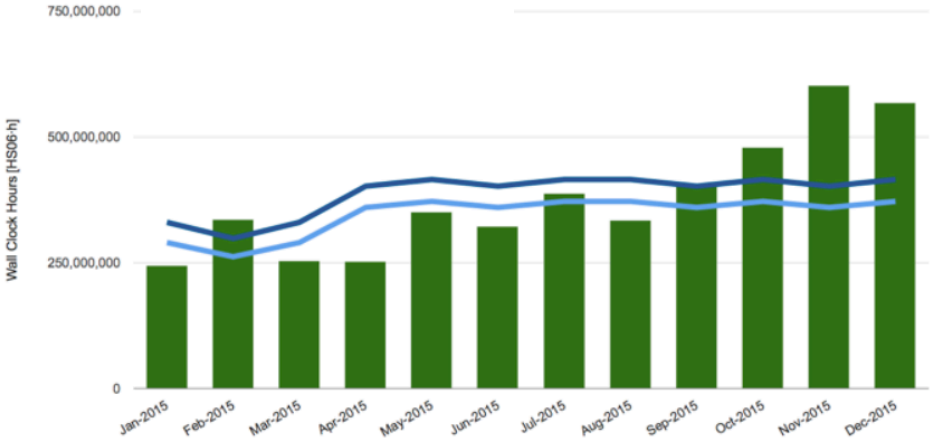
- MC:
  - 2 large sets of GEN-SIM events. The second was needed to move the beam spot to its actual location
  - Corresponding DIGI-RECO campaigns (first CMSSW_7_4, then CMSSW_7_6). Software change to incorporate fixes needed for 25 ns running
- Data: End-of-year reprocessing done with multicore

Stable operations across CMS computing centers

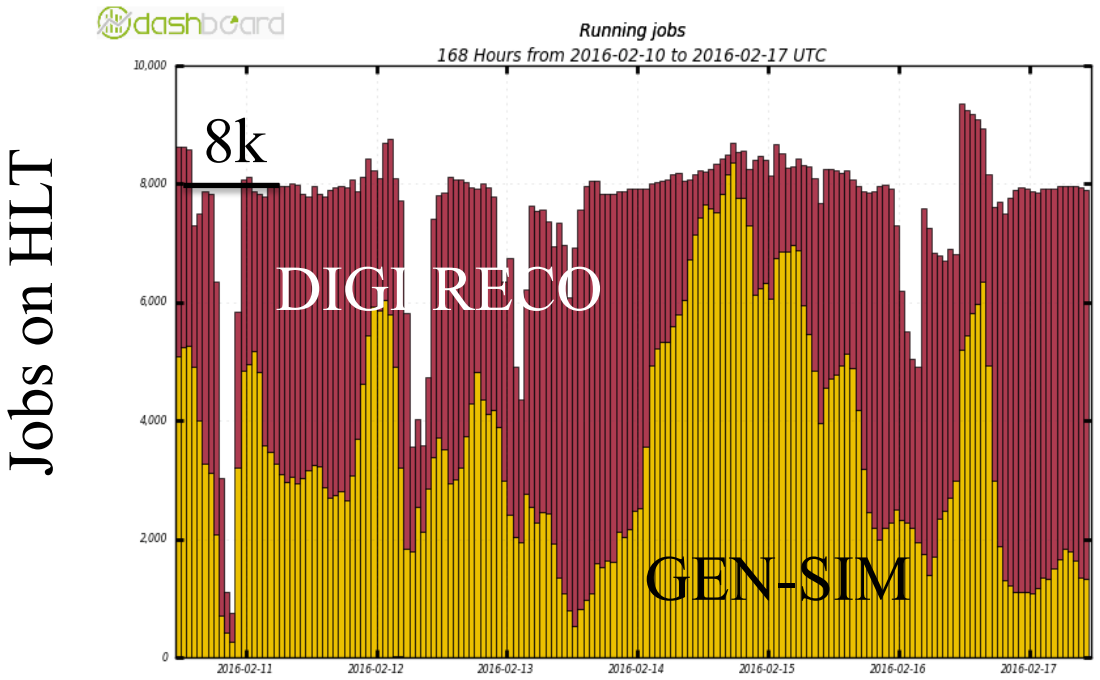
2015 T1 CPU



2015 T2 CPU



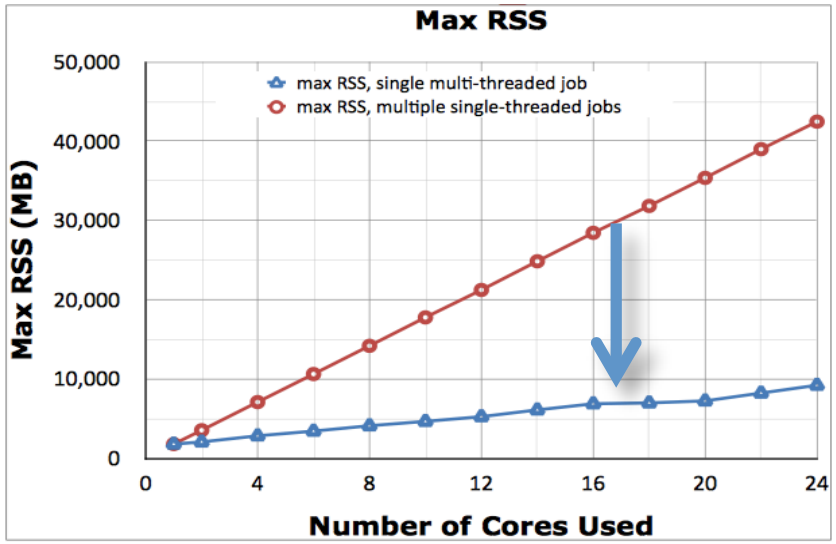
HLT in routine use for production (both SIM and high-I/O DIGI-RECO)



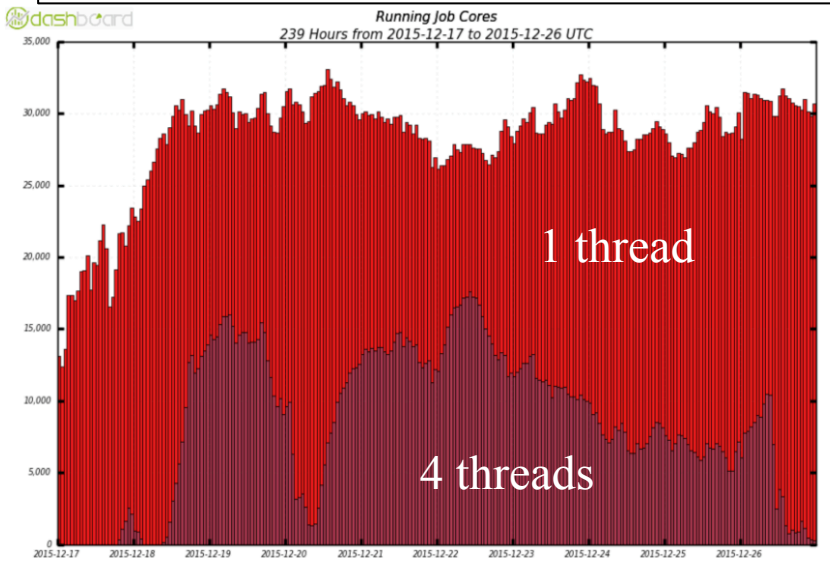
Given the major CPU upgrade in April/May, the HLT will be an especially important resource for CMS.
Advanced planning become increasingly important.

CMS multi-threaded applications in production on Tier-0 and Grid

Novel threaded processing framework in CMSSW brings dramatic memory saving



~50% of CMS Tier-1 resources used for end-of-year data processing in multicore



- 2016: Entire CMS MC simulation, digitization and reconstruction chain as well as data processing is multi-threaded capable

Use of the new framework brings a substantial improvement in efficiency to CMS operations

2016/ICHEP production

- Main changes for LHC/CMS:
  - Higher pileup
  - Upgraded L1 trigger (again)
- Planning based on pileup evolution, past production achievements and resource evolution

tranche-1 pre-ICHEP (critical, 3 B evts)

tranche-2 pre-ICHEP(2 B evts - *5B evts total*)

- Once we hit June 2016, we continue to work on tranche-2 above. At this stage we can evaluate the progress and adjust the program of work as needed

tranche-3 post-ICHEP (critical, e.g. 2 B evts - *7 B evts total*)

- in the worst case scenario (excellent machine performances, plenty of analysis load, suboptimal completion of disk cache cleaning plans, etc) this is where we stop in 2016

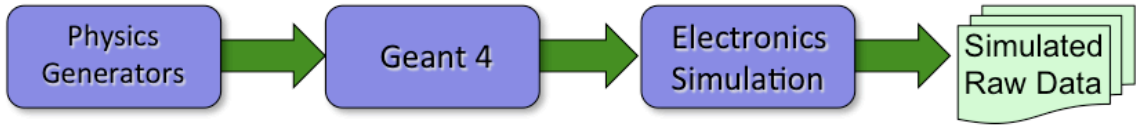
tranche-4 post-ICHEP (e.g. 4 B evts - 11 *B evts total*)

Technical changes in place for 2016 production

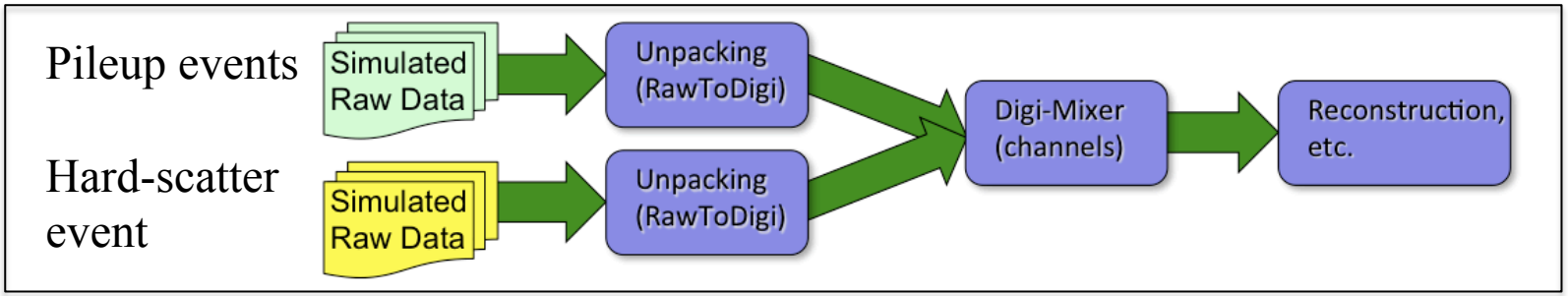
- SIM, DIGI, RECO, HLT all running efficiently in multicore processing jobs
  - Primary accomplishment CMSSW8 is that the mixing module is now thread-efficient
- Most Tier-2 resources now capable of running multicore pilots
  - Plan to migrate Digi-Reco to multicore setup
- Move to GCC5.3.0 (from 4.9.3)
- Move to ROOT 6.0.6 (from 6.0.2)

Premixing

- Our 2015 pileup simulation software is the largest CPU component of the DIGI-RECO production and presents a major I/O challenge for sites.
  - Pre-mixing the pileup events is a solution to both issues:



- Then the two streams are merged



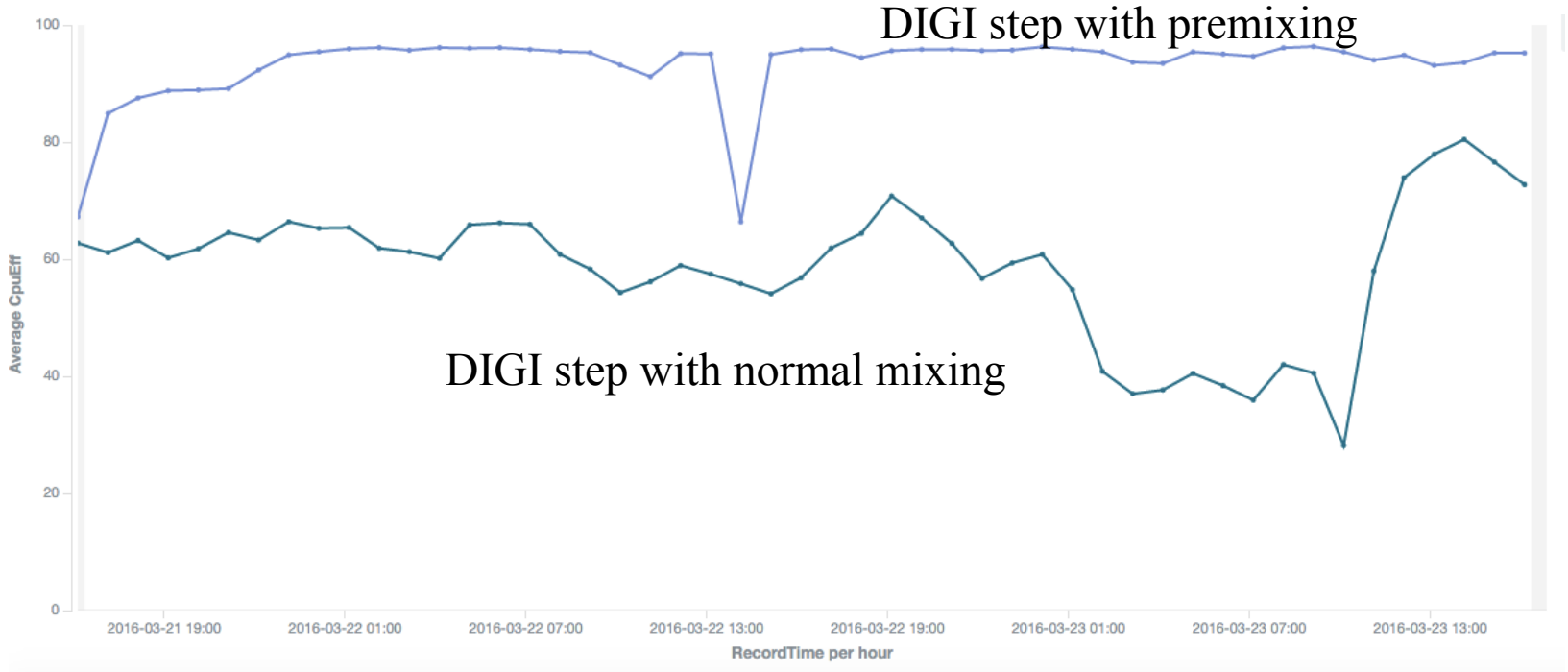
Benefits:

- CPU reduced by more than a factor of two for the total DIGI-RECO process
- I/O burden reduced by 200x for 2016 pileup levels

Costs:

- Large sample of premixed events needed (essentially to run the current digi step)
- Reuse of combinations of pileup events across samples (not an issue within single samples except potentially the very large ones)

CPU efficiency w/ pre-mixing



Future challenges

- 2016 – 2017 Year-End Technical Step
  - Pixel detector replacement
  - Hadron calorimeter front-end and endcap PMTs

  → Requires simulation in 2016 w/ updated reconstruction
- Phase 2 upgrades
  - Technical design reports for 2017
  - Intermediate updates for ECFA workshop in October

  → CMS must be prepared to demonstrate that computing costs for Phase 2 are not prohibitive