



# Capteur HVCMOS pour upgrade de phase II du trajectographe d'ATLAS

Marlon Barbero

Aix Marseille Université / Centre de Physique des Particules de Marseille

[barbero@cppm.in2p3.fr](mailto:barbero@cppm.in2p3.fr)

Journée thématique réseau R&D semi-conducteurs

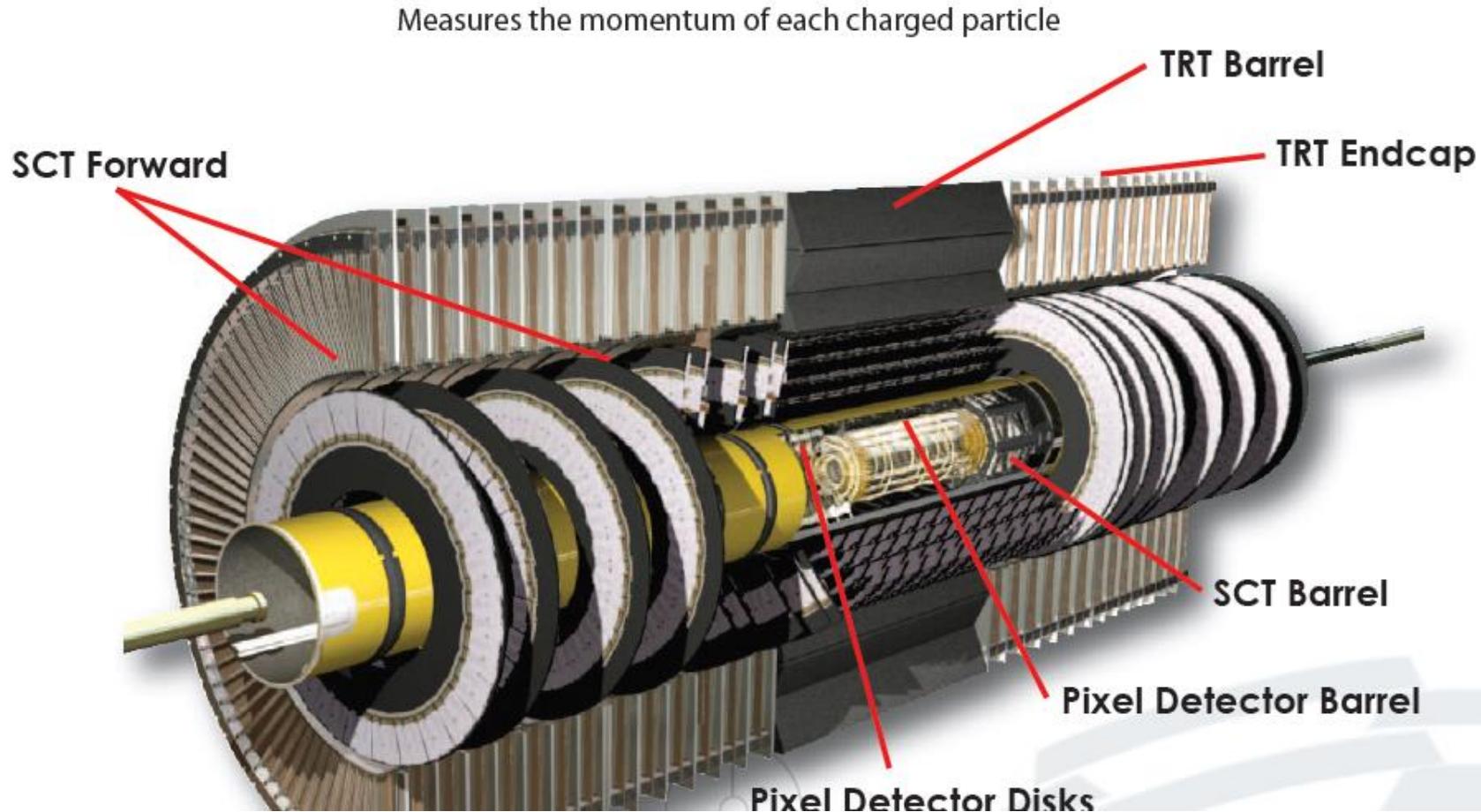
# Contenu

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- Programme d'upgrade Inner Tracker (ITk) phase II d'ATLAS.
  - Environnement HL-LHC.
  - Capteurs HV/HR CMOS (DMAPS/Depleted-MAPS) dans l'ITk.
- HV/HR CMOS program.
  - Point focal récent:
    - Simulations TCAD
    - (TCAD / Geant4 workshop au CPPM en Mai <https://indico.cern.ch/event/497449> )
    - Characterization.
    - Programme démonstrateur.
    - Designs
- Impact physique en couche interne.
- Perspectives et conclusion.

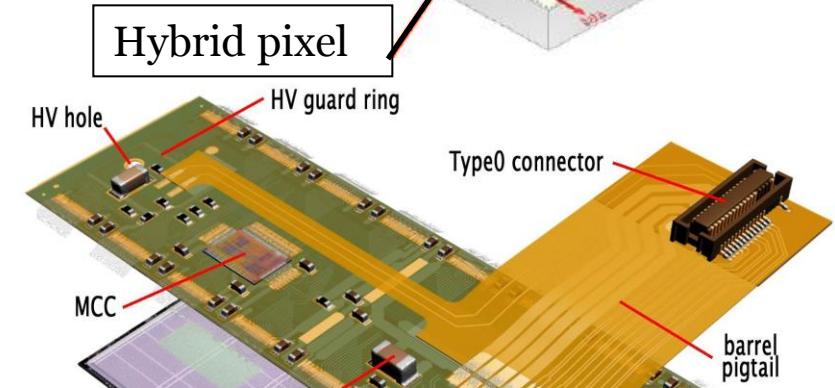
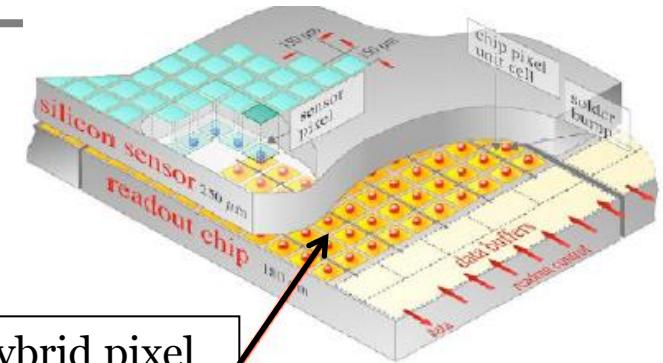
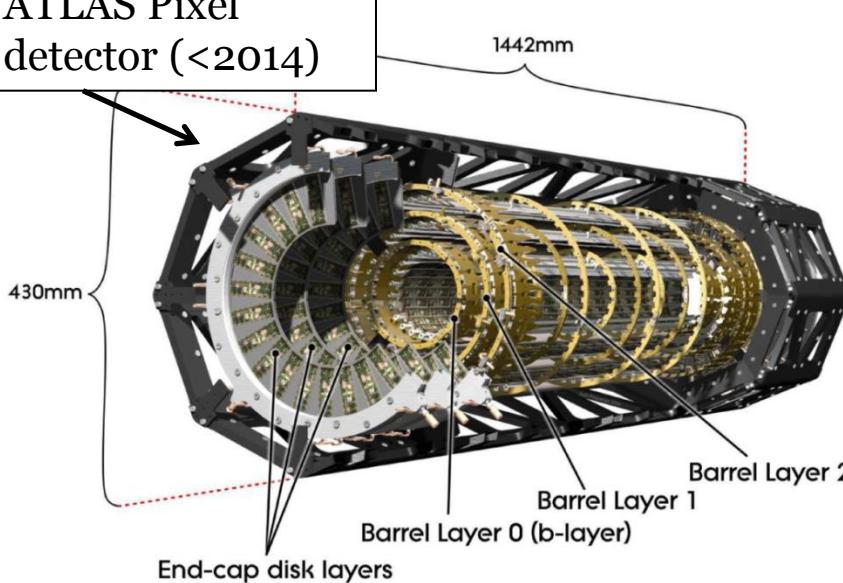
En présence de NIEL + TID!

# ATLAS silicon tracker (now 10m<sup>2</sup> → 200m<sup>2</sup> in future!)



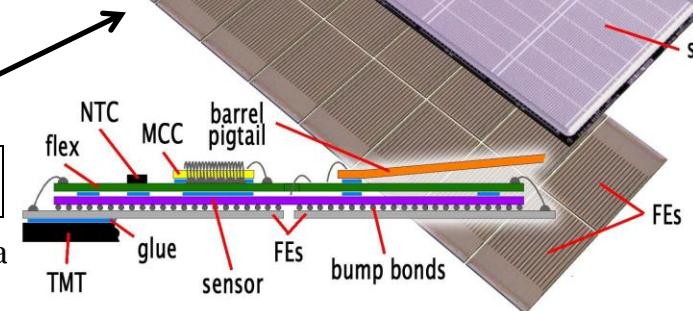
# Pixel detector (now $\sim 1.5$ m $^2$ , futur $\sim 10$ m $^2$ )

ATLAS Pixel  
detector (<2014)

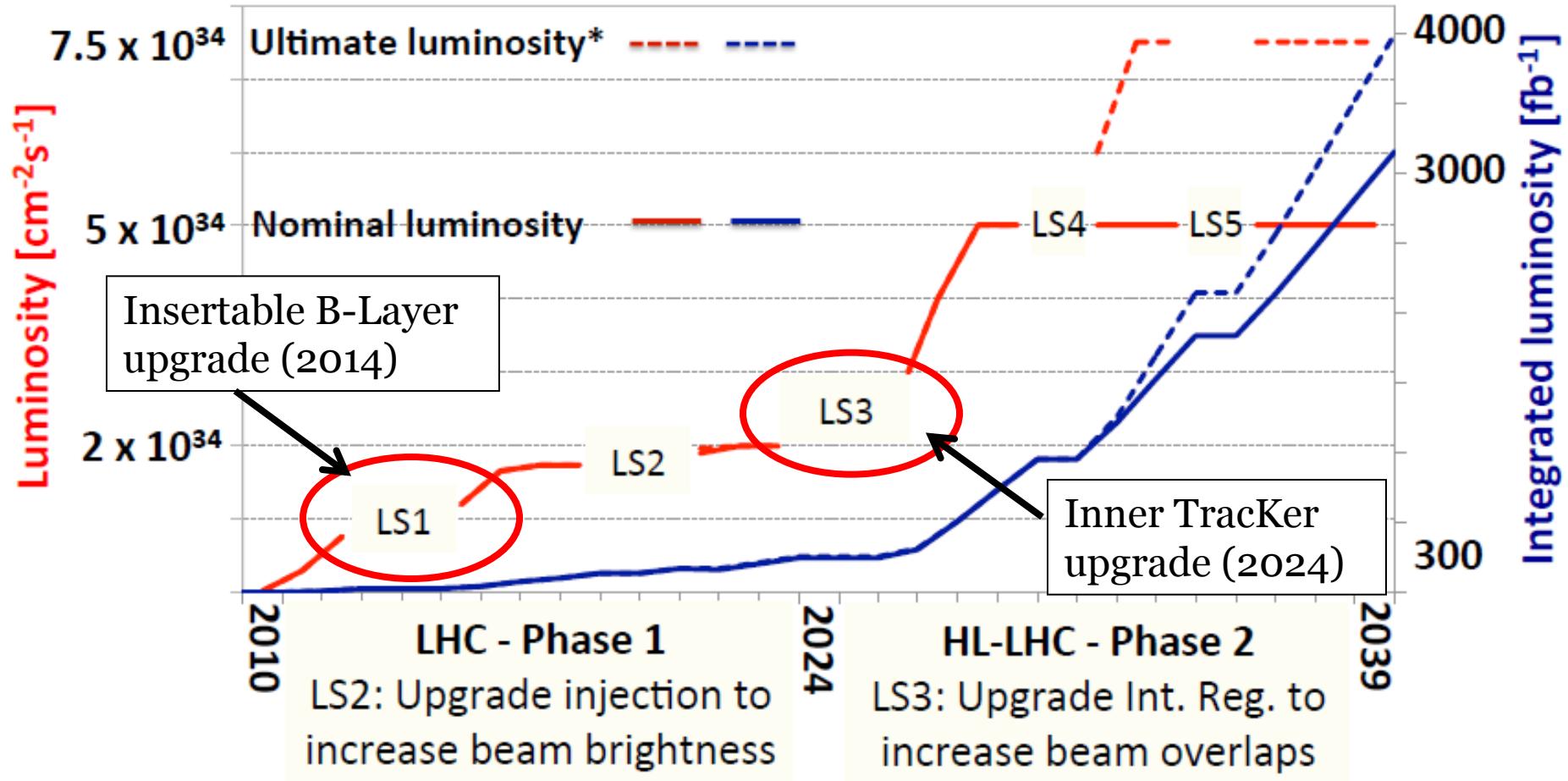


The initial ATLAS pixel detector: **87 millions pixels of size  $50 \times 400 \mu\text{m}^2$ , in a 3-layer cylinder**, cooled down at -15°C, measuring particle crossing 40 millions times per second!

Original hybrid module

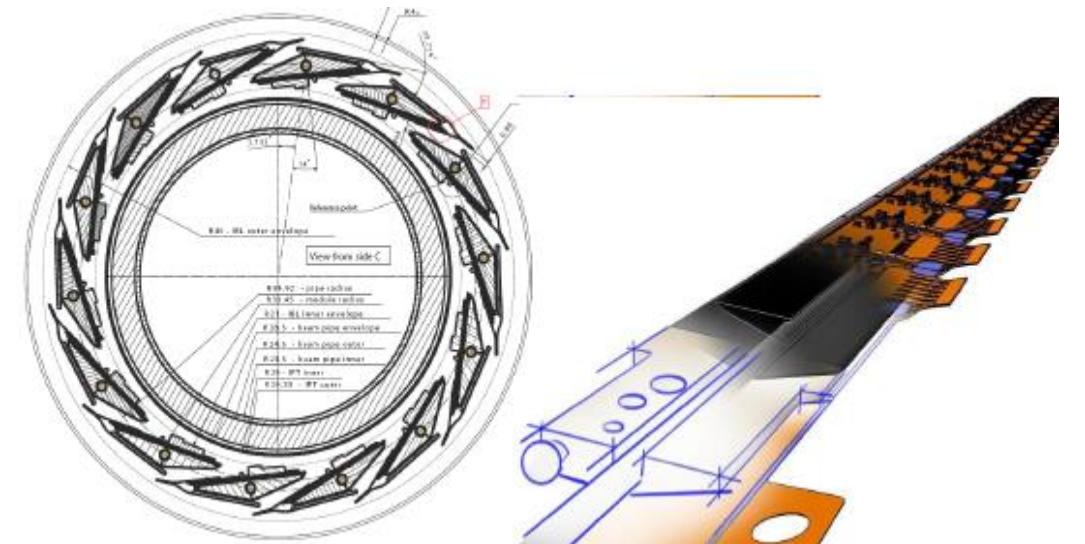
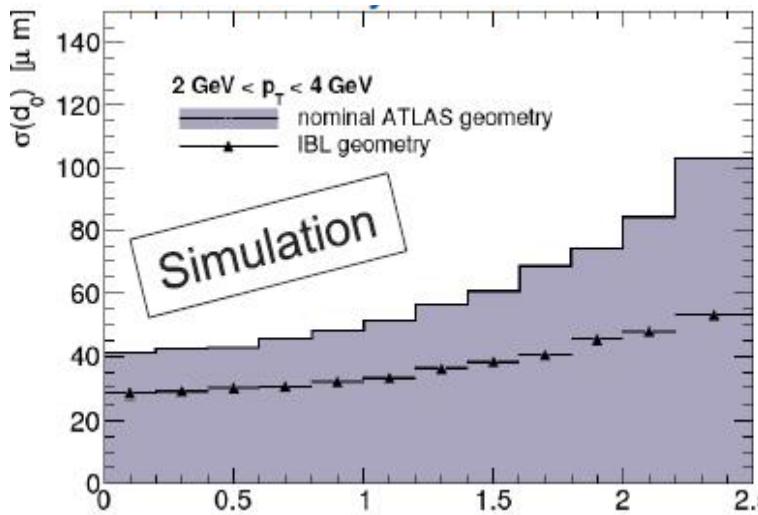


# Long Shutdowns & Upgrades



# IBL motivation

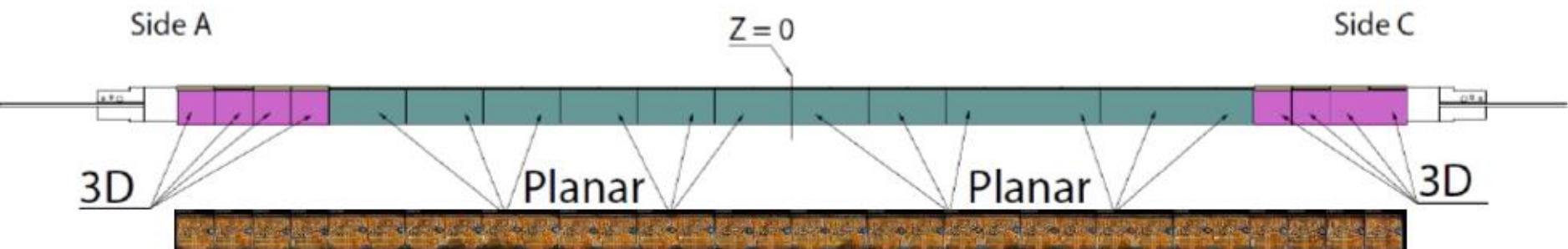
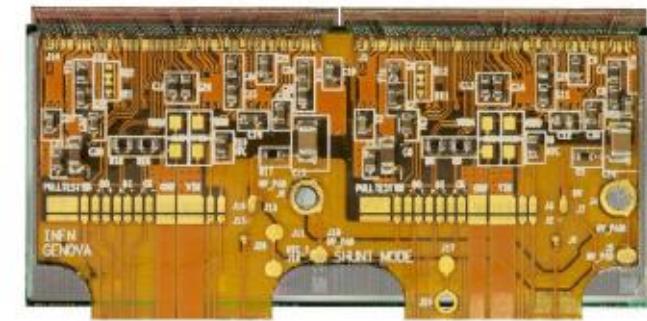
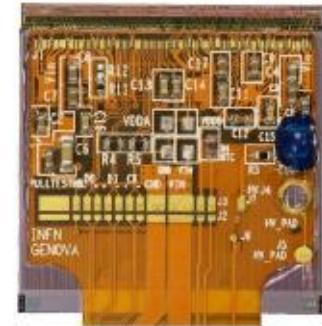
- Improve **b-tagging performances**:
  - Impact parameter resolution improves by factor  $\sim 2$ .
  - Light jet rejection at higher pileup  $> 2$  better (for fix b-tag efficiency).
- Increase **robustness of pattern recognition**, in particular in case of B-layer modules failures.
- New innermost **layer between beam pipe and initial inner layer**.
  - 2 mm mechanical clearance!
- **Short distance to interaction point**:
  - High particle flux.
  - High occupancy ( $10^{-4} \rightarrow 10^{-3}$  / pix.)
  - Radiation damage 250 MRad.



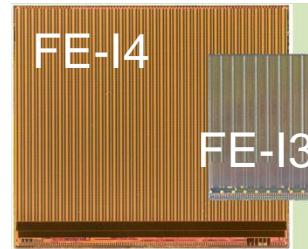
# IBL staves

IBL staves are based on 2 technologies:

- 14 staves:
  - 12 planar n-in-n double chip modules (sensor fabricated by CiS).
  - 8 single chip 3D modules (sensor fabricated by CNM and FBK).
- FE-I4B readout chip, IBM 130nm technology
- 12.042.240 pixels,  $250 \times 50 \mu\text{m}^2$ .
- Radius: 3.27 cm, ~70 cm long.



# Electronics for the IBL



The FE-I4

Need for a new FE for IBL?

→ Higher hit rate → local memories.

→ Smaller pixel size: granularity.

→ Reduced periphery & bigger chip: high active area fraction

→ Simple module: No MCC, digital functions into the FE.

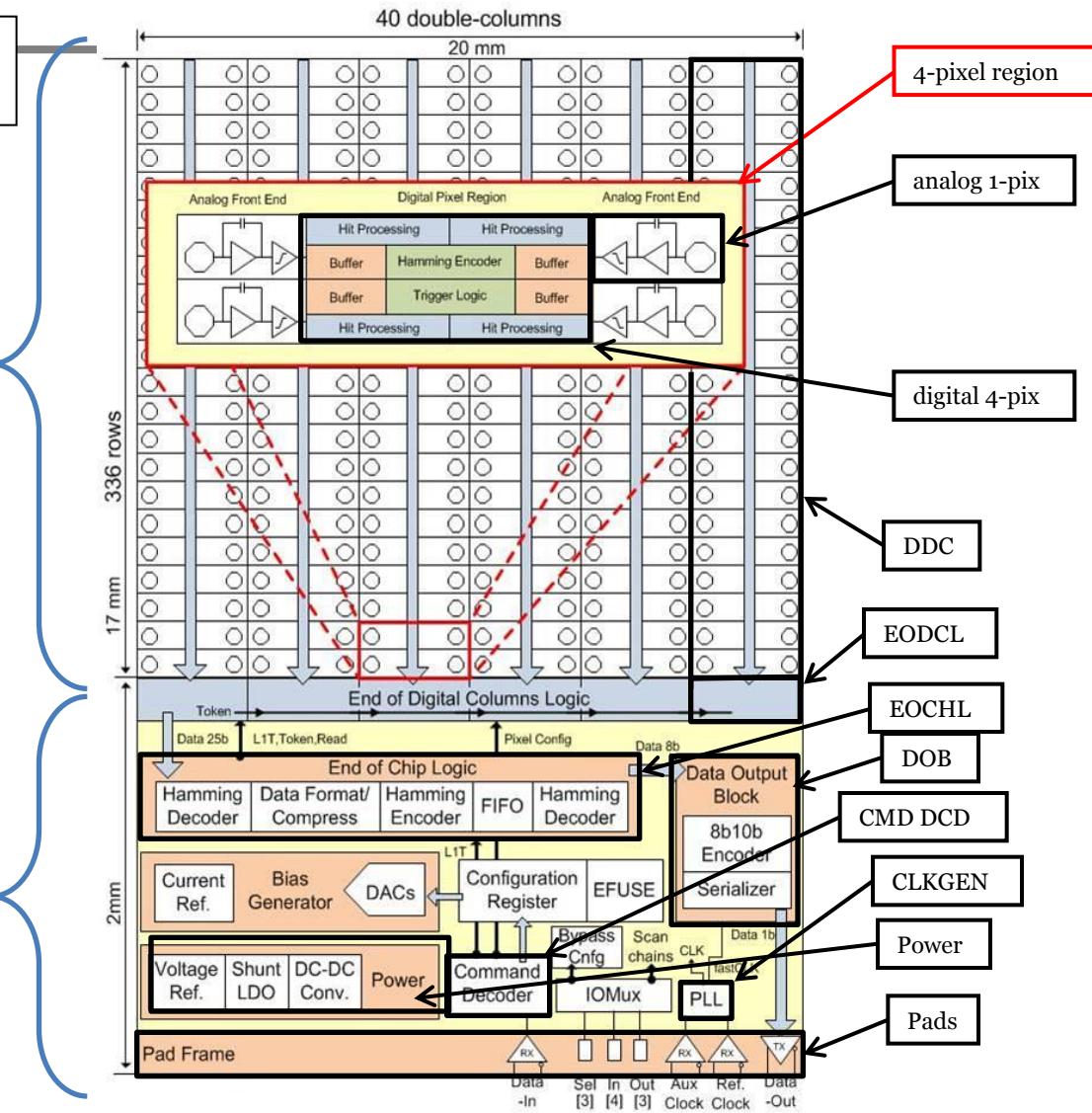
→ Power efficient design & new concepts: Analog design; digital activity down.

New technology:

periphery

IBM 130 → Higher integration density digital circuits, radiation-hardness (no ELT), availability timescales of our experiments.

pixel array:  
 $336 \times 80$  pixels

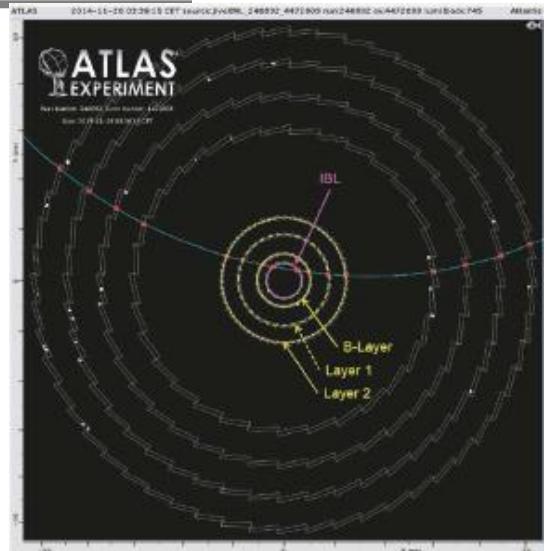


# IBL upgrade

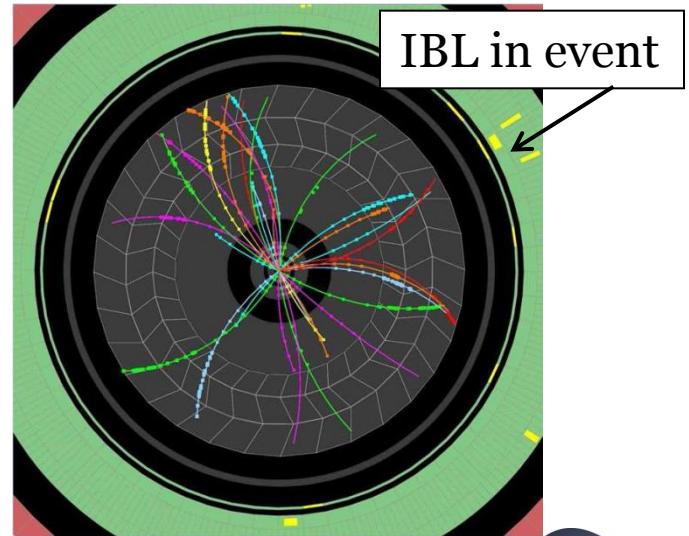
- 2014: The IBL upgrade!



IBL w. cosmic

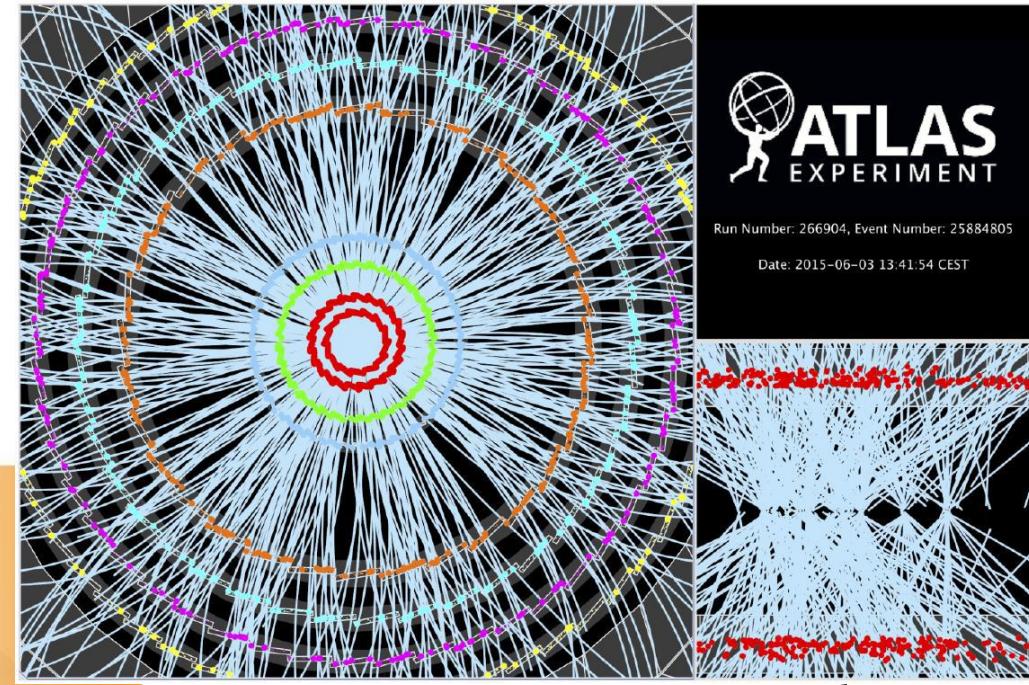
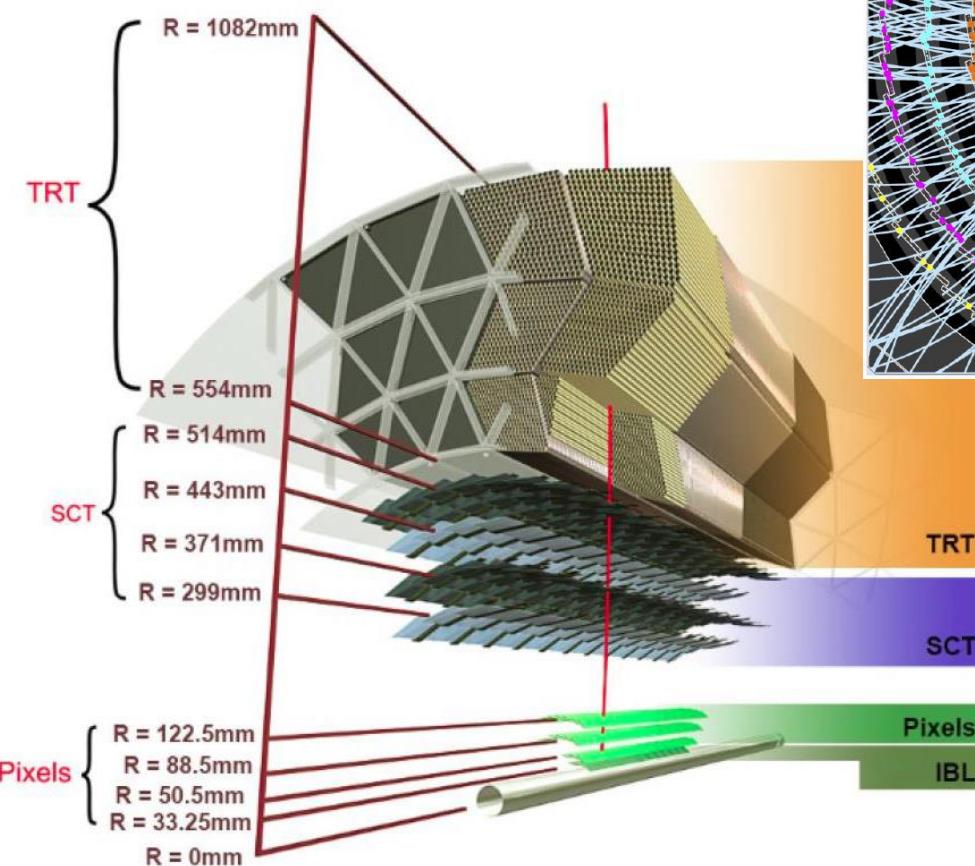


IBL in event



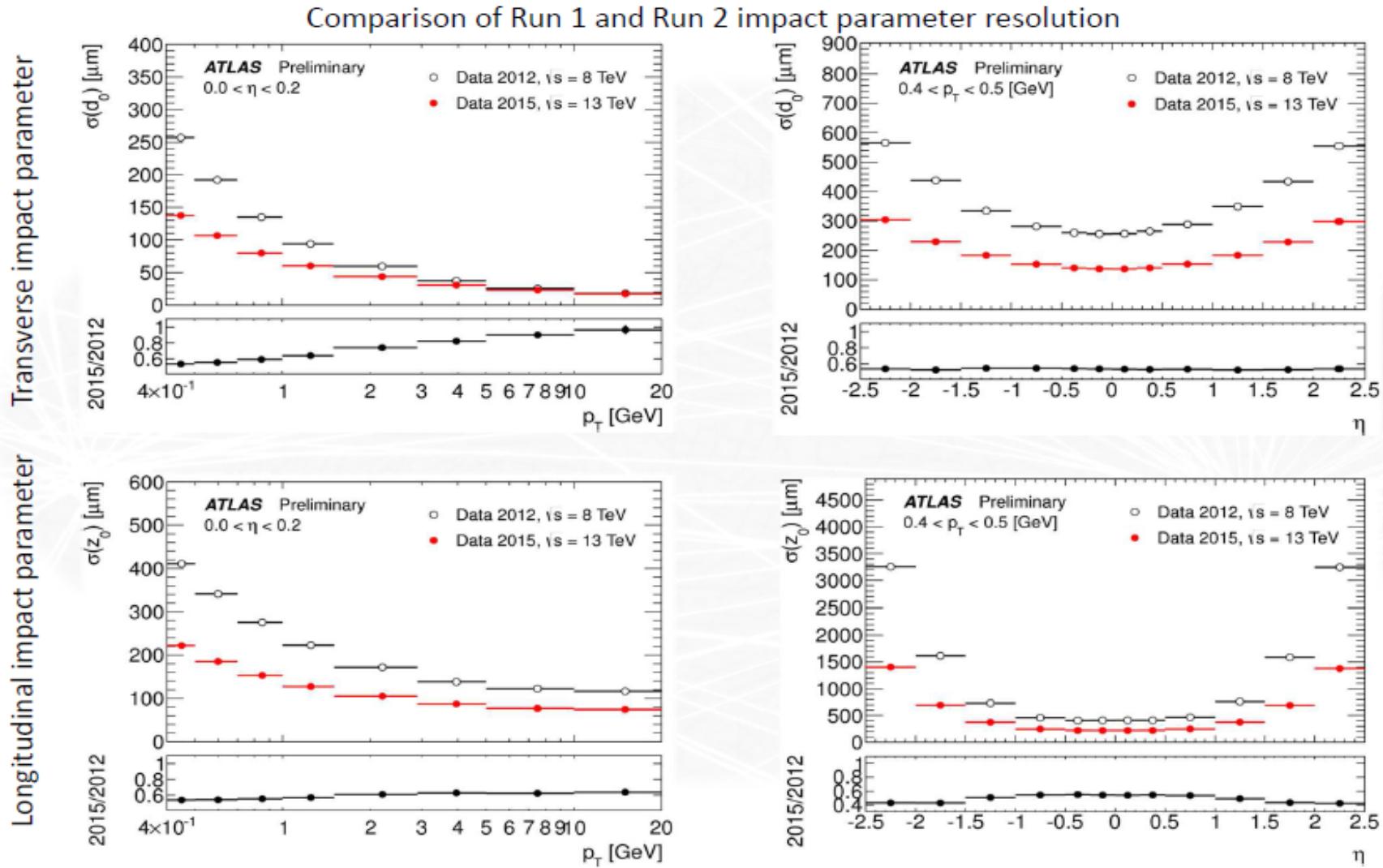
# Run II operation: 4 pixel layers

Configuration for Run II  
and Run III → 2022



Multiple vertices  
disentangled with the IBL!

# Tracking improvement with IBL

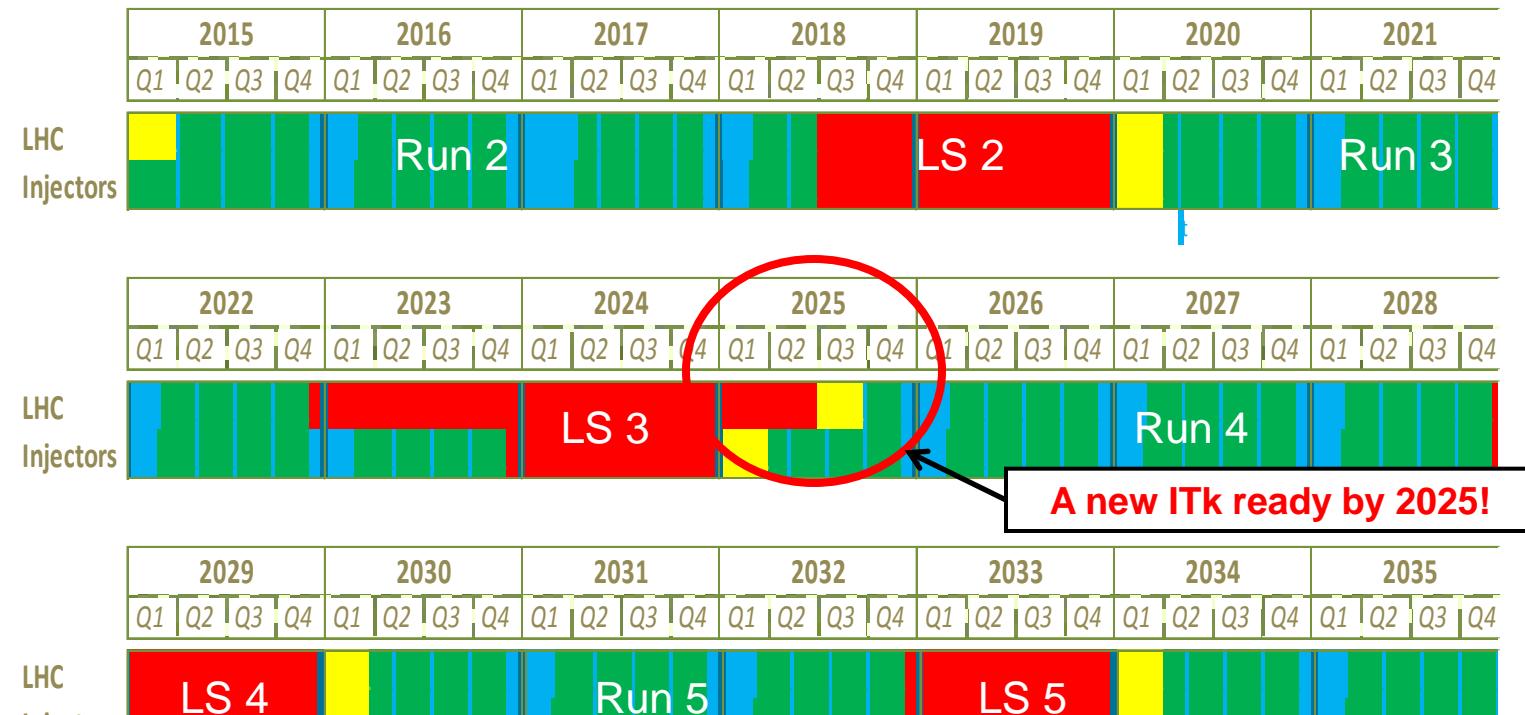


# HL LHC schedule

Only EYETS (19 weeks) (no Linac4 connection during Run2)

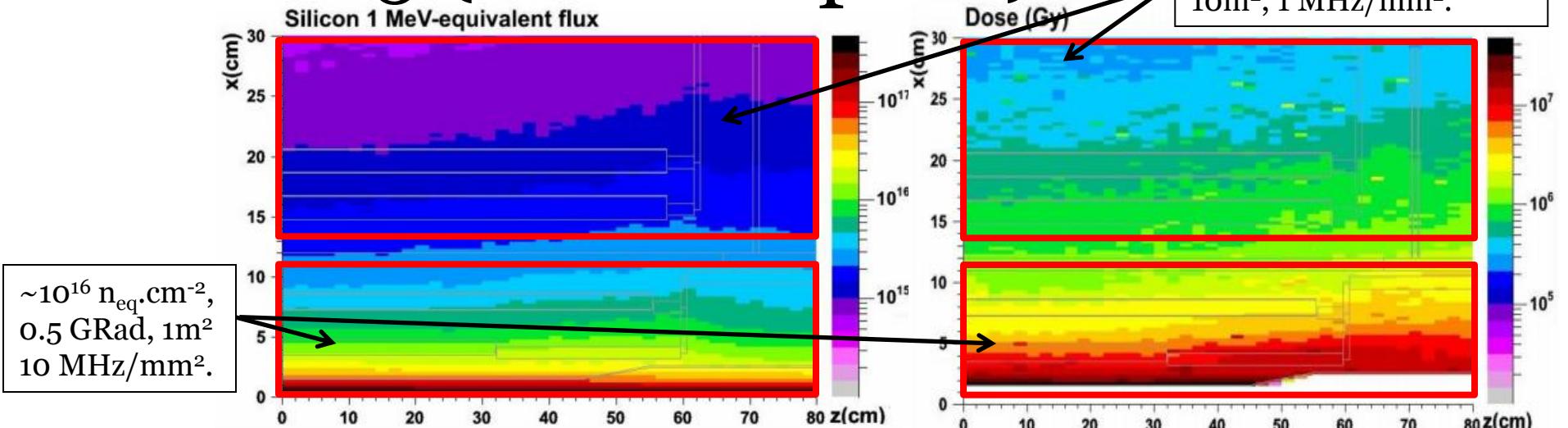
LS2 starting in 2018 (July) 18 months + 3months BC (Beam Commissioning)

LS3 LHC: starting in 2023 => 30 months + 3 BC  
injectors: in 2024 => 13 months + 3 BC



# HL-LHC environment

## >2025 (focus on pixel)



Fluence at low radius ( $3000 \text{ fb}^{-1} / 10 \text{ y}$ ):

NIEL:  $\sim 1-2 \cdot 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$

TID:  $\sim 500-1000 \text{ MRad}$

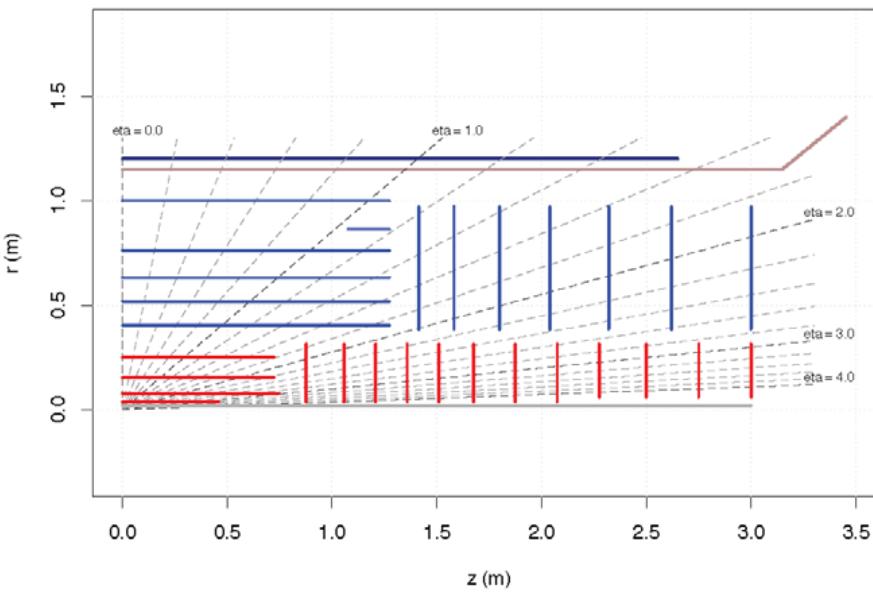
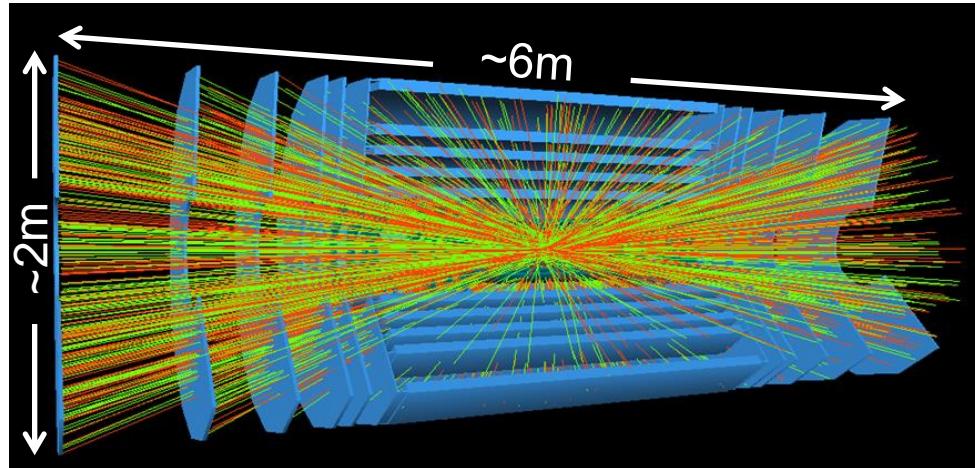
The new Inner Tracker should be rad-hard and cope with high occupancy.

A first possibility for pixels is **the use of a hybrid technology**:

- Sensor: planar silicon or 3D, diamond...
- Readout-Out Chip: deep-submicron rad-hard ICs (130nm,65nm) $\Rightarrow$  high granularity $\Rightarrow$  high resolution, low occupancy  $\rightarrow$  RD53

A second possibility is **an integrated technology** (electronics INTO the sensing element)  $\rightarrow$  **HVCmos**. Level of integration has range (passive  $\rightarrow$  “smart” pixels  $\rightarrow$  fully monolithic).

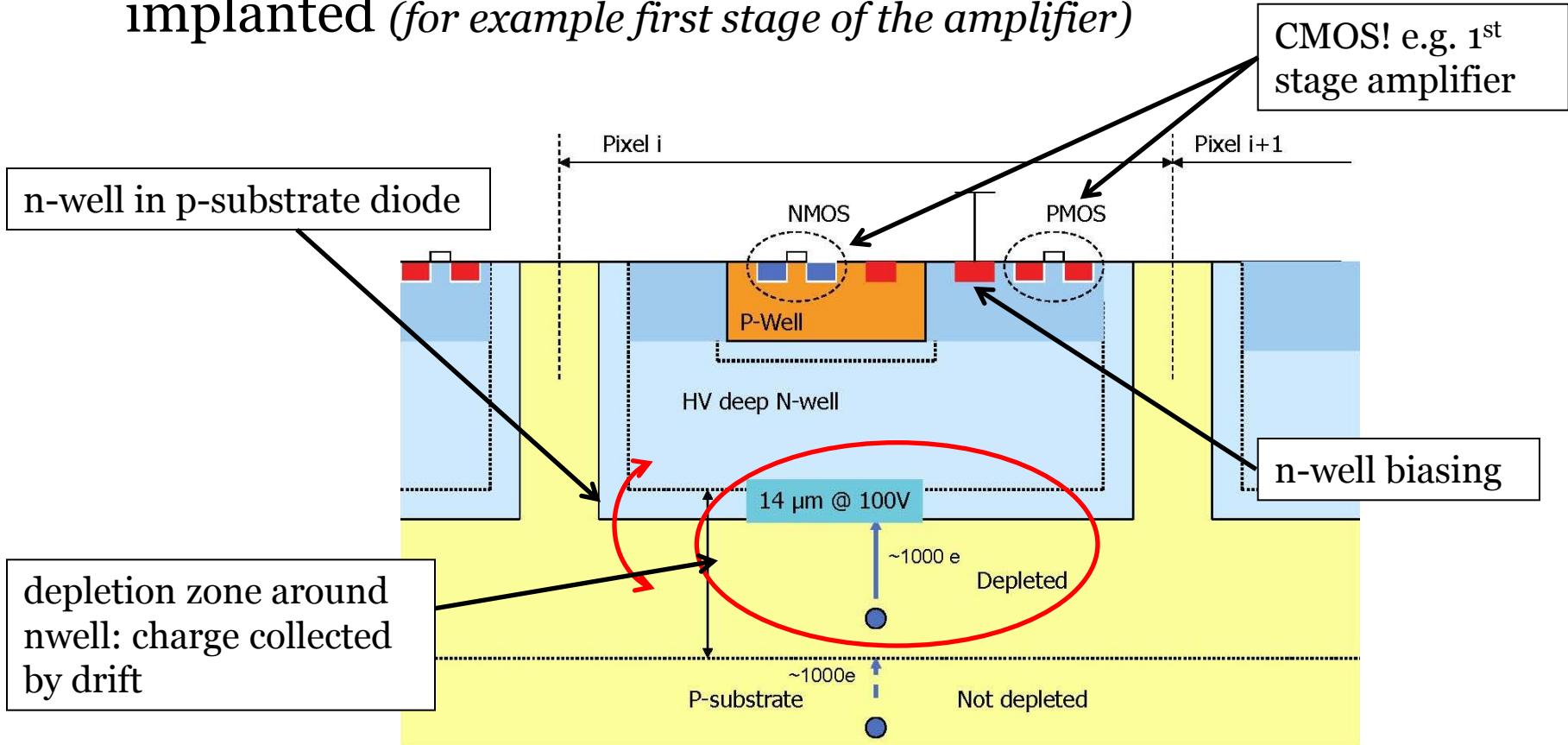
# New ITk



- **Pixel: ( $R < 40\text{cm?}$ )**  
→ 5 barrel layers
  - Inner 2: 3D/planar/CMOS
  - Outer 3: planar/CMOS
- $13\text{m}^2$  silicon
- $\sim 5000$  6 Gb/s links
- **Strip Tracker:**  
→ 4 barrel layers
  - Default: Double-sided Si-strips but could be CMOS !
  - $\sim 200 \text{ m}^2$  silicon
  - 2300 10 Gb/s links

# Sketch of HV-CMOS concept

- N-well in the P substrate where CMOS transistors are implanted (*for example first stage of the amplifier*)

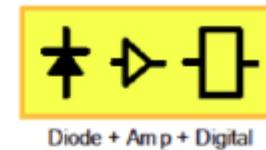
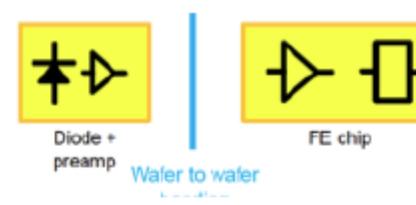


# Why HVCMOS pixels?

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- Collection of **charge by drift** → rad-hardness /speed.
- **Commercial processes** in large 8in or 12in wafers → potentially much cheaper than custom sensors.
- Potential for cheap **bonding process** (capacitive coupling gluing → CCPD, oxide or Cu-Cu bonding).
- Potential for **smaller pitch** due to separation sensor+analog tier and digital tier (a la 3D!): dedicated digital IC or use available IC with sub-pixel coding in CMOS tier  
(explanations on sub-pixel encoding later in this talk)
- **Thin depleted zone** (15-100 $\mu$ m) reduce cluster size at large  $\eta$  (reduce data rate, enhance 2 tracks resolution, better rad-hard)

# CMOS sensor implementations



## Passive CMOS sensors

- Study charge collection
- Passive Sensor to hybrid detector
- Possible cost advantage

## Active sensor + Digital chip

- Hybrid detector for high hit rates
- On-sensor Digital functionality like sub pixel encoding
- CCPD hybrid detector

## Active Sensor with standalone readout

- Thin monolithic CMOS sensor (DMAPS)
- Analog stage optimization
- On-chip digital readout

## Several concepts:

- **With digital tier**: For initial prototypes, FE-I4 digital tier is available, for final **FE-RD53 (TSMC 65nm)** will be suitable (or adapted design to smaller pitch?).
- **Low occupancy layers** (outer pixel, even strips) can be made in one tier with classical column or periphery readout architecture reducing the cost for large areas → **real monolithic concepts**.

# in ITK 2024

- Restricted here to pixel detector.
- **Inner pixel layers** ( $R=3\text{-}6\text{ cm}$ ). Strong radiation hardness demand to  $\sim 500\text{ MRads}$ . Use of **FE-RD53** in **65nm** technology with  $50\times 50\text{ }\mu\text{m}$  pixel size. **Four CMOS  $25\times 25\text{ }\mu\text{m}$  sub-pixels** with thickness  $<50\text{ }\mu\text{m}$ ? “à la 3D elect.” → **Higher granularity!**  
(solutions: sub-pix encoding / 4 inputs per  $50\times 50\text{ }\mu\text{m}^2$  region)
- **Outer pixel layers**  $R > 15\text{ cm}$ .  $\sim 100\text{ MRads}$ . Use **FE-Ix** digital tier with **HVCMOS** pixels  $50\times 250\text{ }\mu\text{m}$  or smaller. Low cost bonding (gluing or C4 bumps) mandatory for cost reasons.
- **Outer pixel layers**  $R > 15\text{ cm}$ .  $\sim 100\text{ MRads}$ . Use **Full monolithic CMOS chip** with classical column readout. **Simpler modules, cheaper technology...**

# Goals for pixels: 2015/6

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- Many prototypes produced, in many technologies.
- Large area demonstrator for 2015/6: HVHR-CMOS capacitively coupled to FE-I4B. Need to demonstrate:
  - Operate **1×1 or full size 2×2 cm<sup>2</sup>** demonstrator.
  - Low noise (**<1% pixels masked**).
  - MIP **>99 % detection efficiency**.
  - Limited radiation hardness (**~100 Mrad, ~10.<sup>15</sup> n<sub>eq</sub>.cm<sup>-2</sup>**).
  - Glue **coupling** (but bump-bonding explored in //).
  - Module: **Wire-bonds**.
  - **Granularity**: conservative  $50 \times 250 \mu\text{m}^2$  or more aggressive  $33 \times 125 \mu\text{m}^2$ .
  - **Depleted zone of order 100 μm** or less.

# CMOS demonstrator program thus far

from N. Wermes 09/05/2016

Technology	comments	Groups involved in design (D) & characterization	prototypes	demonstrator	monolithic
<b>AMS 350/180 nm HV, &gt;10 kΩcm</b>	3-well process extensive tests	Karlsruhe (D), GVA, Liverpool (D), CPPM, Glasgow, Oxford, Barcelona (D), BN, CERN,	✓ CCPDv1 – v4 (180nm) + FE-I4	✓ H35_DEMO 350 nm (back 1/2016)	H35_DEMO has monolithic part
<b>Global Foundry 130 nm HR: 3 kΩcm</b>	huge vendor	CPPM (D), Karlsruhe (D), Geneva, Bonn, CERN	✓ HV2FEI4_GF		
<b>Tower Jazz 180 nm, 1-3 kΩcm, epi</b>	little dedicated attention so far	Bonn (D), Strasbourg (D)	✓ ? Pegasus_1&2 stand alone, monolithic		ALPIDE developments
<b>ESPROS 150 nm HR: 2 kΩcm</b>	back contact in process, generic design not for LHC	Bonn (D), Prague (D)	✓ EPCB01, EPCB02 stand alone		
<b>XFAB 130 nm 0.1 – 1 kΩ SOI</b>	<b>SOI technology</b>	Bonn (D), CERN CPPM	✓ XTB01, XTB01	planned ?!	planned ?!
<b>Toshiba 130 nm 3 kΩcm</b>	designs not yet thoroughly tested	Bonn (D)	✓ TSB01		
<b>LFoundry 130 nm 2-3 kΩcm</b>	extensive tests	Bonn (D), CPPM (D), IRFU (D) SLAC (D), CERN, Glasgow	✓ CCPD_LF CCPD_LF + FI-I4	✓ CCPD (CPPM, IRFU, Bonn) (subm. Feb. 16)	MONOPIX_01 (5/2016) (Bonn, CPPM, IRFU) COOL_01 (SLAC)
<b>ST-M (BCD8) 160 nm selectable kΩcm</b>	bipolar+CMOS+DMOS epi selectable	INFN Milano (D), Genova, Bologna, IIT Mandi	✓ KC53AB Testchip	planned TPM1	

# Demonstrator in LF technology

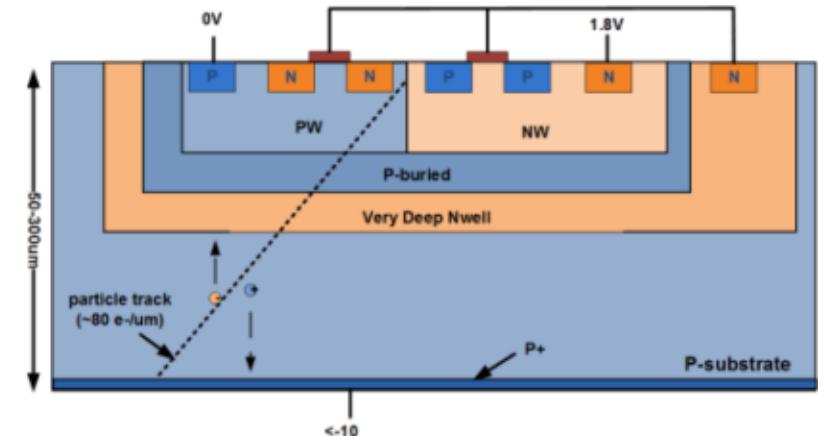
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# Background

- Team: Bonn/CPPM pursue long standing collaboration → HV/HR-CMOS LF since ~2014. IRFU has joined forces more recently on this topic (2015).
- **LFOUNDRY technology & projects**

## LFoundry CMOS3E technology:

- 150nm CMOS ( Avezzano, Italy)
- $2\text{k}\Omega\text{cm}$  p-type bulk
- Deep NWell available in real triple-well process
- HV process
- Thinning and back side metallization possible
- MLM3 (25.840mm x 9.505mm)



## LFoundry Projects

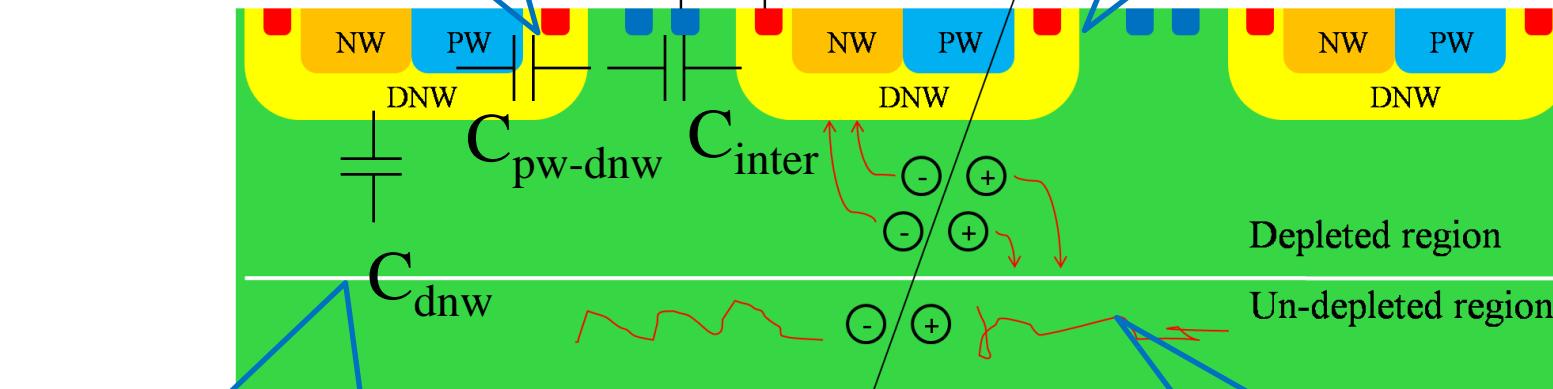
- CCPD-LF VA chip :  $5 \times 5 \text{ mm}^2$  ( Bonn, CPPM, KIT) submitted july 2015
- CCPD-LF VB chip :  $5 \times 5 \text{ mm}^2$  ( Bonn, CPPM, KIT) submitted july 2015
- **LFCPIX VA chip** :  $10 \times 10 \text{ mm}^2$  ( Bonn, CPPM, IRFU) submitted Feb 2016
- **LFCPIX VB chip** :  $10 \times 10 \text{ mm}^2$  ( Bonn, CPPM, IRFU) submitted Feb 2016
- **LF\_MONOPIX\_01 chip** :  $10 \times 10 \text{ mm}^2$  ( Bonn, CPPM, IRFU) submission April 2016
- **COOL 1 chip** :  $12 \times 10 \text{ mm}^2$  (SLAC, UCSC, KIT) submission April 2016

# What has been done using TCAD

AC: Input capacitance from the Pwell and DNW.

DC: Breakdown voltage in the critical region.

Jian Liu CPPM/ SDU

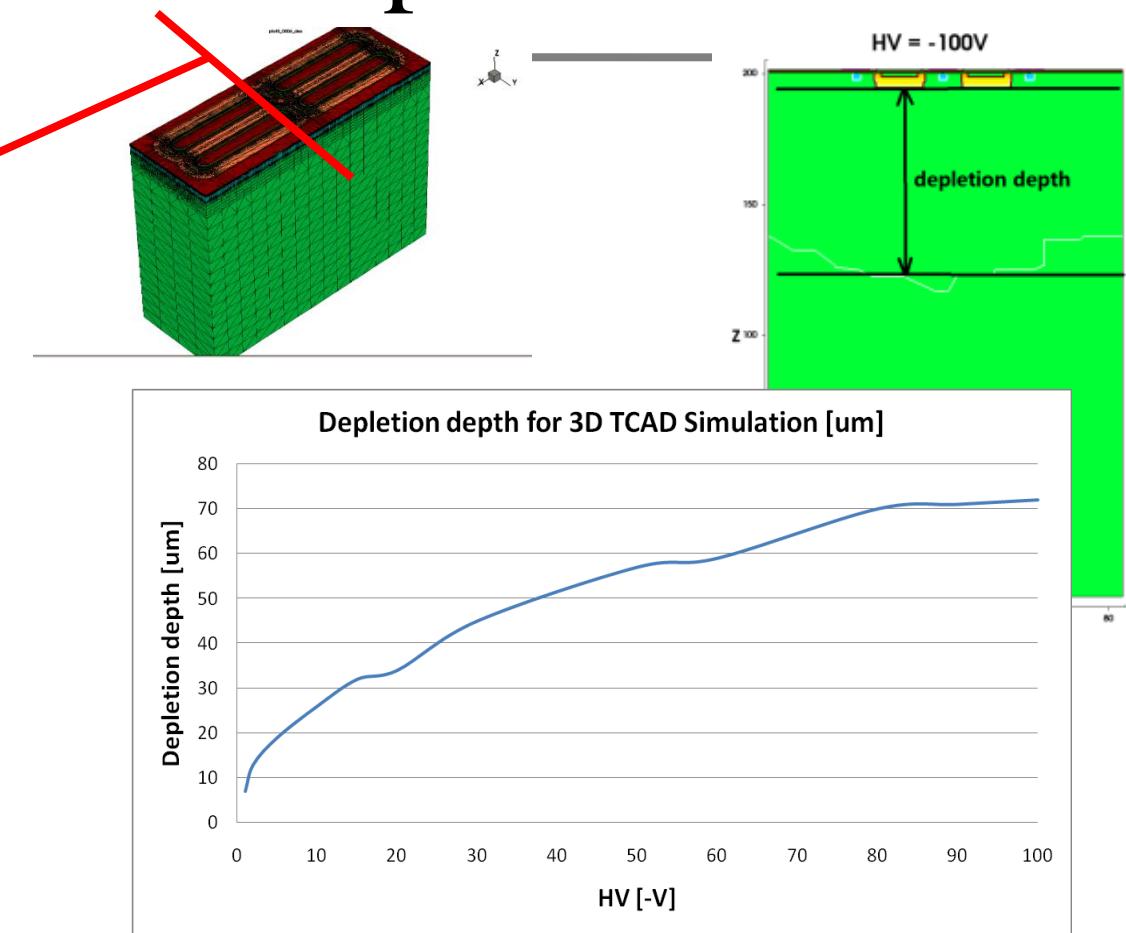
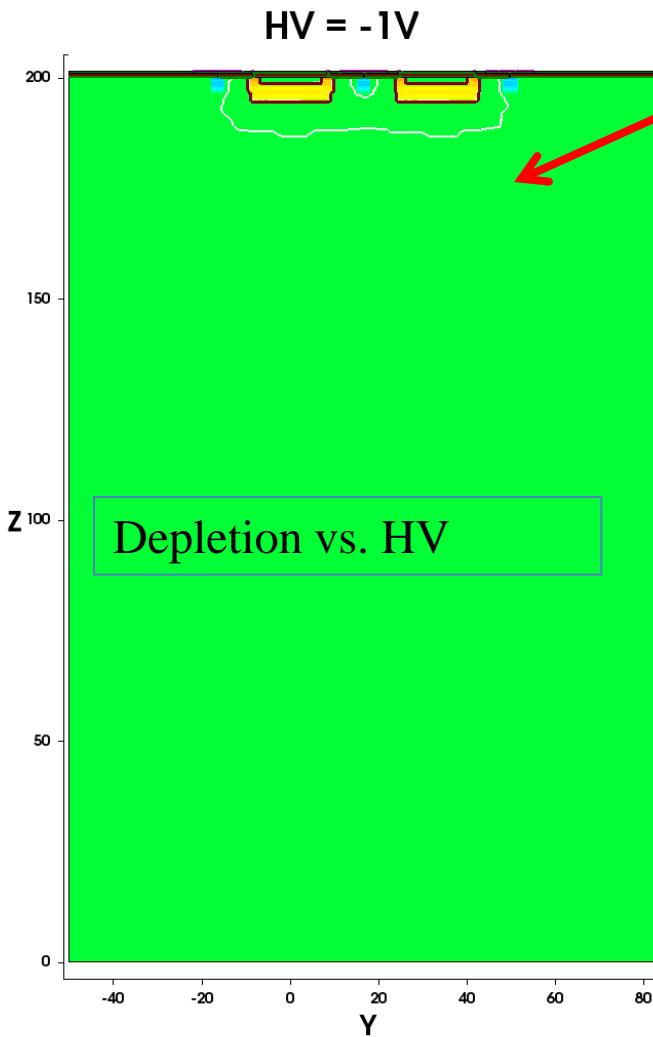


DC: Depletion evaluation depending on the biasing voltage and the resistivity.

DC: Leakage current.

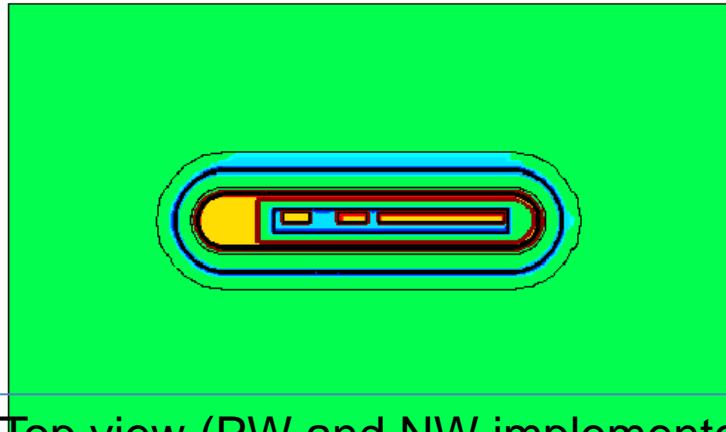
Transient: Charge collection behavior.

# LF VerA depletion

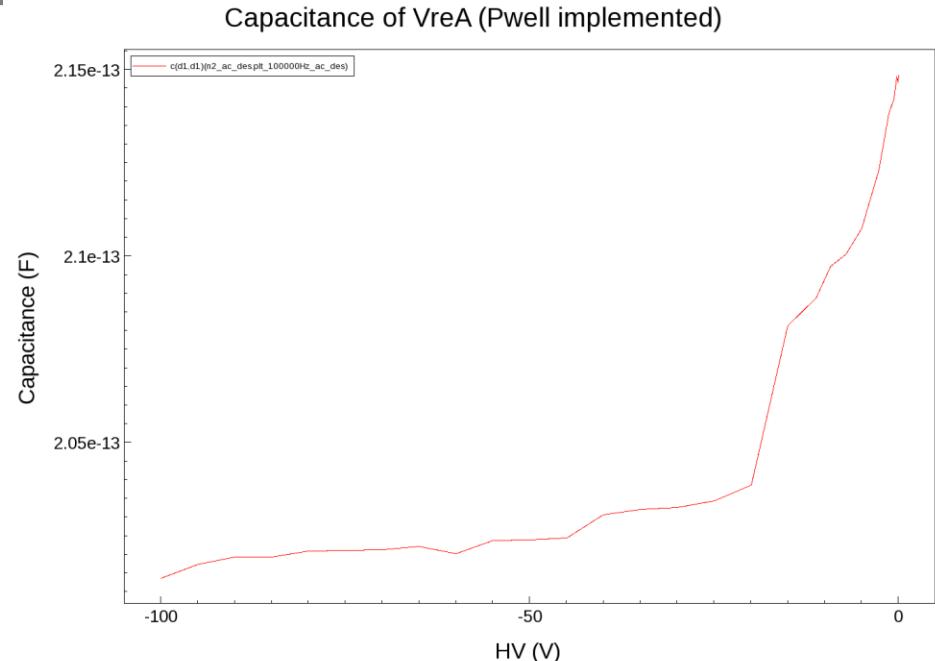
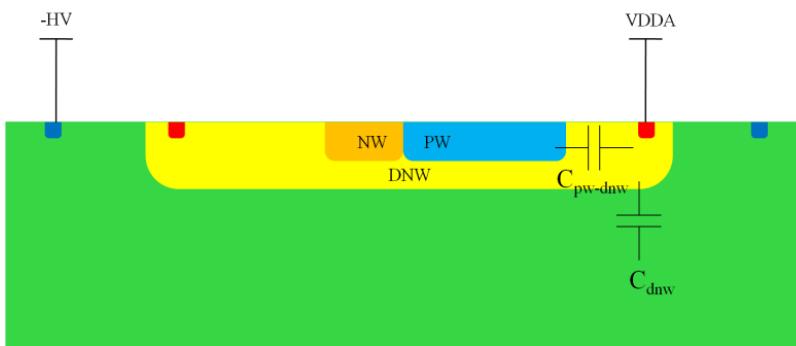


~70  $\mu\text{m}$  of depletion depth can be obtained @HV=-100 V

# LF VerA capacitance



Top view (PW and NW implemented)

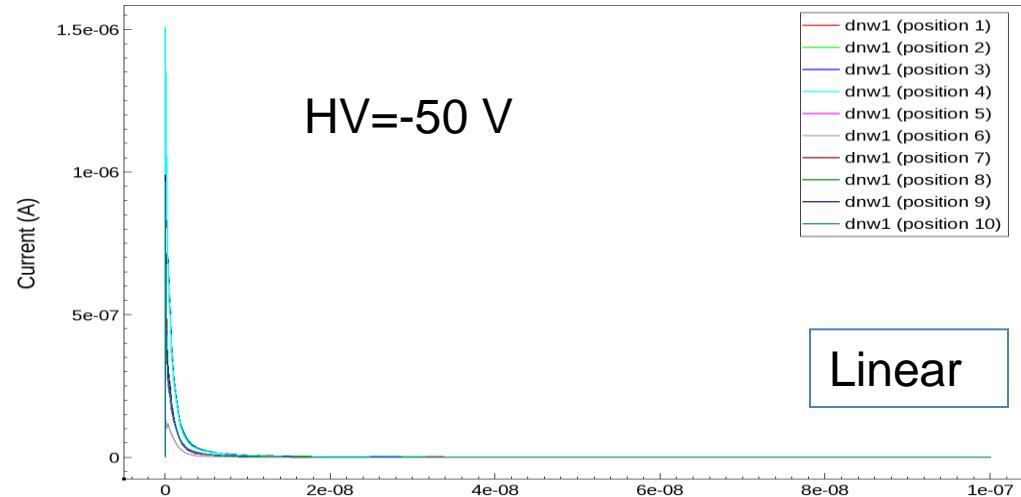


$C_{dnw}$  is  $\sim 50 \text{ fF}$  @  $\text{HV} = -50 \text{ V}$   
 $C_{pw-dnw}$  is  $\sim 150 \text{ fF}$  @  $\text{HV} = -50 \text{ V}$   
Total capacitance is  $\sim 200 \text{ fF}$  @  $\text{HV} = -50 \text{ V}$

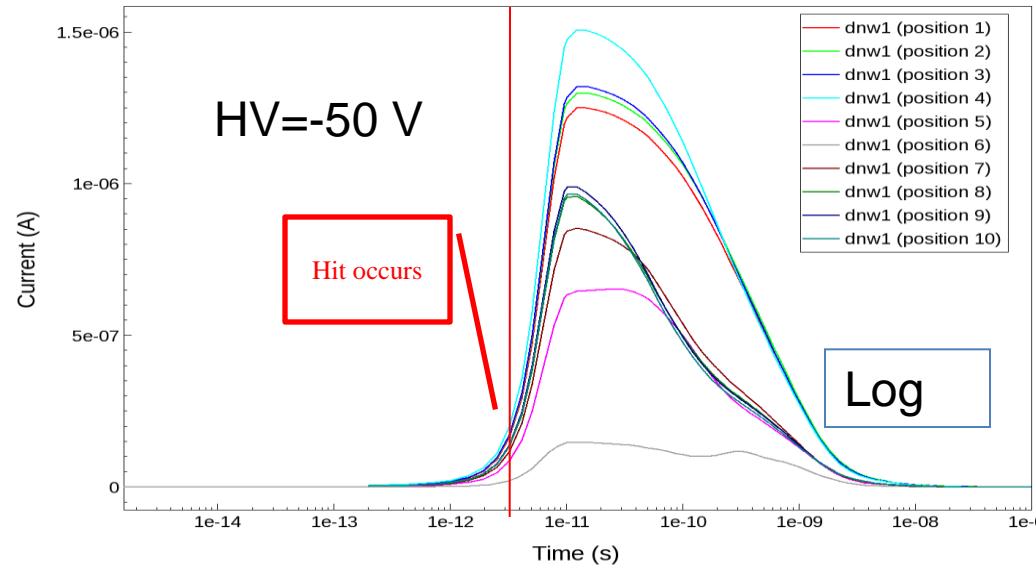
The capacitances mainly come from the  $C_{dnw}$  (between the DNW and the substrate) and the  $C_{pw-dnw}$  (between the PW/PSUB and the DNW)

# LFvA transient charge collection

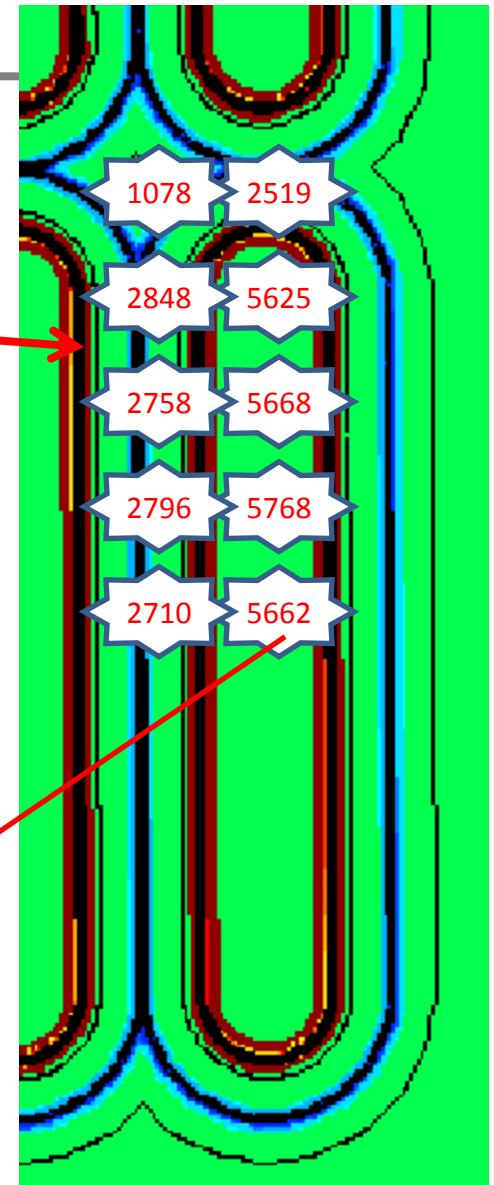
MIPs Responses with different impinging positions (HV=-50V)



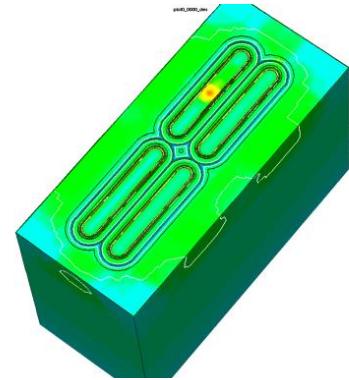
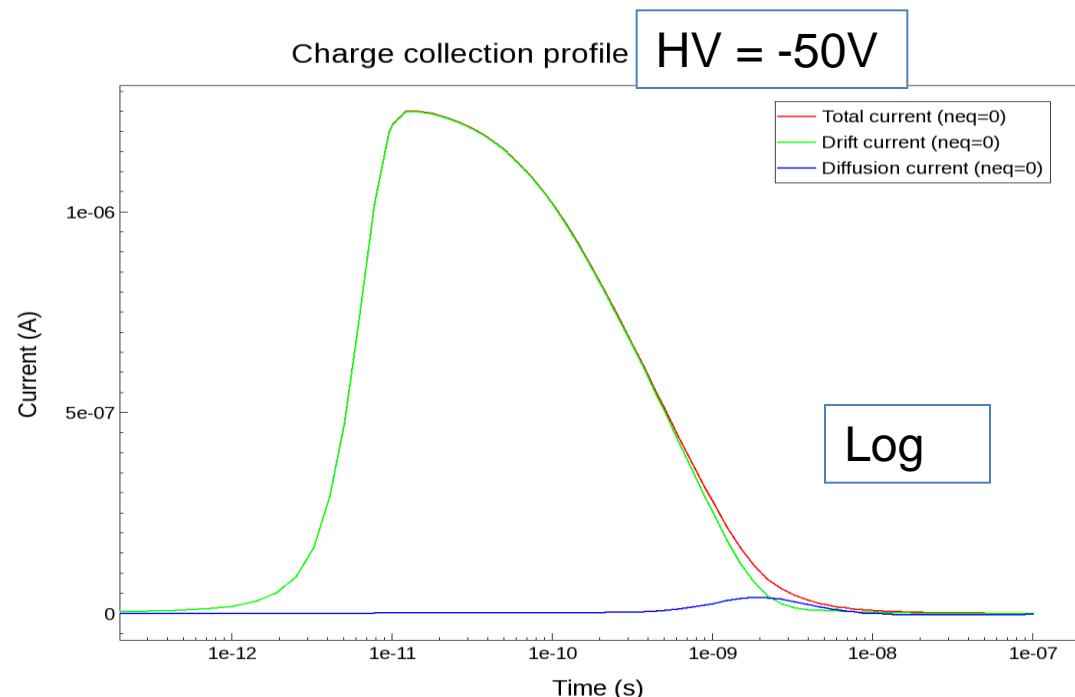
MIPs Responses with different impinging positions (HV=-50V)



Collected  
charges  
within 5 ns.



# LFvA transient charge profile



*x* *y* *z*

Table 2. p-type silicon trap model [5]

Type	Energy(eV)	$\sigma_e(\text{cm}^2)$	$\sigma_h(\text{cm}^2)$	$\eta(\text{cm}^{-1})$
Acceptor	E <sub>c</sub> -0.42	$9.5 \times 10^{-15}$	$9.5 \times 10^{-14}$	1.613
Acceptor	E <sub>c</sub> -0.46	$5 \times 10^{-15}$	$5 \times 10^{-14}$	0.9
Donor	E <sub>c</sub> +0.36	$3.23 \times 10^{-13}$	$3.23 \times 10^{-14}$	0.9

concentration =  $\eta \times \text{fluence}$

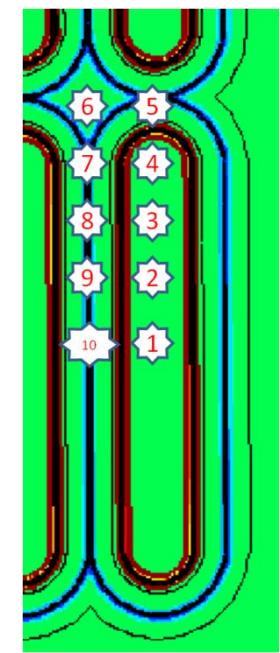
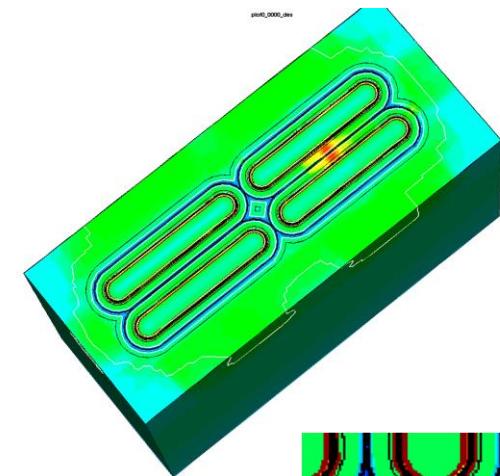
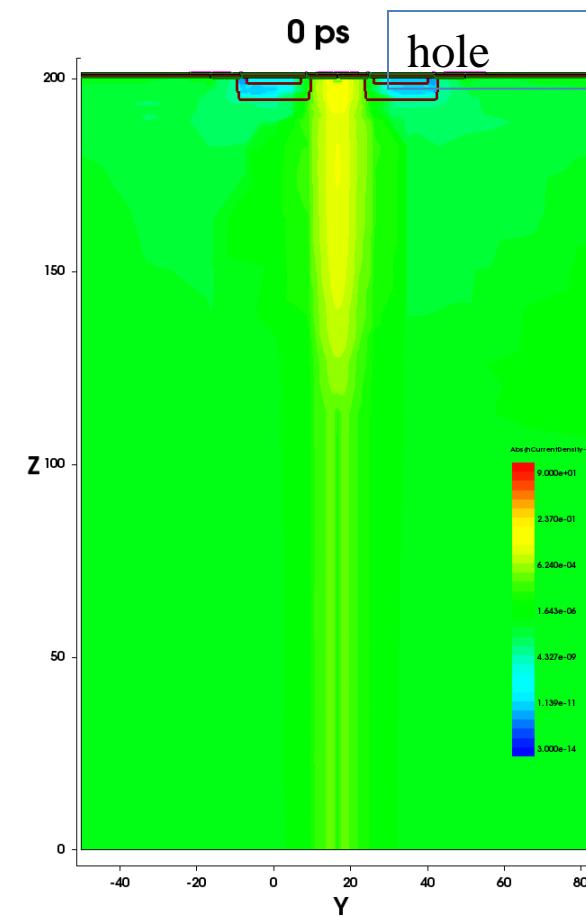
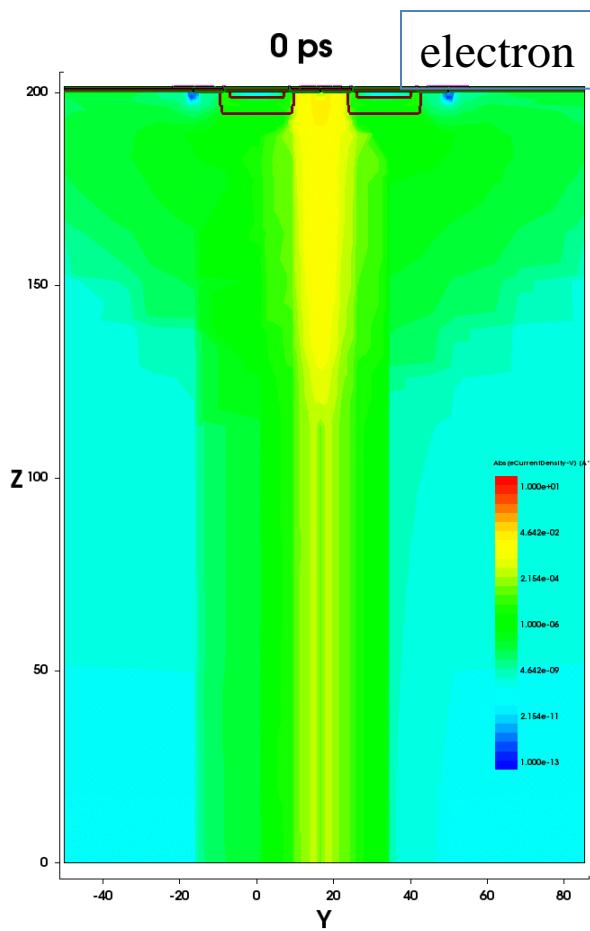
Enable the excess carrier generation in specific regions: depleted and un-depleted.

Fluence (neq.cm <sup>-2</sup> )	Drift(e-) @ -50V	Diffusion(e-) @ -50V
0	4812	850
1e14	4507	491
1e15	2536	188
1e16	1081	0

Before irradiation:  
 $Q_{\text{drift}} = 4812 \text{ e-}$  (85%) peaking at  $\sim 100 \text{ ps}$ .

$Q_{\text{diffusion}} = 850 \text{ e-}$  (15%) peaking at  $\sim 2 \text{ ns}$ .

# LFvA e/h current density (pos10)



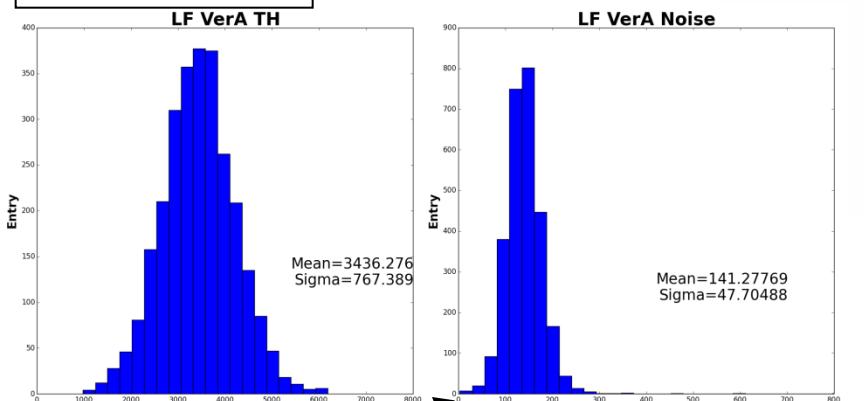
Electrons in depletion region drift towards DNW.

Holes in the upper side of depletion region drift towards p+.

Holes in the lower side of depletion region are swept out towards bottom.

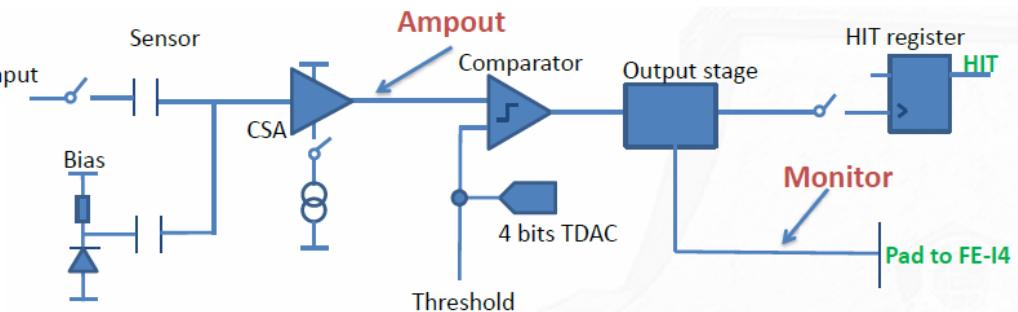
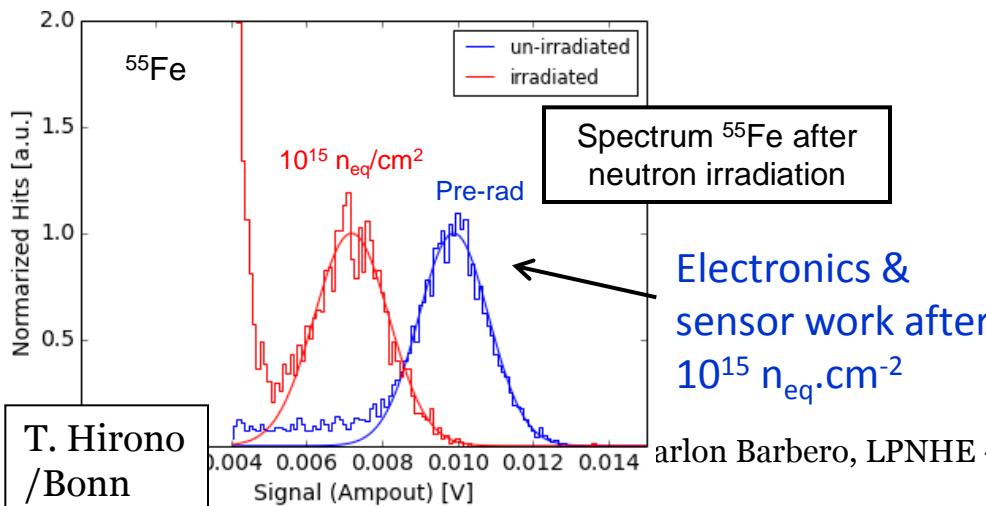
# LF VA/VB 2015 version

J. Liu / CPPM



Threshold and noise LF VA  
after 100 MRads proton

Pixel electrical parameter  
not much affected by 100  
MRads irradiation

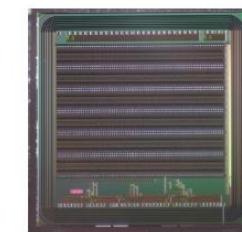


- CCPD LF VA

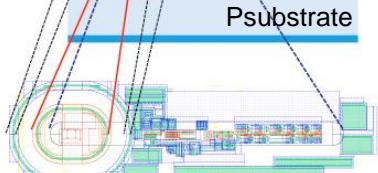
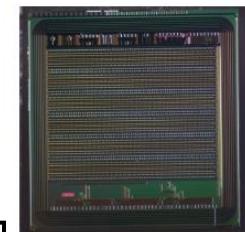
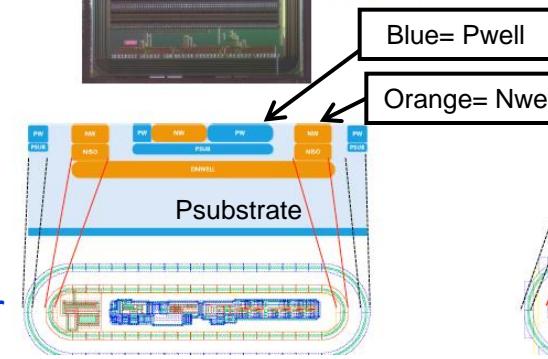
- CMOS inside collection electrode
- Test structures: NMOS and PMOS transistors

- CCPD LF VB

- Smaller collection electrode
- Test structure: diodes

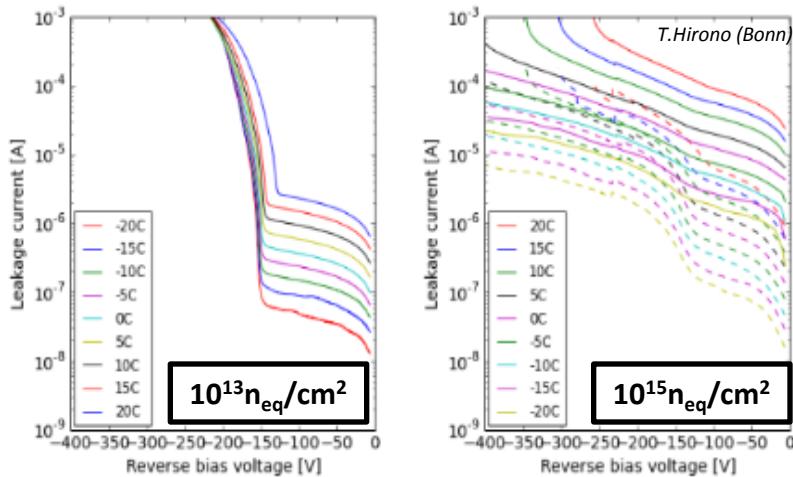


Design: Bonn, CPPM,  
Heidelberg

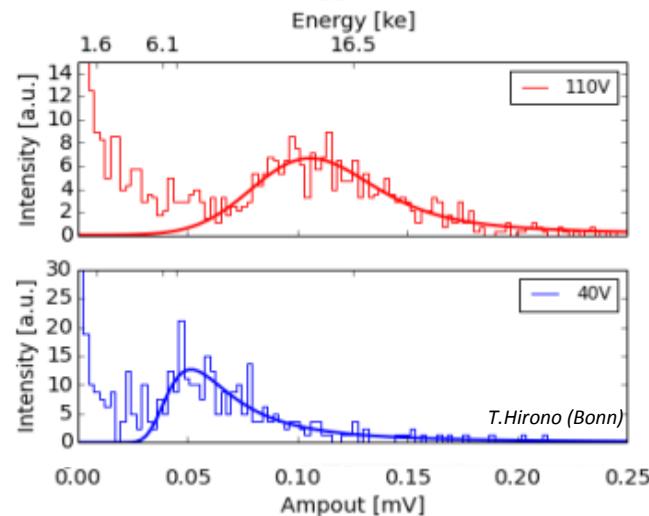


# LFoundry (first submision results)

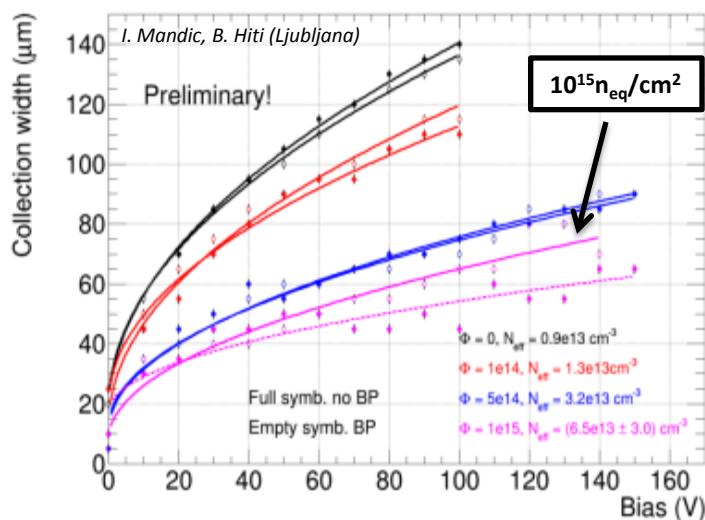
## Sensor reverse current



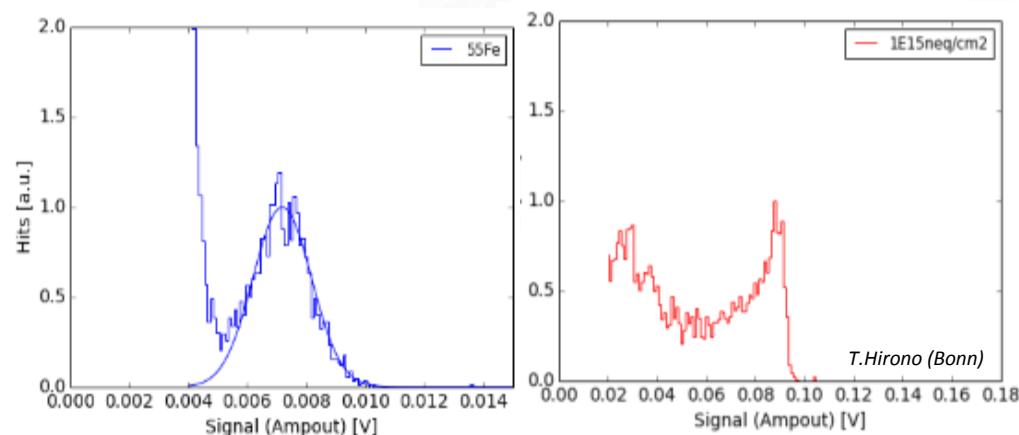
## MIP (3.2 GeV) spectrum (before radiation)



## Collection width (edge-TCT)

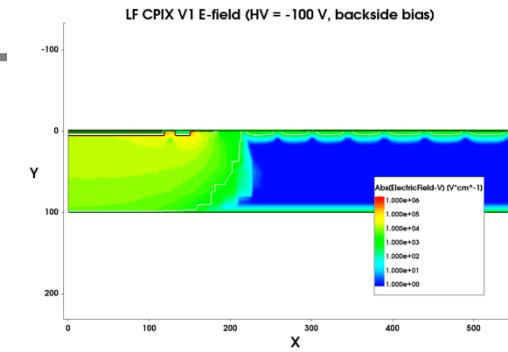
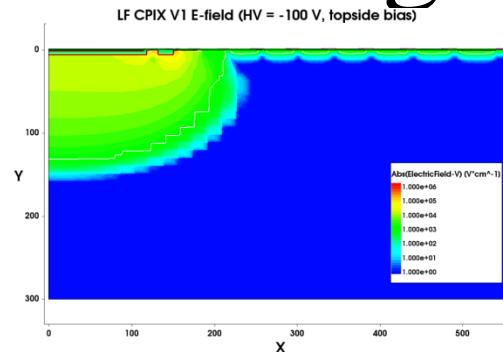


## Spectrum of $^{55}Fe$ and $^{241}Am$ after $10^{15} n_{eq}/cm^2$



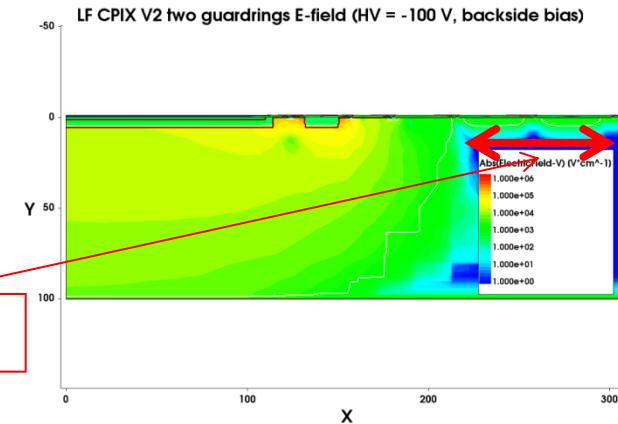
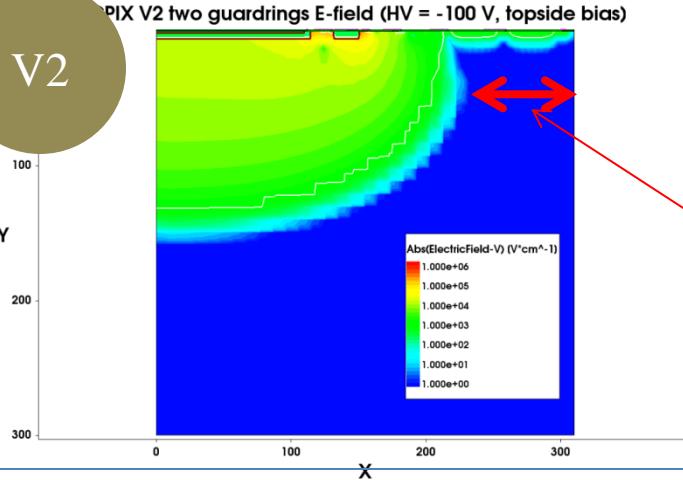
# Guard-ring for LF CPIX demo

V1



Big un-depleted area between depleted edge and cutting edge → guard-ring reducing is possible → reduced dead region.

V2



Pwellring + 2 floating guard-rings + backbias + seal-ring.  
The depleted region can not reach the chip edge even with removed 5 outer guard-rings.

# $10 \times 10 \text{ mm}^2$ demonstrator

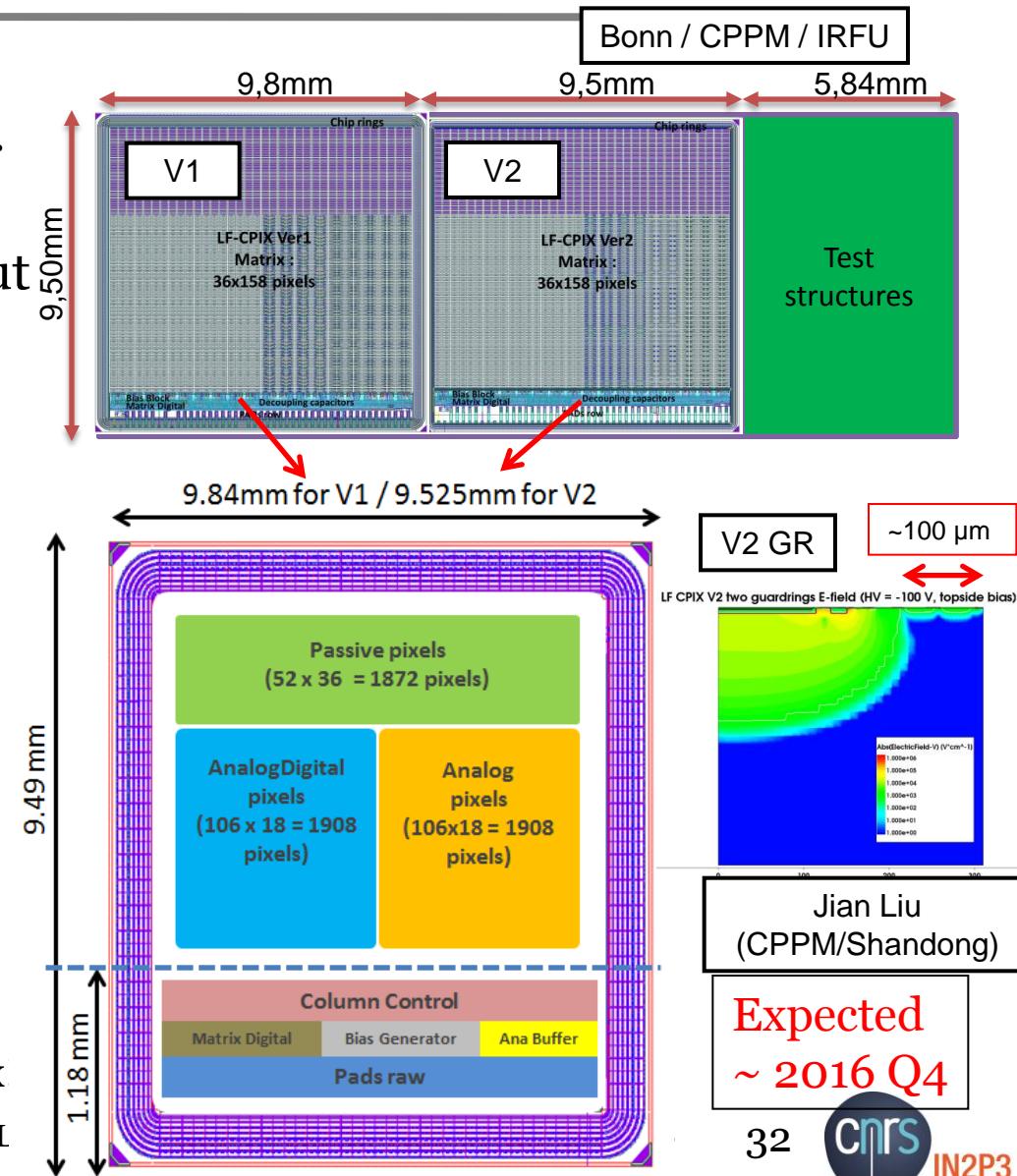
- Feb. 2016: MLM3.
- V2: V1 + new guard ring strategy.

Bottom matrix: Col. ctrl, bias gene.,  
analog buff., glob. config./SR readout

## Pixel Matrix :

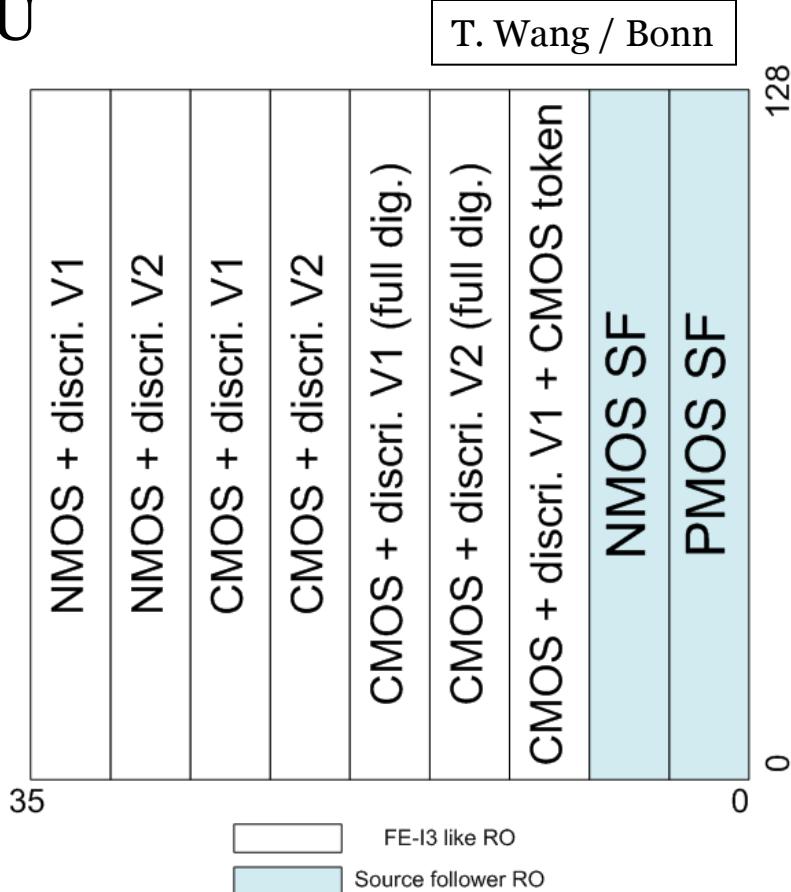
- Pixel  $250\mu\text{m} \times 50\mu\text{m}$  (FEI4-like)
- All pixels have bond pad to FEI4
- 3 sub-matrices :
  - **Passive**: only DNwell sense diode
  - **AnalogDigital**: à la LF VA, 4 flavors (different diode bias, diff. input transistors NMOS and PMOS).
  - **Analog**: preamp with complementary input CMOS, and 8 flavors (diode polarization, outputs “linear”, “saturated” or “digital”...).
  - Preamp out / hitOR available for all pix

HVCMOS pour SLHC, Marlon Barbero, I



# On-going: monolithic LF design

- Monopix design: Bonn/CPPM/IRFU
- 9 different flavors
  - Each has 4 columns
- **2 RO architectures**
  - **FE-I3 like pixels**
    - NMOS/CMOS pre-amp.
    - Old/new discri.
    - Different power domain for discri.
    - CS /CMOS token transmission
  - **Pixel without RO logic**  
(logic at end of column)
- Expected **submission date: end June**



# Performances using HV-CMOS

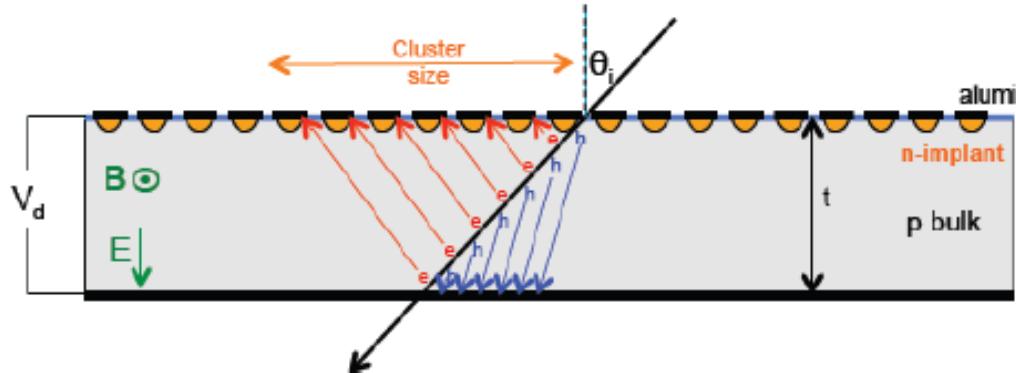
- Changes brought to Geant4-based simulation of current ATLAS pixel geometry.
- As a first try, to get faster results, **no fundamental change to current 3+1 pixel layer geometry.**
- HVCMOS could be exploited for outer layers, but we advocate here their use for the inner layer (current IBL) where they can have large impact on physics.

Alessandro Calandri / CPPM

# Modifying the sensor thickness

Current digitization method is the drift model:

- carriers drift in the depleted sensor depth taking into account direction of electric field, the Lorentz angle and the diffusion
- Geant4 provides entry point, exit point and energy loss
  - drift path is divided into 50 segments and the total charge is uniformly spread within these segments
  - for each segment, the charge is divided into 10 sub-charges to ensure randomness of the diffusion process.
- The drift is performed between the entrance and the exit point following the Lorentz angle + a Gaussian smearing that accounts for the thermal diffusion
- The signal on each pixel is the sum of all sub-charges that reached that pixel



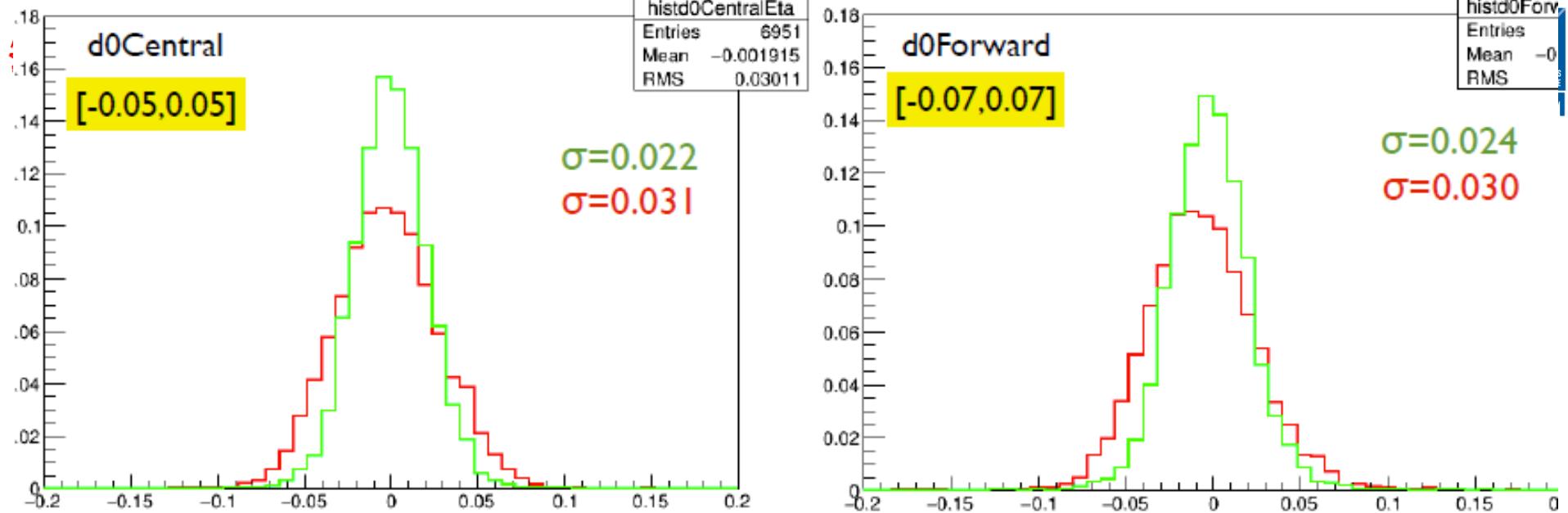
- The ionization potential for the silicon is regarded as constant
- The Lorentz angle is computed from the conditions of the database (temperature, bias voltage applied on the sensors)

[IBLPlanarChargeTool](#) and [IBL3DChargeTool](#) inside the package PixelDigitization can be modified to reduce the sensor thickness and perform the charge drift in a smaller depth



for this study, I've just modified the depletion depth for planar sensors ([IBLPlanarChargeTool](#))

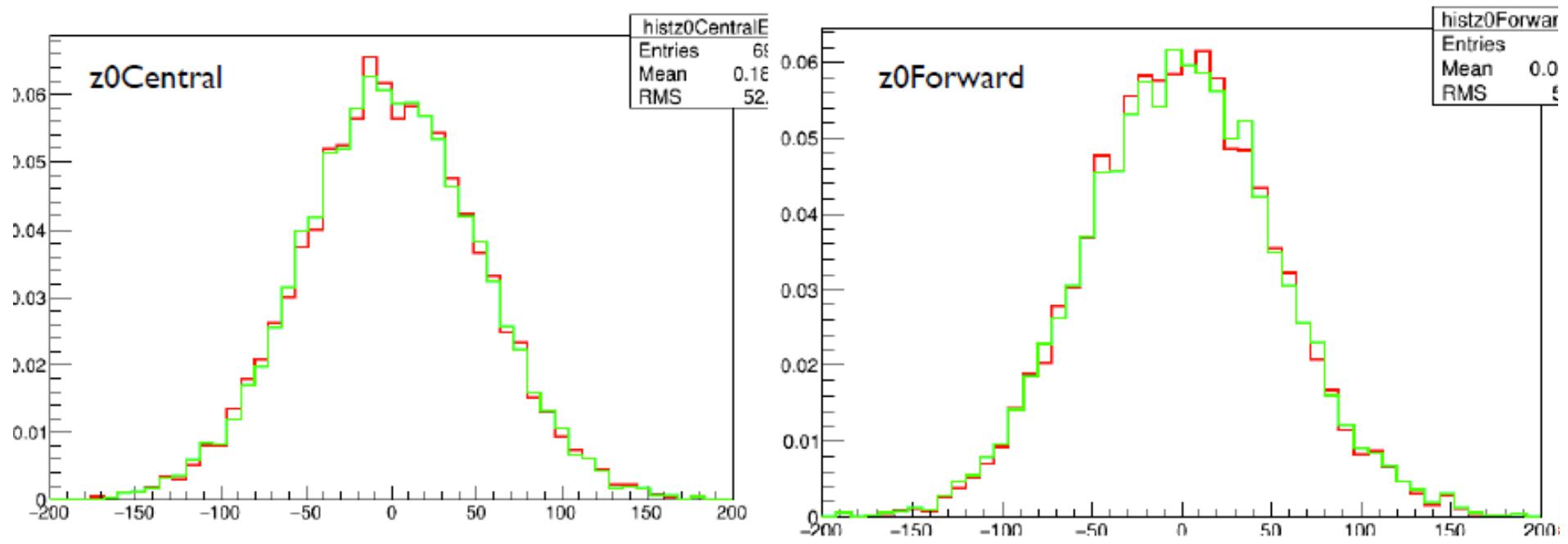
+ pitch reduction  $R\phi$  & z → next slides

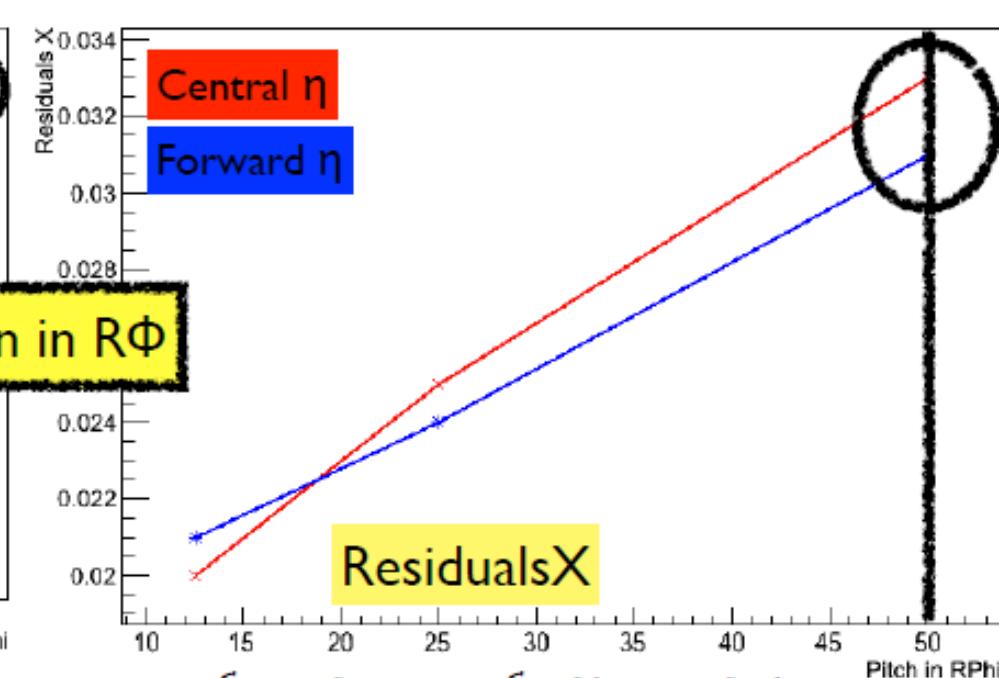
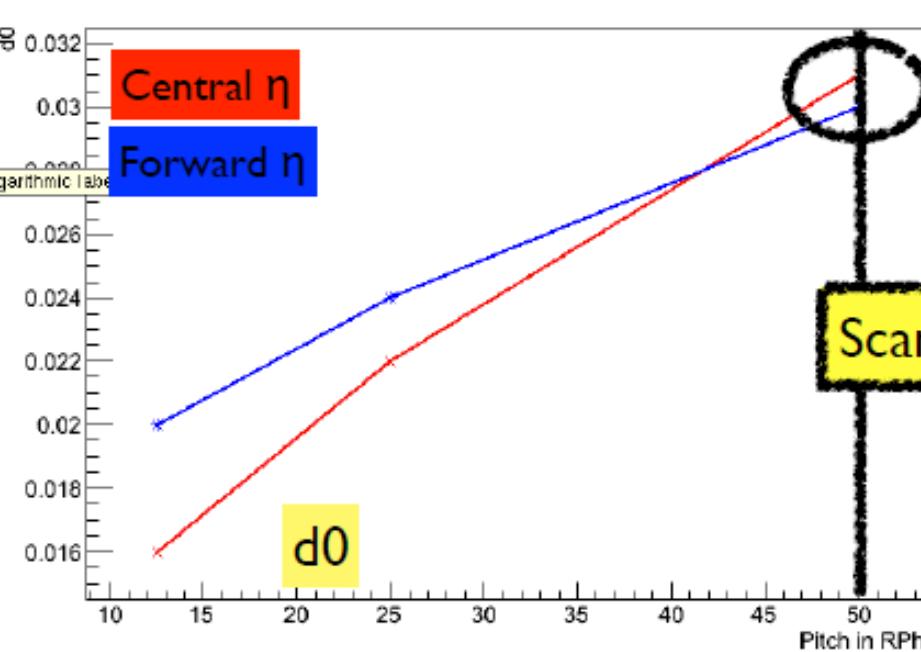


Default

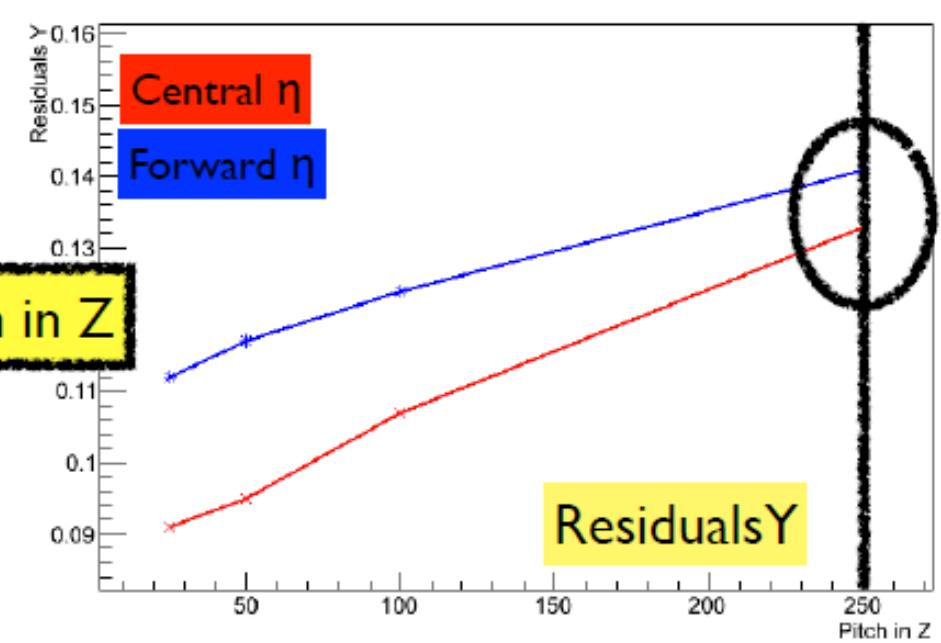
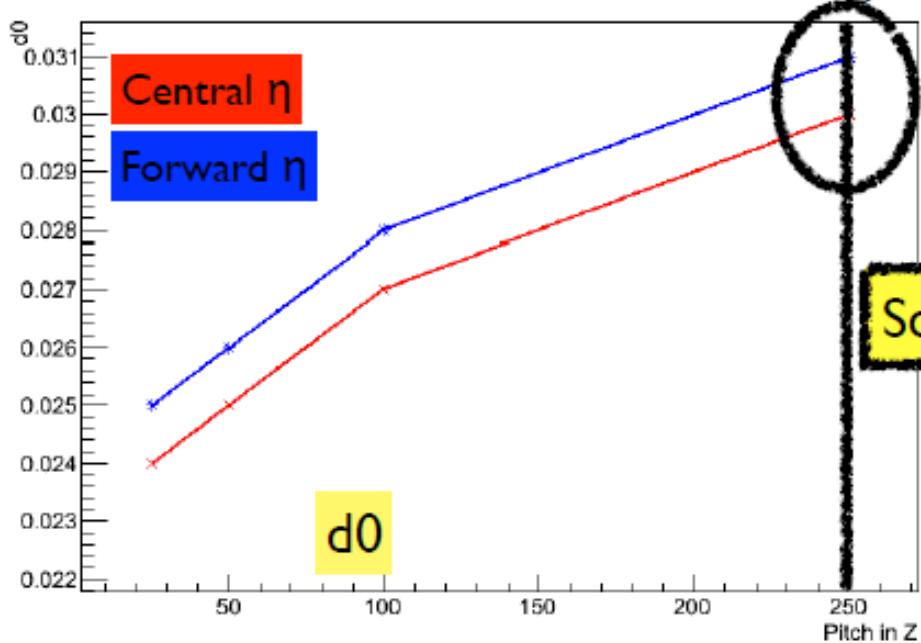
- Modified configuration: pitch in RΦ divided by 2 (50 → 25 micron)

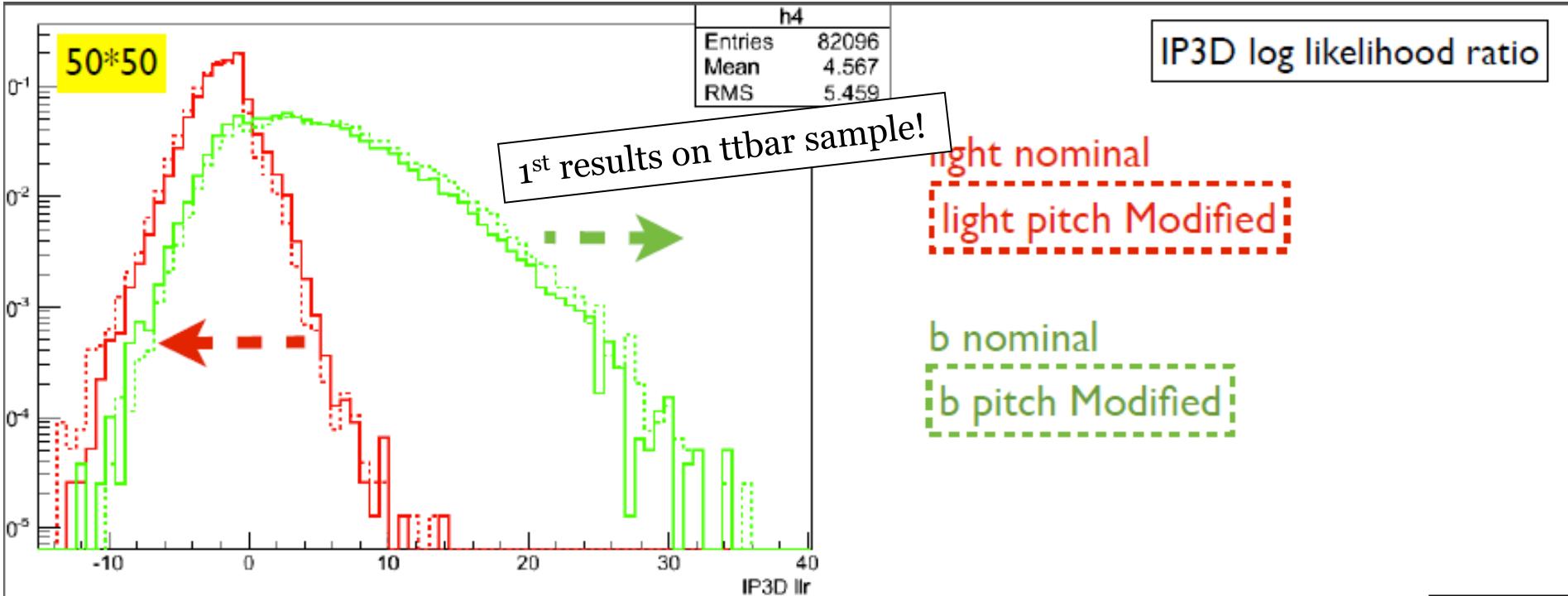
Modified



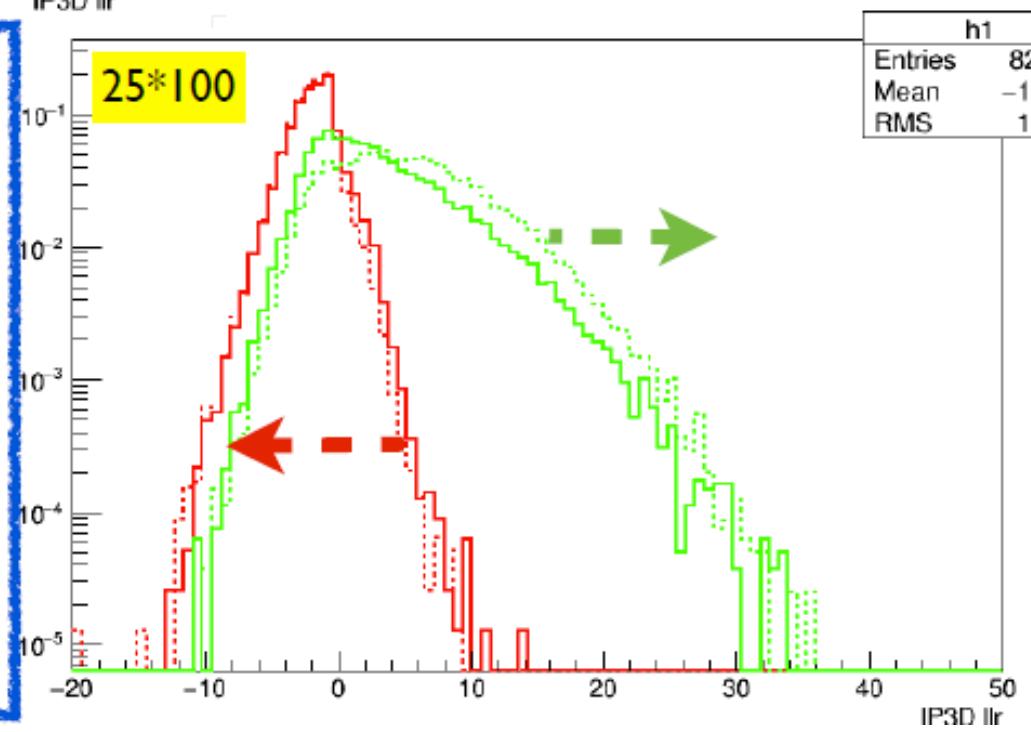


Resolution of tracking parameters as a function of the pitch size  
(single tracks)



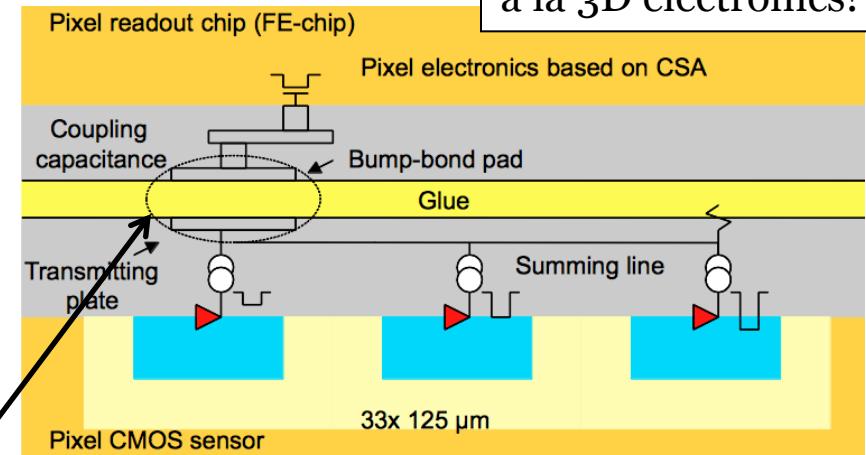
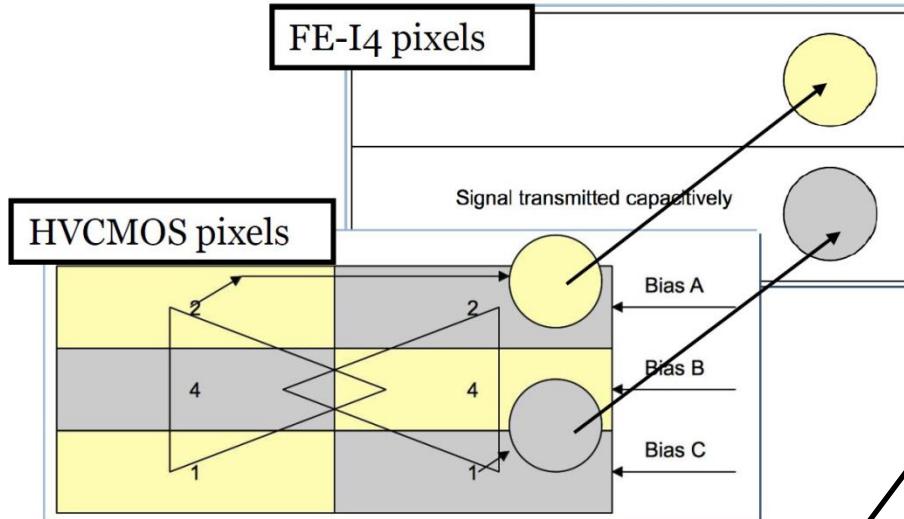


- Improvement in IP3D separation for modified pitch due to the gain in performance on the tagger input variables
- will produce the ROC curve b-jet efficiency vs light/c rejection to check the gain for a given working point of the new approach b-tagging performance-wise
- gain on final IP3D configuration can be easily translated in overall improvement on MV2 at the end of the b-tagging chain



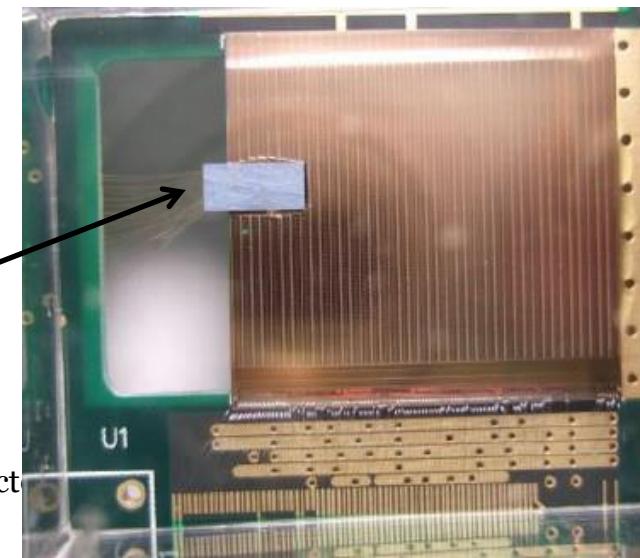
# Readout -with larger pixels-

- Combine **3 pixels** together to fit one FE-I4 pixel ( $50 \times 250 \mu\text{m}^2$ ), with HVCmos pixels **encoded by pulse height**.



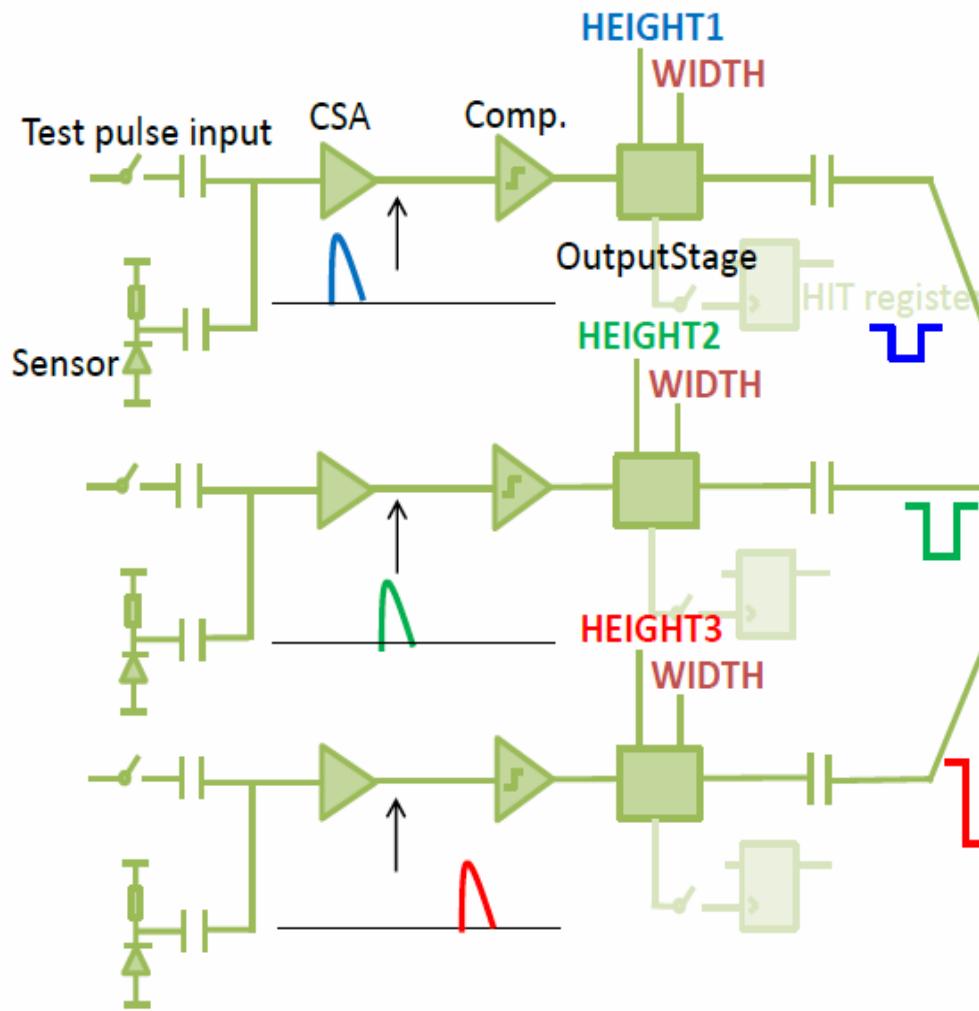
- Capacitive coupling OK: gluing!  
(perspective to avoid bump-bonding?)

The tiny HV2FEI4p1 prototype  
glued on the large FE-I4

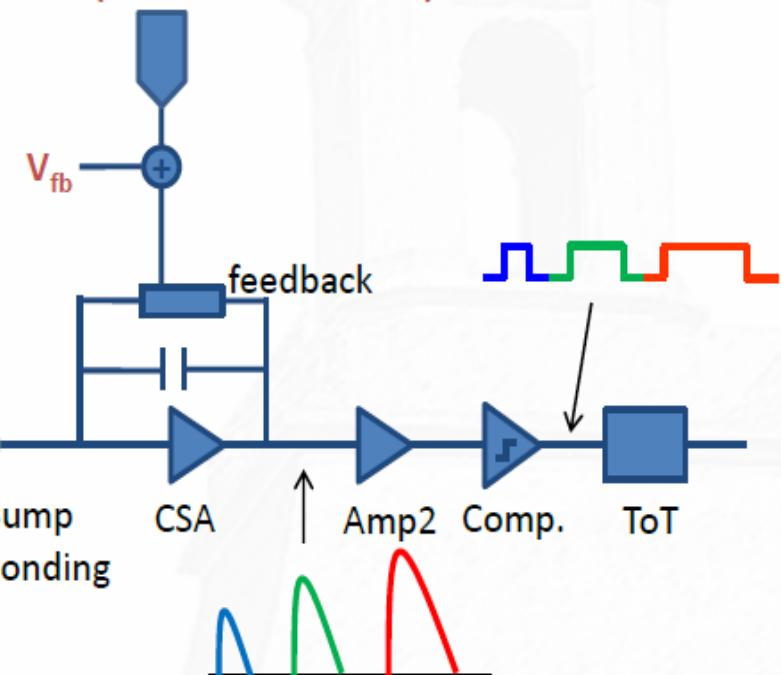


# Readout of CCPD\_LF and FEI4

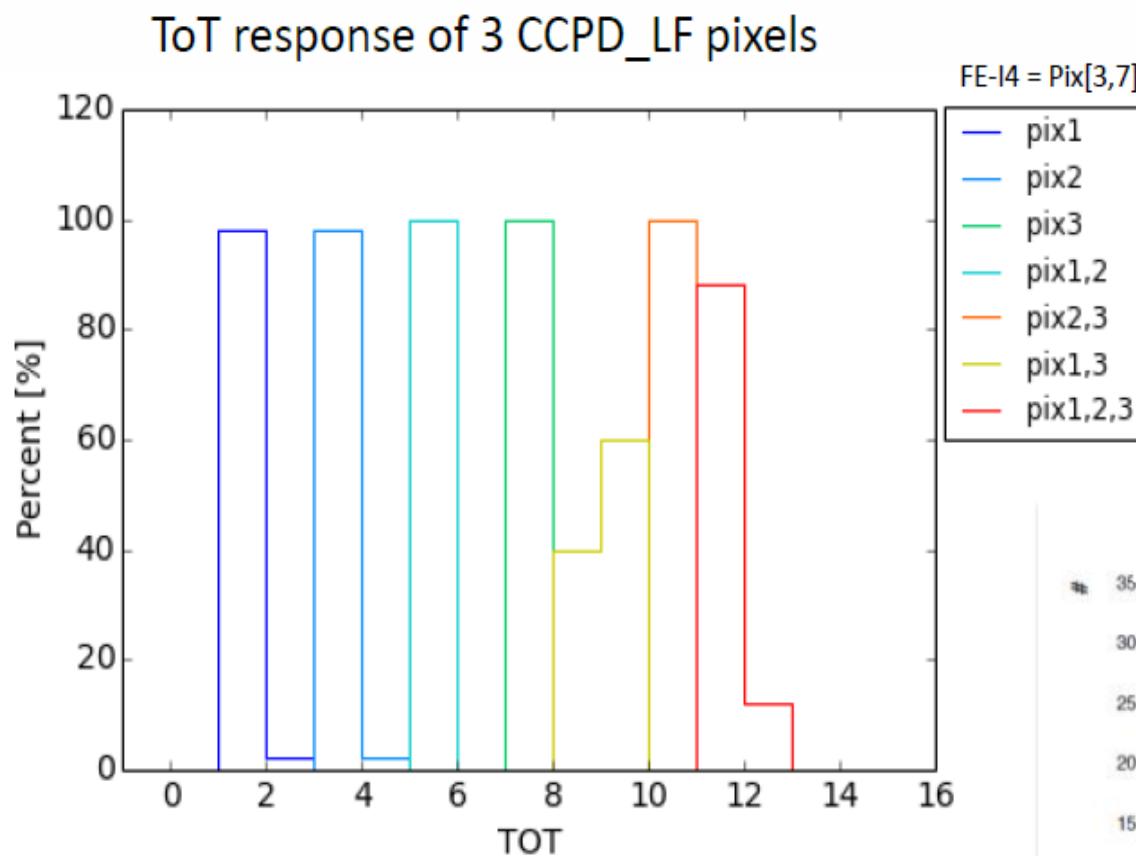
## CCPD\_LF



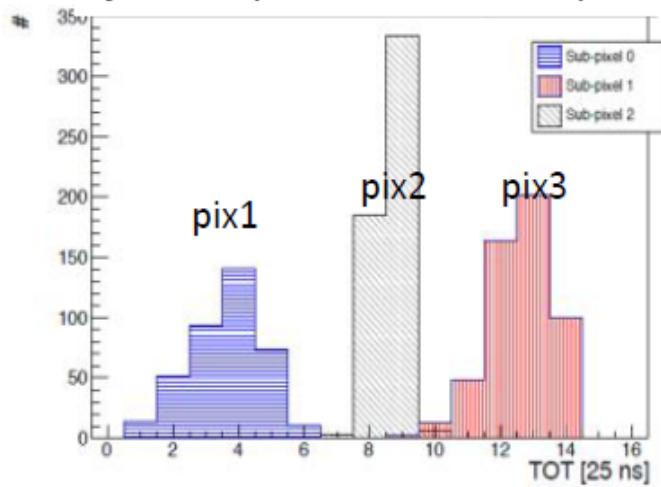
4-bits FDAC  
(local feedback tune)



FE-I4



cf. ToT response of 3 HV2FEI4 pixels



- Subpixel encoding works in some pixels
- Dispersion of ToT can be tuned to be  $\sim 2$  ToT

M. Backhouse Thesis (2014)

# Wrap-up

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- 2016+:
  - Module concept (coupling, TSV...), mechanics (power, cooling,...)
  - Increased radiation hardness.
  - Study efficiency at various test-beams (DESY, SLAC, CERN...).
- Wrap-up:
  - **TCAD simulations → sensor designs → Testing.**
    - CCPD LF Demonstrator submission in February (back in fall).
    - Monolithic demonstrator in LF (submission June).
  - **Simulations Geant4-based (single tracks / ttbar). Parameters: granularity, sensor thickness, detector arrangement.**
    - Two different goals:
      - 1- Low cost, **large scale**, high yield. → outer layers
      - 2- **Ultimate performance** → small granularity!

# Conclusion

- ATLAS: A rich physics program for many years, needs improved tracker → ITk project!
- CMOS Demonstrator Task Force → Large scale demonstrator available (AMS) or submitted (LF):
  - Waiting for these large size prototypes and extensive testing
- In concert with ATLAS/CMS RD53 electronics in TSMC 65nm.
- → New perspectives for better tracking at HL-LHC!

More studies of Higgs boson, Beyond the Standard Model theories -SUSY- and hope for the unexpected!

