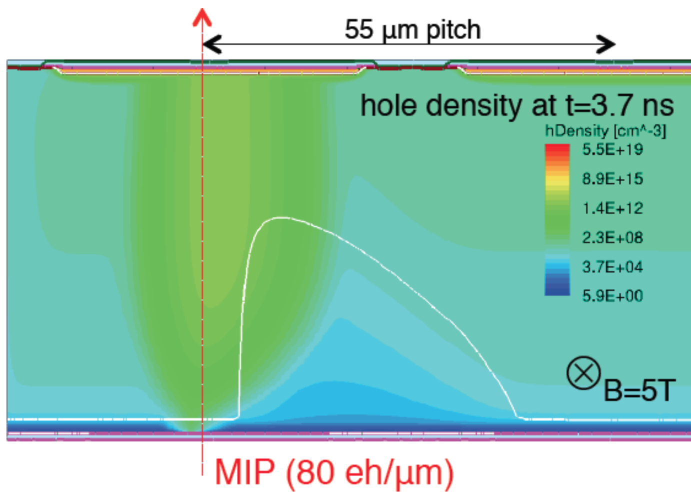
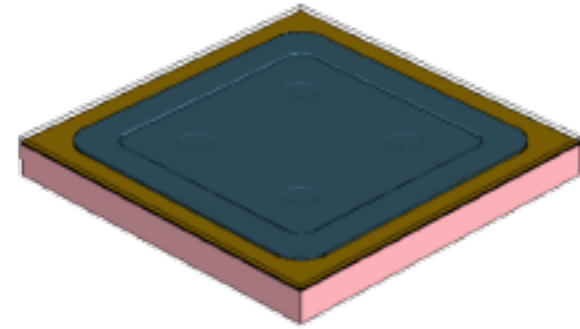




Simulation of Silicon detectors using Synopsys Sentaurus

Mathieu Benoit

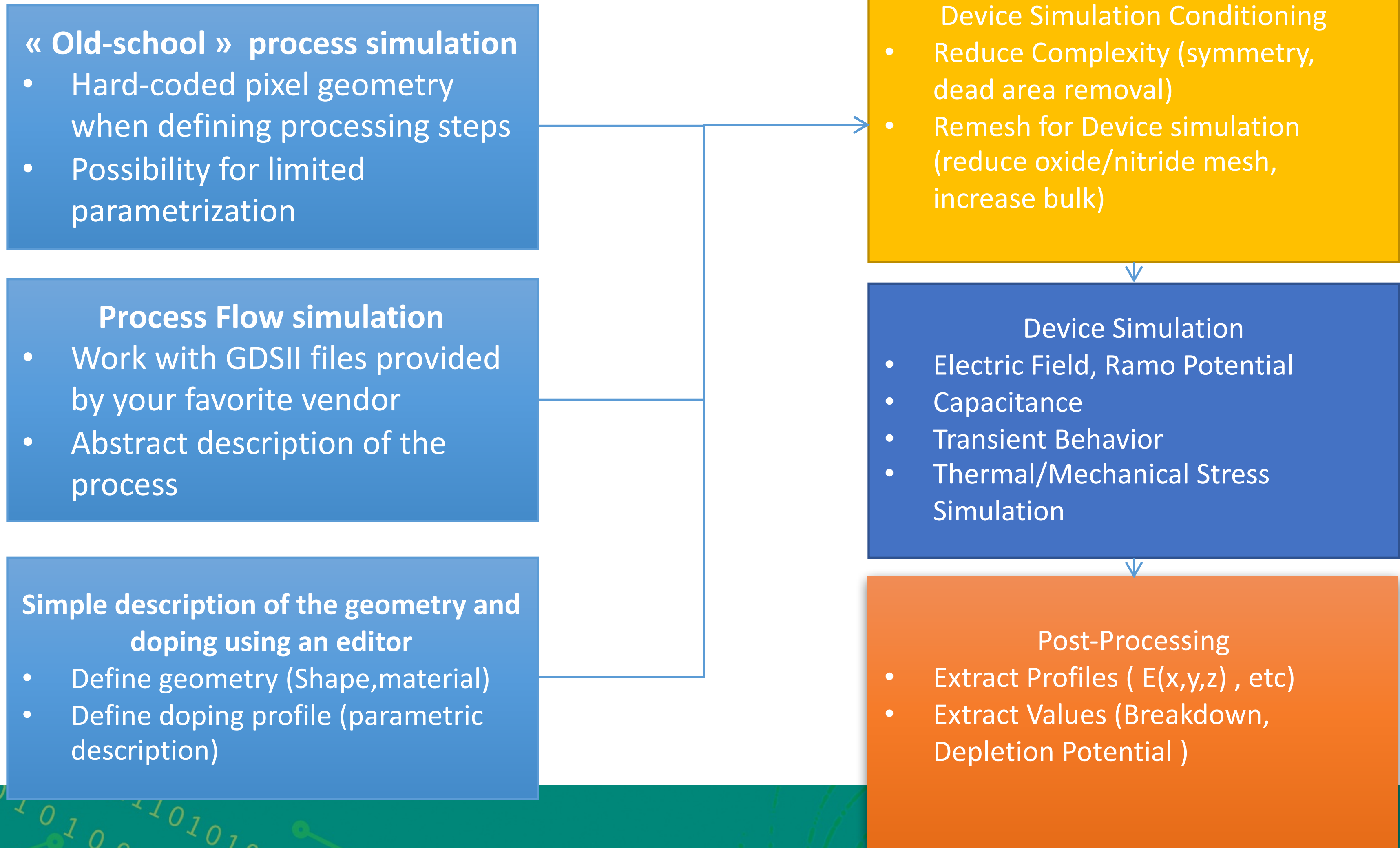
Thanks to Francesco di Bello (UNIGE), Matthew Buckland (CERN), Daiki Hayakawa (UNIGE), Lingxing Meng (UNIGE-University of Liverpool)

For the great content

Outline

- Simulation flow in synopsys Sentaurus
- Examples of process simulation
  - Process flow simulation using ligament
  - CMOS Sensor process simulation
  - CMOS device editor simulation
- Example of Device simulation
  - CMOS Sensor simulation
  - Guard ring structure optimization

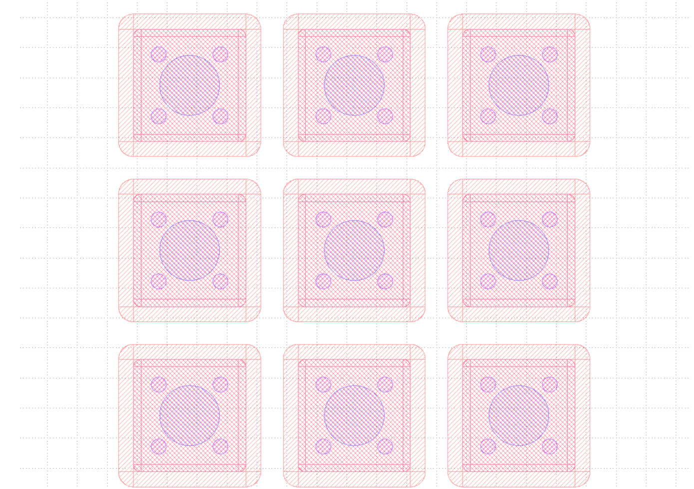
TCAD simulation workflow



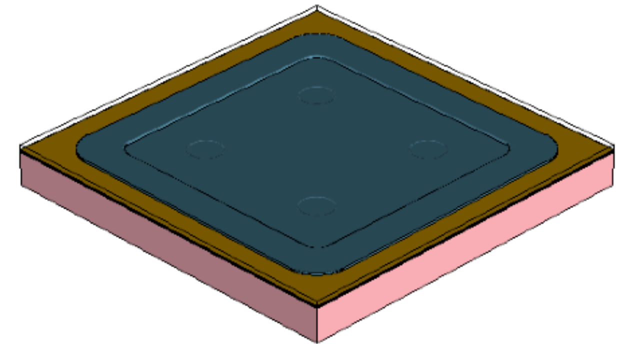
Process Flow Simulation

- Process Flow simulation allows for more automated studies of different geometries
  - Generate mask using your favorite software (pyGDS, Cadence, etc)
  - Use GDSII mask to define geometry
  - Use abstract and parametric description of the process
    - Implantation, lithography, deposits, annealing etc…
- Takes Advantage of multiplication of available CPU/RAM in the HEP Community
  - Chose a set of geometrical/Process/Electrical parameter to scan
  - Launch simulation in parallel using LSF Infrastructure (Synopsys Sentaurus @ CERN)

https://github.com/mathieubenoit/GDSII_Generator



Timepix 3x3 Pixel Mask set generated using pyGDS



Structure Generated using process Flow

Process Flow Simulation

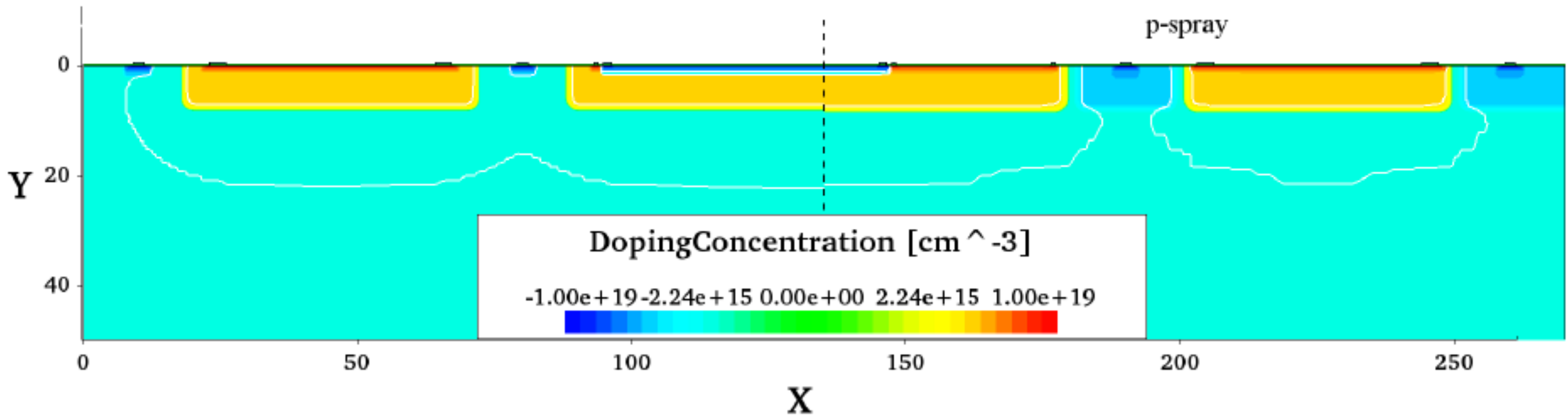
Variables & Macros | Flow | Unfolded Flow

Names	Arg	Value	Arg	Value	Arg	Value	Arg	Valu
Unfolded Flow								
#header								
insert	dios		sprocess	math coord.ucs	sde		tsuprem4	
environment	title	MPX3x3	save	true	grid	true	debug	false
substrate	material	Silicon	dopant	boron	concentration	0 /cm3	resistivity	5000 ohm
comment	text	Added process f						
insert	dios		sprocess	math numThread	sde		tsuprem4	
insert	dios		sprocess	#pdbSet Grid sM	sde		tsuprem4	
insert	dios		sprocess	grid remesh	sde		tsuprem4	
save	basename	After_first_mesh	format	plot	dios		sprocess	
#endheader								
deposit	material	Oxide	thickness	100 nm	dopant	default	concentration	/cm3
deposit	material	Nitride	thickness	200 nm	dopant	default	concentration	/cm3
implant	species	boron	dose	1e12 /cm2	energy	@PSPRAYENEF	tilt	0 deg
pattern	layer	IMPLANT	polarity	dark_field	thickness	0.1 um	side	front
save	basename	after_resist	format	plot	dios		sprocess	
insert	dios		sprocess	#etch type=anisi	sde		tsuprem4	
etch	material	Nitride	thickness	200 nm	etch_type	anisotropic	overetch	1
etch	material	Oxide	thickness	50 nm	etch_type	anisotropic	overetch	0
etch	material	Resist	thickness	default	etch_type	strip	overetch	0
implant	species	phosphorus	dose	@NDOSE@ /cm	energy	@NENERGY@ k	tilt	0 deg
save	basename	after_oxide_etch	format	dump	dios		sprocess	
pattern	layer	CONTACT	polarity	dark_field	thickness	0.1 um	side	front
etch	material	Oxide	thickness	default	etch_type	anisotropic	overetch	0
etch	material	Resist	thickness	default	etch_type	strip	overetch	0
save	basename	after_oxide_hole	format	plot	dios		sprocess	
deposit	material	Aluminum	thickness	300 nm	dopant	default	concentration	/cm3
pattern	layer	CANOD	polarity	light_field	thickness	0.1 um	side	front
etch	material	Aluminum	thickness	default	etch_type	anisotropic	overetch	0
etch	material	Resist	thickness	default	etch_type	strip	overetch	0
anneal	time	30 min	temperature	960 degC	pressure	1 atm	nitrogen	0 l/min
save	basename	top_n@node@	format	plot	dios		sprocess	
insert	dios		sprocess	paste direction=i	sde		tsuprem4	
insert	dios		sprocess	paste direction=l	sde		tsuprem4	
save	basename	one_per_three_i	format	plot	dios		sprocess	

Process Simulation

Process Simulation allow to define the bulk properties of the device to simulate

- Doping concentration
- Electrode position and contact surface
- Oxide surfaces
- Traps and defect concentration
- Well defined Mesh



CMOS Sensors process flow simulation

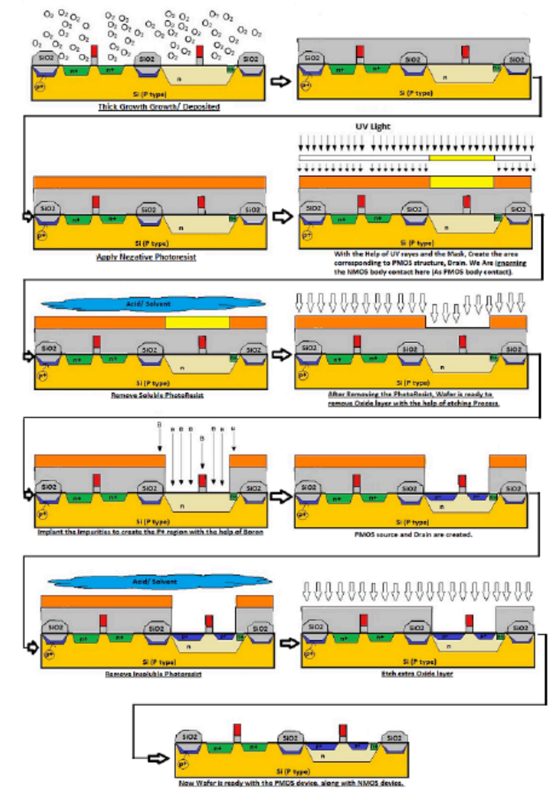
LFoundry CMOS process simulation

- Use sprocess script to simulate wafer processing
- $>$ 1200 lines of code
  (incl. empty lines and comments, but without mesh commands and masks)
- A lot of wafer surface preparation
- Not all steps are used: some are for other technologies
- Nice people, very responsive and helpful

LFoundry CMOS process simulation

1. Define gas mixings and flows
2. Define temperature ramps
    - Temperature
    - Ramping rate
    - Apply flow of gas mixture
3. Apply on process:
    - Move in wafer
    - Gas in
    - Ramp up temperature
    - Diffusion process
    - Ramp down temperature
    - Move out wafer
4. Define masks
5. Apply masks on etching (e.g. deep trench isolation)
6. Define implantation
    - Element, dose, energy, angle, tilt
7. Apply implantation process using only photo mask*
8. Annealing

Note: only some of the parameters are named here.



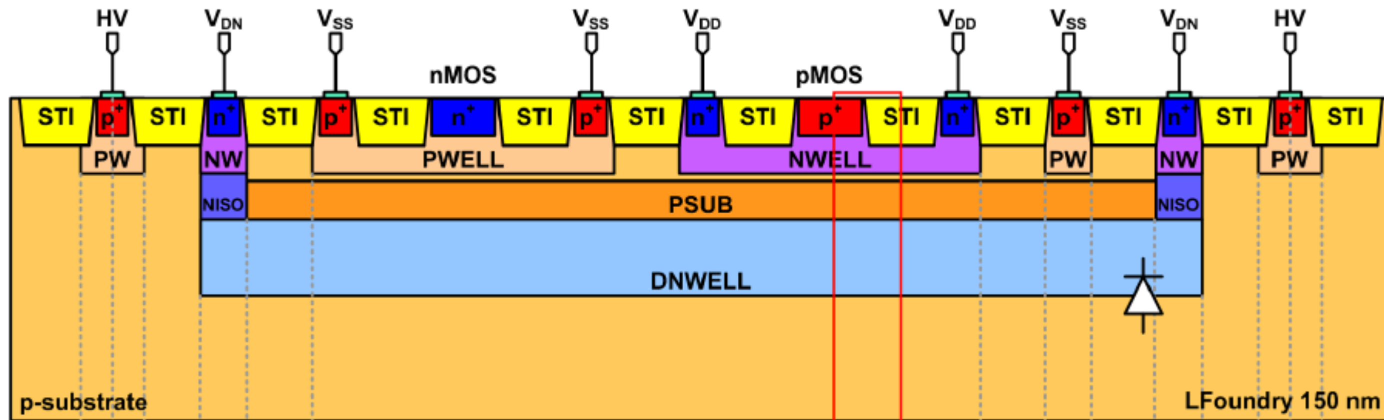
LFoundry CMOS process simulation

Starting from full process file:

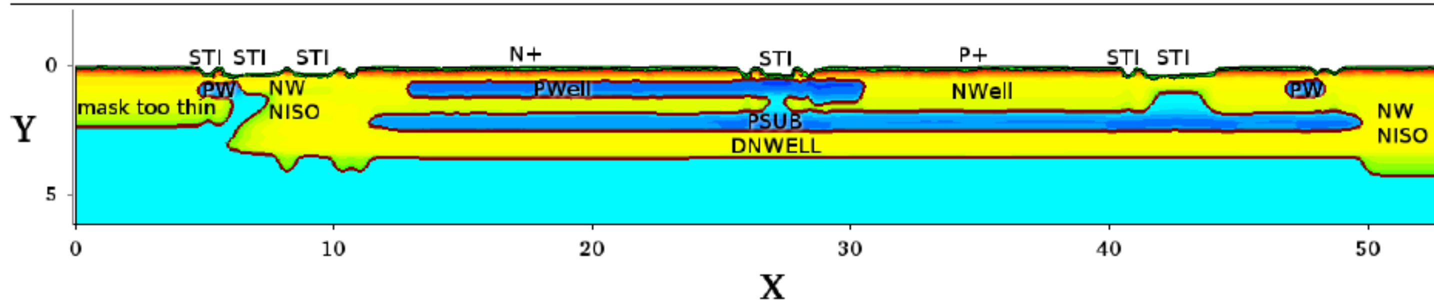
- Half transistor
- $< 1\ \mu m$ wide
- Full process:
  - > 20 masks
  - Full (!) thermal history (no multi-threading)

[Eva Vilella, University of Liverpool]

LFoundry CMOS process simulation



[Eva Vilella, University of Liverpool]



- Mesh reduction: noisy surface
- CPU time: 42 h
  real time: 34 h

- Mask too thin for DNWELL
- PSUB and PWELL shifted (coordinates calculation)
- Issues with masks for n+ and p+

LFoundry CMOS process simulation

Process simulation:

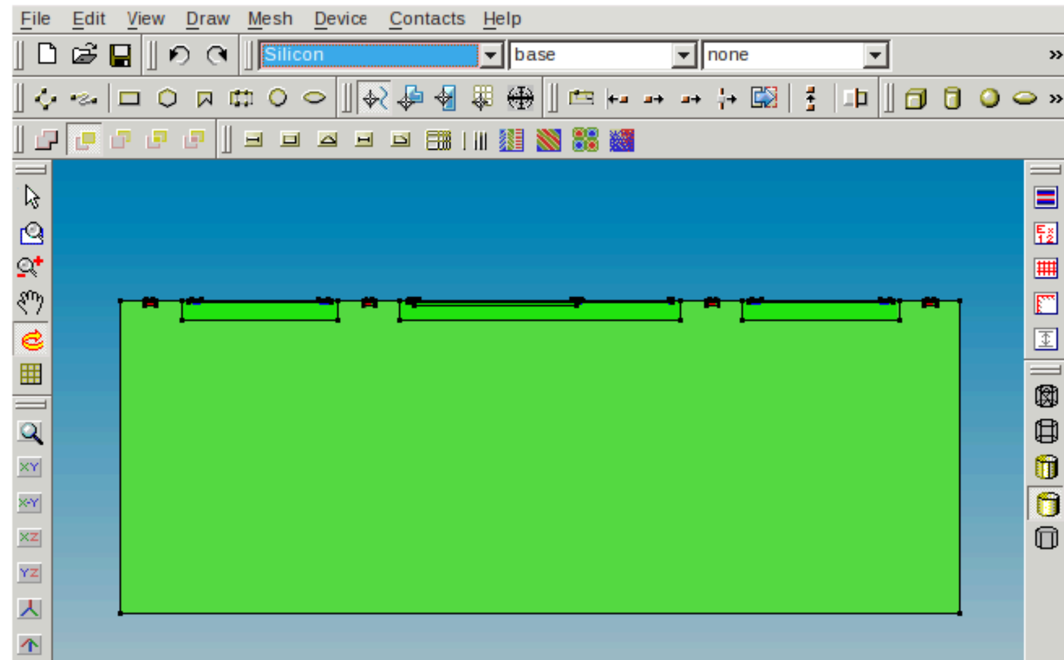
- Corrected masks for process simulation
- Restored all the thermal diffusion steps
- Finding a suitable mesh (again)
- Running on a faster PC

In parallel:

- Due to long computing time
  $\rightarrow$ moving to structure simulation
- Different interleaving features within less than 1 μm:
  - Run the half-transistor process file step by step
  - Extract doping profiles (different dopants)
  - Use effective doping concentration
  - Input doping profiles in structure editor

LFoundry CMOS process simulation

- Define (reference) regions
- Define materials
- Define doping profiles
- Abrupt, clean shape (not realistic)

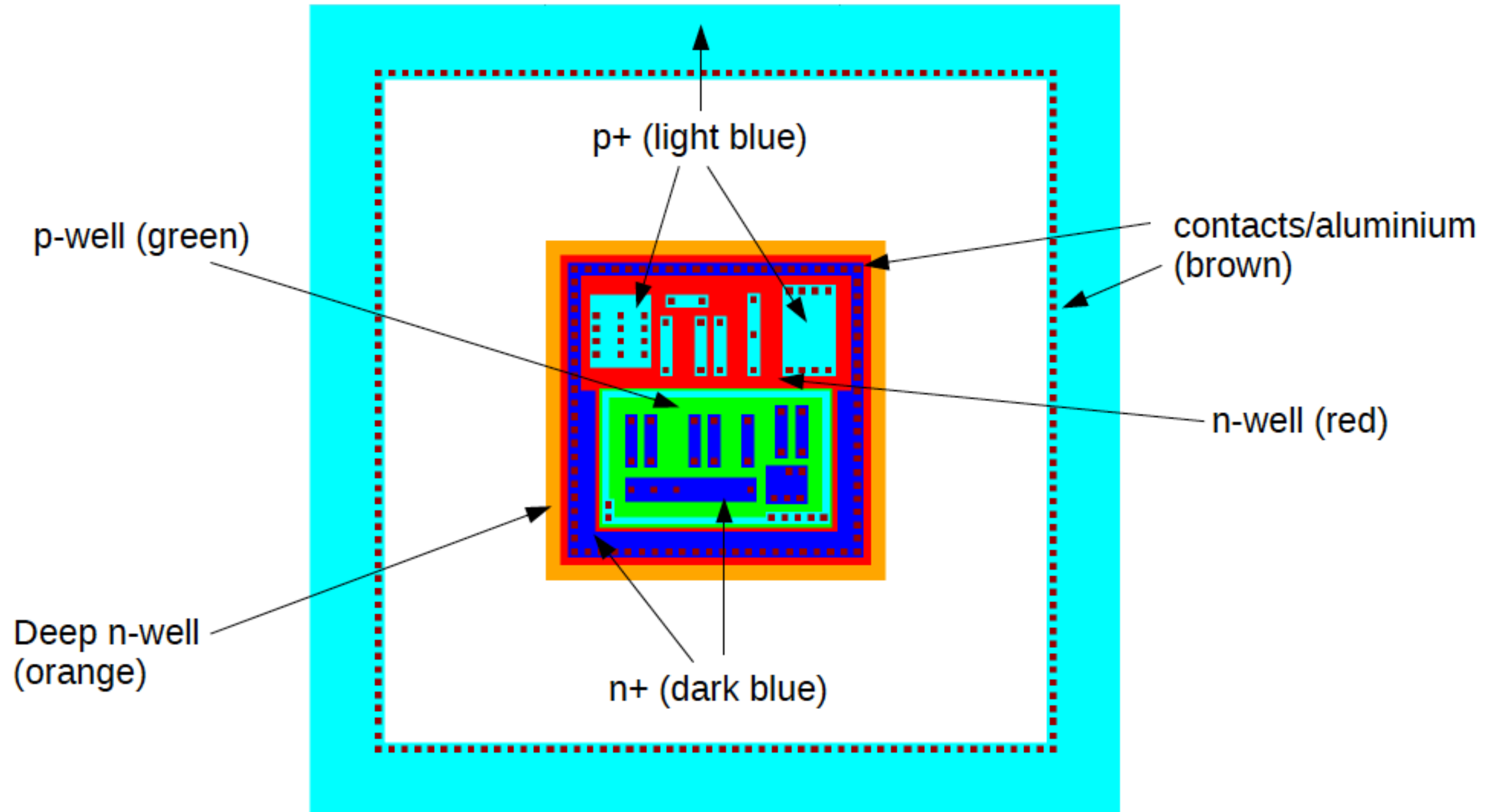


LFoundry CMOS process simulation

- Execution time of structure simulation: 7 s

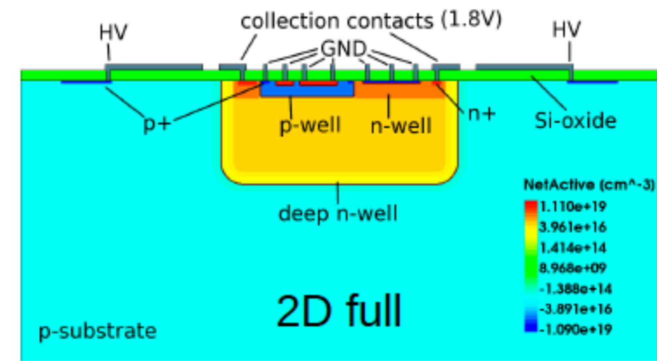
AMS CMOS process simulation

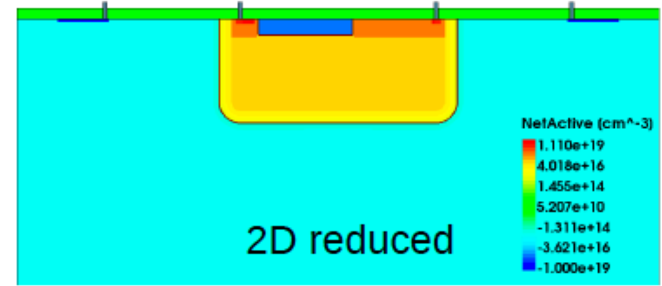
- Layers obtained from the design file (gds layout file), imported to ligament layout
- Full implant structure, no metal lines shown



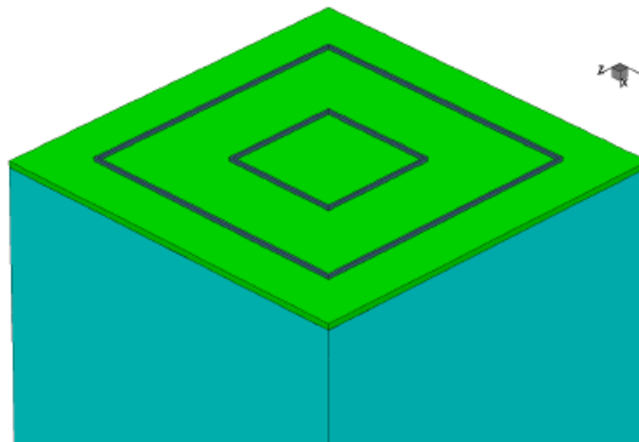
Simulated TCAD structures

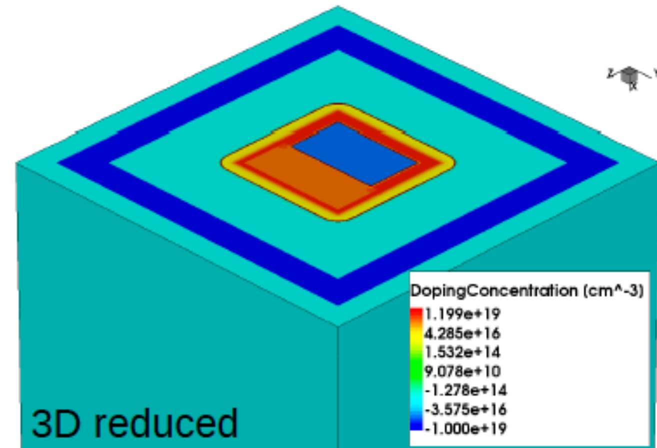
- 3 structures simulated: 2D full, 2D reduced and 3D reduced
- 2D full has all the implants and contacts
- The 2D reduced and 3D reduced structures both have the same implant structure
- 100 µm thick 31.5 µm wide, 10Ωcm
- Created in Sentaurus structure editor
- "Net active" is the doping concentration





3D reduced with oxide and aluminium





Device simulation

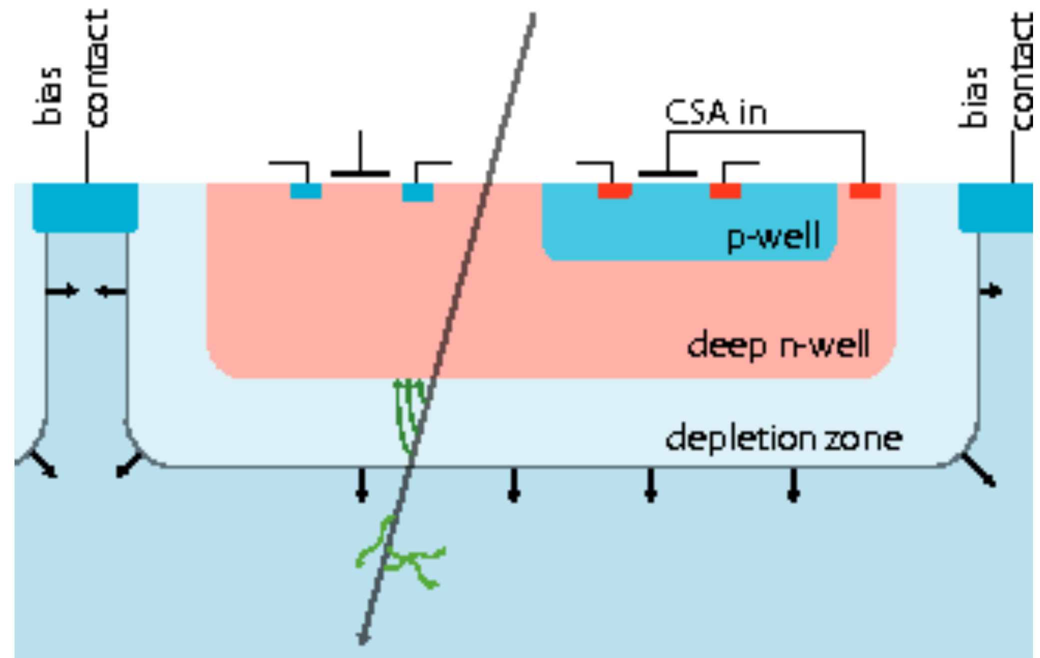
CMOS Pixel sensors

HV-CMOS process can be used for particle detection

- Large-scale production capabilities
- Electronics can be integrated in the pixels
- Bias is usually applied from the top
- Typically low-resistivity substrate but high-resistivity is possible

This pose new challenge in terms of TCAD simulation

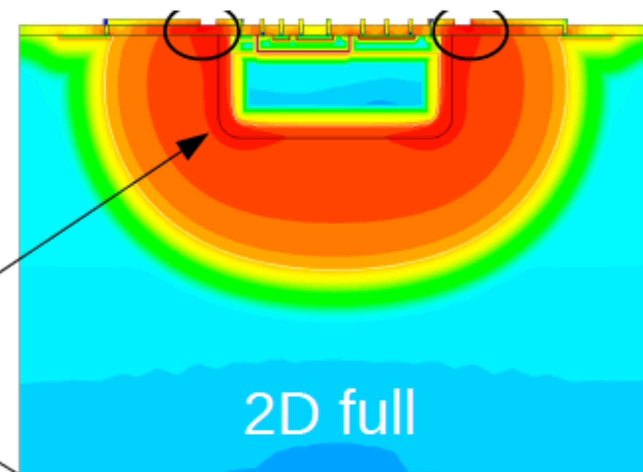
- More complex geometry
- Possibility to optimize important parameters such a capacitance and signal speed

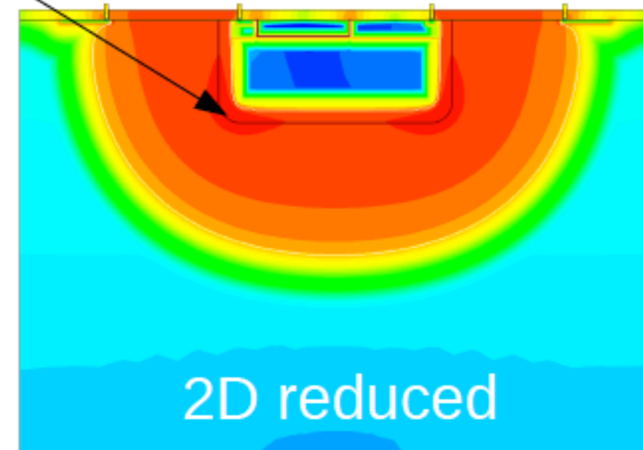


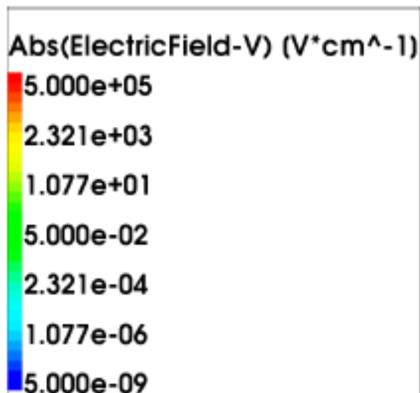
AMS H18 sensors

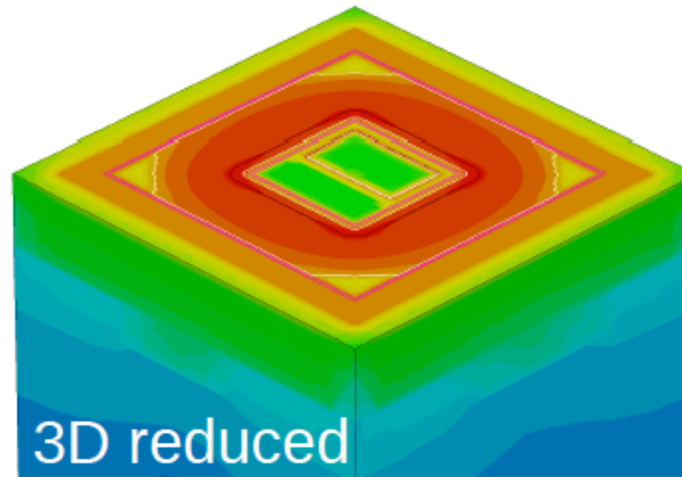
E-field comparison

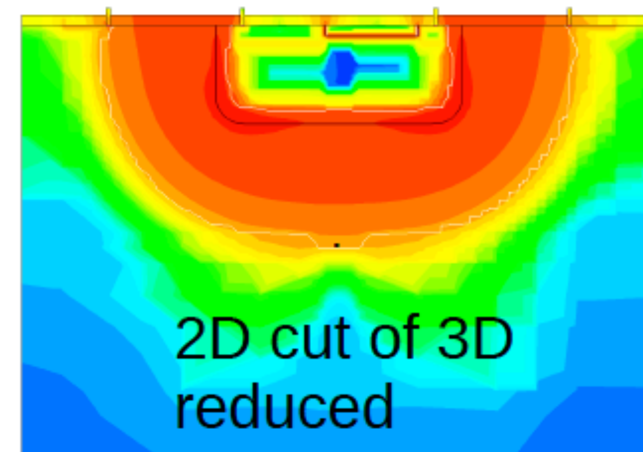
- Biased to -60V, operating voltage of device
- All electric fields are roughly the same:
  - higher value at edges of the deep n-well
  - Lower value in deep n-well and outside depletion
- One difference: 2D full model has a higher electric field value in the oxide because of the metal layer





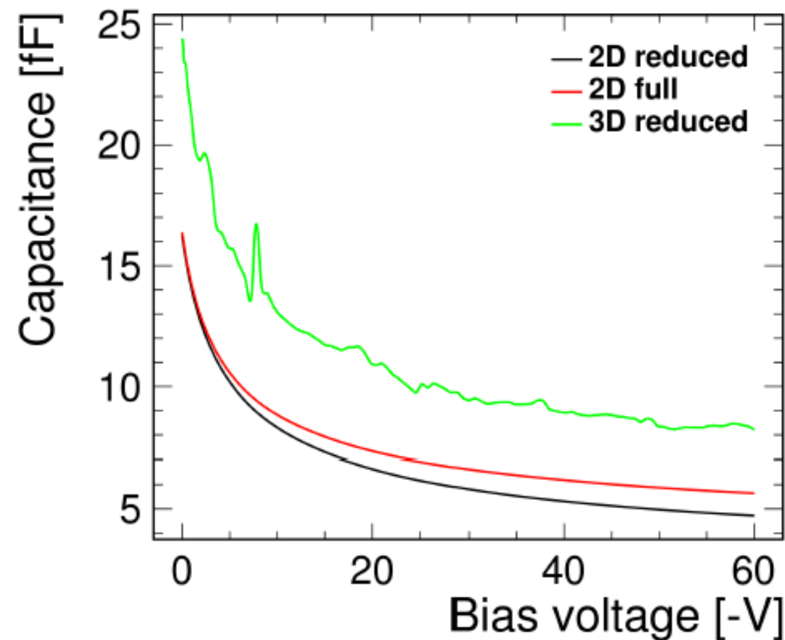






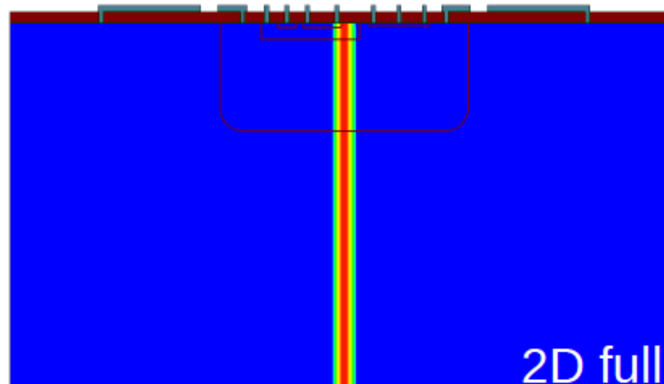
Capacitance comparison

- Deep n-well to bulk
- Test bench calculation: ~10 fF (I. Peric)
- Simulations are consistent with the calculation
- 2D simulation results are given in F/µm, then multiplied by deep n-well length hence only estimates



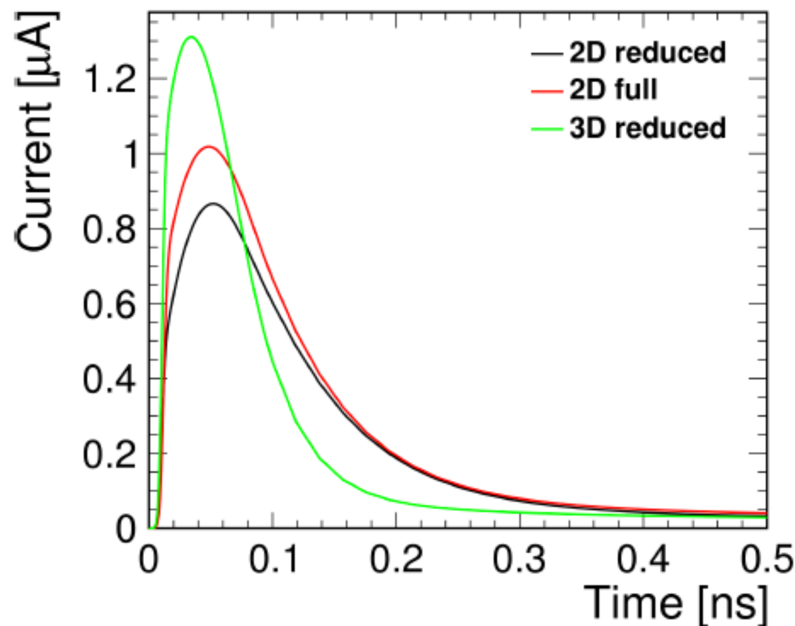
MIP simulation

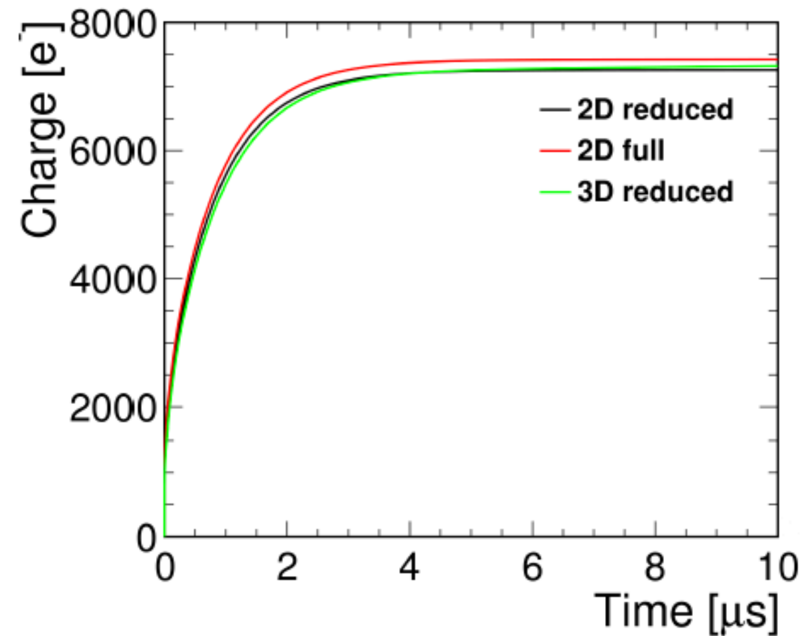
- In TCAD specify time, direction, position and charge deposition of the particle
- The MIP passes the centre of all three structures
- MIP enters at 10ps
- Gaussian in time (sigma of 2ps) and in width (sigma of 0.035μm)
- Deposits 80 electron-hole pairs per micron, no landau fluctuations
- Transient simulation from 0-10μs is performed at bias voltage -60V
- Thickness of 100μm to save memory



MIP signal

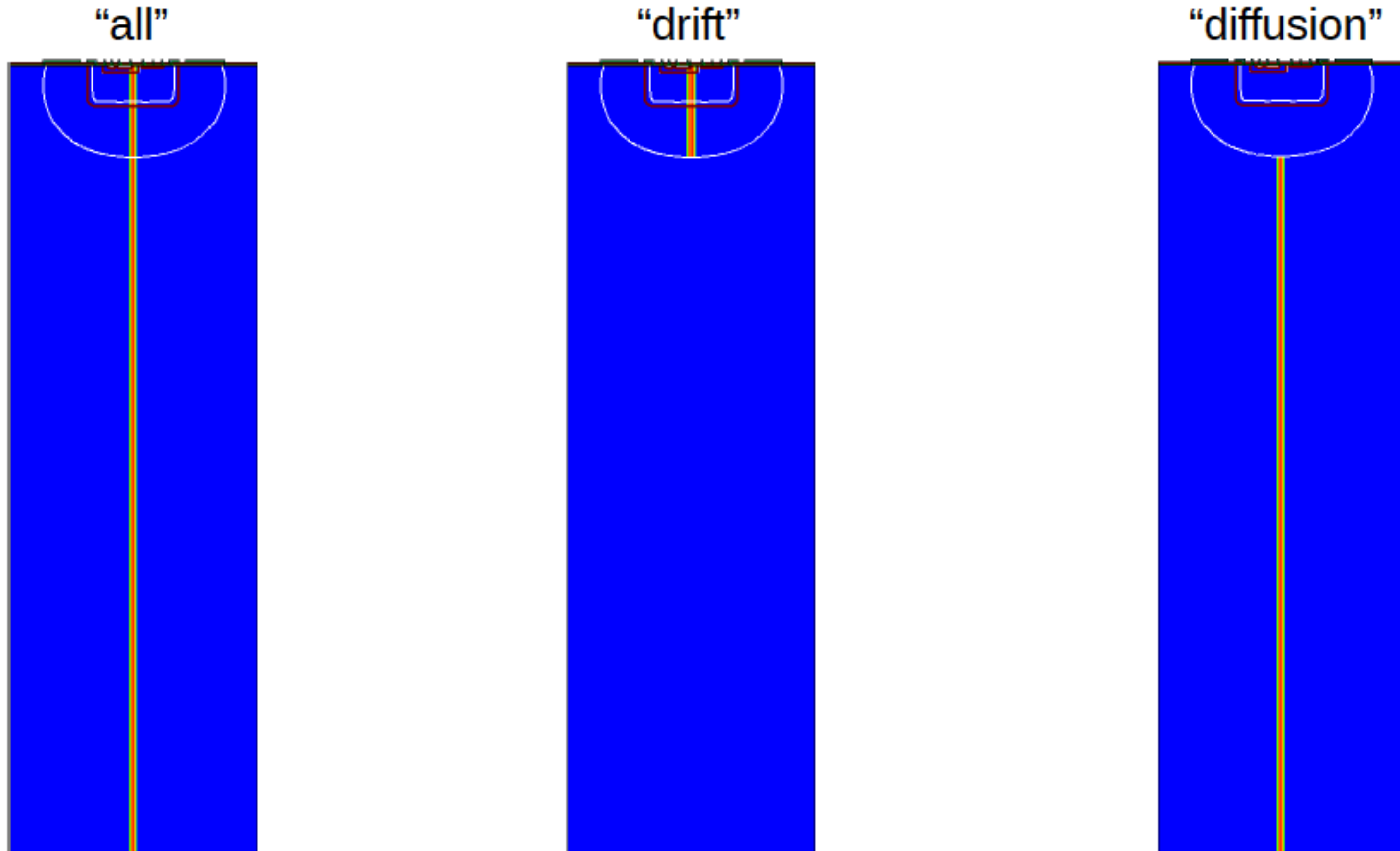
- Signal seen at the collection contact
- 3D reduced model has the largest peak but quickly drops to the lowest value
- The 2D full model has larger current value than the 2D reduced model
- After 10μs difference in charge is around 200e⁻, around 3%





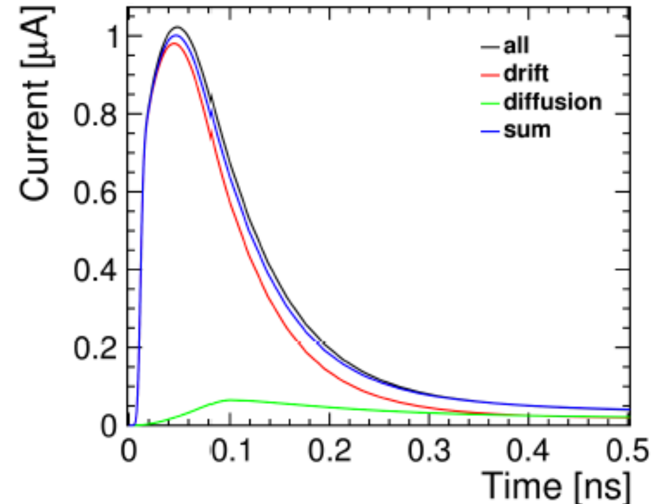
MIP signal separation

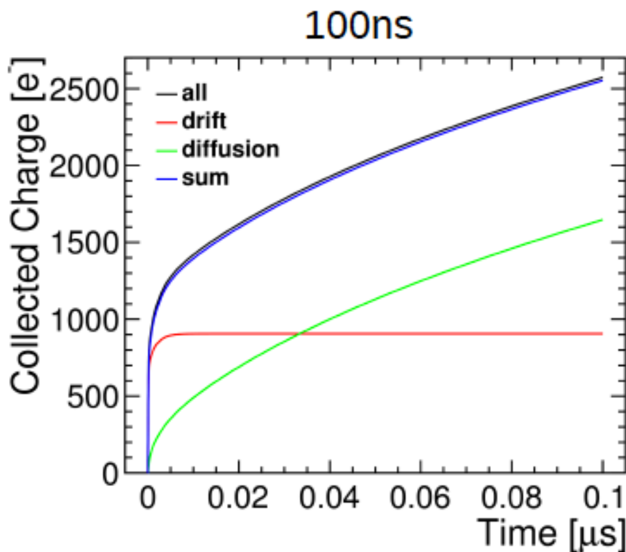
- Split the MIP path in two: “drift” and “diffusion”

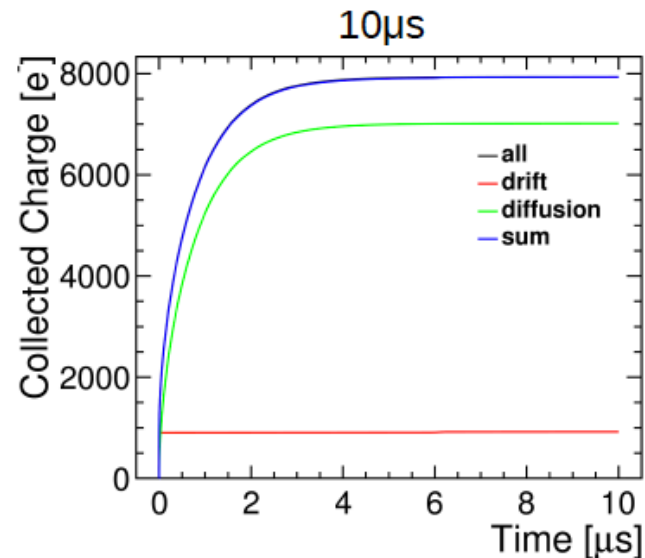


MIP signal separation

- "Drift" pulse height and peak time similar to "all"
- Difference between "all" and "sum" is around 2%
- "Drift" collects charge very fast, 700e⁻ in ≈0.3ns but is limited, plateaus at ≈10ns
- "Diffusion" becomes dominant after 35ns
- After 10μs "diffusion" contributes around 90%

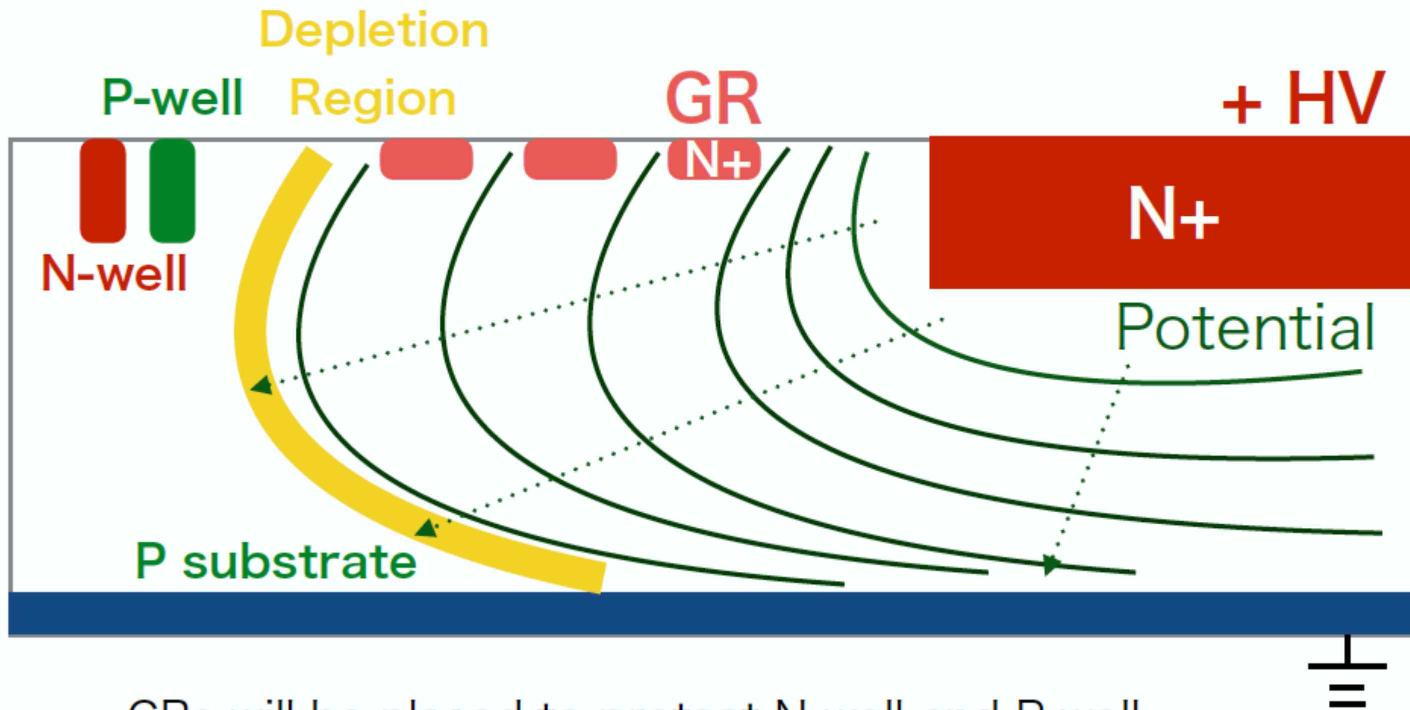






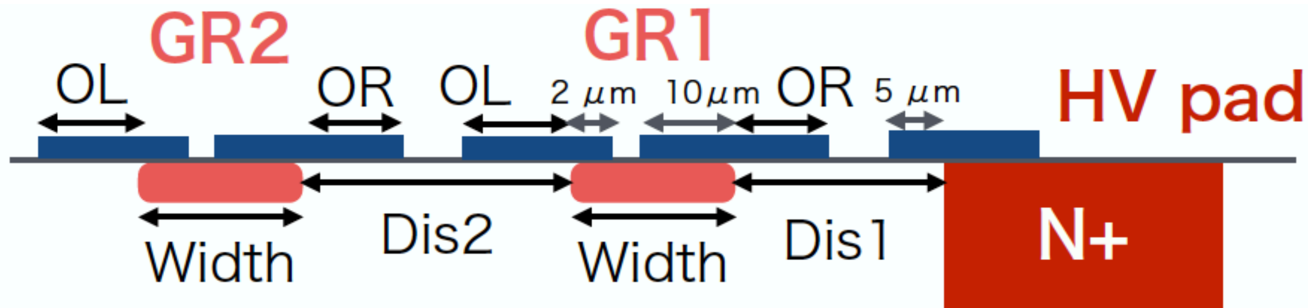
Guard ring structure simulation

Optimisation of Guard ring structures



- GRs will be placed to protect N-well and P-well
- Need optimisation of the GRs
  - Number of GRs
  - Parameters of GRs

Optimisation of Guard ring structures

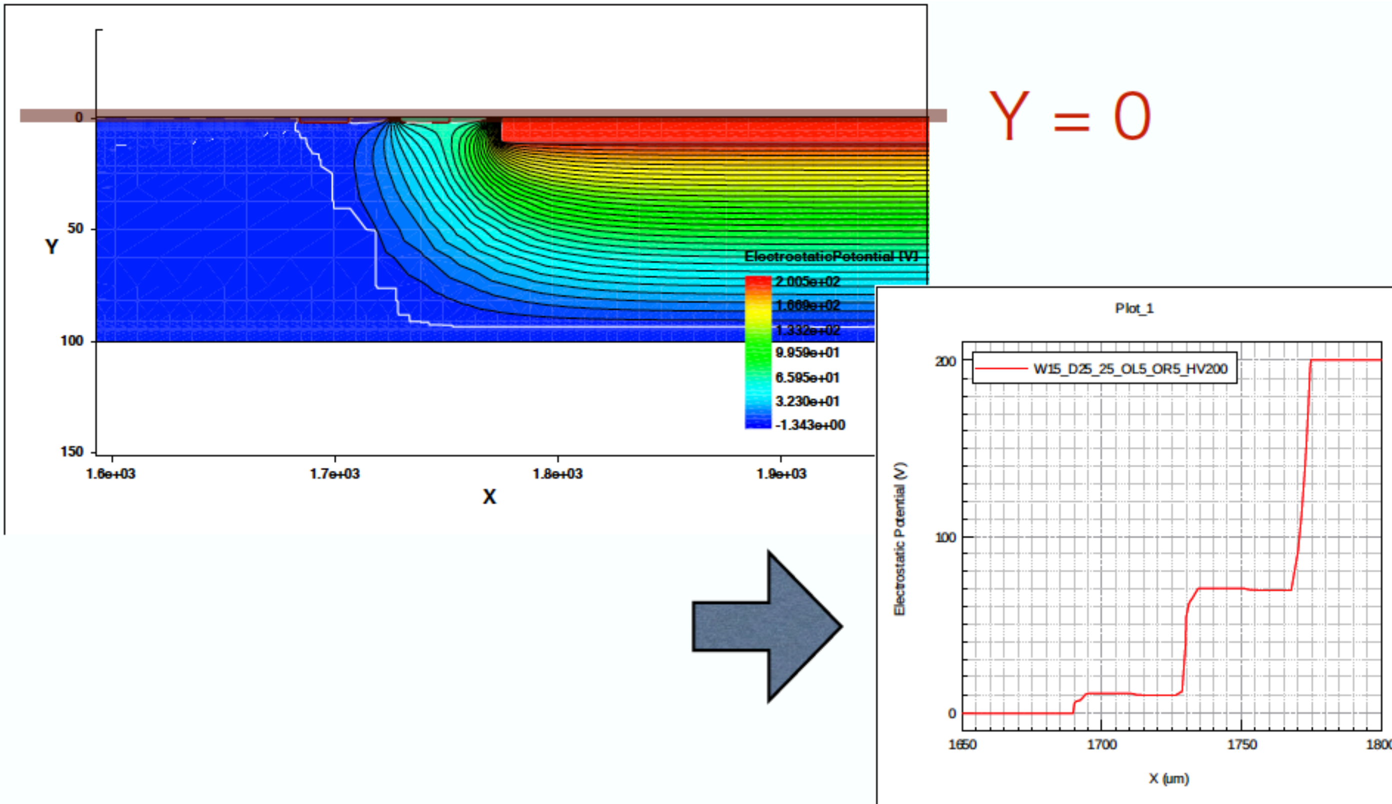


Width	Dis1	Dis2	OL	OR
15	25	25	5	5
25	35	35	15	15

[μm]

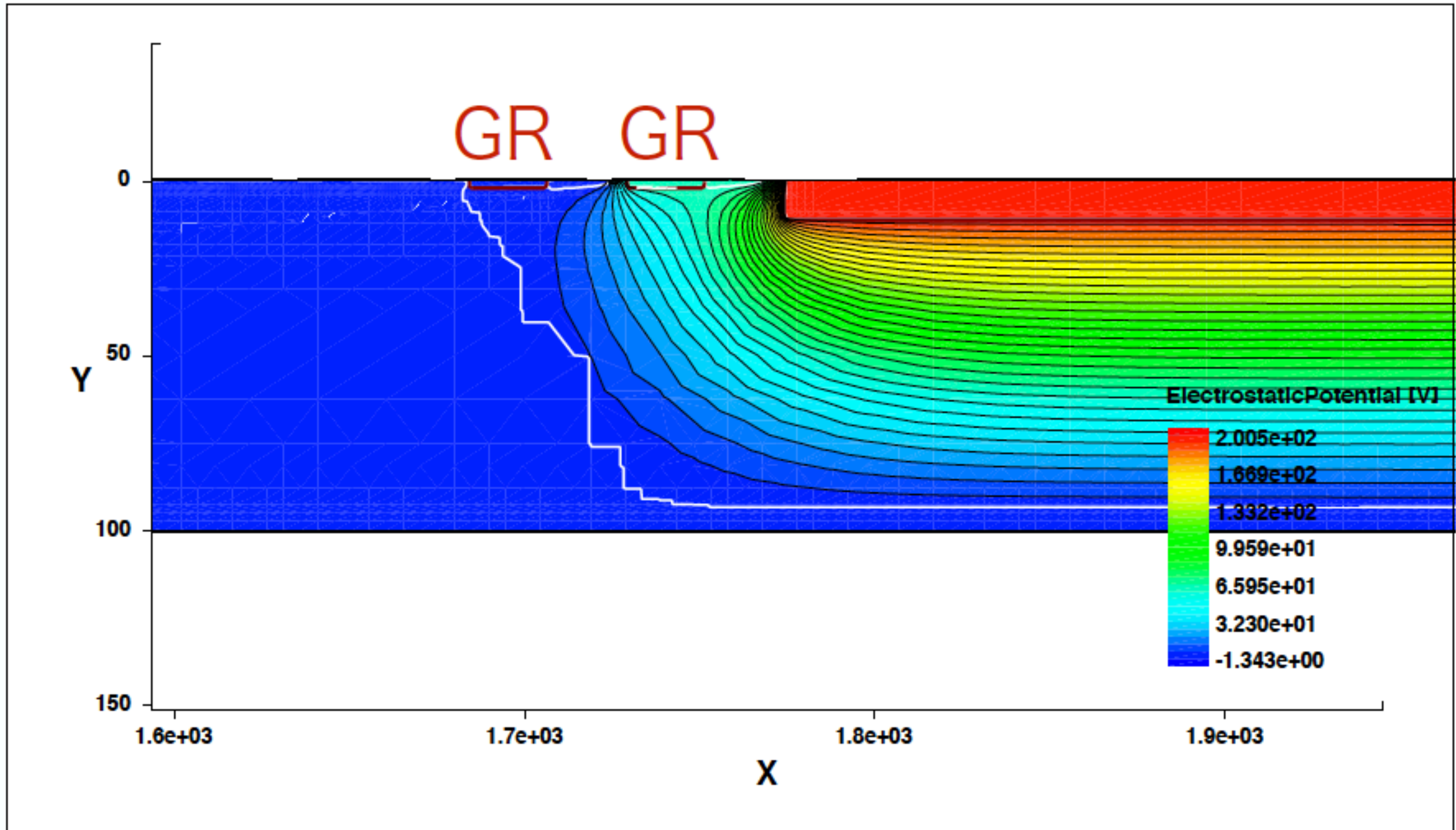
- Fixed nGRs = 2
- HV = 200 V only for 1 pad
- Chose 5 parameters (Simulated 2^5 = 32 patterns)
- Looked into electrostatic potential for each pattern

Optimisation of Guard ring structures

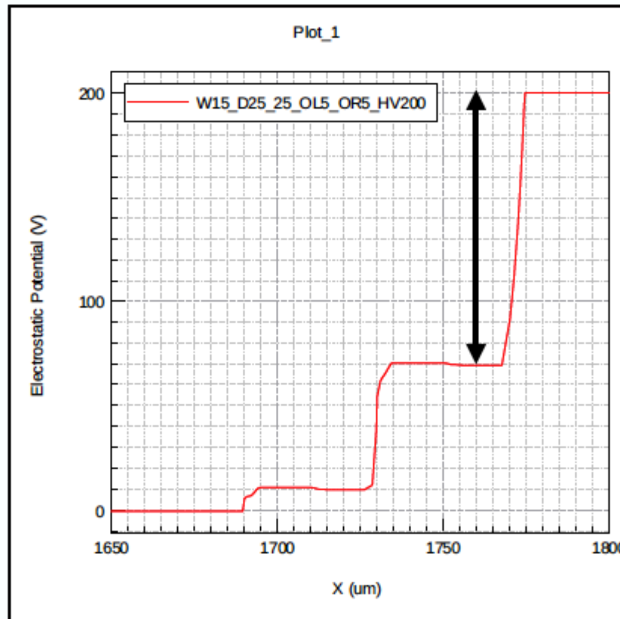


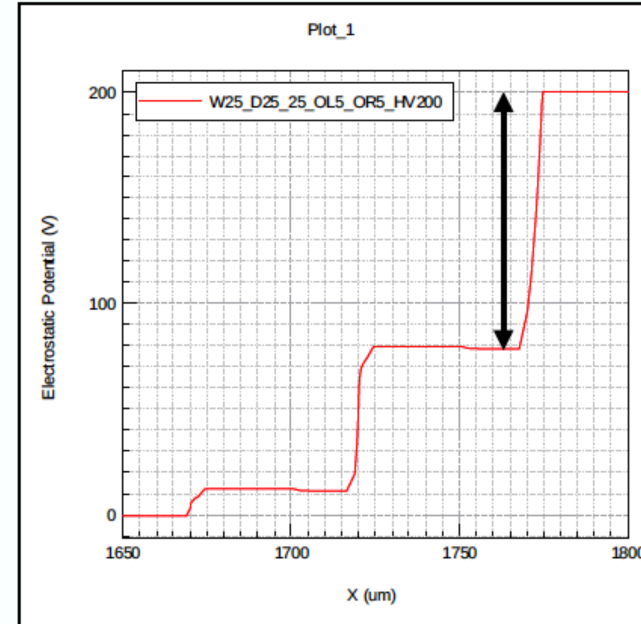
- Simulated electrostatic potential in 2D map
- Projected it to 1D (y=0) map (cutline)

Optimisation of Guard ring structures



Optimisation of Guard ring structures

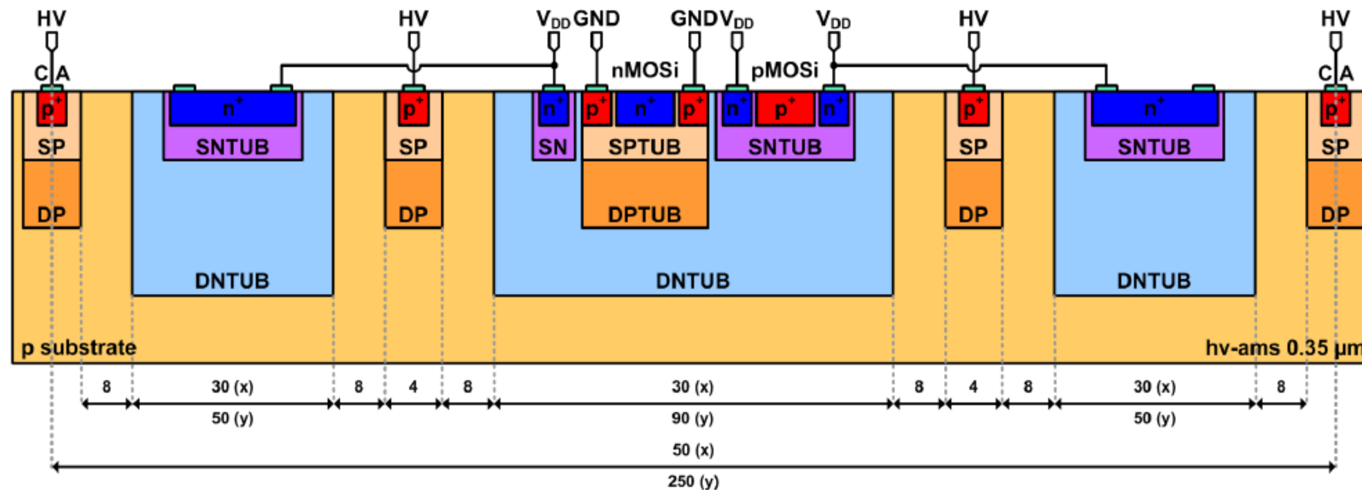




- Width: 15 μm -> EP drops 130 V
- Width: 25 μm -> EP drops 120 V

AMS H35DEMO Sensors

AMS H35 HV/HR-CMOS Pixel sensors



Eva Vilella-Figueras, https://indico.cern.ch/event/361445

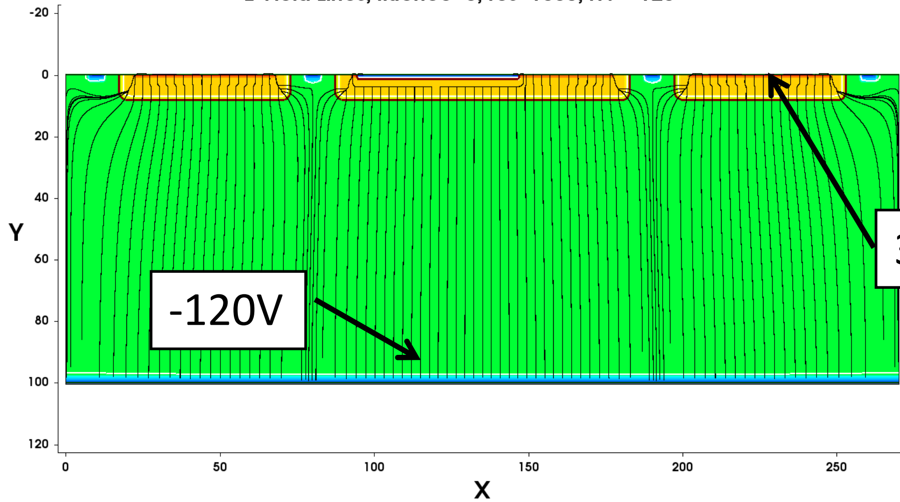
- VSS: 0.0 V
- VDD: 3.3 V
- HV: 0 – -200 V
- Resistivity: 20, 80, 200, 1000 Ωcm
- Top bias without back process
- Back bias with floating top contacts

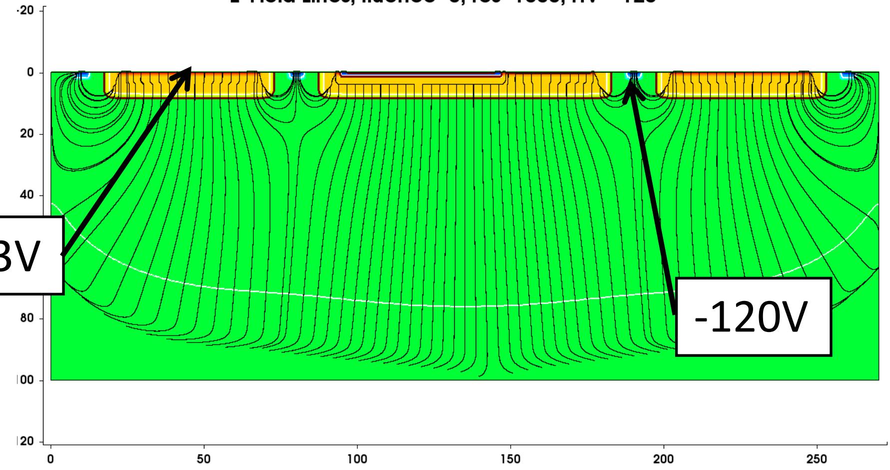
Extra deep p-well

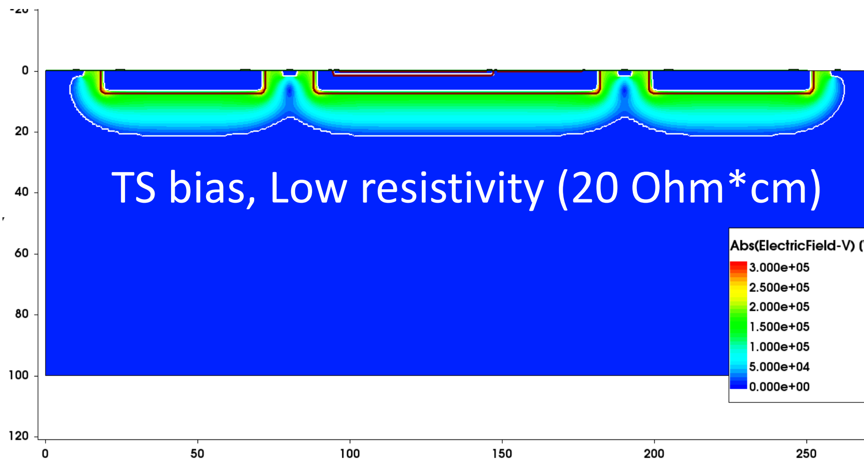
(M. Benoit in comm. with AMS)

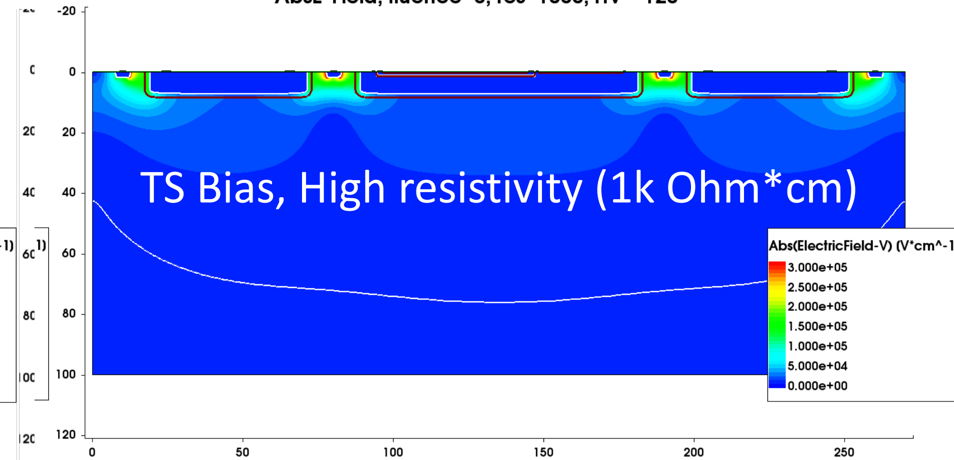
- Inverting DNTUB mask
- Same doping concentration as DNTUB

Back-side versus top biasing

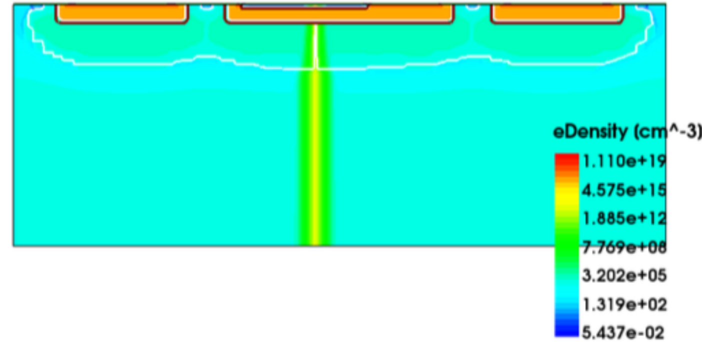


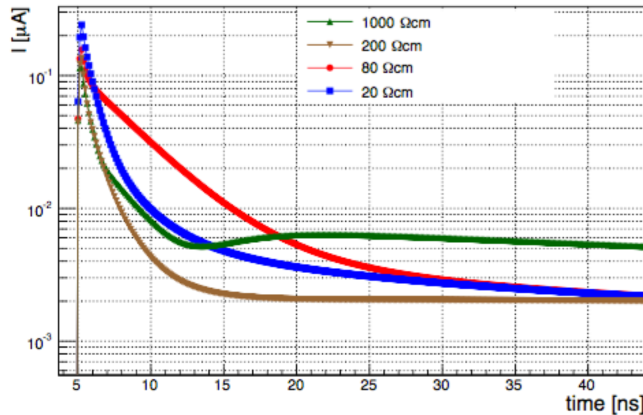


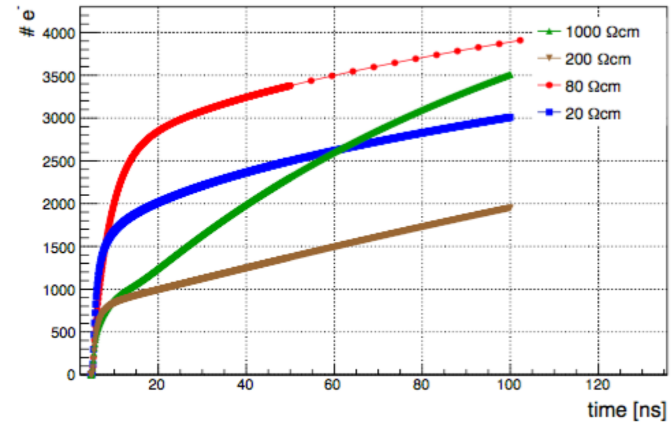




Effect of Top and backside biasing

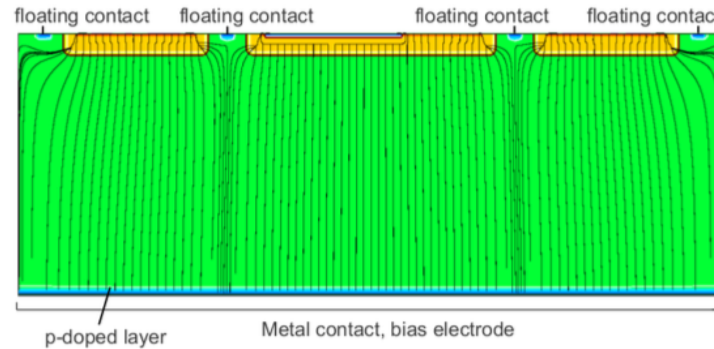


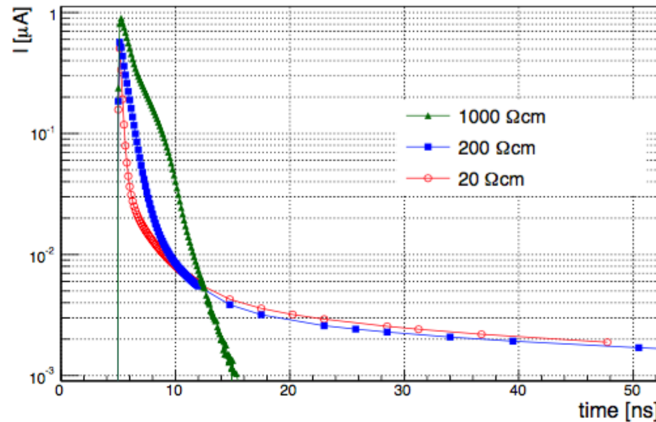


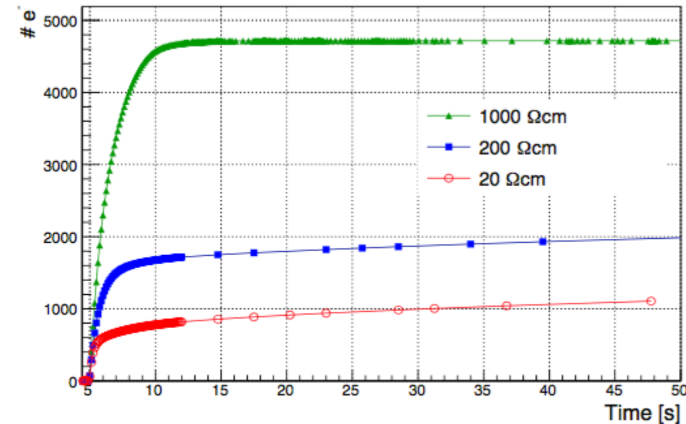


Non standard results → low resistivities better performance

Effect of Top and backside biasing



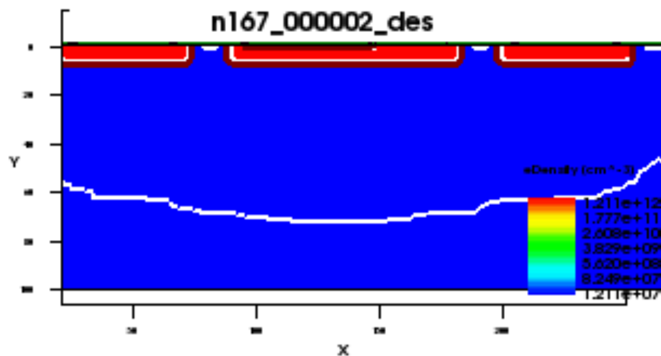




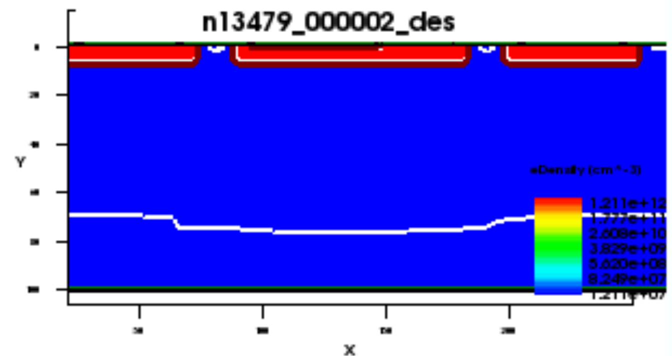
Standard results → high resistivities better performance

Effect of Top and backside biasing

Top-Bias

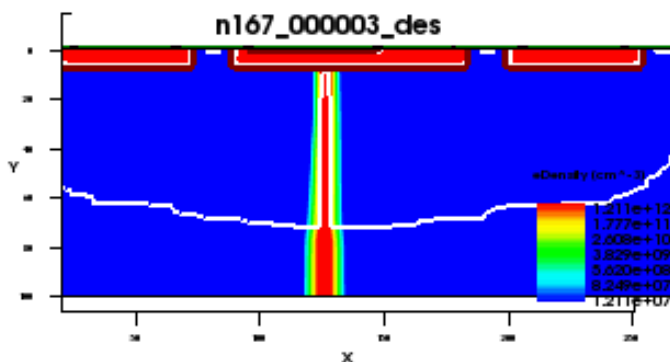


Back-Bias

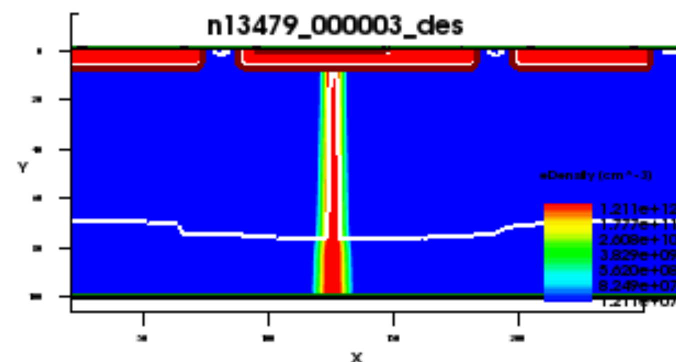


Effect of Top and backside biasing

Top-Bias



Back-Bias



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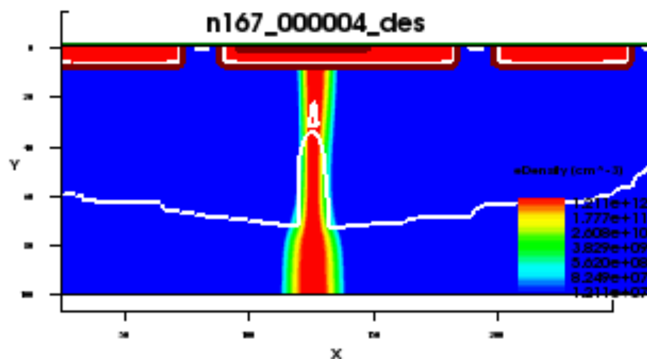
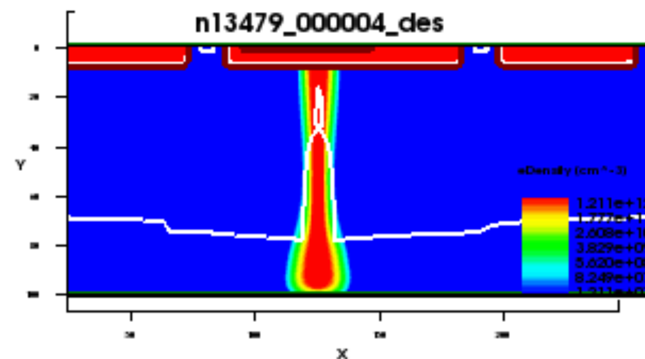


Back-Bias



Effect of Top and backside biasing

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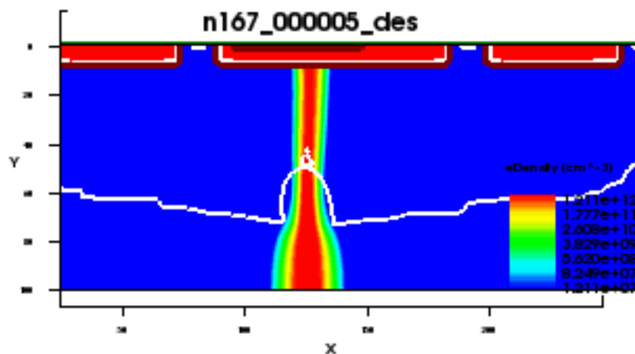
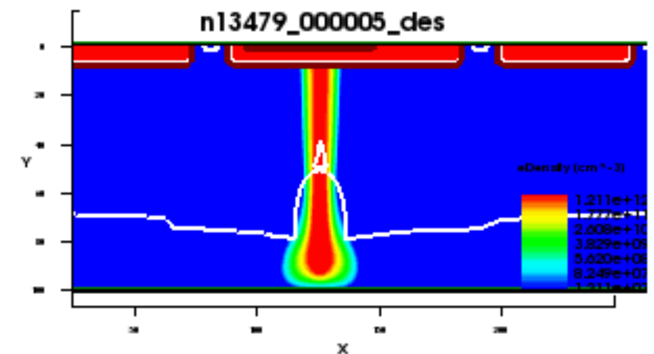
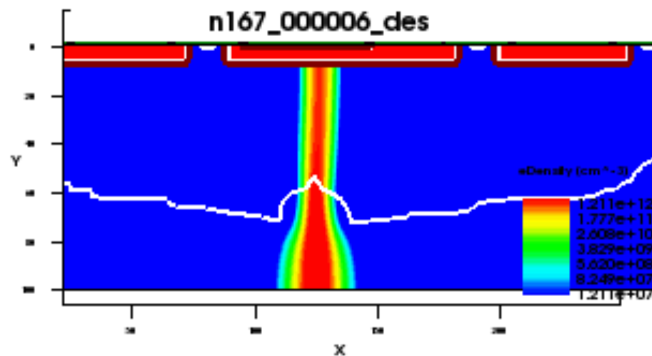


Back-Bias

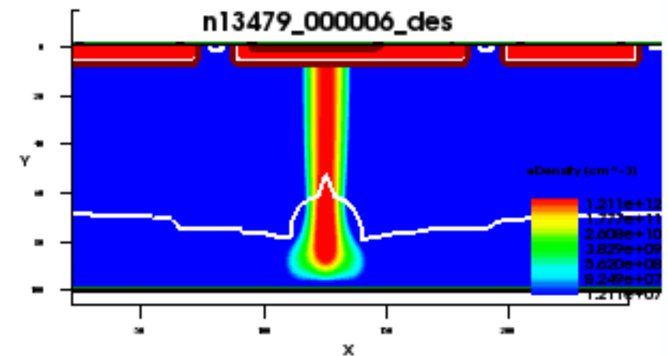


Effect of Top and backside biasing

Top-Bias

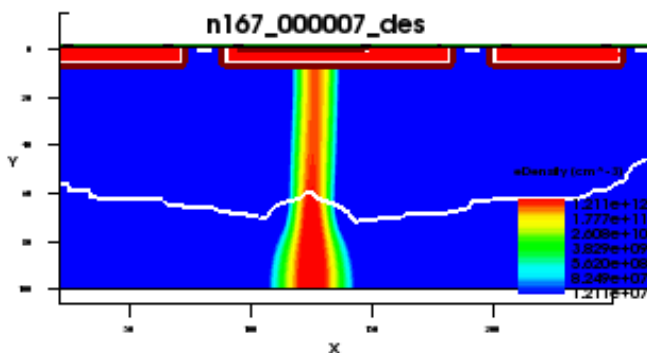


Back-Bias

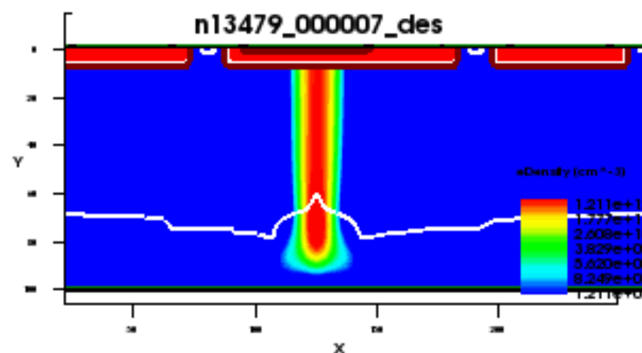


Effect of Top and backside biasing

Top-Bias

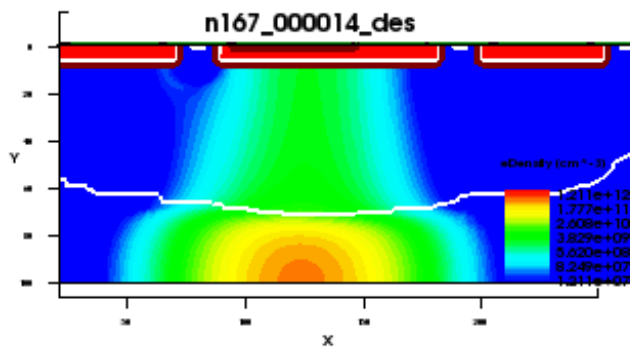


Back-Bias

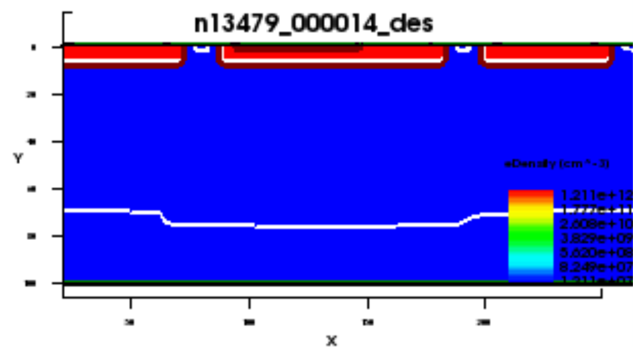


Effect of Top and backside biasing

Top-Bias



Back-Bias



Conclusion

- Synopsys Sentaurus offer a complete TCAD suite that allow for :
  - Full process simulation when available
  - Approximation of structure using device editors

- TCAD Simulation is suitable to obtain information on structure before sumbission
  - Guard ring structure optimisation
  - Effect of radiation damage
  - Response to particle stimulus
  - Capacitance extraction
  - Layout optimisation

- **Please assist to the hands-on session to learn about :**
  - **Process and device simulation**
  - **The Sentaurus workbench workflow**
  - **Extracting and interpreting results of TCAD simulation**

Link for tutorial

- GR Simulation example
  - https://gitlab.cern.ch/dhayakaw/TCAD_test_160620
- Simple pixel projects
  - https:
- AMS Pixel example