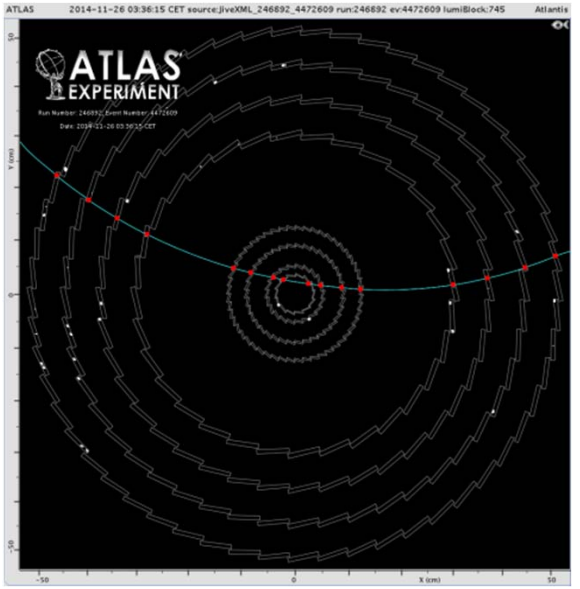
Journées VLSI 2016

Configuration Column Chip (C3) en 65nm TSMC



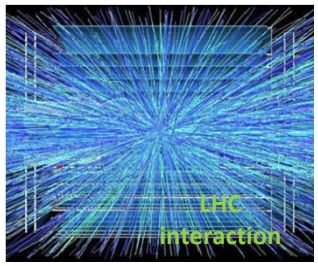
(et activités **pixels** au LAL)

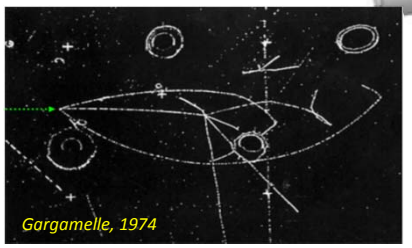
Maurice Cohen-Solal, Mowafak EL Berni,
Olivier Lemaire, Philippe Vallerand

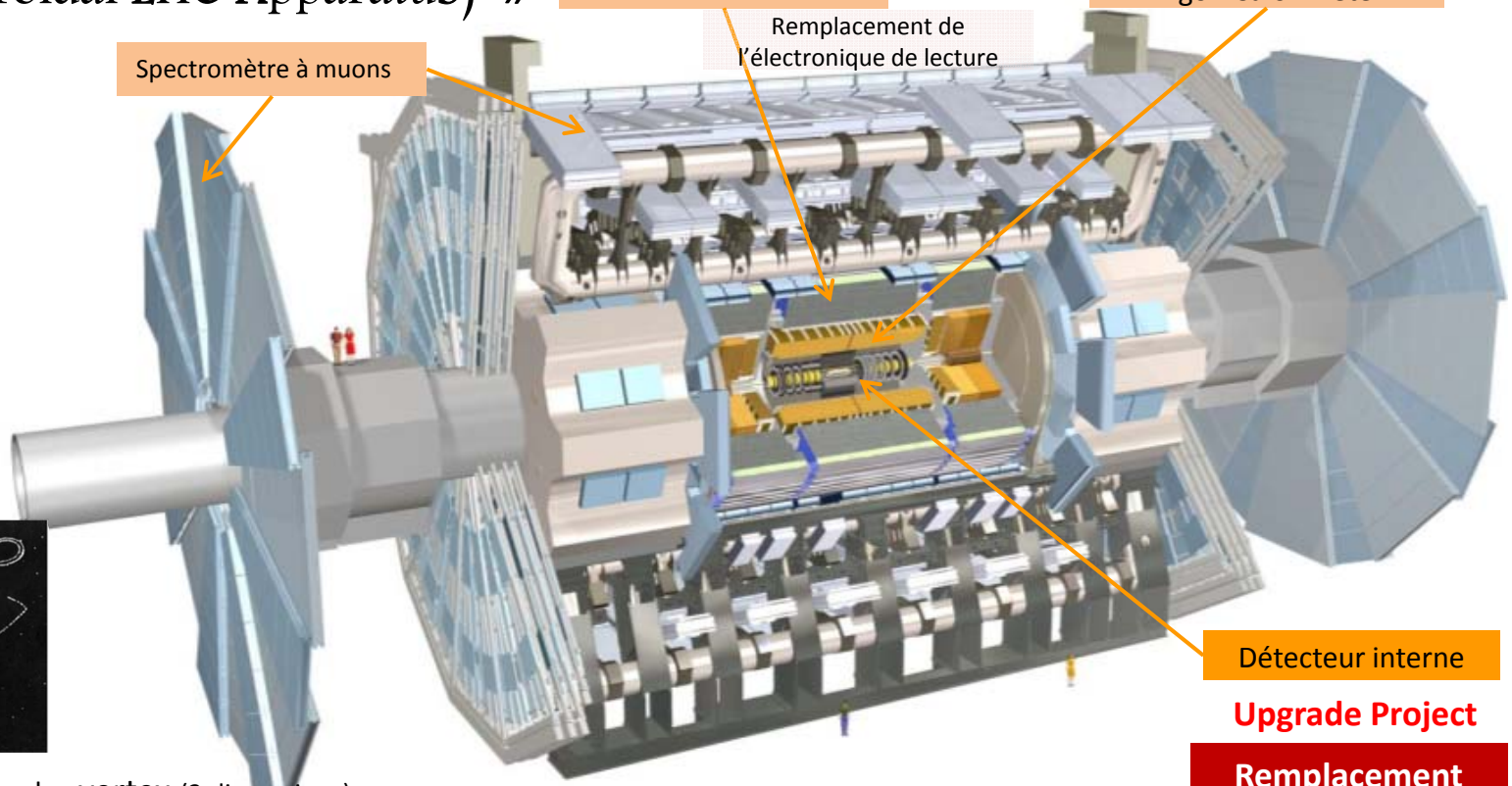
LAL – Orsay Université Paris-Saclay

« **ATLAS** (A Toroidal LHC ApparatuS) »

Contexte





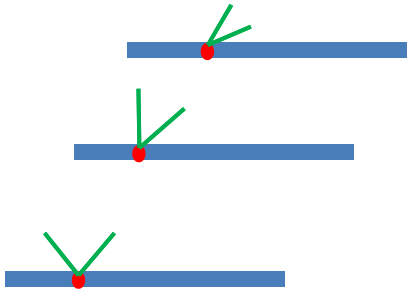


Upgrade Project

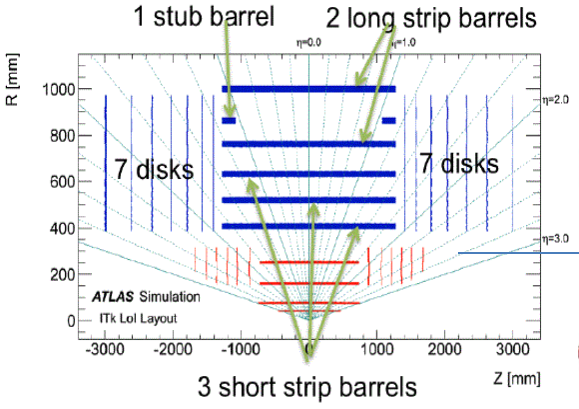
Remplacement intégral

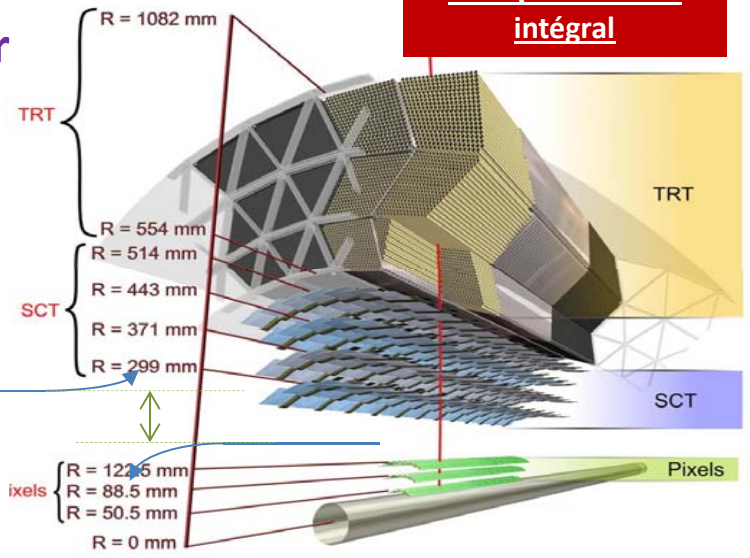
- Localiser les vertex (3 dimensions)
- Haute résolution en r.φ (50µm)
- Paramètres d'impact (15 µm)

détecteur de positions → tracking



Tracker

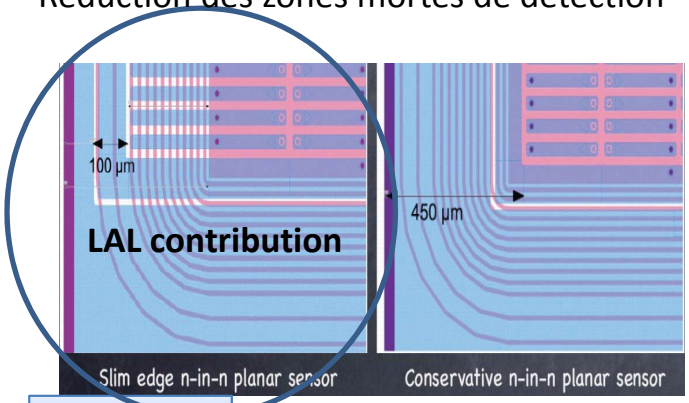




Sensor ∝ irradiation

Anneau de garde

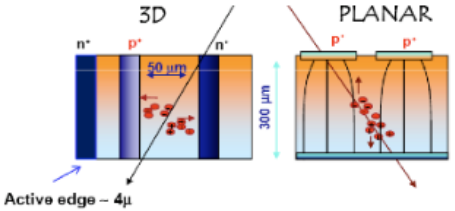
Reduction des zones mortes de détection



Final design

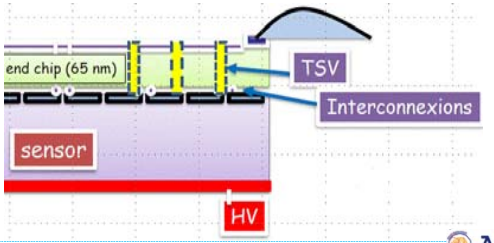
VTT Edgless pixel matrix

(R&D ligne de champs)



(R&D amplification)

«LGAD » (RD50)

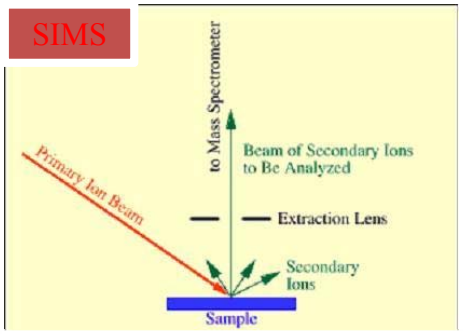


AIDA 2020

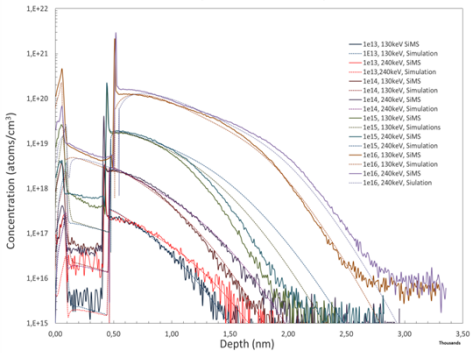
Instead of wire or bump bonding,
TSV could be considered in chip periphery for improved the time transit.
(Collaboration with the LETI-Grenoble)

Profiles de dopages

SIMS



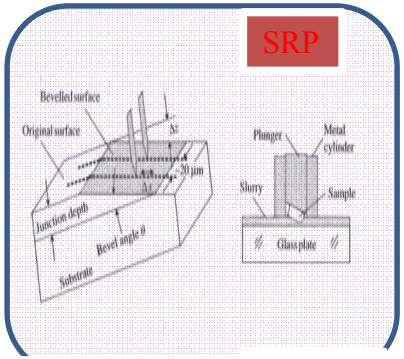
ADVACAM 2Ωhm*cm, 100nm Screen Oxide, Non-etched

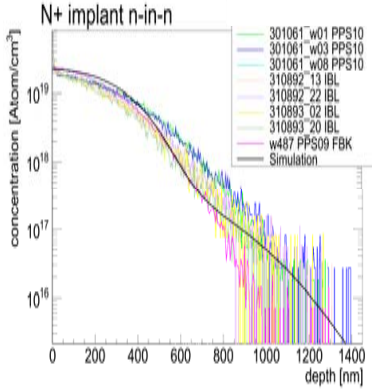


Secondary **I**on **M**ass **S**pectrometry

(concentration de dopants vs profondeur)

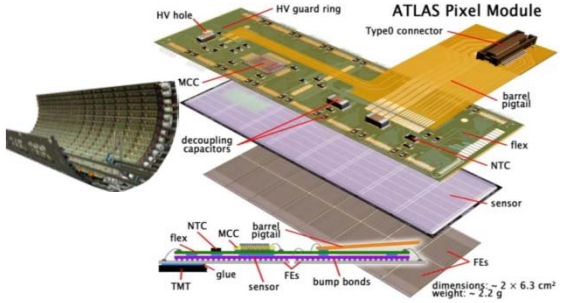
SRP





Spreading **R**esistance **P**rofiling

(concentration de porteurs vs profondeur)



Caractérisation au LAL

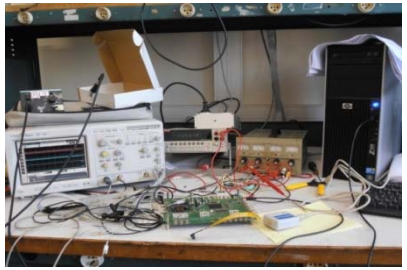
3 dimensions

Omégapix2

(130nm)

Pitch : 35 µm x 200 µm

96 x 24 = **2304 pixels**



2D — Digital tier

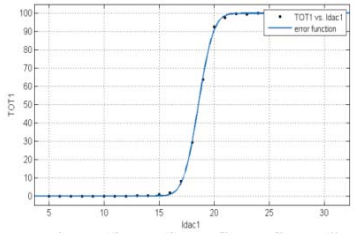
3D — Analogue tier / Digital tier — **TSV** Tezzaron process

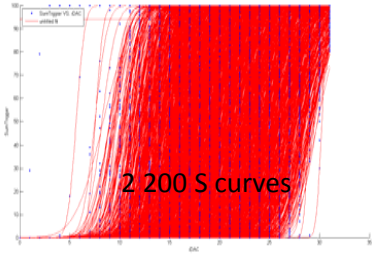
Global Foundries

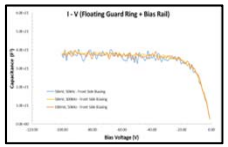
Full — Sensor / Analogue tier / Digital tier

VTT

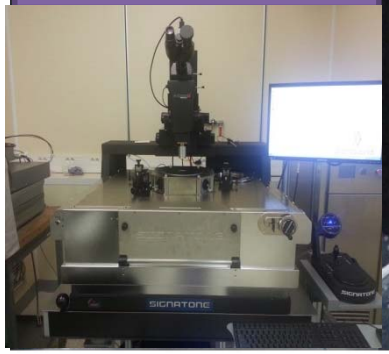
Leti connexion





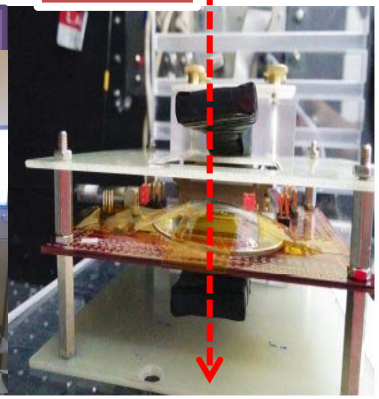


SEMI AUTOMATIC PROBE STATION



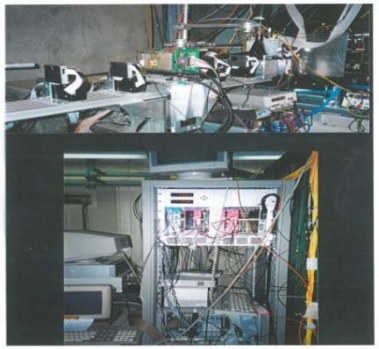
Si Pixel cosmic bench

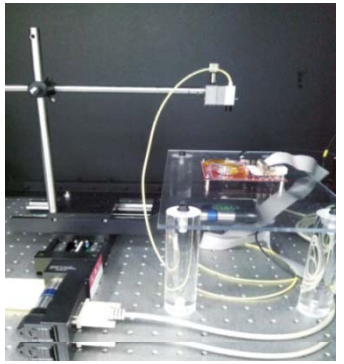
Source



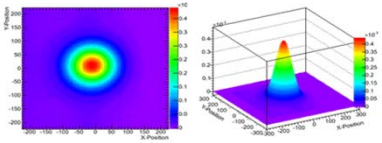
Measurement
from -60 °C to 300 °C

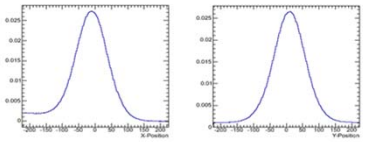
BEAM TELESCOPE





Laser Testing Station



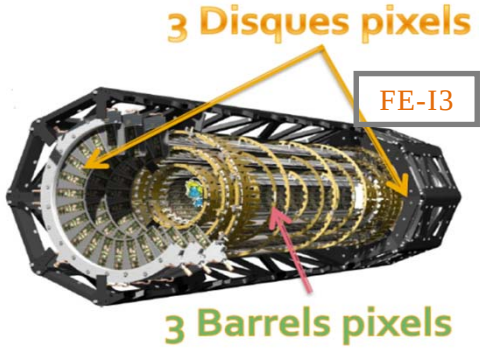


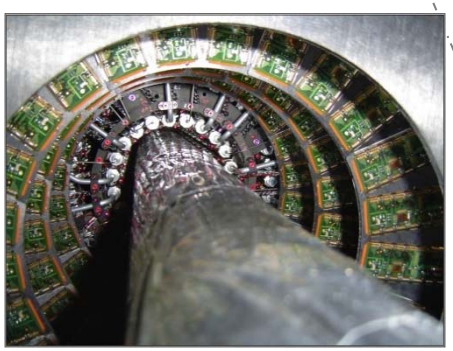
Beam Shape

Nouveau système d'acquisition

Carte SPEC + M-LIB + Front End

LHC-HL« Upgrad» (2025)





Present beam pipe & B-Layer

FE-I4

5 (**7**?) couches de pixels ~ 180 m pixel

(début production 2022) :

Array : = 134,400 pixels

pitch : 50µm x 50µm

Puce ~ 20 mm x 20 mm (~10^9 transistors)

400 colonnes x 400 lignes

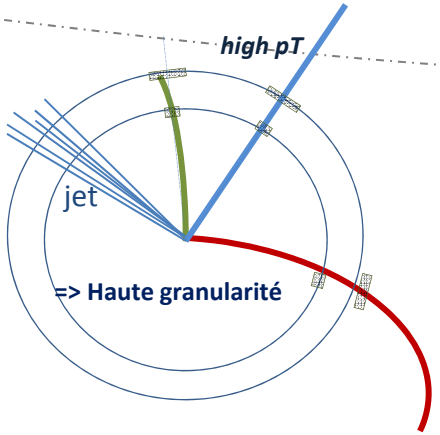
Hit ~ 2(3) **GHz / cm²**

3 Gb /s /chip (actuellement 10 fois moins)

1 Watt / cm²

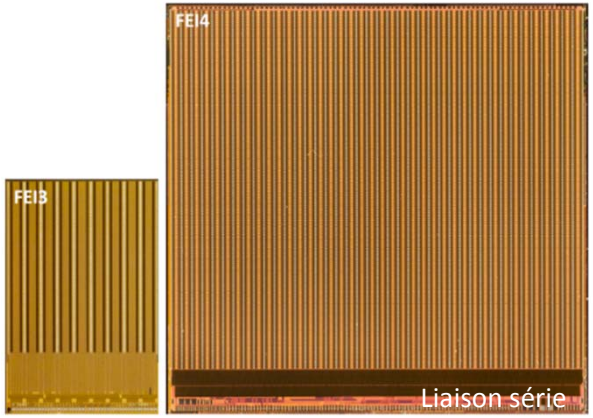
L1 Latence ~ 10.5 µs (actuellement 3µs)

Trigger: 1MHz



Fréquence collision 40 MHz ≡ **25 ns**

5 ATLAS pixel institutes



FEI4 compared to its predecessor FEI3

	FEI4B	FEI3
Year	2011	2003
Technology	130nm	250nm
Chip size	20x19mm²	7.6x10.8mm²
Active area	89%	74%
Array	80x336 (26'880)	18x160 (2'880)
Pixel size	50x250µm²	50x400µm²
Number of transistors	87M	3.5M
Data rate	320 Mb/s	40Mb/s
Wafer yield	60%	80%

Luminosité 7x LHC = HL-LHC = $7.10^{34}cm^{-2}s^{-1}$

10^{11} protons par paquet

~ **190 événements** (interactions) par Beam Cross

(actuellement 24)

Radiation 10MGy = 1 GRad (actuellement 200MRad)

10^{16} neq/cm2

RD 53 Collaboration :

Development of pixel readout integrated circuits for extreme rate and radiation

⇨ Design the next generation of pixel readout chip

for futur HEP experiment (ATLAS & CMS phase 2, …)

Challenges : smaller pixel size (density), higher hit rates, radiation tolerence, faster readout.

Low power consumption

Analogue & digital

65 nm technology

4meters

~ 700MRad

Long term availability

Access by the community

Proposal **accepté** sept.14

Guest (Jan 15)

Working Group

WG1 : Radiation (*Marlon Barbero*)

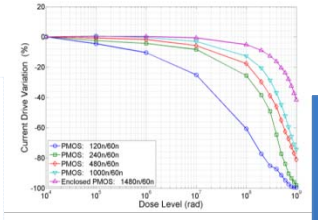
WG2 : Top Level Design (Maurice Garcia)

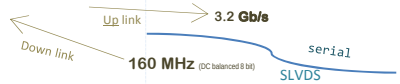
WG3 : Simulation Test Bench (Tomasz Hemperek)

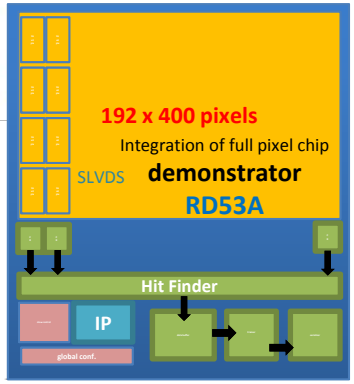
WG4 : **I/O** (Roberto Beccherle)

WG5 : Analog Design (Valerio Re)

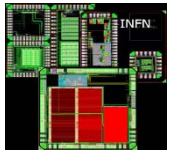
WG6 : IP Blocks (Jorgen Christiansen)

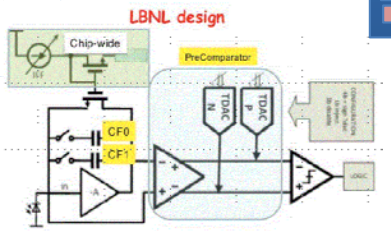


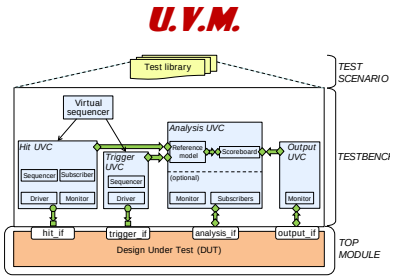




fin 2016





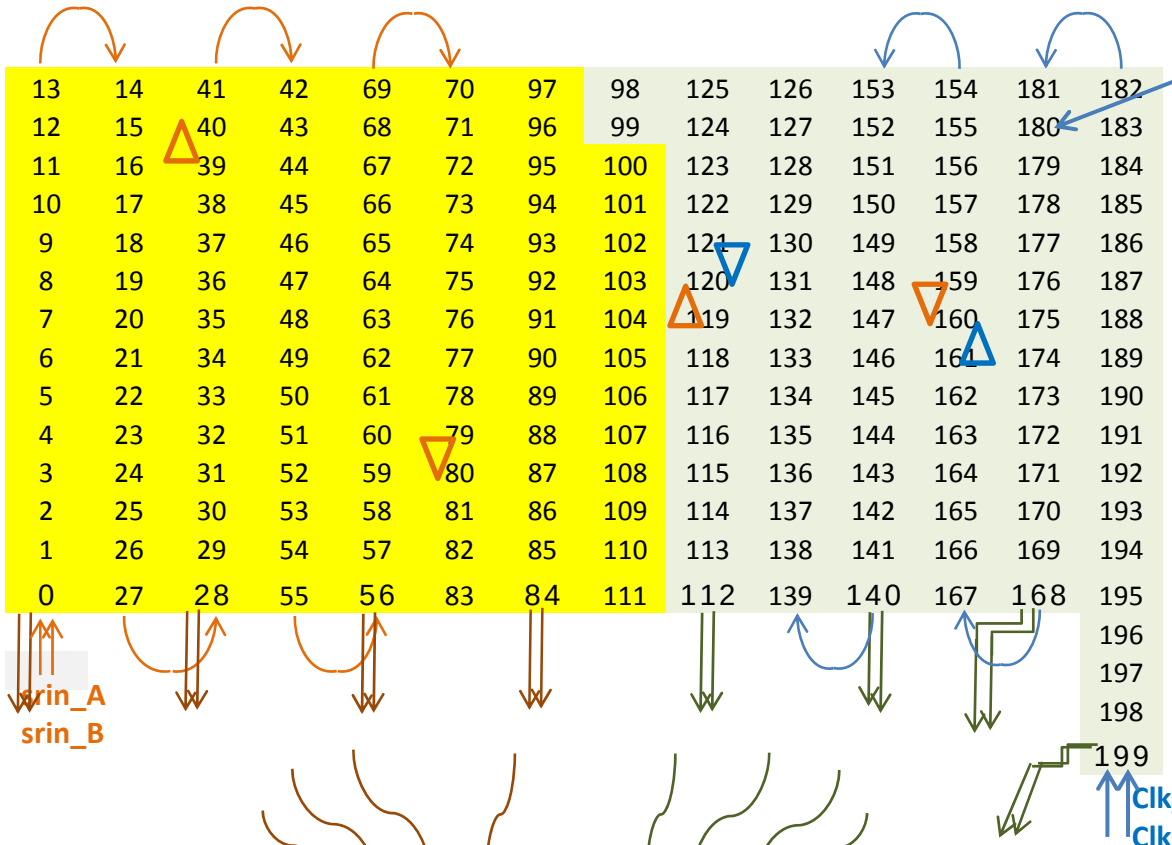


LAYOUT = 1/2 column of 200 PIXELS

1 mm x 1 mm au pas de **50µm x 50µm**

serpent

(design 14 x 14 + 4 cells **chained**)

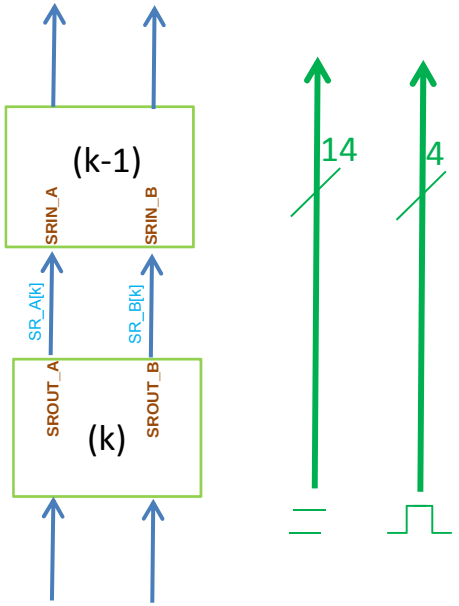


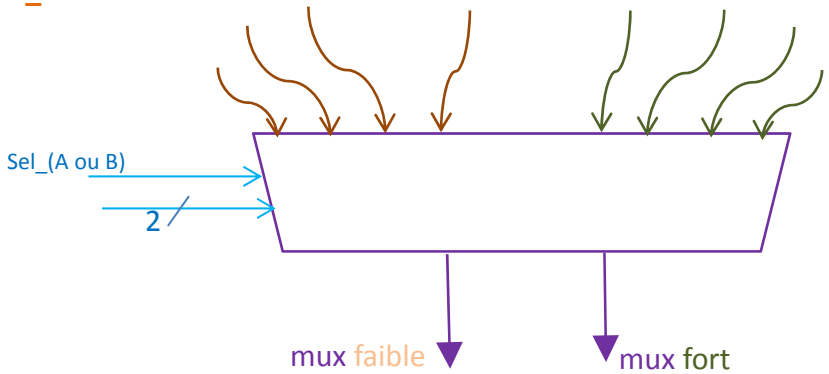
Configurations

- [0]: output enable (hit-en)
- [1:5]:Threshold_DAC
- [6]:large injection capacitor
- [7]:small injection capacitor
- [8:11]: TOT_DAC

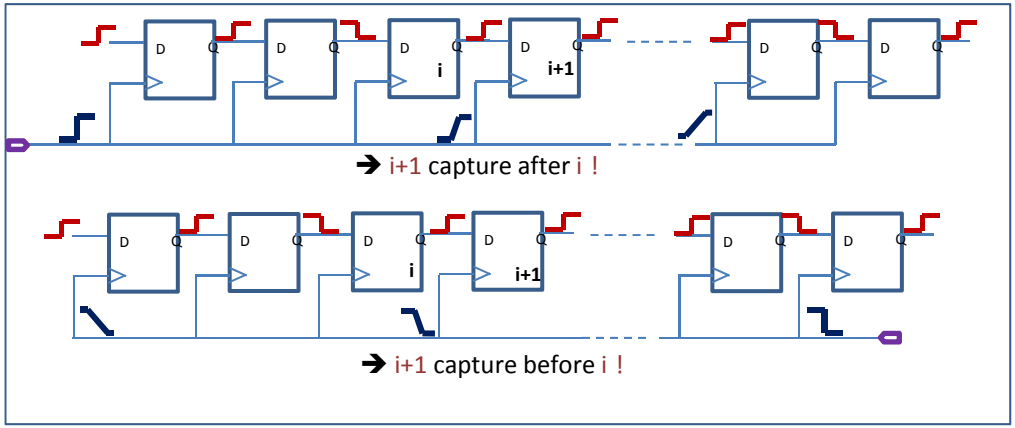
CPPM latch « normal »

CPPM Latch « enclosed »





CPPM recommandation :



One pixel configuration

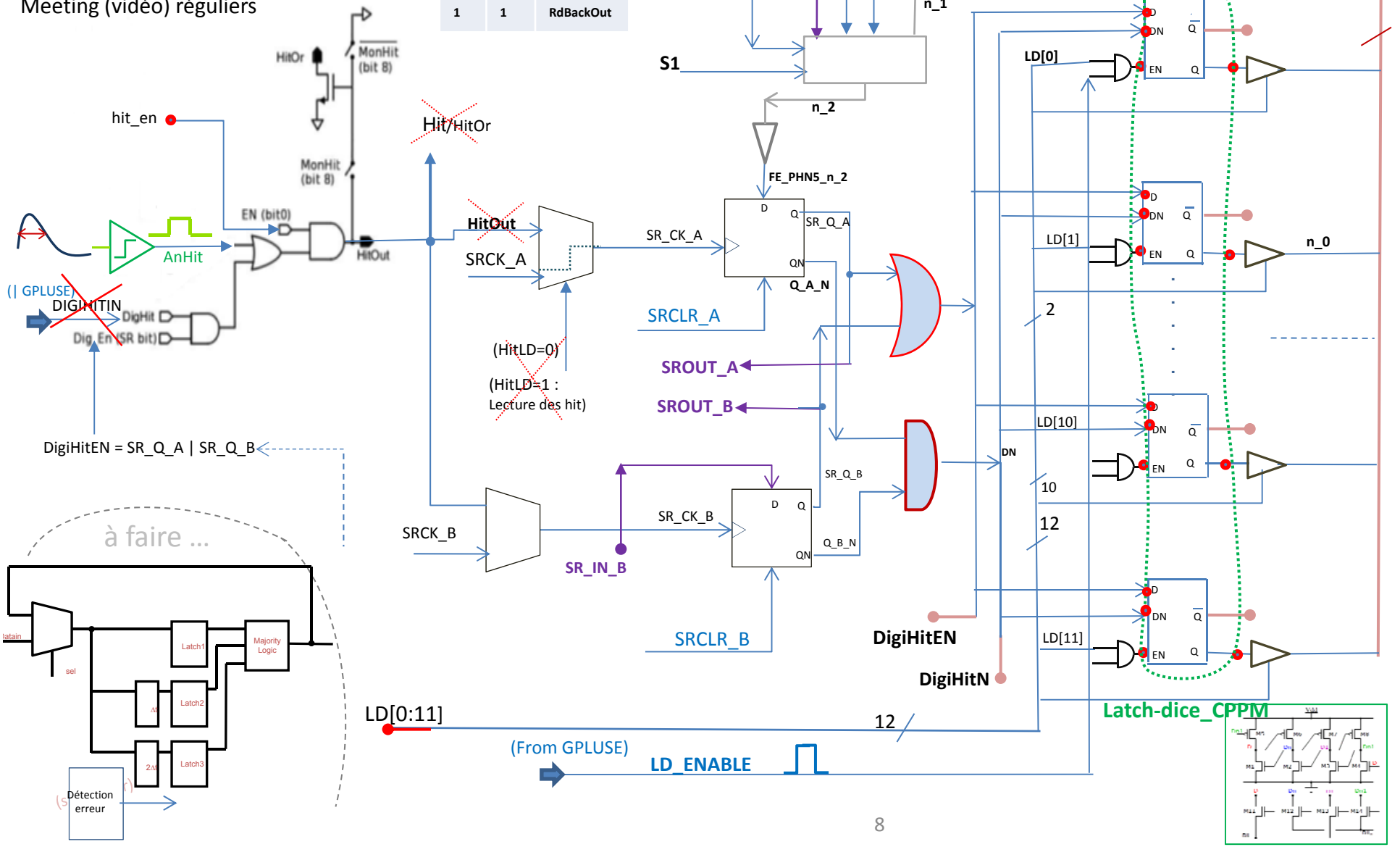
Collaboration avec CPPM Marseille (dec.14- **oct.15**)

Moshine Menouni & Denis Fougeron

Meeting (vidéo) réguliers

(HitLD=0)

S1	S0	SR_D_A
0	0	SRIN_A
0	1	1
1	0	0
1	1	RdBackOut



65 nm

9 layers stacks :

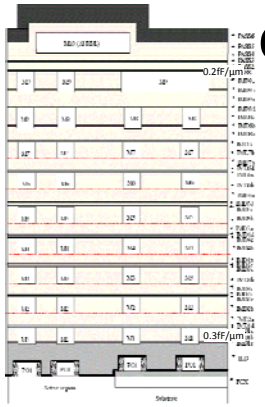
(for routing)

Supply Voltage	1.2V

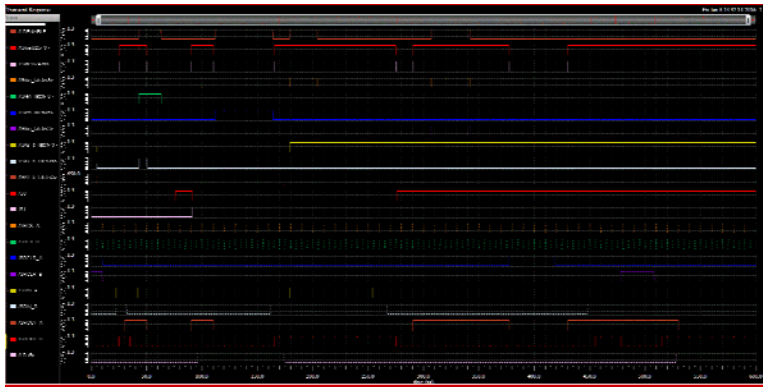
Vth = 0.450 V

encombrement

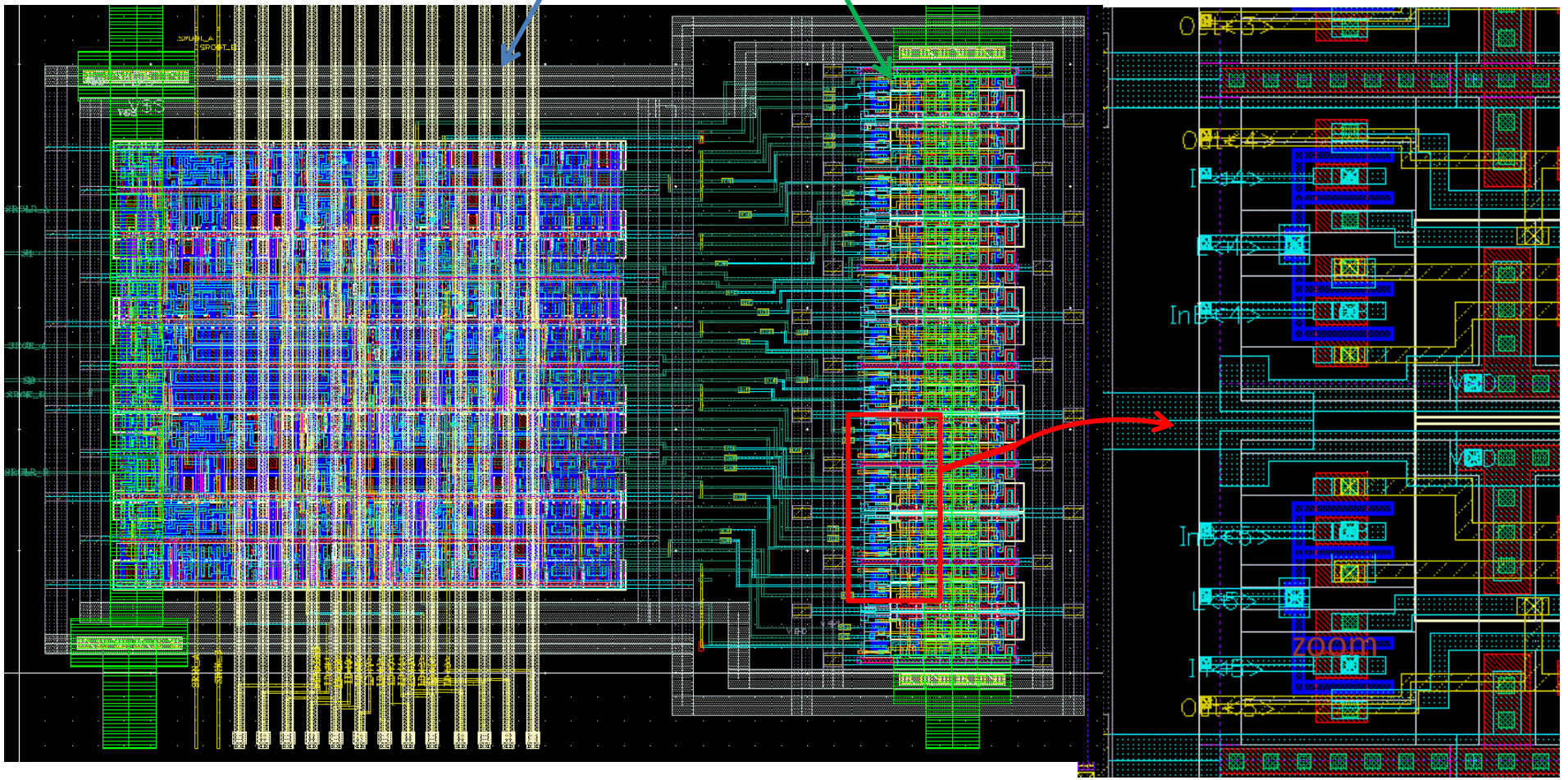
¼ (2500) = 625 µm²



Config one pixel (12 bit)



LAL – CPPM

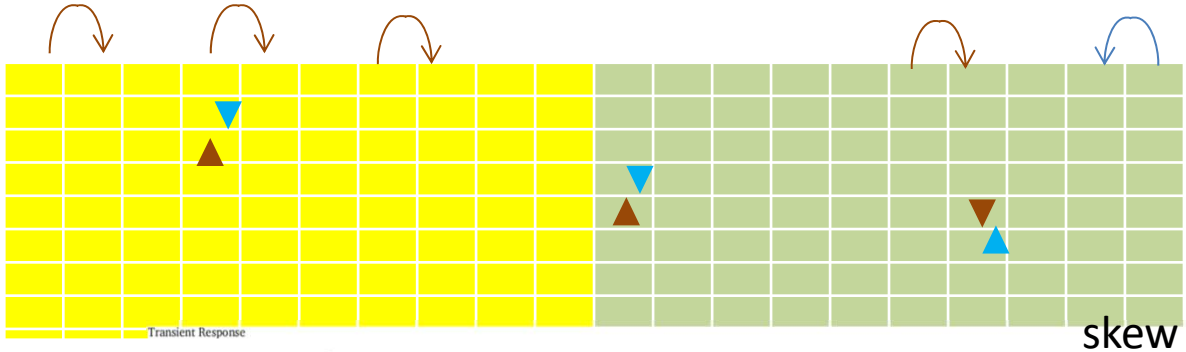


Configurateur : 20.73 x 19.5 = 404.2 µm²

1 Radhard latch 12 bits = 10.35 x 29.32 = 303.5 µm²

Optimisation buffers & lines pour 1 column de 400 pixels

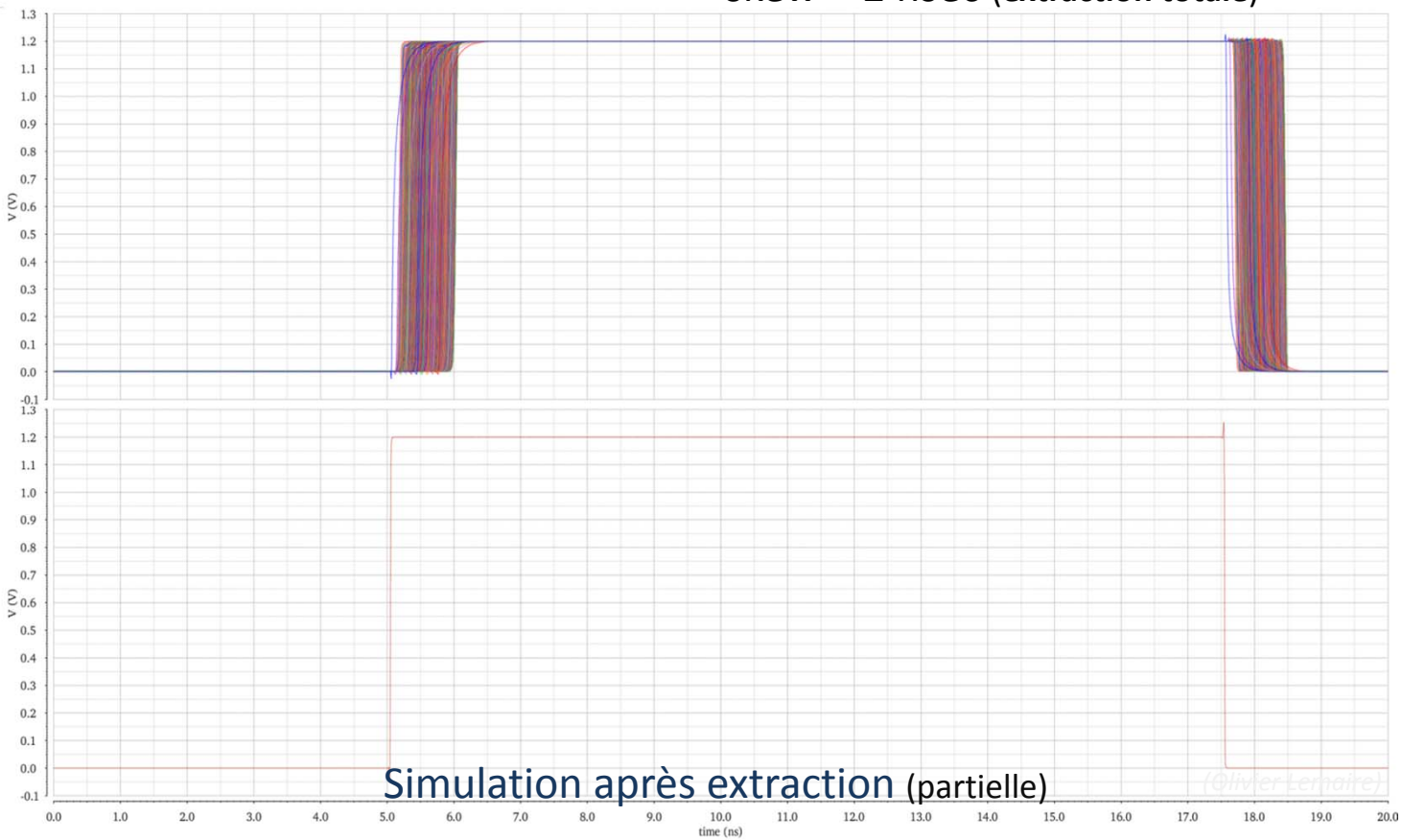
LAYOUT = 20 LIGNES X 20 COLONNES = 400 PIXELS 1 mm x 1 mm pitch **50µm x 50µm**



Clock : length line
400 x 50 µm = 20 mm !

Correction cellule dans le code synthétisé

skew = 2 nsec (**extraction totale**)



Simulation après extraction (partielle)

Optimized under Virtuoso

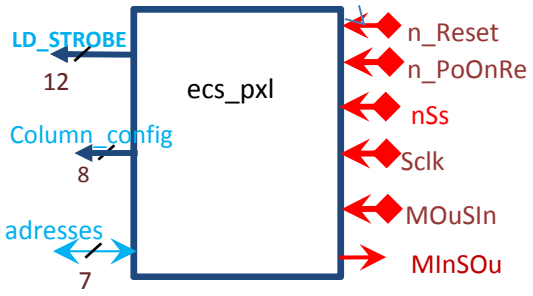
Do not use higher metals
(too width)

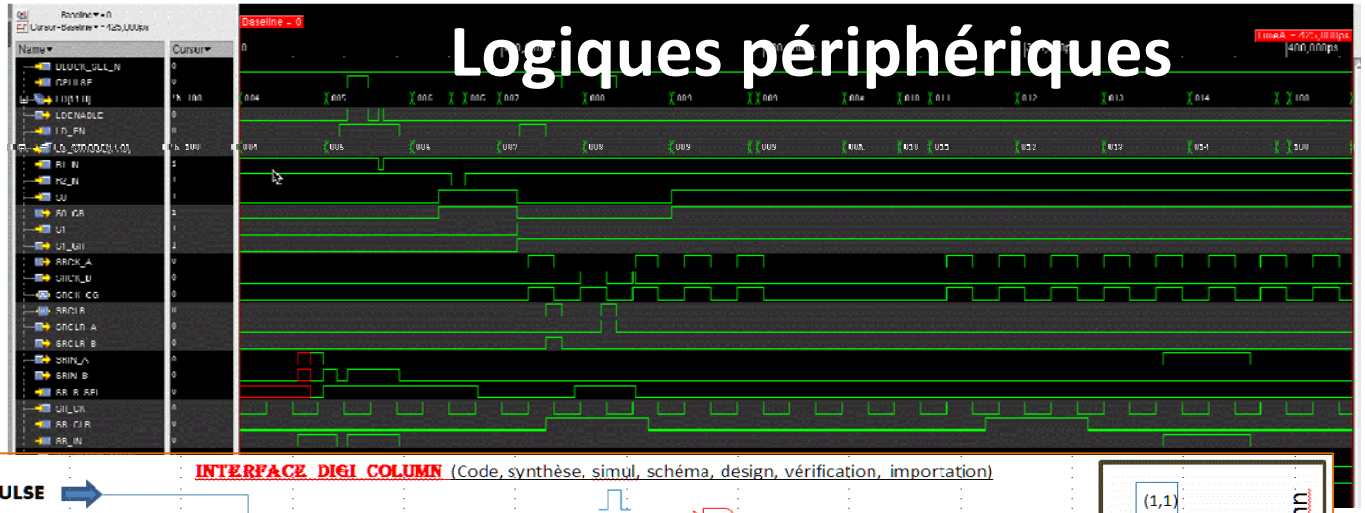
Optimum found :
buffer each 40 pixels

(The buffers are inside the pixel)

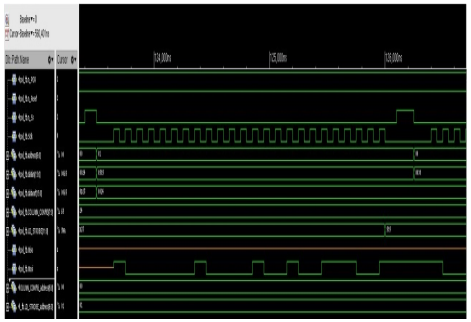
Logiques périphériques

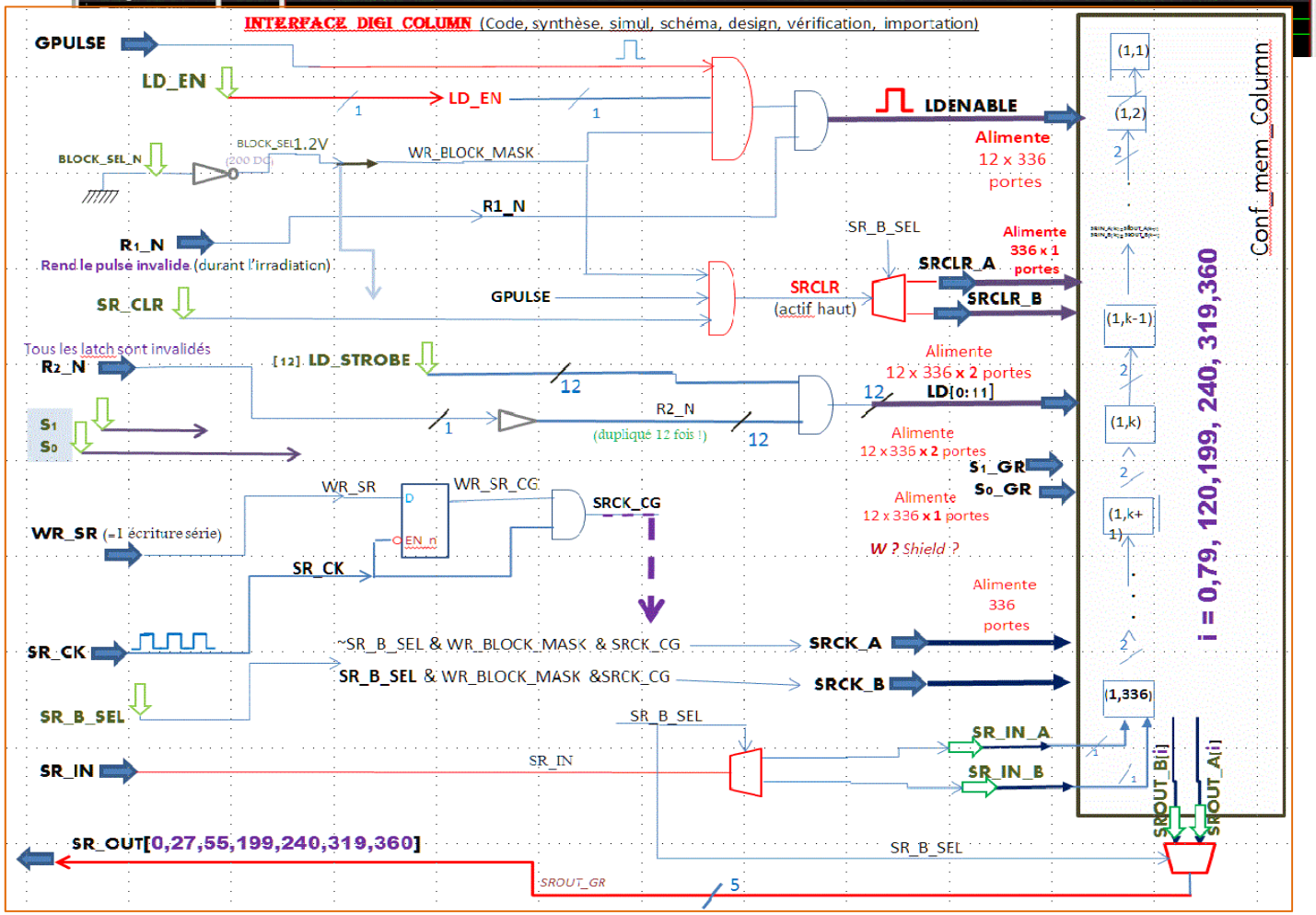
encapsuled_pixel



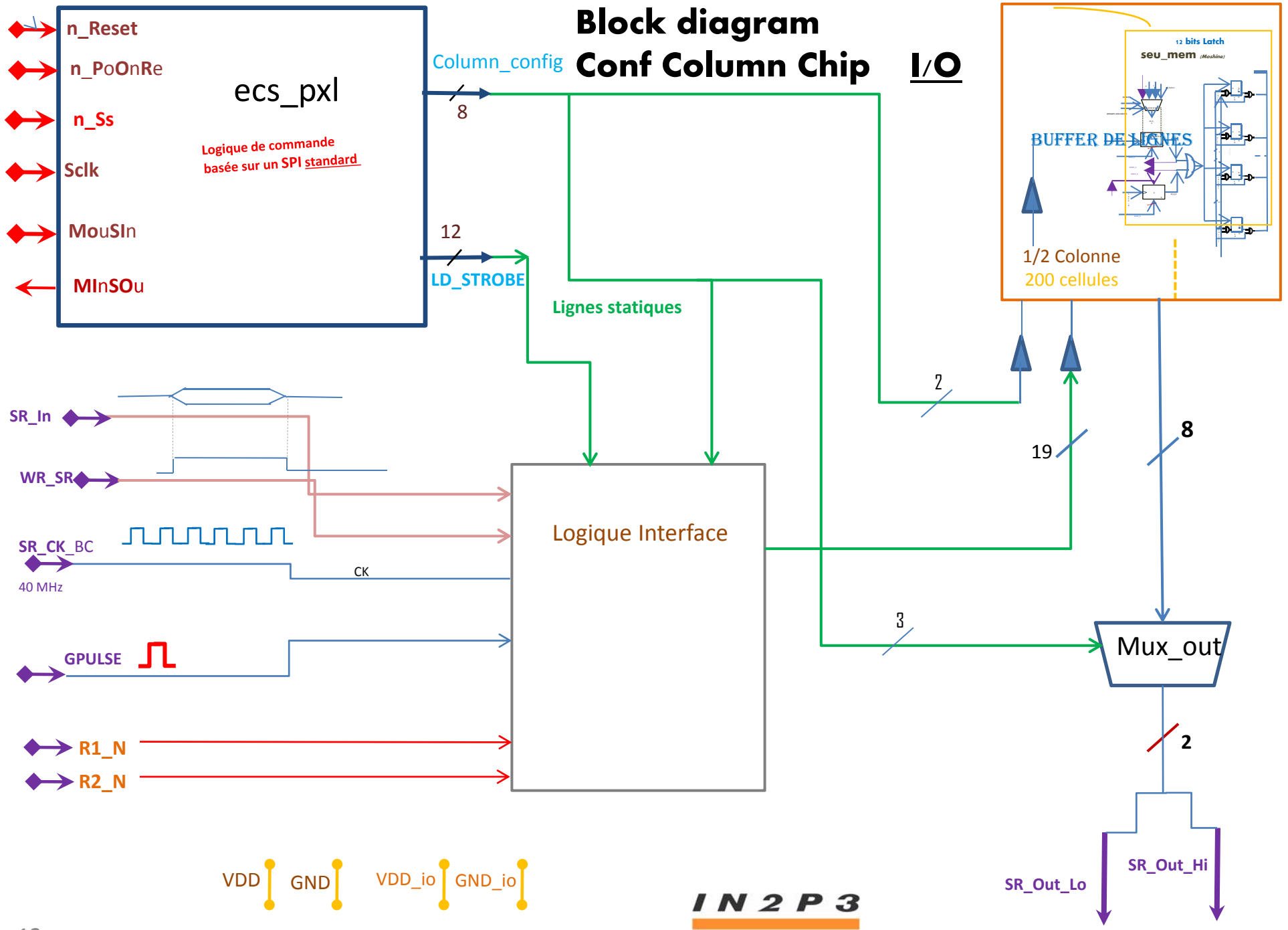


Basé sur un SPI
(triple voting)



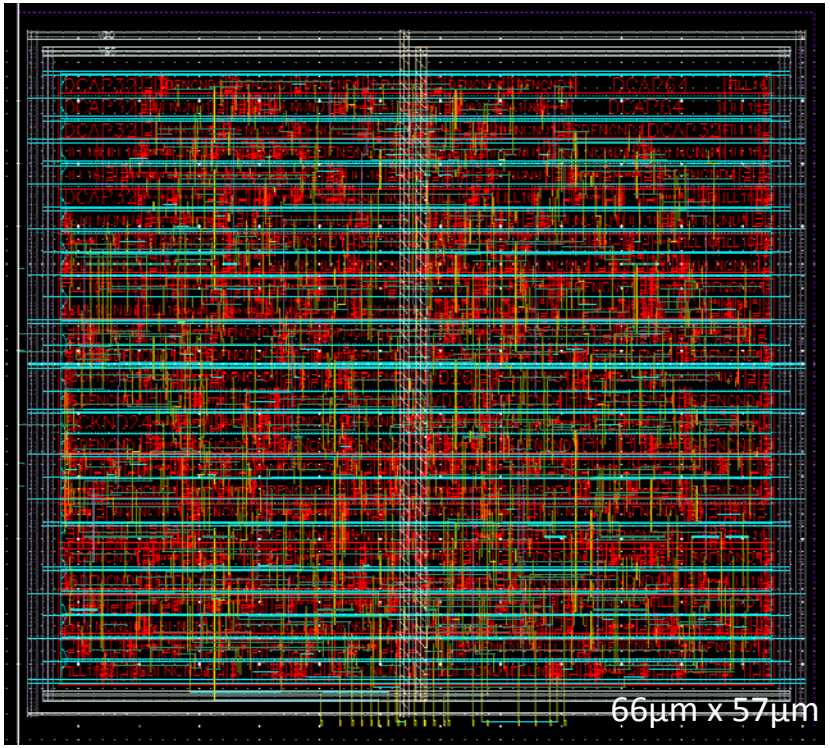


Block diagram
Conf Column Chip I/O

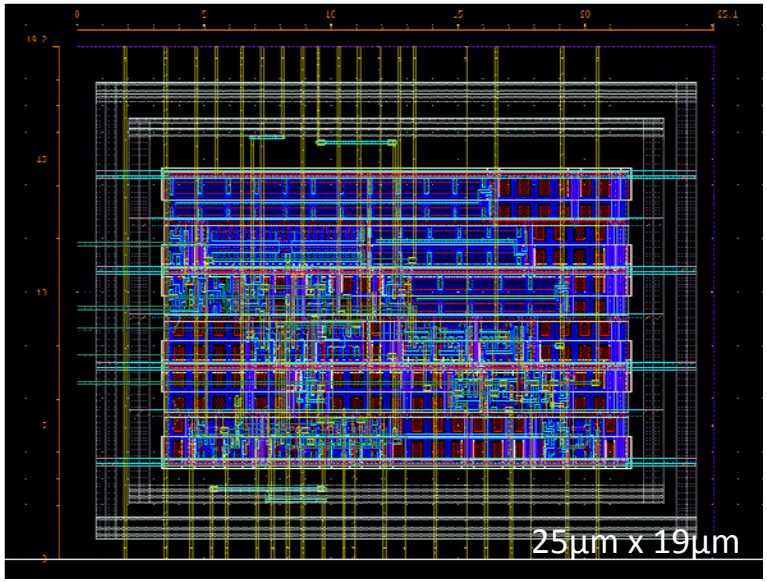


IN2P3
Institut National de Physique Nucléaire et de Physique des Particules

Blocks périphériques



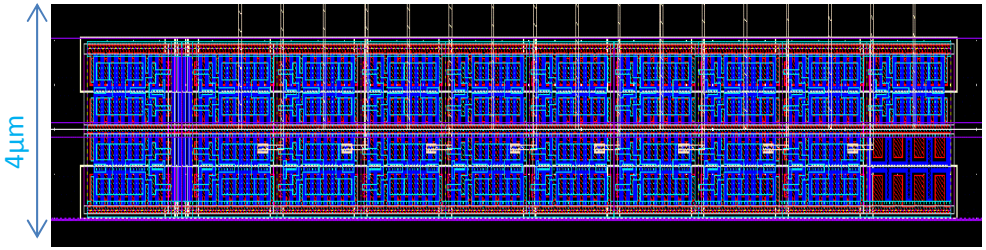
1.2 Volt

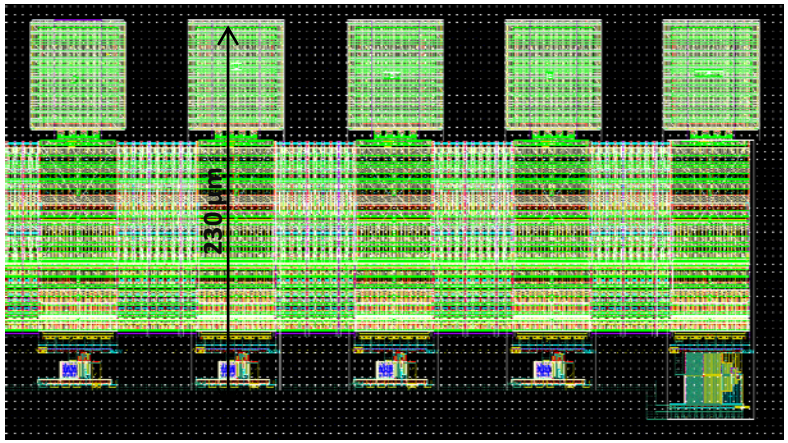


Logique d'interface

Encapsulé SPI

Buffers lignes





PADs

Top level integration :

« Génération matrice automatique »

Blocks simulation : spectre

Top level simulation : AMS & behaviour

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Coût

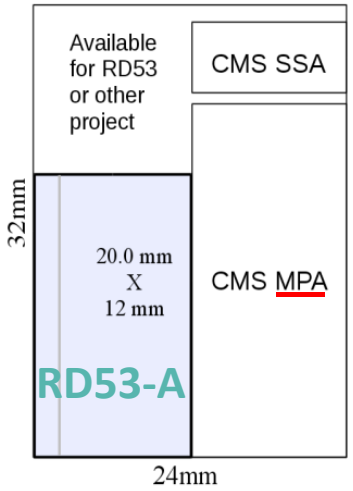
- ## MPW – Multi-Project Wafer

  price ~ 90% engineering run (Full Maskset)

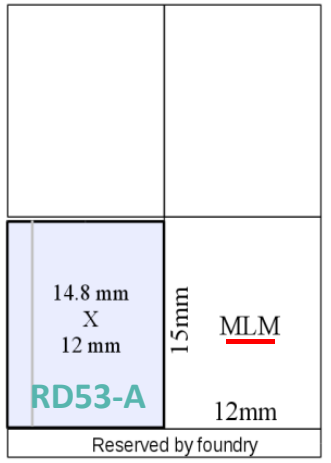
  Mini ASIC 2mm x 2mm = 17 000€ + 1 000€

  (C3) → 1 mm x 1mm = ¼ (18 000) = **5 150 €**

  (RD53-A) → 20 mm x 12mm **~ 500 k€**



(fin 2016)



Back-up solution

- ## MLM – Multi Layer Mask (Reticle)

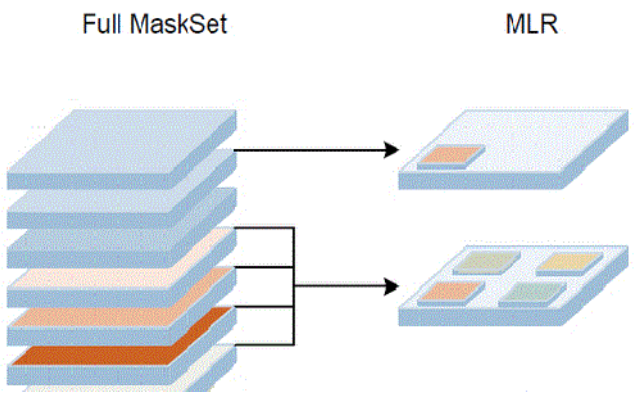
  NRE (Non-Recurring Engineering) ↘ ↗ wafer price

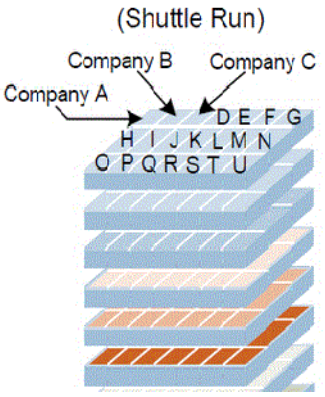
  220 k$ / mm²

- ## Engineering Run

  (RD53-A) → 20x12 mm² ≡ ~ 1 M€

  (RD53) → 400 mm² ≡ 2,2 M€





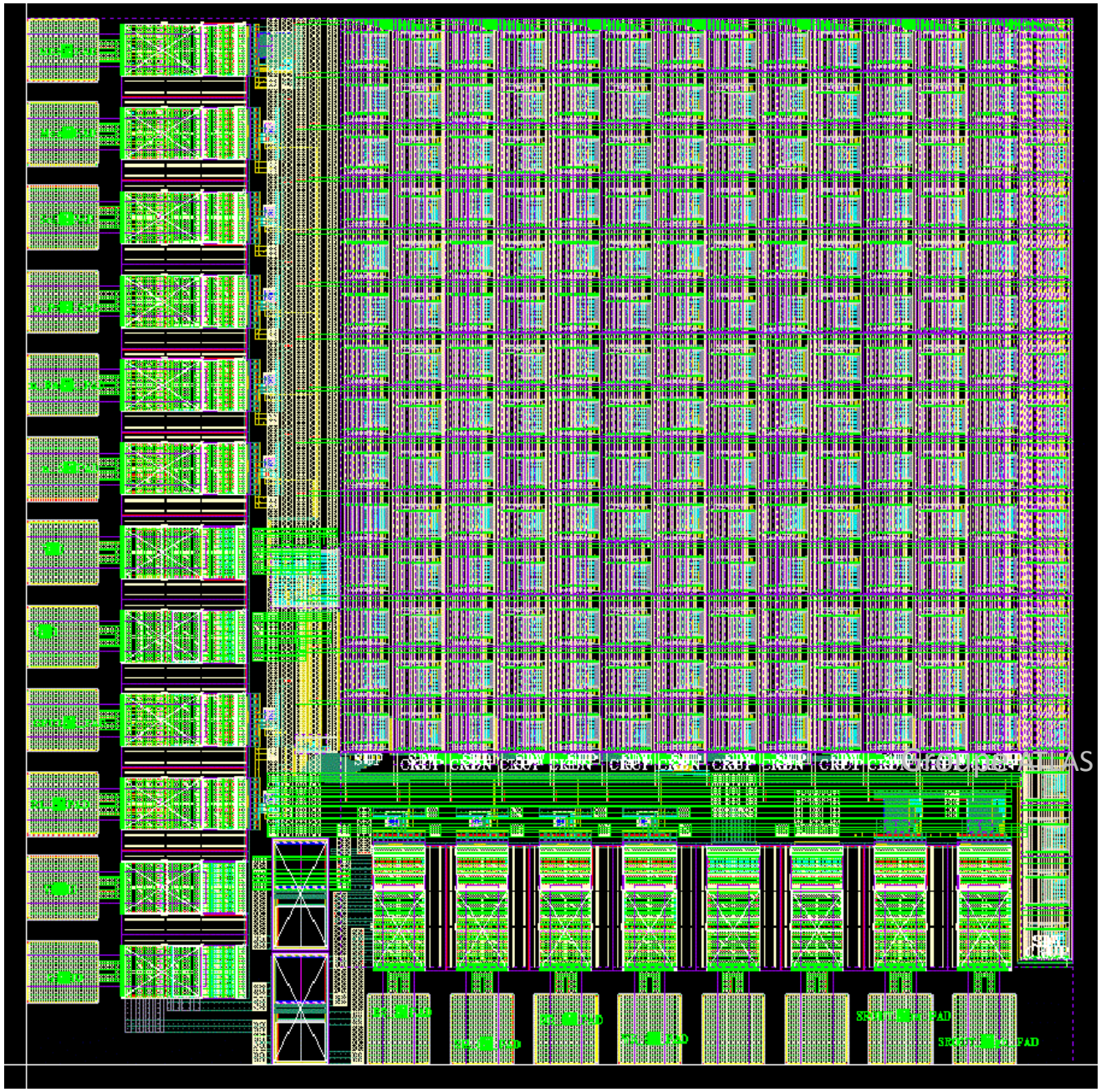
Conf Column Chip (C3)

Layout « top level »

- Size 1 mm x 1 mm
  (pitch 50µm x 50µm)
- PADs on 2 sides

14 x 14 + 4 pixels

Submitted
on 23rd march



LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Groupe ATLAS

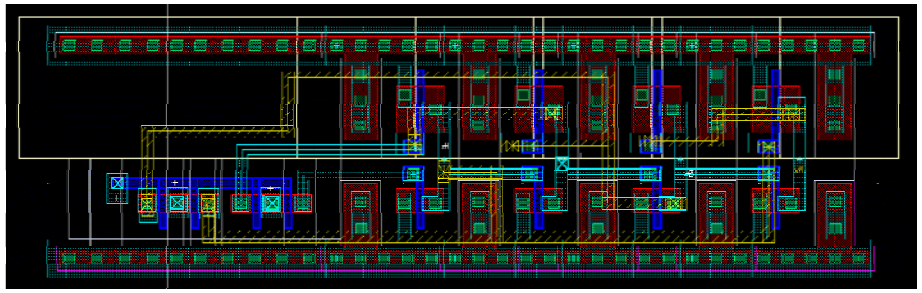
SERDI
Service d'Electronique, Recherche en Détecteurs et Instrumentation

Futur développements

- Reprendre le Rad Hard Latch
- Reprendre la cellule (CPPM & RD53-A)
- *Implémentation Triple Module Redundancy*
- Implémentation cellule dans RD53-A
- **U**niversal **V**erification **M**ethodology ***V**erification **E**nvironment for RD**53 PIX**el chips*

26 avril 16 : présentation au meeting RD53-A

Simulation consommation et SEU de la configuration d'une colonne



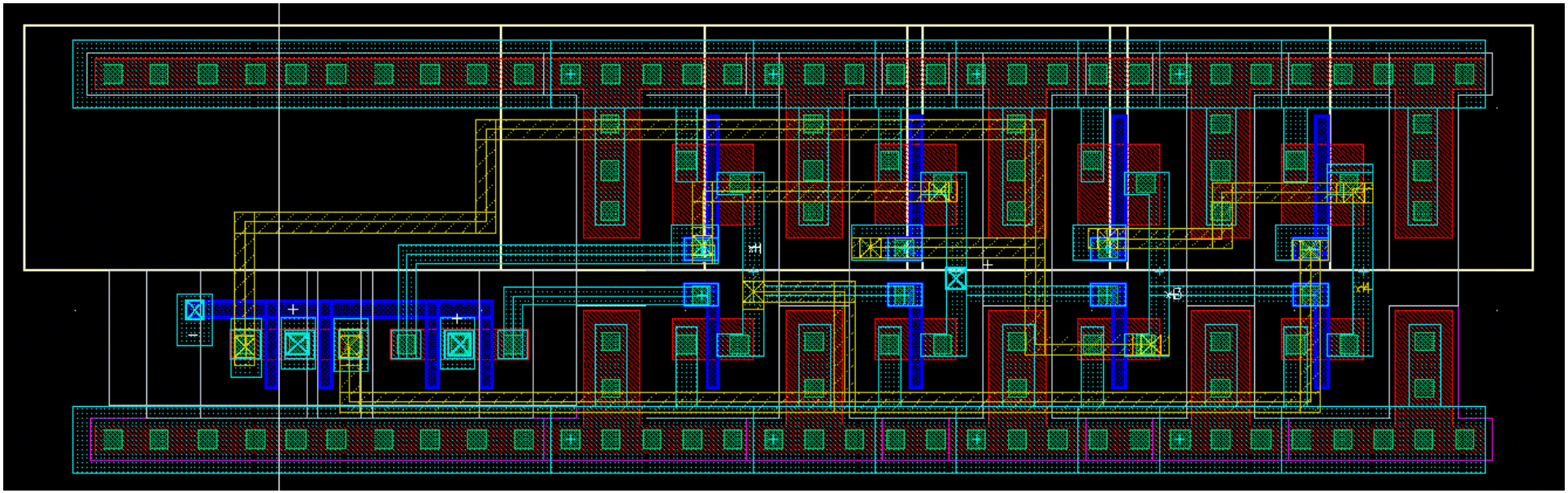
- *Cartes de test*
- *Firmware, software*
- Test irradiation

(Set-up, hardware, software, formation, suivi médical, accès)

Zone controlée

Zone surveillée

Backup slides

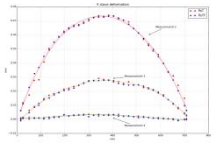


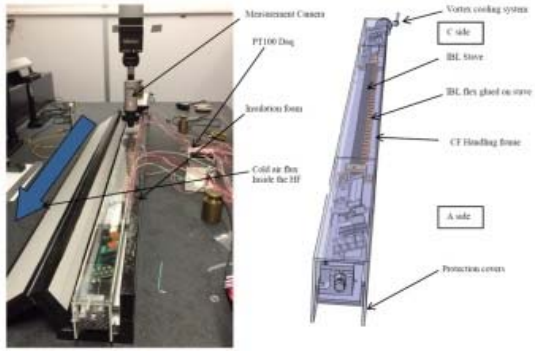
IN2P3 dans ATLAS tracker Phase-II Upgrade

Pixels:

CPPM(Marseille), LAL(Orsay),

LAPP(Annecy), LPC(Grenoble), LPNHE(Paris)





Mécanique

Tests détecteurs

Tests modules

Fast Tracker:

LPNHE(Paris)

Pixel microélectronique :

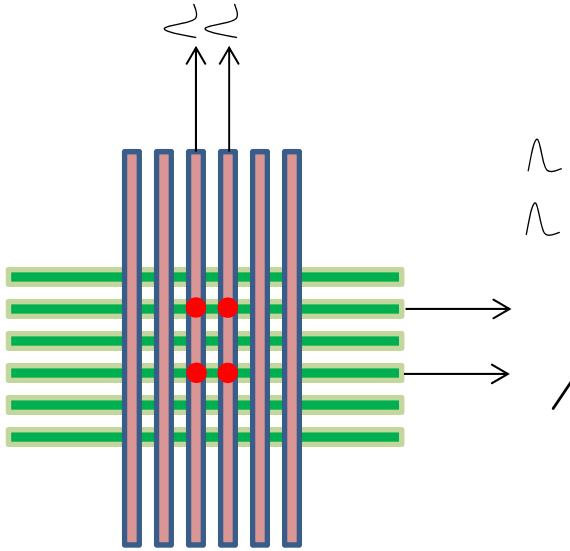
CPPM(Marseille), LAL(Orsay), LPNHE(Paris), ? .

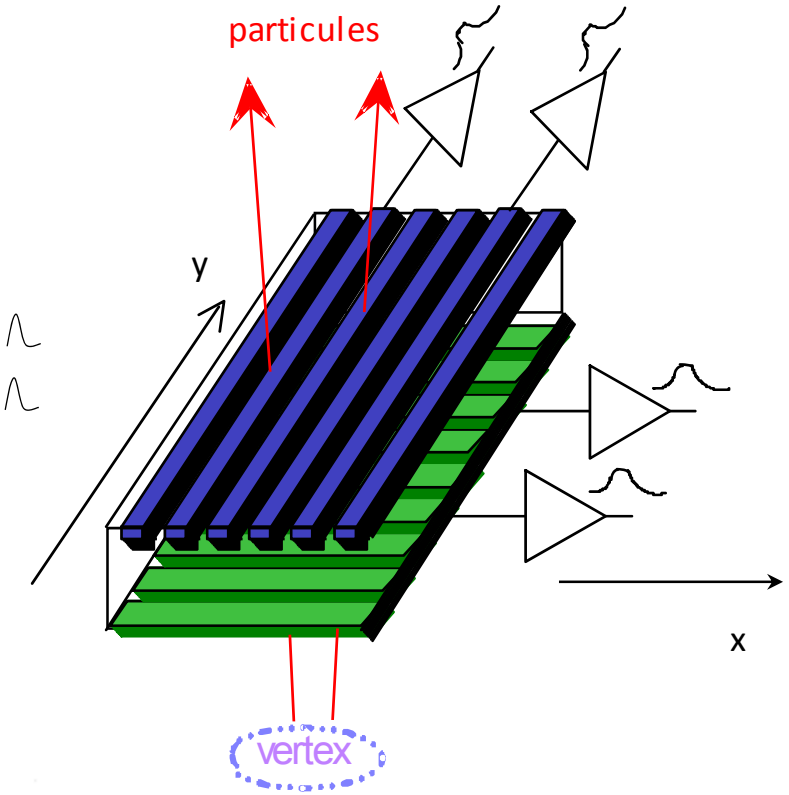
⟶ Réunion des 3 laboratoires

Représentation dans **RD53 : LBNL, SiLab, CERN, INFN,** ? IN2P3

Pourquoi le développement des détecteurs pixels ?

- Micro-bandes (double faces)



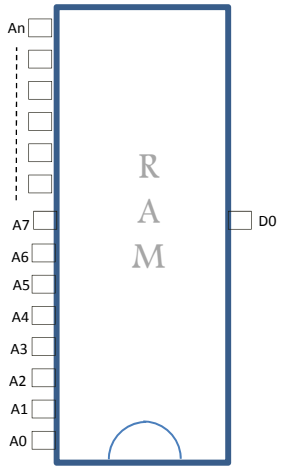


The silicon micropattern detector : a dream ?

(1987)

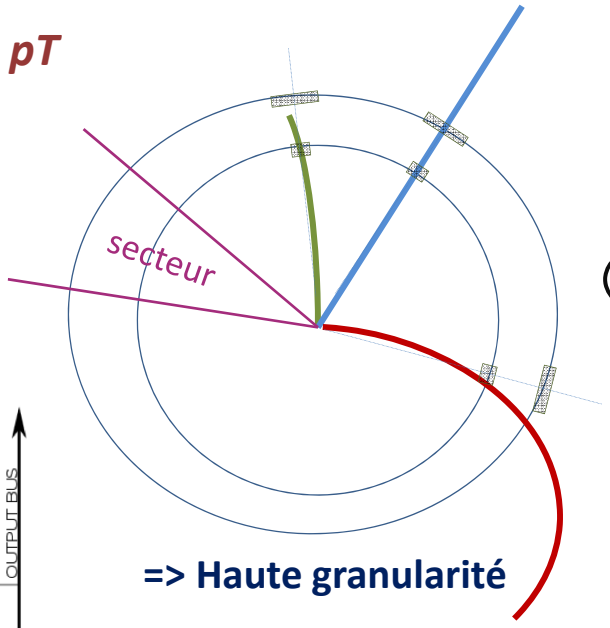
ABSTRACT

The present use of silicon microstrip detectors in elementary particle physics experiments is described and future needs are evaluated. Possibilities and problems to be encountered in the development of a true two-dimensional detector with intelligent data collection are discussed. This paper serves as an introduction to various other contributions to the conference proceedings, either dealing with futuristic device designs or with cautious steps on the road of technology development.



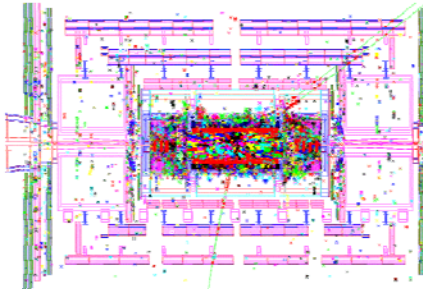
Principe ITK

high pT



$\odot \vec{B}$

3.8 T

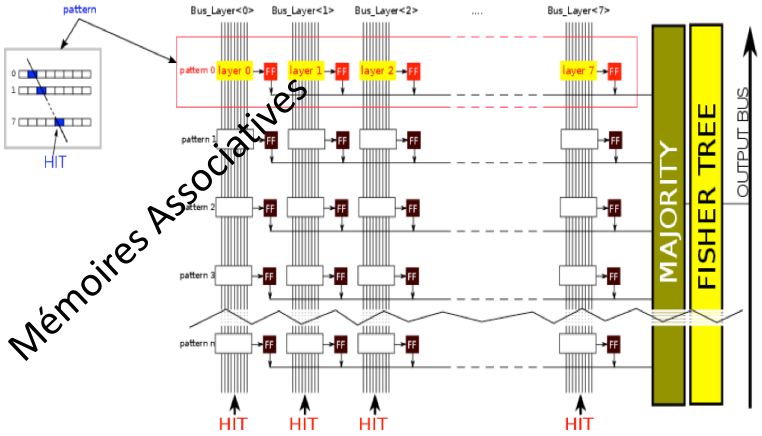


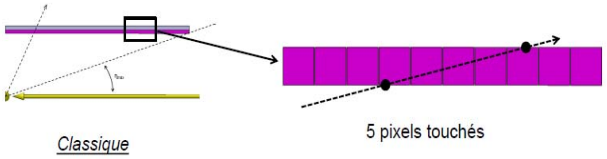
H -> ZZ -> 2e + 2µ

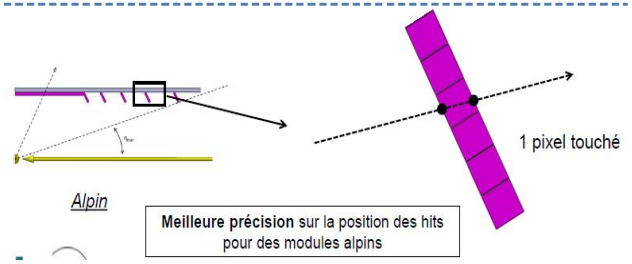
=> Haute granularité

L1 :

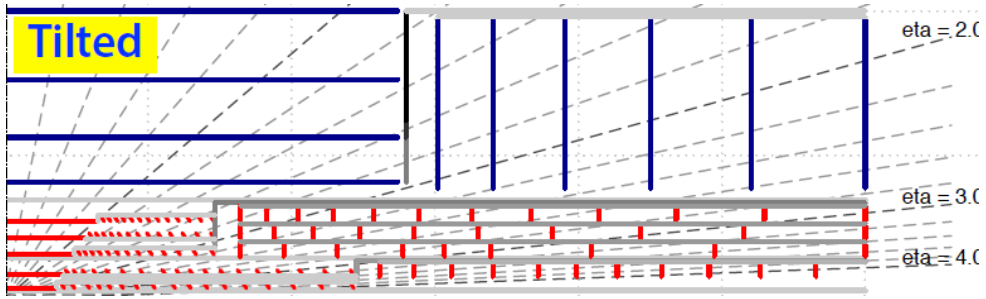
Inner tracker (SCT ; micro-pistes)
Calorimeter
Muon detector





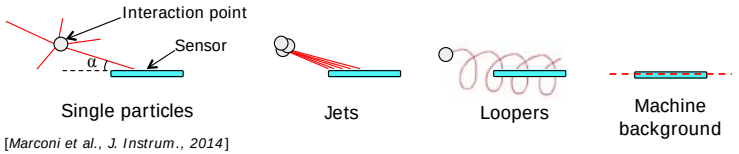


Strip module



r < 20 cm
*TID ~ **1 Grad***

5 couches de pixels



[Marconi et al., J. Instrum., 2014]

Le trigger

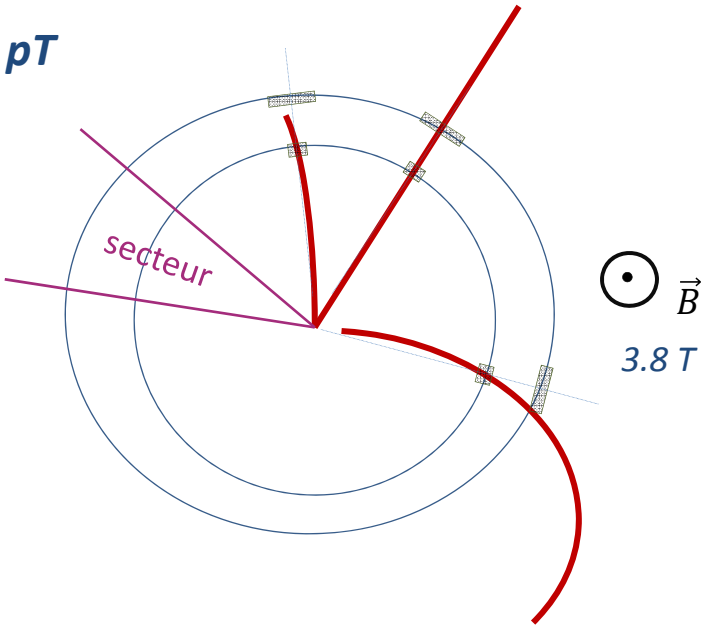
L1

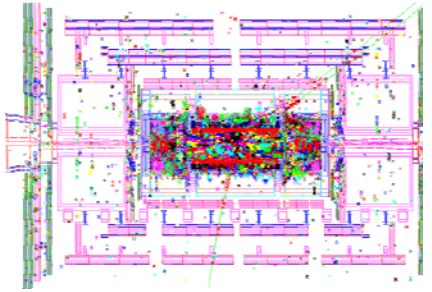
1MHz (100 kHz actuellement)

Latence ~ 10 µs

(3 µs actuellement)

high pT





H -> ZZ -> 2e + 2µ

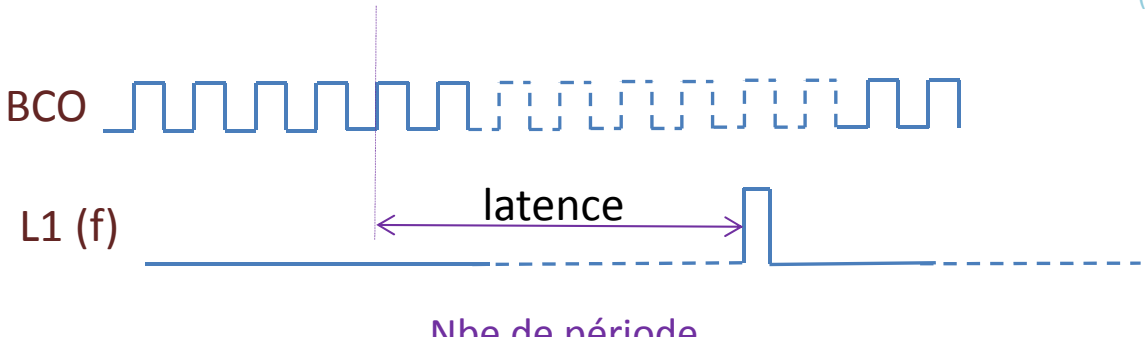
L2 (including tracking)

400 kHz (10 kHz actuellement)

Latence ~ 30–60 µs

L1 :

Inner tracker (SCT)
Calorimeter
Muon detector

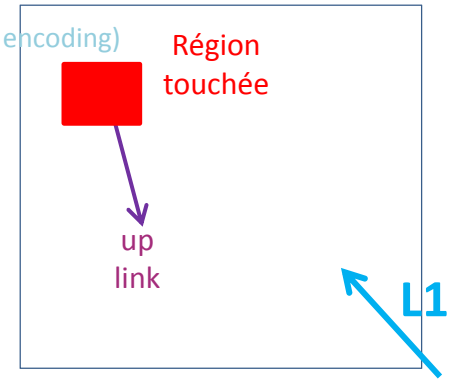


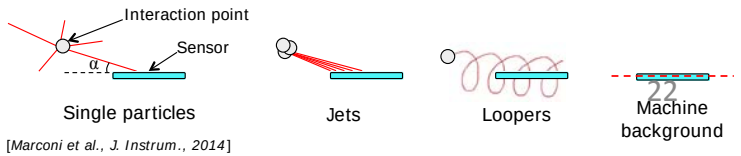
Nbe de période

10µs / 25ns

400

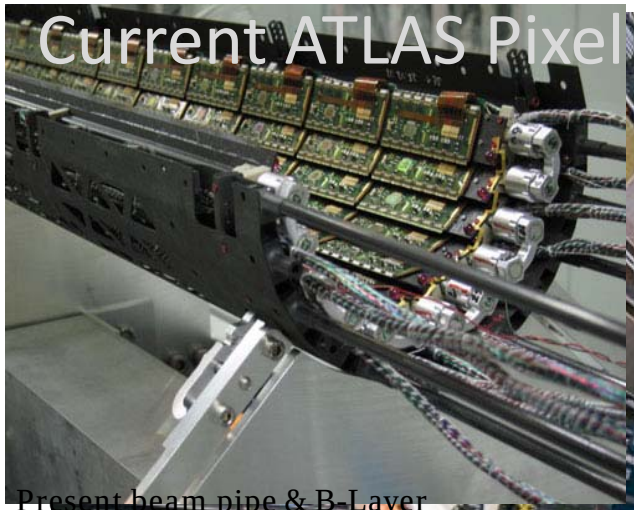
(Centroid position encoding)



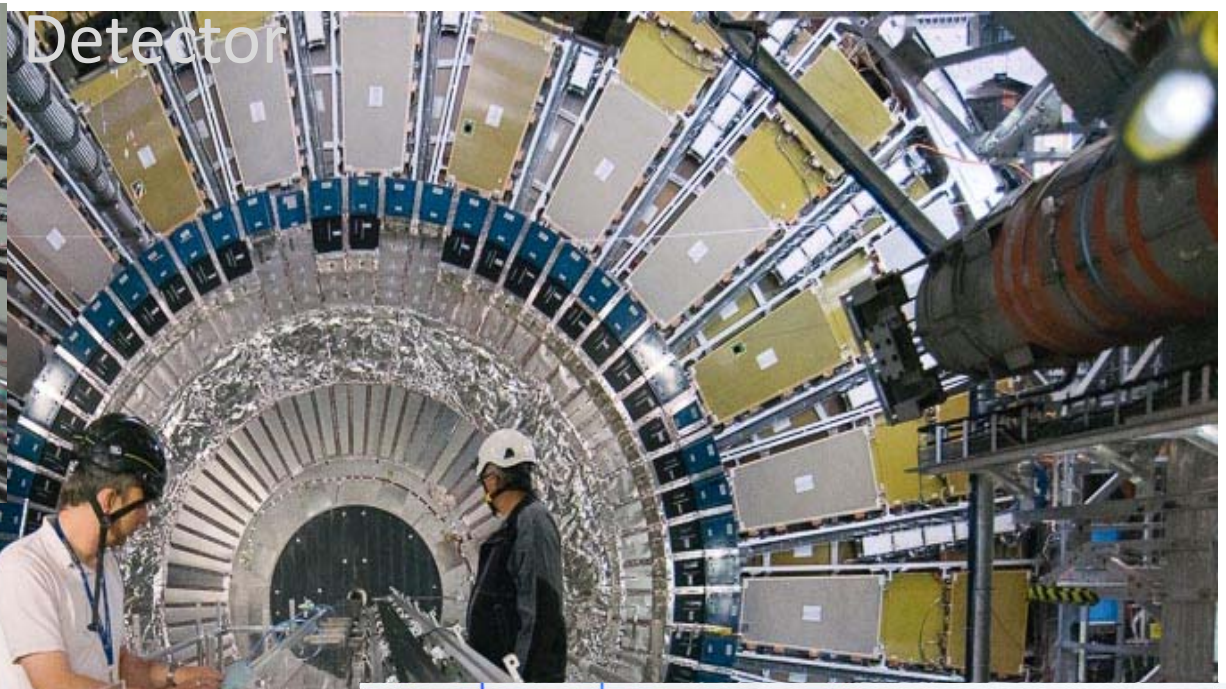


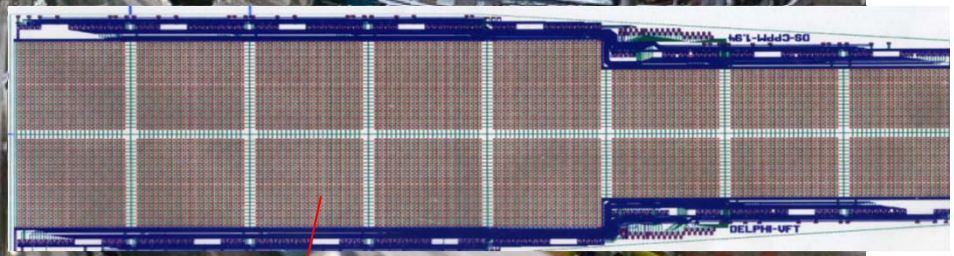
[Marconi et al., J. Instrum., 2014]

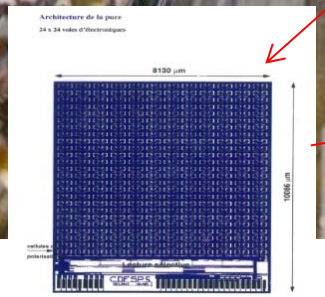
Current ATLAS Pixel Detector

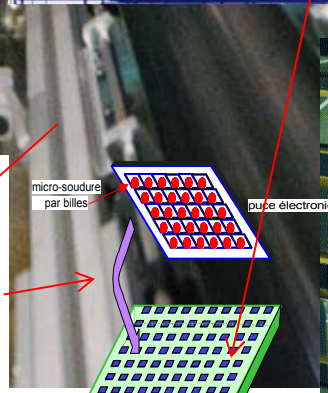


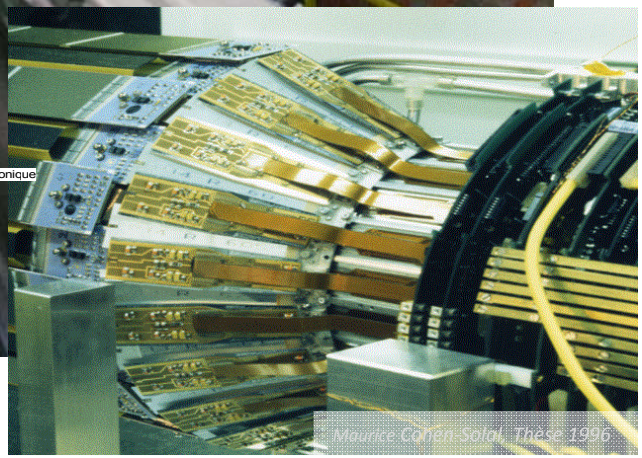
Present beam pipe & B-Layer









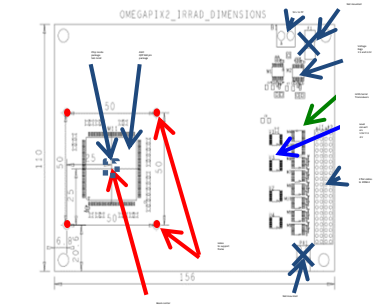


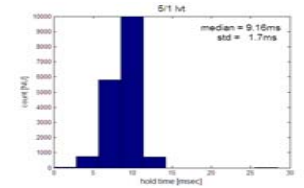
Test d'Irradiation du Circuit Omegapix2 (130nm)

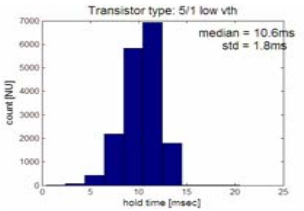
LPNHE PARIS

Proton Facility, PS East Hall (building 157)

Test of the analog pipline memory







ZONE 2 (IRRAD 9) | **ZONE 4** | **SALLE DE CONTRÔLE**

ZONE CONTROLEE ACCES REGLEMENTE

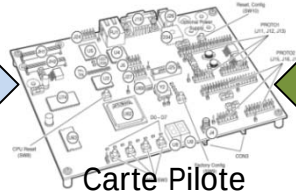
Faisceau

Zone moins exposée

ASIC | Logique I/O

Carte Irradiée OMEGAPIX2_IRRAD

~30 I/O + Alim



Carte Pilote FPGA+Interface

2 câbles plats => IRRAD 9
1 câble Alim LV
1 barette 220V CH
1 câble Ethernet

ETHERNET ~10 m

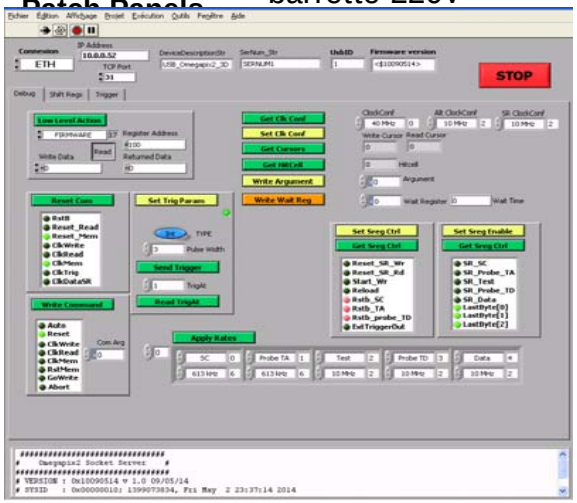
PC de monitoring Soft Labview ou Appli (Labview Application Builder)

Possibilité d'éteindre et allumer la barrette 220V

2m ~7m 2m

Irradiation @ CERN (24 GeV p)
Integrated Fluence 3.5*1015 p/cm2

run **mai 2015**

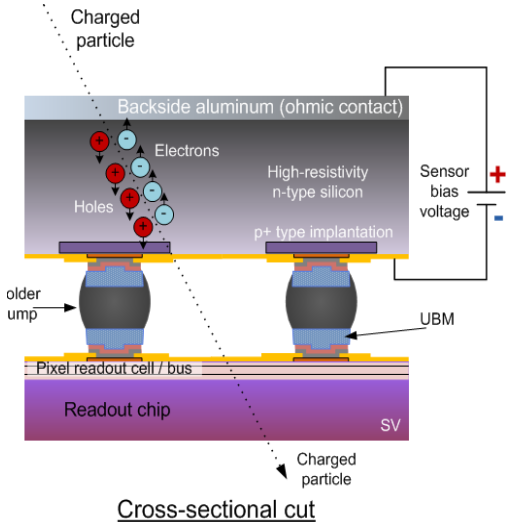


LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

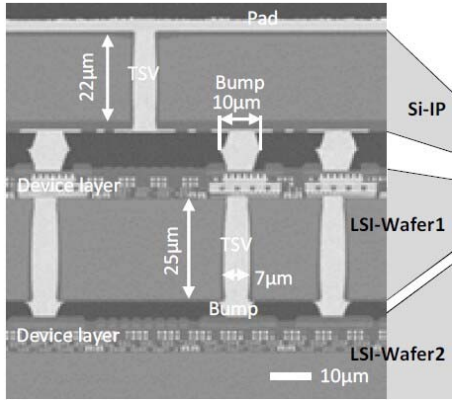
Pixel sensor(s) *not yet determined*
Innovation dans les Interconnections des modules

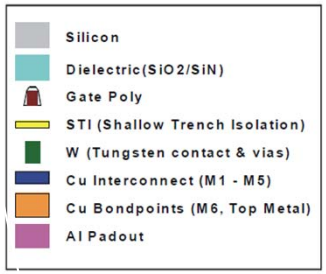
Module ~170 SFr/cm^2

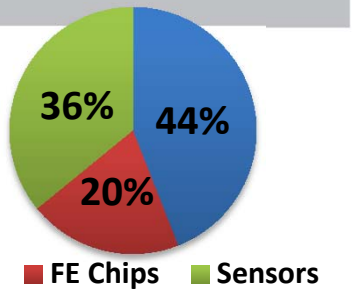
Problématique : Réduction du coût total système des pixels (~32MSFr) dont (18MSFr) Modules hybrides



Cross-sectional cut







Interconnect FE Chips Sensors

Objectif : réduire le coût de 40%

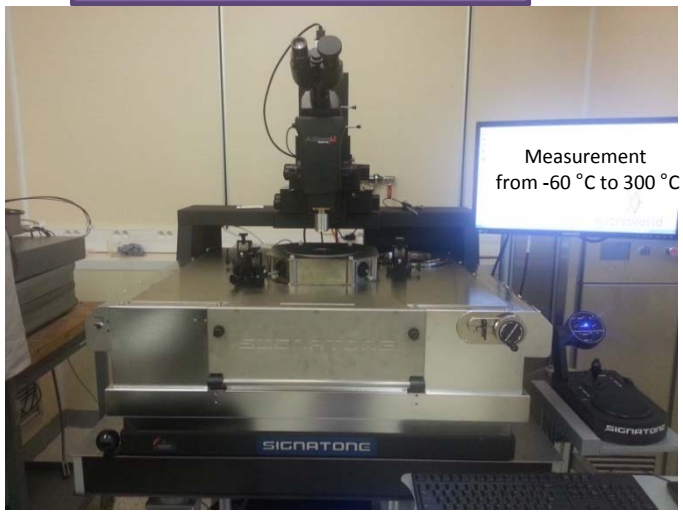
Partenariat CERN, MPI, Glasgow, LAL avec leCEA/LETi Grenoble

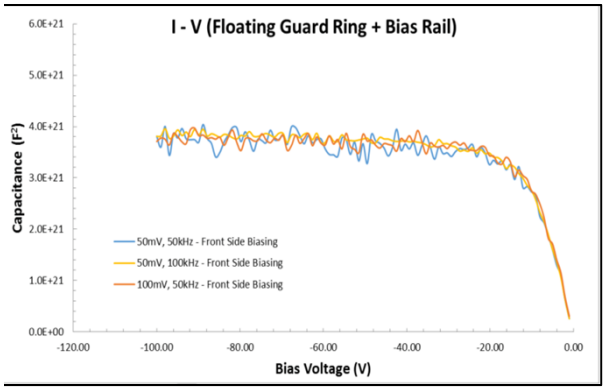
AIDA 2020

Sigmatone

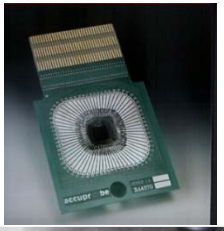
New 50 m2 cleanroom with acquisition of semi-automatic testing system machine.
For medium or large scale testing, such as for the HL-LHC.

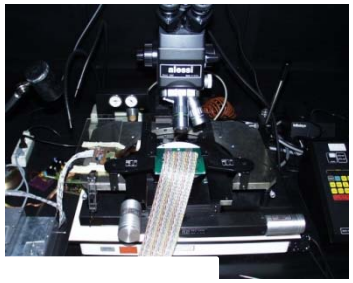
SEMI AUTOMATIC PROBE STATION





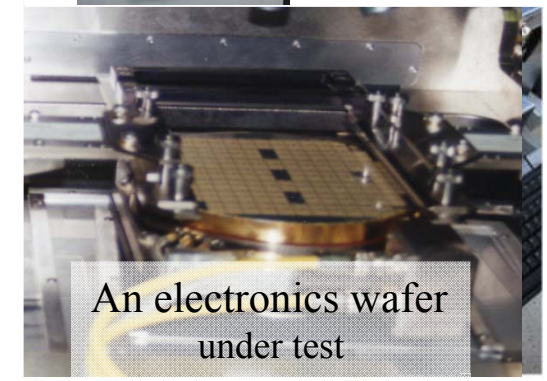
Test, caractérisation & appariement

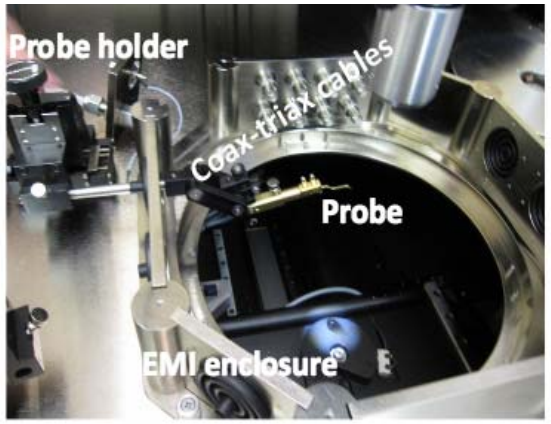


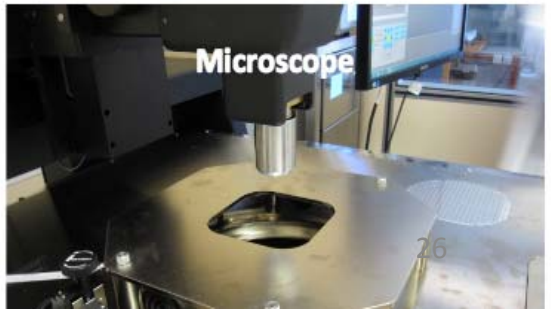


KEITHLEY
A Tektronix Company

Test de semi conducteur







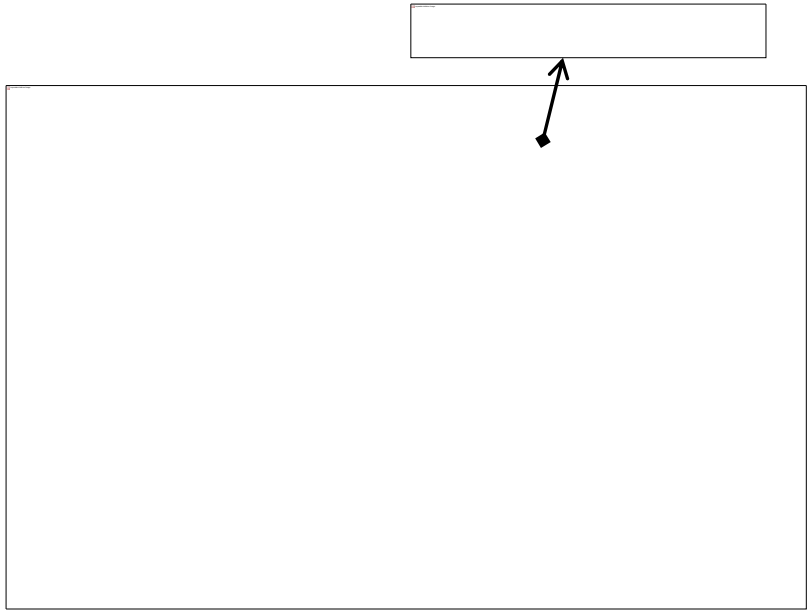
Technologies

Omegapix_1 130 nm Chartered Semiconductor

64 x 24 pixels, pas : 50µm x 50 µm

Omegapix_2 (3D) **130 nm Global Foundries**

96 x 24 pixels, pas : 35µm x 200 µm



FE-I3 (2003) 250 nm IBM

18 x 160 pixels, pas : 50µm x 400 µm

FE-I4-B (2011) 130 nm IBM

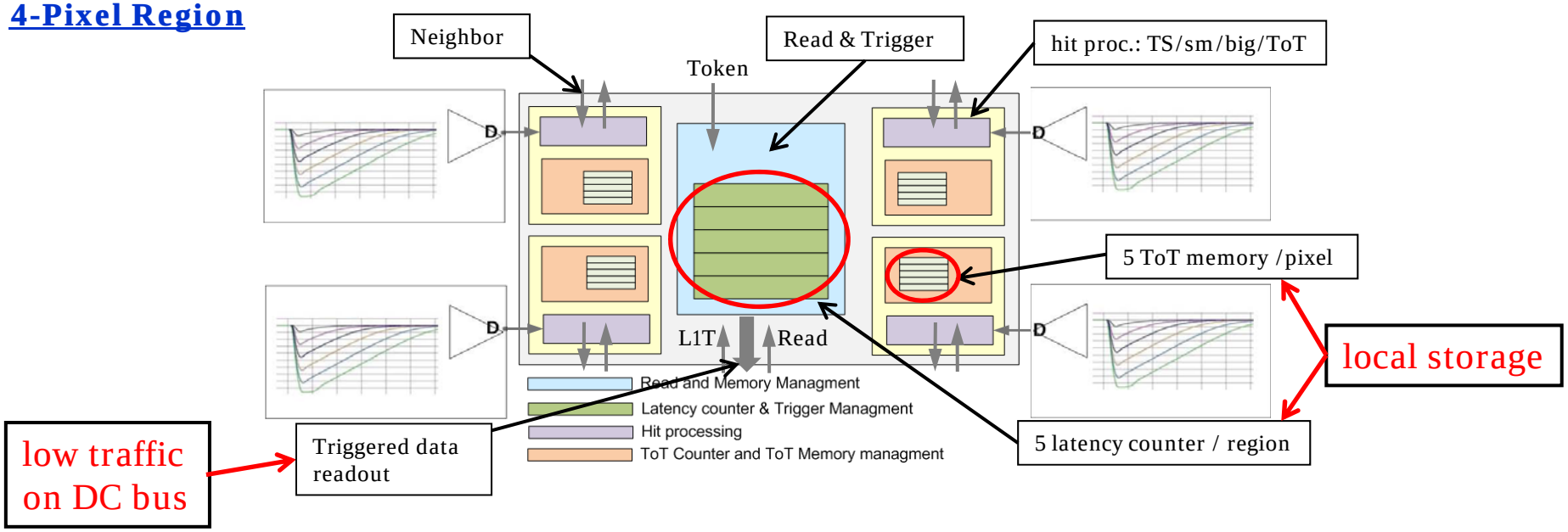
80 x 336 pixels, pas : 50µm x 250 µm

RD53-A (2016) 65 nm TSMC

400 x 200 pixels pas : 50µm x 50 µm

Digital Pixel: Regional Architecture

4-Pixel Region

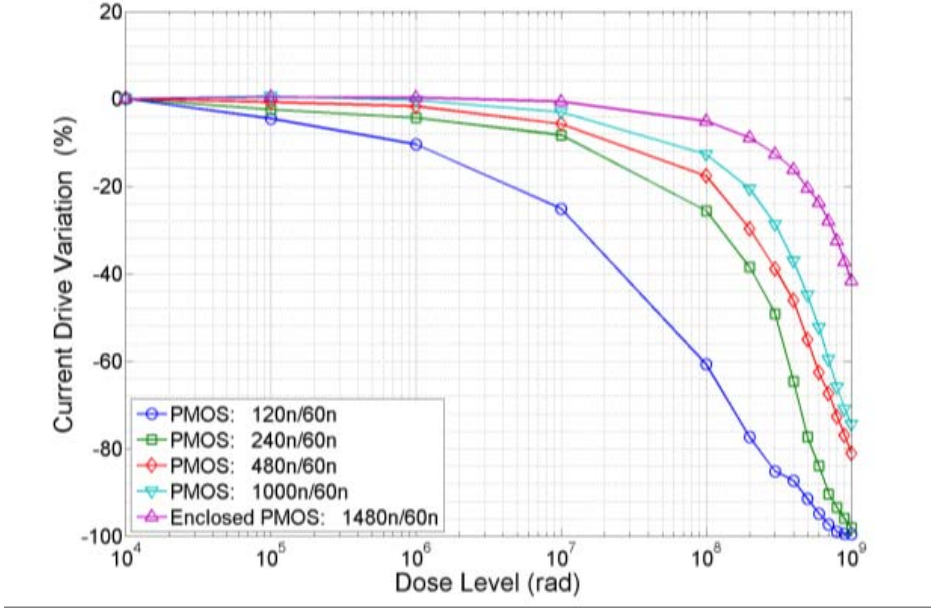


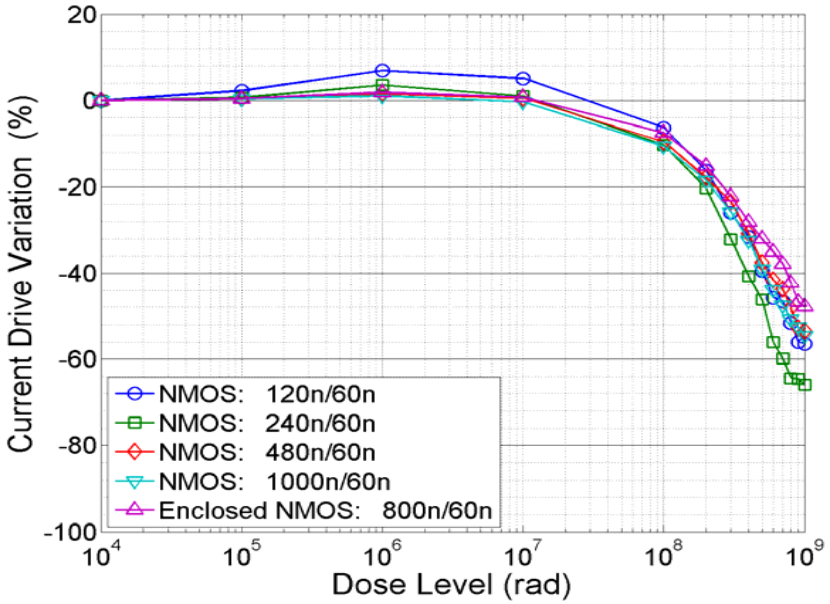
- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC → DC bus traffic "low".
- Each pixel is tied to its neighbors -time info- (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time. Handle on TW.

Summary:

- Physics simulation→Efficient architecture.
- Spatial association of digital hit to recover lower analog performance.
- Shared resources & hit not moved around → Lowers digital power consumption.

WG1 : Radiation

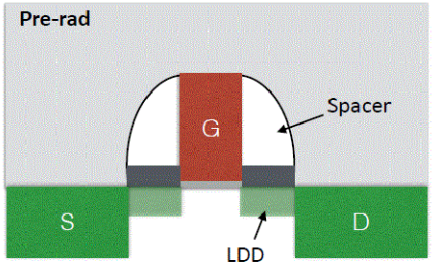


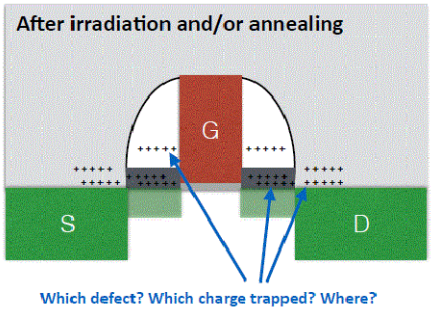


Recommandations analog block :

–**PMOS W≥300nm, L≥120nm** ; NMOS L≥120nm → **puissance, surface, performance**

–Travail présent : **Modélisation** (extraction de paramètres "Radiation corner").



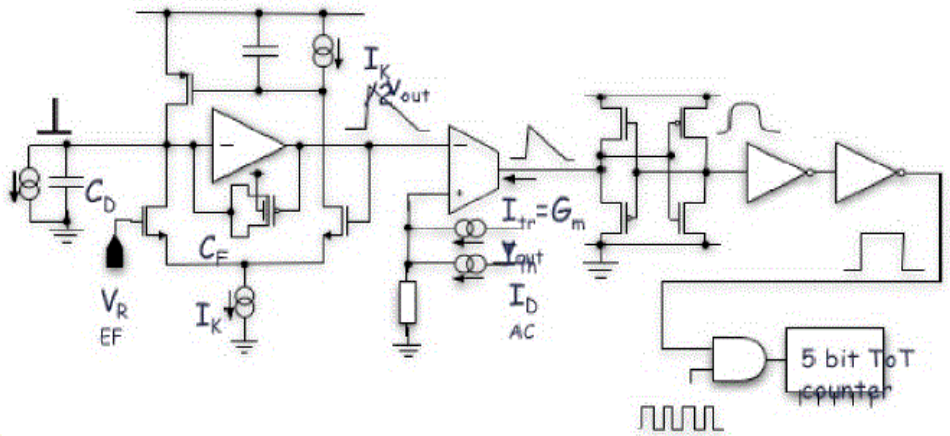


TRL with delays

SEU		Error rate Number of errors/ spill		
	area	0 to 1	1 to 0	All
DFF for shift register	14.4 µm²	5.6	2.9	4.2
TRL for configuration	40 µm²	0.082	0.04	0.06
TRL + delay	54 µm²	0.064	0.015	0.04

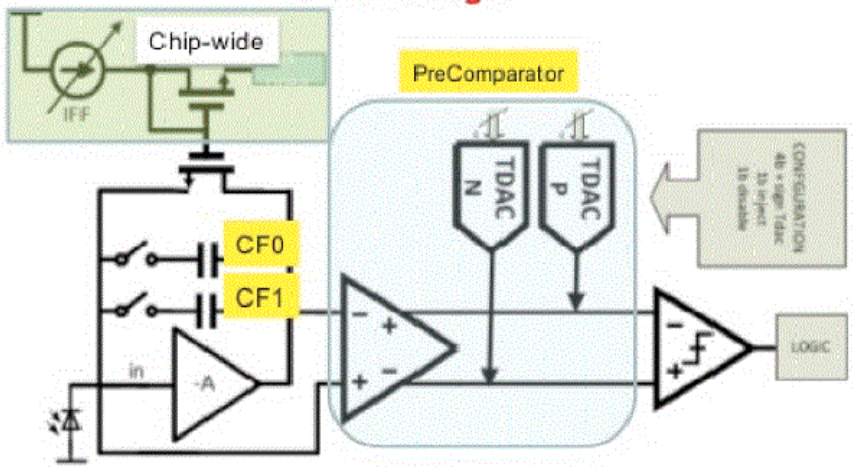
WG5 : Analog Front-End Design

INFN-Pavia design



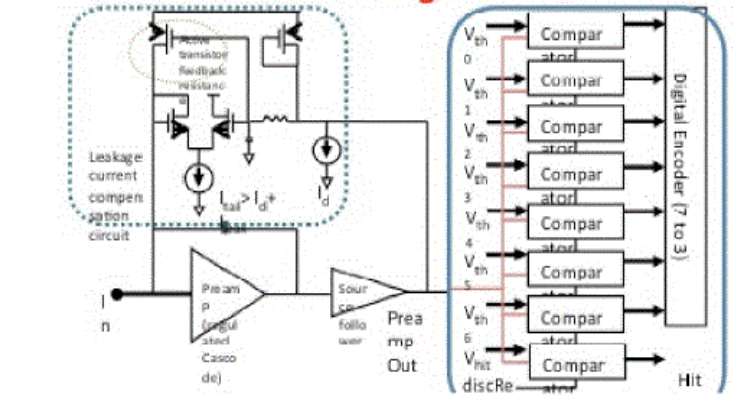
Single stage with current comparator and ToT counter

LBNL design



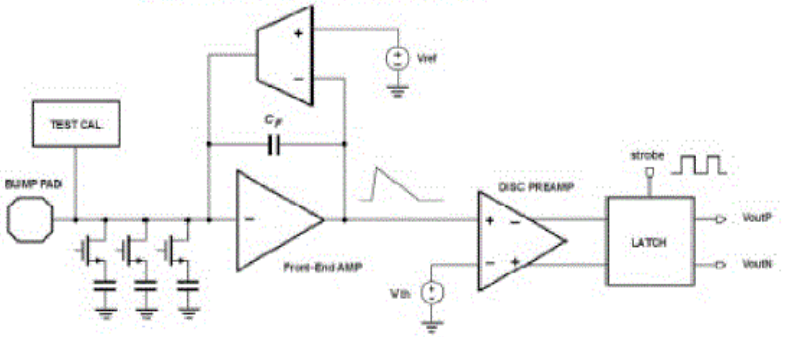
1 of 4 in quad "analog island" of FE65_P2

FNAL design



Synchronous: resets every bunch crossin. Flash ADC

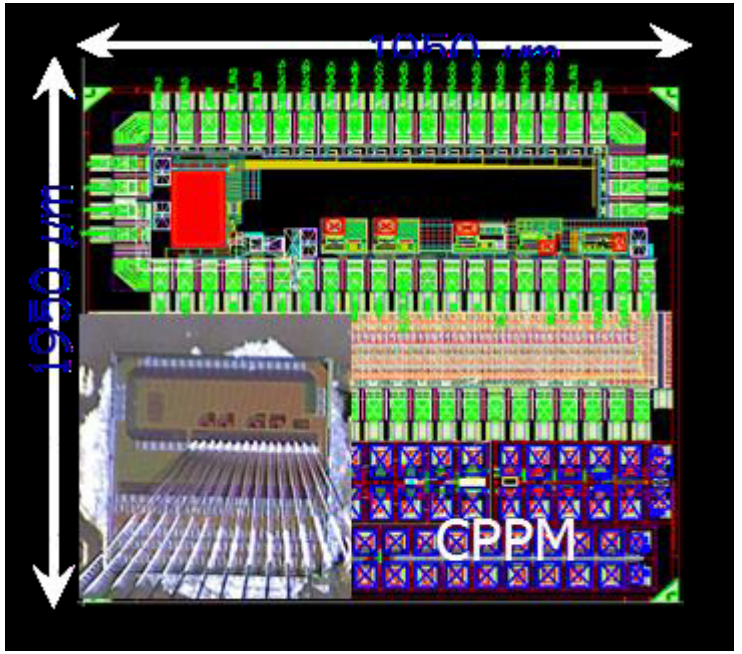
INFN-Torino design



Single stage with SAR-like ToT counter using synchronous comparator

Block IP : WG 6

ADCs, DACs, sensors (temp, current, radiation), Bandgap references, analog buffers, specialized storage cells, PLL, programmable delay, serializer, differential inputs/outputs, shunt-LDO, etc.



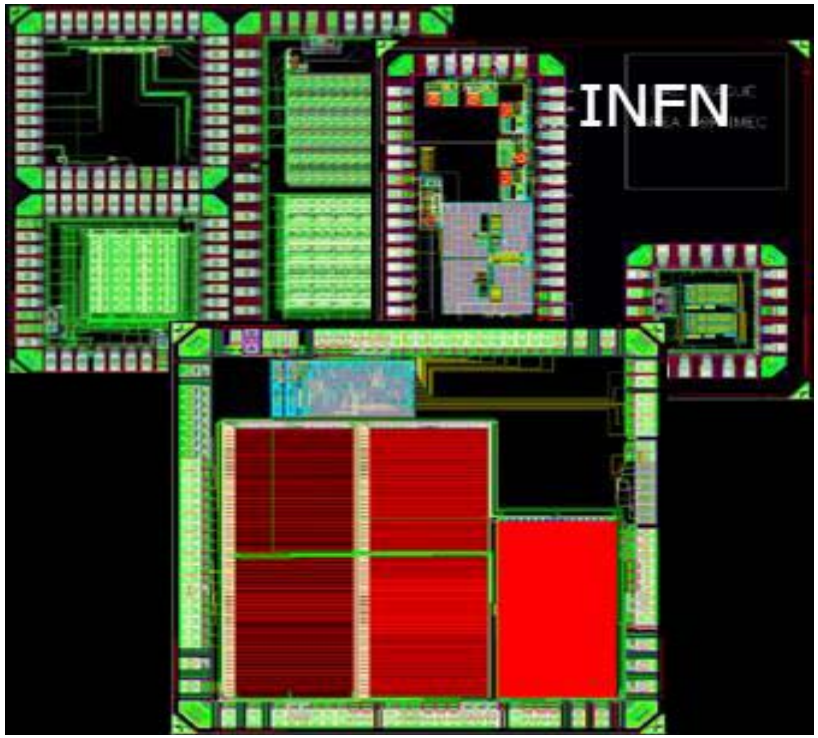
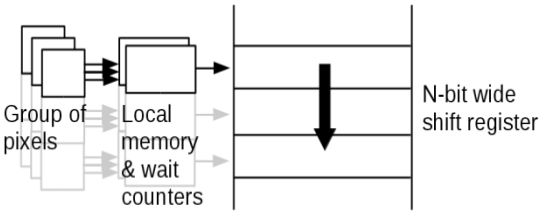
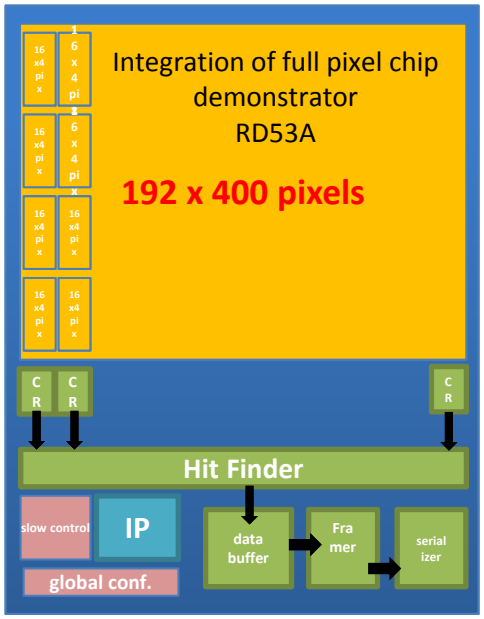


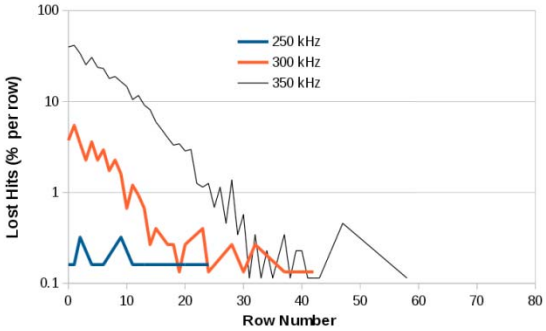
Schéma band gap

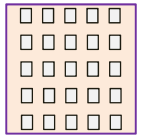
Top Level Integration (WG2)

Specification	Value	Comment or Test Conditions
Input polarity	Negative	
Interior pixel capacitance	<100 fF	this applies to most pixels
Edge pixel capacitance	<200 fF	see subsection on edge pixels
Interior pixel leakage current	<10 nA	
Edge* pixel leakage current	<20 nA	*see Sec. 5.2 for details
Min. stable threshold setting	600 e^-	With 50 fF load, 4 μA/pixel analog. For free running discriminated pixel. See Sec. 3.1
Min. charge above threshold resulting in <25 ns time walk	600 e^-	With 50 fF load, 4 μA/pixel analog. For free running discriminated pixel. See Sec. 3.1
Min. in-time threshold with free-running front end	1200 e^-	With 50 fF load, 4 μA/pixel analog. Simply the sum of the two above lines
Min. in-time threshold if using synchronous reset	750 e^-	With 50 fF load, 4 μA/pixel analog. See Sec. 3.1
Hit loss from in-pixel pileup	$\leq$1%	at 75 kHz avg. hit rate. See Sec. 3.2
Recovery from saturation	<1 μs	See Sec. 3.2 for discussion
Trigger rate	1 MHz	
Trigger latency	12.5 μs	
Noise occupancy per pixel	$< 10^{-6}$	50 fF load; in a 25 ns interval
Single pixel noise (ENC)	design-dependent	See Sec. 3.1
Radiation dose	500 Mrad	delivered at -15 C. Room T annealing only
Temperature range	-40C to +40C	
Current consumption, analog	4 μA/pixel	periphery consumption not included
Current consumption, digital	<4 μA/pixel	periphery consumption not included
Current consumption, Total	<500 mA/cm^2	Note this is 1 W/cm^2 at 2 V input
SEU upset rate, full chip	<0.05/hr	in 1.5 GHz/cm^2 particle flux
SEU upset rate affecting single pixel configuration	<100/hr	in 1.5 GHz/cm^2 particle flux

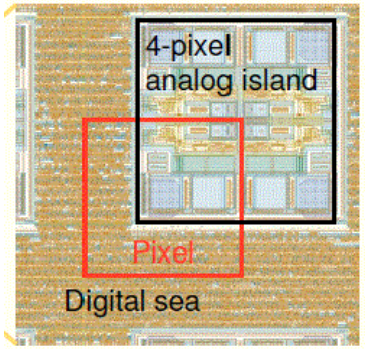


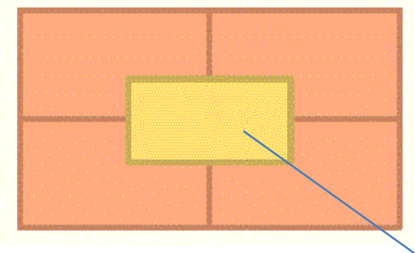






RD53-A





50 x 250 µm^2
130 nm
Type FEI-4

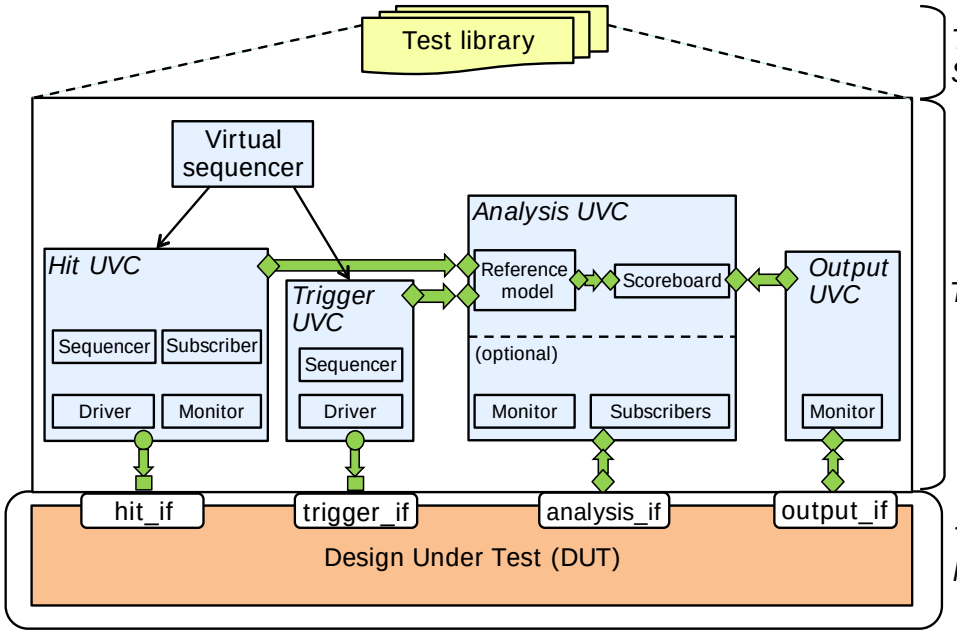
Digital

analog

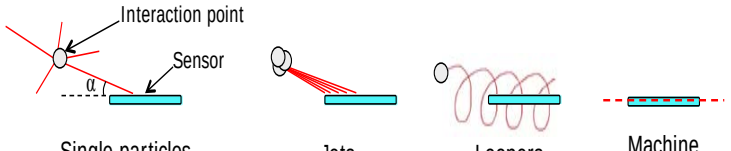
50 x 50 µm^2
65 nm
Type RD53

***VEPIX53**: **V**erification **E**nvironment for RD**53 PIX**el chips*

*(SystemVerilog/**U.V.M.**, available: git.cern.ch/reps/VEPIX53)*



verifications



[*Marconi et al., J. Instrum., 2014*]

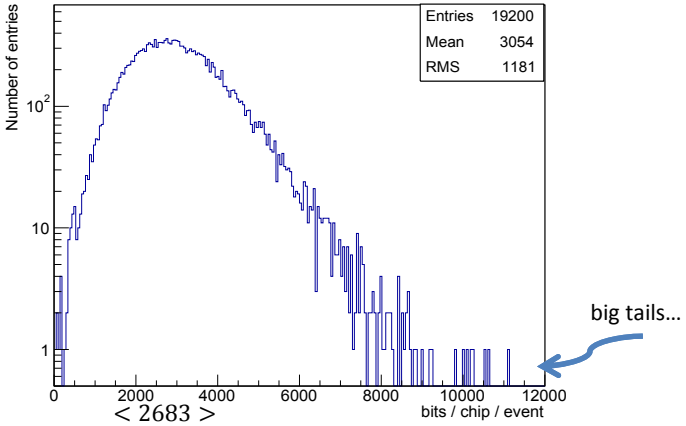
- hit generation and injection
- monitoring of pixel chip input and output
- conformity checks and statistics collection
- S.E.U.

Hit : ~ 2 GHz/cm2

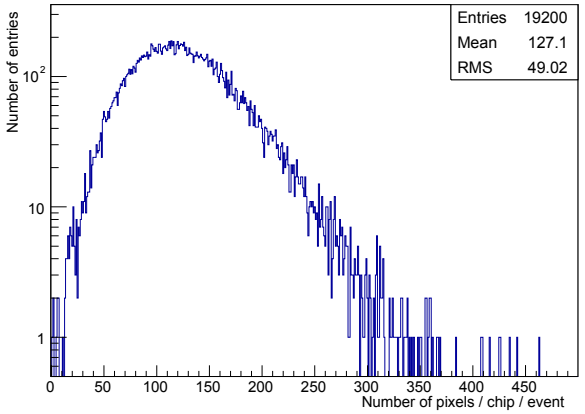
Readout rate (~ 4.8 Gbits/s per chip for 1MHz L1 trigger rate)

Number of active pixels per chip per event

(No compression)



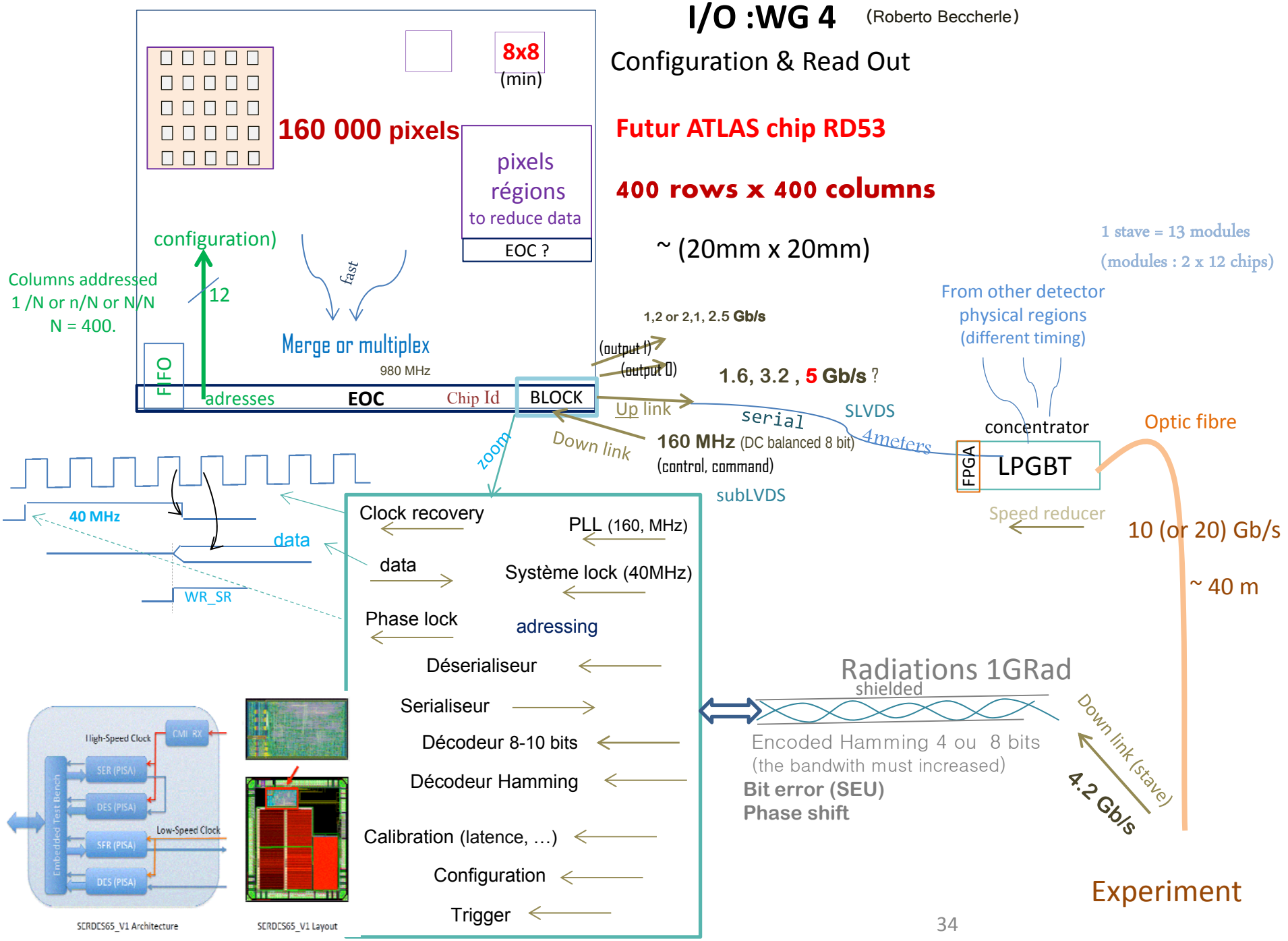
(Compression)



320 MHz working clock
320 clock cycles to the compression

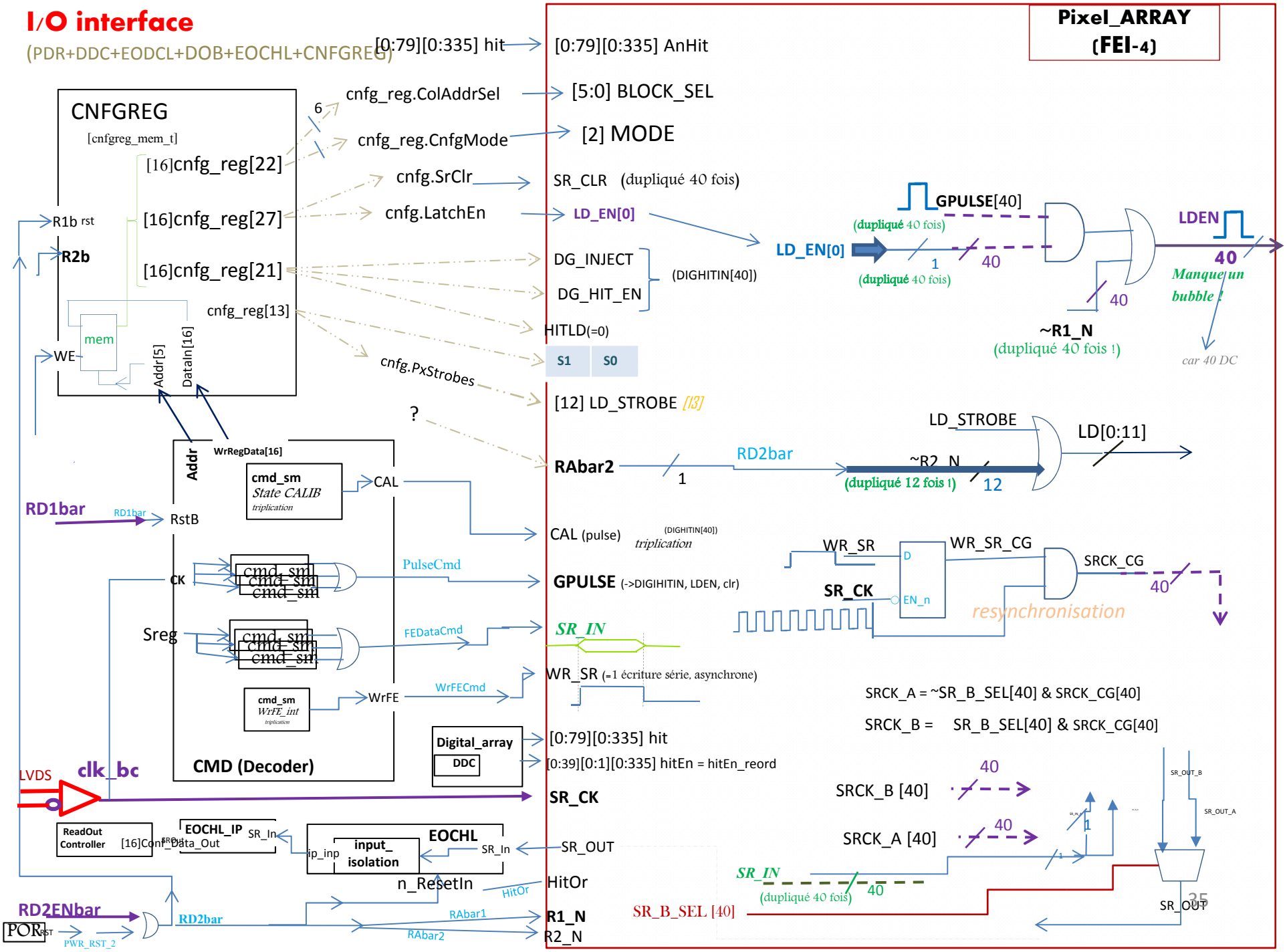
I/O :WG 4 (Roberto Beccherle)

Configuration & Read Out



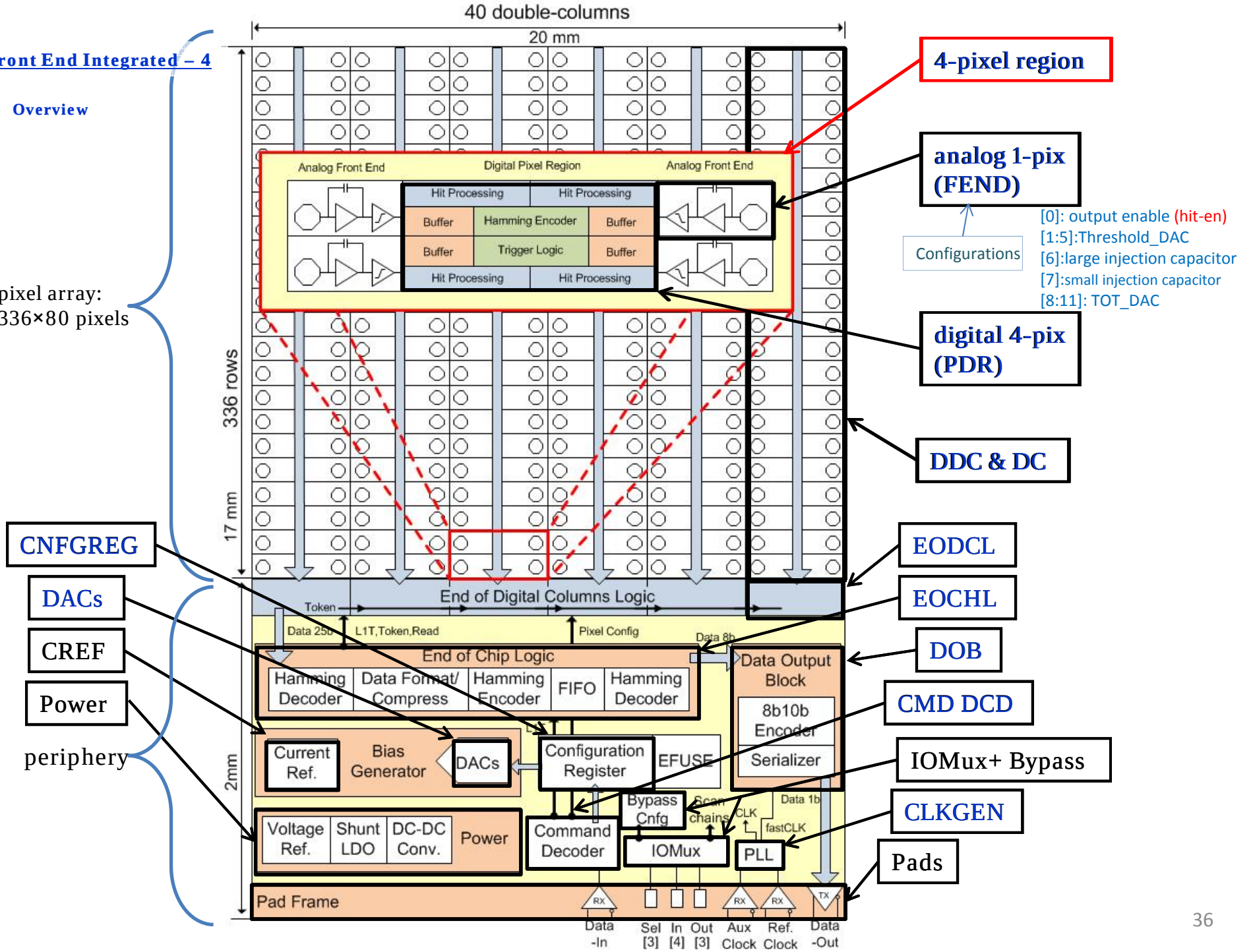
I/O interface

(PDR+DDC+EODCL+DOB+EOCHL+CNFGREG)



Front End Integrated – 4

Overview



- message pas clair -> configurer)
- nombreux warning à la **synthèse** (reprendre le code Verilog, options de compilation)

RTL Compiler 12.10

Foundation Flow Wizard (organisation, les techfiles, corner, …)

Licences permettant d'utiliser les librairies ARM de TSMC

Problème de version 11.1 et 14.1

65nm

Erreur : cellule d'ajustement fit pas sur les sites technologiques !

Vérification

Etapes EDI

floating gate (D & S)

EDI (faire et refaire; rails d'alim! ; …, I/O,..

Slack hold time

Simulation

Incisive 12.10

connect rules à éc

Simulation AMS !

Double panne !

Impédance d'entrée

Clock tree

calibre not be licensed sufficiently

simvision ne se lance pas !

Extraction ecspixl

Sealing ring

Chip Corner Stress Stress Relief Pattern

ftp : permission denied

USE PORET or PASV first

Texte

RVE Calibre

GDS

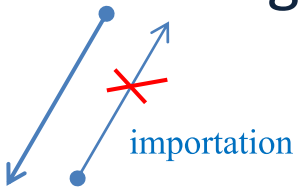
Data base results from IMEC

Competences outils

DIGITAL

Comportemental	Verilog System
Simulation	Incisive 12.1
Sythèse	RTL Compiler 12.1
Layout	Encounter Digital Implementation 14.1

(clock tree generation)



ANALOGIQUE

Analogique	Virtuoso
Simulation	Spectre & **AMS**
Verification	Calibre

« ANALOG ON TOP »

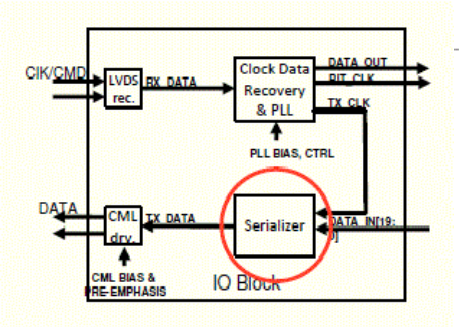
(Assemblage , vérification, simulation post layout)

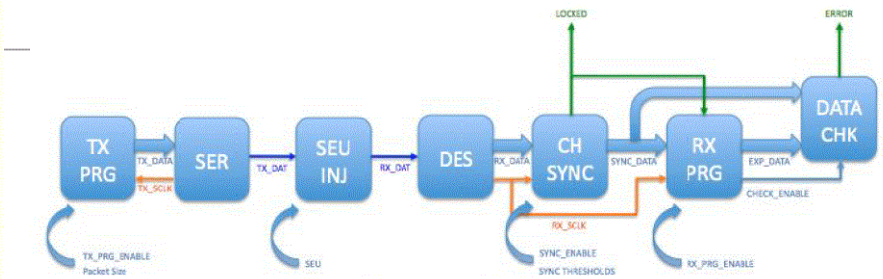
IO WG

In order to work on the RD53-A chip, have to be implemented.

- PLL, SerDes, Clk alignment, …
- Command Decoder, Configuration Memory, event builder, data compression, …

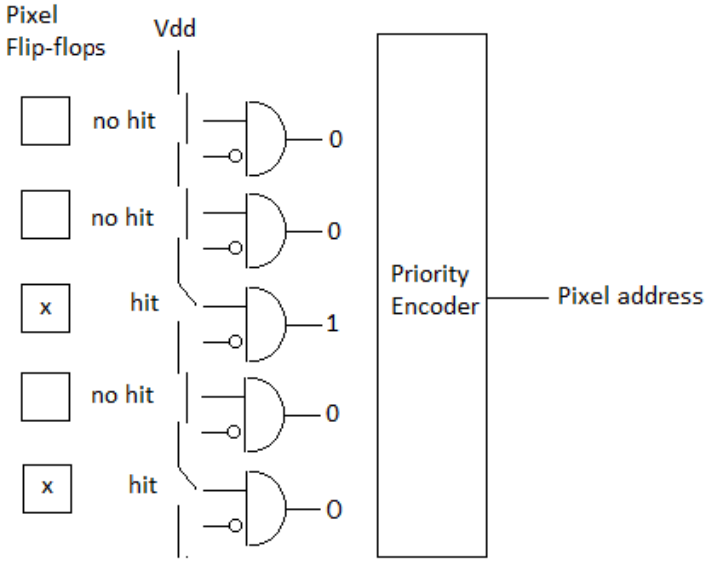
Group	Area of Interest	Foreseen manpower (over 6 months)
Bonn	CDR, PLL, SER,CML TX	0.9
Torino	PLL	0.4
Pisa	Command Decoder, SerDes, Channel Synchronization, SLVS Driver-Receiver	1.3
LBNL	5Gbps output, data compression	0.2
LPNHE	EoC Data Path	0.5
		3.3





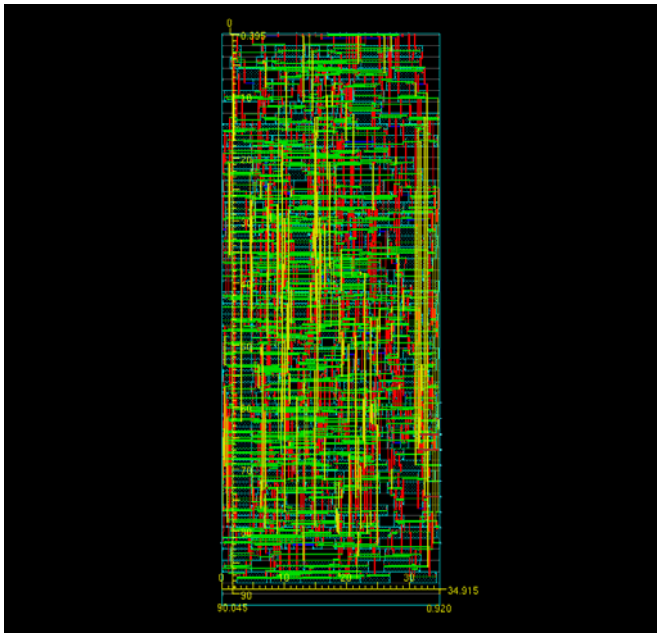
TEST BENCH (VHDL) FOR THE CHANNEL SYNCHRONIZATION MODULE

Proposal …

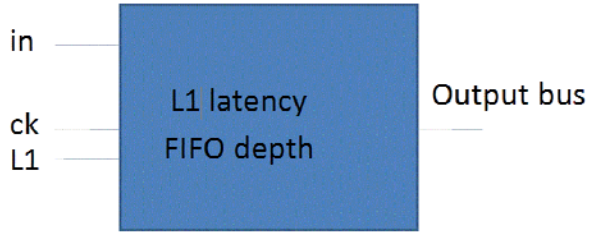


sparse scan readout

Extract a stack of addresses of pixels hit in time with L1



Building block



- VHDL model	OK
- Cells library	65nm TSMC
- I/O locations file (x,y in microns)	text file
- Dimensions (FIFO depth 16)	35 x 70 μm^2

FIFO depth 24

35 x 90 mm2

AIDA

European project

Advanced European Infrastructures for Detectors at Accelerators

Tec**H**nology
Innovations for
IN**t**elligent
Trac**K**ers

Projet phare p2io

(Labex retenus pour 2ème lecture)

AIDA 2020

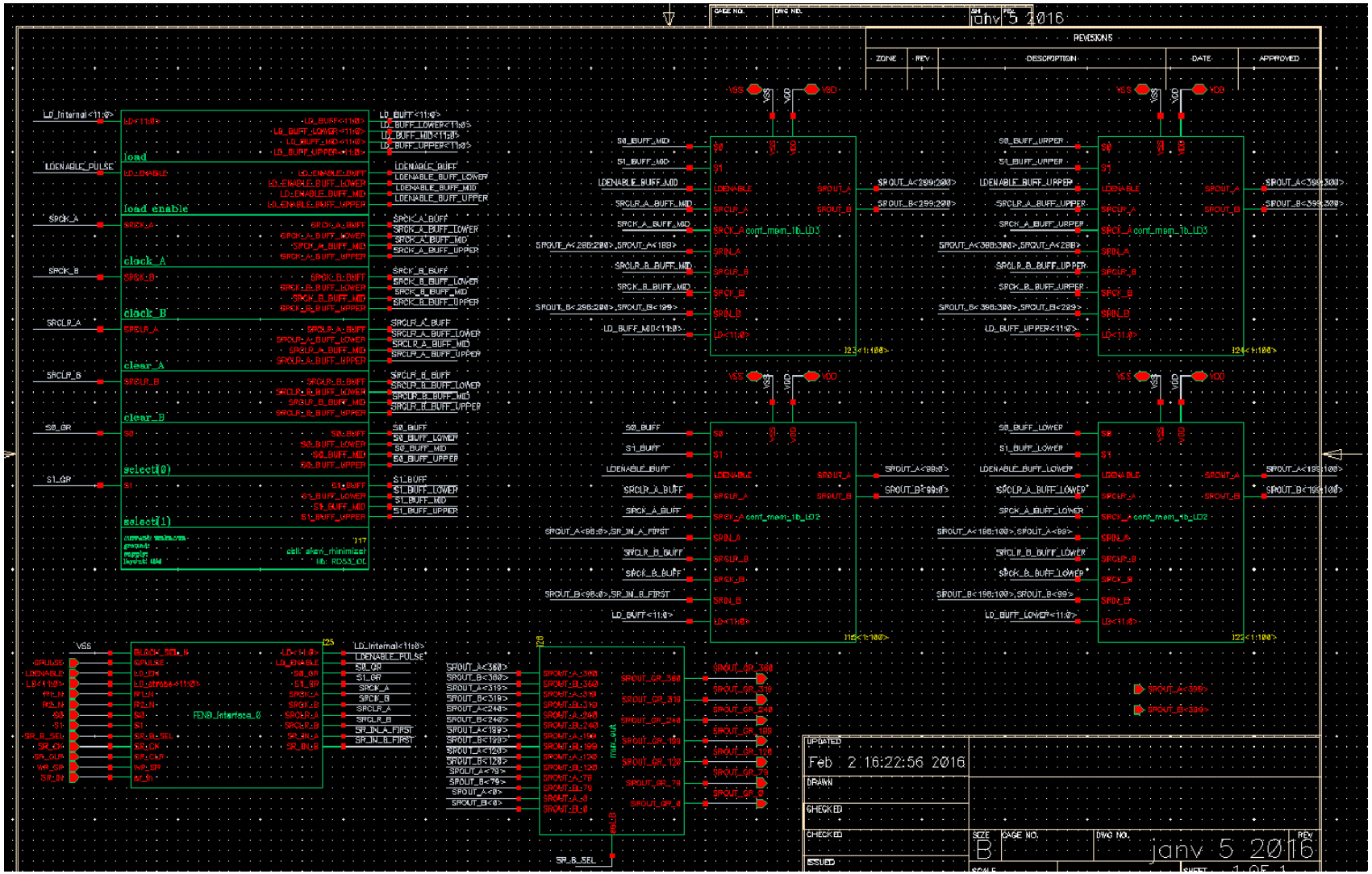
Schematic « **top level** »

Final integration : Conf Column Chip ; C3

- « Génération automatique »
- Dimensions ~ 1.0 mm x 1.0 mm
- 1.2 Volt

Blocks simulation : spectre

Top level simulation : AMS & behaviour



Schematic « **top level** »

Final integration : Conf Column Chip ; C3

- « Génération automatique »
- Dimensions ~ 1.0 mm x 1.0 mm

Blocks simulation : spectre

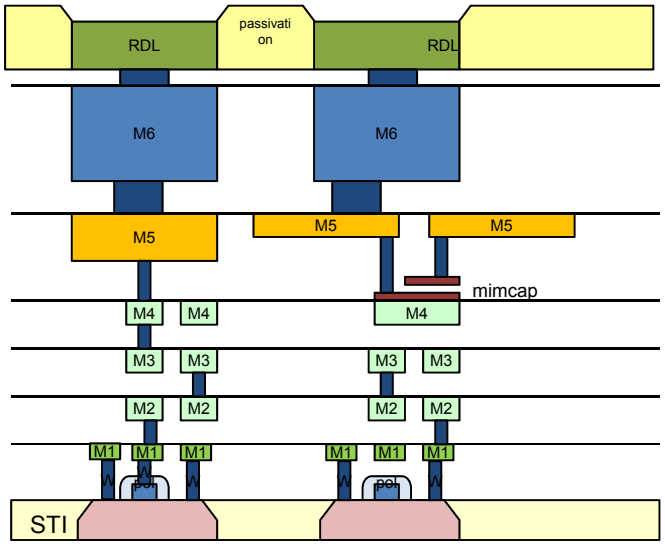
Top level simulation : AMS & behaviour

Rcarré (M1) : 0.16 Ohms
Rcarré (M9) : 0.0218 Ohms
capa (M1) : 0.16 Ohms
capa (M9) : 0.0218 Ohms
Métal (400fF / mm) 20 mm ≡ 8pF ;
1 mm ≡ 50 Ω (pour la clk attention au jitter)
1ns ≡ 1mA ; invD24 : 3mA
Vth = 0.450 V
Tox = 2.6 nm
(fast corner, 1.6V/-55C)

Supply Voltage	1.2V ± 10%

- 3 metal stacks
  - 6+1 metals (“base metal stack”)
    - 4-thin, 1-thick, 1-UTM , RDL
  - 7+1 metals (“CMS MPA metal stack”)
    - 5-thin, 1-thick, 1-UTM , RDL
    - available on special request
  - 9+1 metals (compatible with mini@sic)
    - 7-thin, 1-thick, 1-UTM , RDL
    - Note: 220 k$ NRE price adder
    - with respect to base metal stack (!)

1-Ultra-Thick *Metal*. Last *metal*, redistribution layer (*RDL*)



Quelques dates clés

- Juin 14 : Pré étude microélectronique pixel (t=0)
- 3 juillet 14: **N**on **D**isclosure **A**greement Kit TSMC 65nm pour signature
- 5 sept. 14 : Proposal collaboration RD53 (soumission)
- 15 déc. 14 : 1ère rencontre avec Jorgen Christiansen (responsable RD53)
- janv. 15 : Guest RD53 & 1ère rencontre avec R.Beccherle (responsable WG IO)
- 30 janv. 15: Access Repository FEI-4 (uvm , codes)
- Mai 15 : Etude code RTL chargement configuration FEI-4
- 15 juin 15 : NDA signé
- Juillet 15 : Synthèse, P&R d'une Double Colonne de chargement
- Août 15 : Etude de la partie I/O du FEI4
- 28 oct. 15 : Kit TSMC 65nm installé
- 28 oct. 15 : Collaboration CPPM (officialisée)
- 13 nov. 15 : Réception 1ère version des Latch CPPM
- 11 janv. 16 : Réception Latch CPPM (version finale)
- 4 mars 16 : Présentation puce C3 LAL à Jorgen Christiansen
- 10 mars 16 : Run Multi-Project Wafer (prix & réservation)
- 21 mars : Correction des PADs (Bibliothèques PADs OK)
- 23 mars 16 : (1ère) soumission
- 31 mars 16 : envoi du GDS (2ème soumission)
- 5 avril 16 : confirme le GDS (tape-out) -> fonderie.

- 13 avril 16 : entretien avec R. Beccherle (meeting RD53)
- 26 avril 16 : Participation au meeting RD53-A

Groupe ATLAS